Low I_Q Boost/SEPIC/Flyback/Inverting Converter with 0.5A, 140V Switch

FEATURES

- **Wide Input Voltage Range: 4.5V to 100V**
- **Ultralow Quiescent Current and Low Ripple Burst Mode® Operation: I_Q = 6µA**
- **0.5A, 140V Power Switch**
- **Positive or Negative Output Voltage Programming with a Single Feedback Pin**
- **Programmable Frequency (100kHz to 500kHz)**
- Synchronizable to an External Clock
- BIAS Pin for Higher Efficiency
- Programmable Undervoltage Lockout (UVLO)
- Thermally-Enhanced High Voltage MSOP Package
- AEC-Q100 Qualified for Automotive Applications

APPLICATIONS

- Industrial and Automotive
- Telecom
- Medical Diagnostic Equipment
- Portable Electronics

DESCRIPTION

The LT®8331 is a current mode DC/DC converter with a 140V, 0.5A switch operating from a 4.5V to 100V input. With a unique single feedback pin architecture, it is capable of boost, SEPIC, flyback or inverting configurations. Burst Mode operation consumes as low as 6µA quiescent current to maintain high efficiency at very low output currents, while keeping typical output ripple below 20mV.

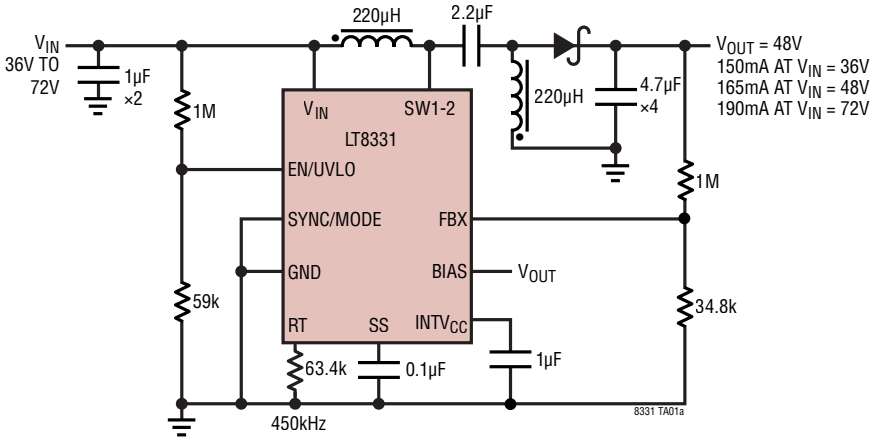
The internally-compensated current mode architecture results in stable operation over a wide range of input and output voltages and programmable switching frequencies between 100kHz to 500kHz. A SYNC/MODE pin allows synchronization to an external clock. It can also be used to select between burst or pulse-skipping modes of operation. For increased efficiency, a BIAS pin can accept a second input to supply the $INTV_{CC}$ regulator. Additional features include frequency foldback and programmable soft-start for controlling inductor current during start-up.

The LT8331 is available in a thermally-enhanced MSOP package with four pins removed for high voltage spacings.

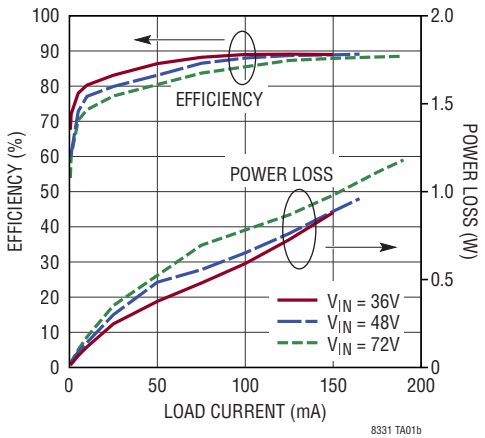
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TYPICAL APPLICATION

48V Output SEPIC Converter



Efficiency and Power Loss

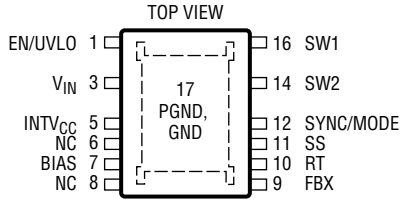


ABSOLUTE MAXIMUM RATINGS

(Note 1)

SW 140V
V_{IN}, EN/UVLO 100V
BIAS 60V
EN/UVLO Pin Above V_{IN} Pin, SYNC 6V
$INTV_{CC}$ (Note 2) 4V
FBX ..... ±4V
Operating Junction Temperature (Note 3)
LT8331E, LT8331I ..... –40°C to 125°C
Storage Temperature Range ..... –65°C to 150°C
Lead Temperature (Soldering, 10 sec) ..... 300°C

PIN CONFIGURATION



MSE PACKAGE
VARIATION: MSE16 (12)
16-LEAD PLASTIC MSOP

θ_{JA} = 45°C/W, θ_{JC} = 10°C/W
EXPOSED PAD (PIN 17) IS PGND AND GND, MUST BE SOLDERED TO PCB

ORDER INFORMATION

LEAD FREE FINISH	TAPE AND REEL	PART MARKING*	PACKAGE DESCRIPTION	TEMPERATURE RANGE
LT8331EMSE#PBF	LT8331EMSE#TRPBF	8331	16-Lead Plastic MSOP with 4 Pins Removed	–40°C to 125°C
LT8331IMSE#PBF	LT8331IMSE#TRPBF	8331	16-Lead Plastic MSOP with 4 Pins Removed	–40°C to 125°C
AUTOMOTIVE PRODUCTS**				
LT8331EMSE#WPBF	LT8331EMSE#WTRPBF	8331	16-Lead Plastic MSOP with 4 Pins Removed	–40°C to 125°C
LT8331IMSE#WPBF	LT8331IMSE#WTRPBF	8331	16-Lead Plastic MSOP with 4 Pins Removed	–40°C to 125°C

Contact the factory for parts specified with wider operating temperature ranges. *The temperature grade is identified by a label on the shipping container.

Tape and reel specifications. Some packages are available in 500 unit reels through designated sales channels with #TRMPBF suffix.

**Versions of this part are available with controlled manufacturing to support the quality and reliability requirements of automotive applications. These models are designated with a #W suffix. Only the automotive grade products shown are available for use in automotive applications. Contact your local Analog Devices account representative for specific product ordering information and to obtain the specific Automotive Reliability reports for these models.

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. V_{IN} = 12V, EN/UVLO = 12V unless otherwise noted.

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
V_{IN} Operating Voltage Range		●	4.5		100	V
V_{IN} Quiescent Current at Shutdown	$V_{EN/UVLO}$ = 0.2V	 ●		1 2	2 5	µA µA
	$V_{EN/UVLO}$ = 1.5V	 ●		2.0 3.6	5 9.5	µA µA
V_{IN} Quiescent Current						
Sleep Mode (Not Switching)	SYNC = 0V	 ●		5.5 8.5	15 25	µA µA
Active Mode (Not Switching)	SYNC = 0V, BIAS = 0V	 ●		780 840	1420 1720	µA µA
	SYNC = 0V, BIAS = 5V	 ●		17 24	40 55	µA µA
	SYNC = $INTV_{CC}$, BIAS = 0V	 ●		700 800	1080 1170	µA µA
	SYNC = $INTV_{CC}$, BIAS = 5V	 ●		17 24	40 55	µA µA

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. V_{IN} = 12V, EN/UVLO = 12V unless otherwise noted.

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
BIAS Threshold	Rising, BIAS Can Supply $INTV_{CC}$ Falling, BIAS Cannot Supply $INTV_{CC}$	● ●	4.10 3.725	4.4 4	4.65 4.275	V V
V_{IN} Falling Threshold to Supply $INTV_{CC}$	BIAS = 12V			BIAS – 1.6V		V
BIAS Falling Threshold to Supply $INTV_{CC}$	V_{IN} = 12V			V_{IN} – 0.4V		V
FBX Regulation						
FBX Regulation Voltage	FBX > 0V FBX < 0V	● ●	1.568 –0.820	1.6 –0.80	1.632 –0.780	V V
FBX Line Regulation	FBX > 0V, 4.5V < V_{IN} < 100V FBX < 0V, 4.5V < V_{IN} < 100V			0.005 0.005	0.015 0.015	%/V %/V
FBX Pin Current	FBX = 1.6V, –0.8V	●	–10		10	nA
Oscillator						
Switching Frequency (f_{OSC})	R_T = 301k R_T = 100k R_T = 56.2k	● ● ●	92 279 465	100 300 500	107 321 535	kHz kHz kHz
Minimum On-Time	SYNC = 0V SYNC = $INTV_{CC}$			165 160	290 290	ns ns
Minimum Off-Time				146	230	ns
SYNC/Mode, Mode Thresholds	Rising to Select Pulse Skipping Mode Falling to Select Burst Mode Operation	● ●	 0.6		2.4	V V
SYNC/Mode, Clock Thresholds	Rising Falling		 0.6	2.0 1.1	2.4	V V
f_{SYNC}/f_{OSC} Allowed Ratio	R_T = 100k		0.95	1	1.25	kHz
SYNC Pin Current	SYNC = 2V		–40		40	nA
Switch						
Maximum Switch Current Limit Threshold		●	0.5	0.6	0.7	A
Switch Overcurrent Threshold	Discharges SS Pin			1.15		A
Switch $R_{DS(ON)}$	I_{SW} = 0.25A			1.7		Ω
Switch Leakage Current	V_{SW} = 140V			0.1	1	µA
EN/UVLO Logic						
EN/UVLO Pin Threshold (Rising)	Start Switching	●	1.576	1.74	1.90	V
EN/UVLO Pin Threshold (Falling)	Stop Switching	●	1.556	1.6	1.644	V
EN/UVLO Pin Current	$V_{EN/UVLO}$ = 1.6V	●	–40		40	nA
Soft-Start						
Soft-Start Charge Current	SS = 1V			2		µA
Soft-Start Pull-Down Resistance	Fault Condition, SS = 0.1V			250		Ω

Note 1: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to any Absolute Maximum Rating condition for extended periods may affect device reliability and lifetime.

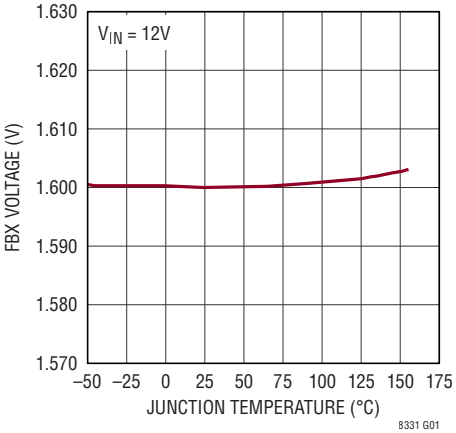
Note 2: $INTV_{CC}$ cannot be externally driven. No external loading is allowed on this pin.

Note 3: The LT8331E is guaranteed to meet performance specifications from 0°C to 125°C junction temperature. Specifications over the –40°C to 125°C operating junction temperature range are assured by design, characterization and correlation with statistical process controls. The LT8331I is guaranteed over the full –40°C to 125°C operating junction temperature range. High junction temperatures degrade operating lifetimes. Operating lifetime is derated at junction temperatures greater than 125°C.

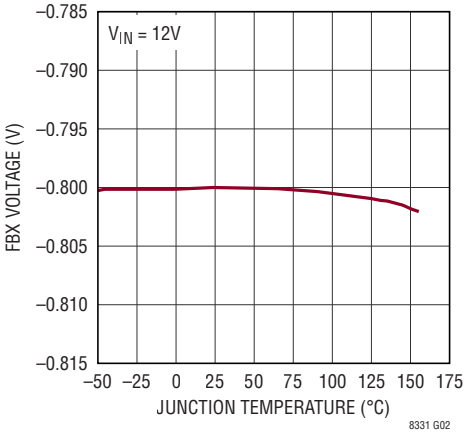
Note 4: The IC includes overtemperature protection that is intended to protect the device during overload conditions. Junction temperature will exceed 150°C when overtemperature protection is active. Continuous operation above the specified maximum operating junction temperature will reduce lifetime.

TYPICAL PERFORMANCE CHARACTERISTICS

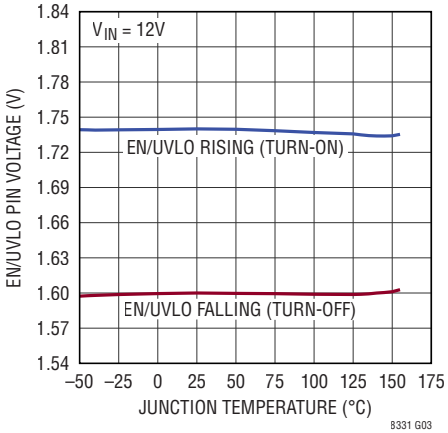
FBX Positive Regulation Voltage vs Temperature



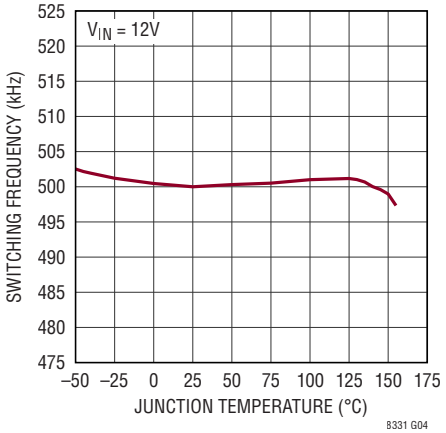
FBX Negative Regulation Voltage vs Temperature



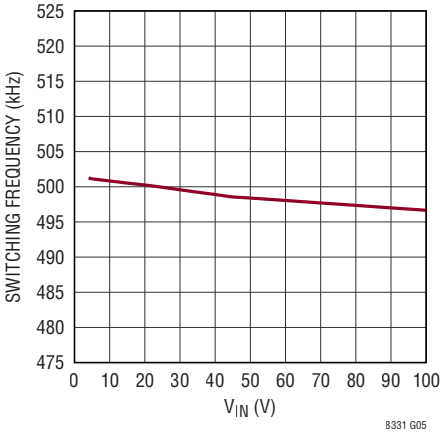
EN/UVLO Pin Thresholds vs Temperature



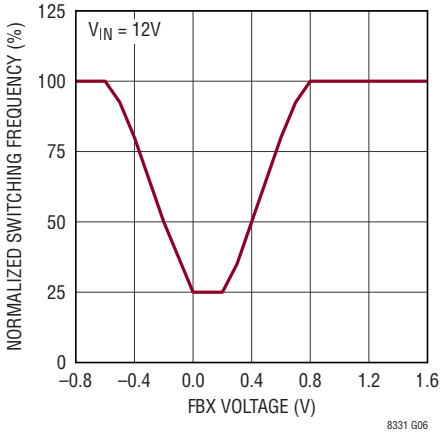
Switching Frequency vs Temperature



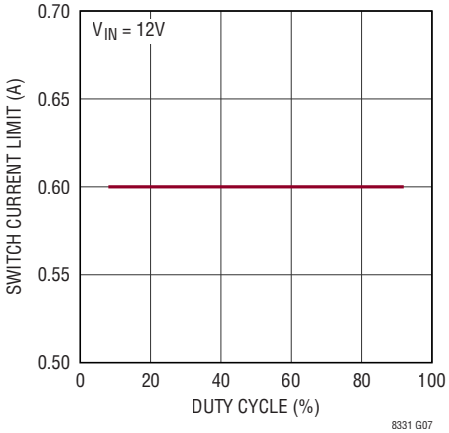
Switching Frequency vs V_{IN}



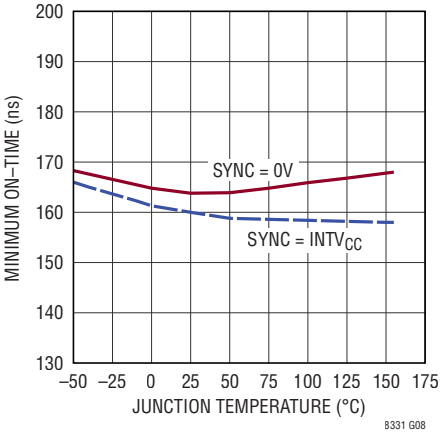
Normalized Switching Frequency vs FBX Voltage



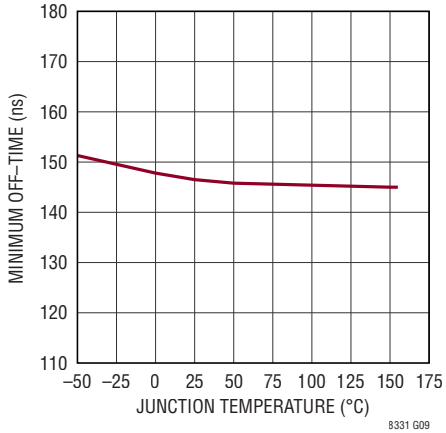
Switch Current Limit vs Duty Cycle



Switch Minimum On-Time vs Temperature

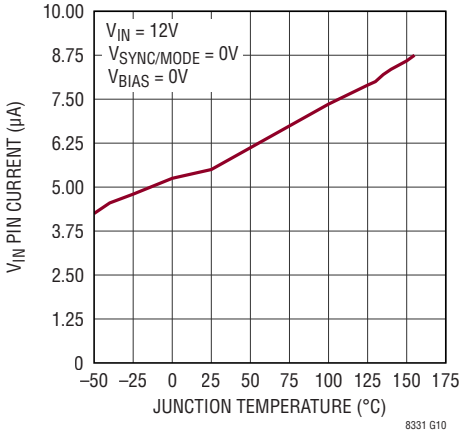


Switch Minimum Off-Time vs Temperature

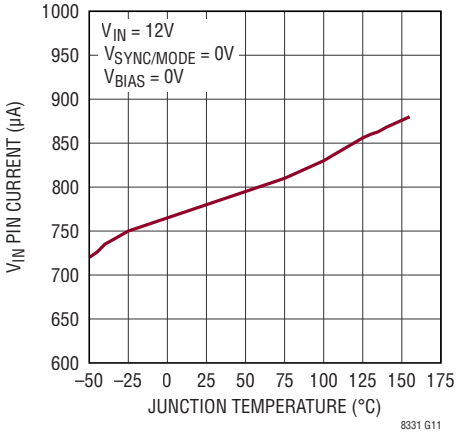


TYPICAL PERFORMANCE CHARACTERISTICS

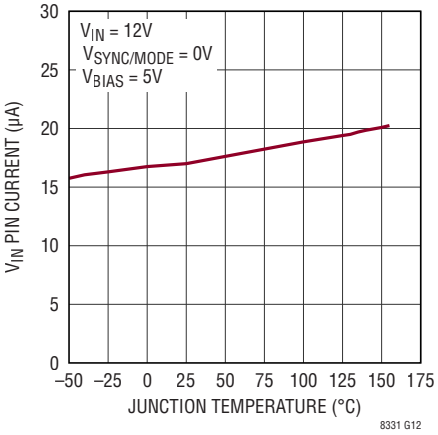
V_{IN} Pin Current (Sleep Mode, Not Switching) vs Temperature



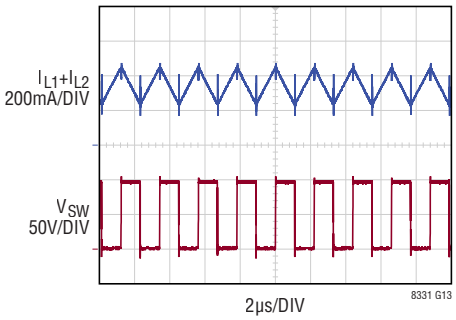
V_{IN} Pin Current (Active Mode, Not Switching) vs Temperature



V_{IN} Pin Current (Active Mode, Not Switching) vs Temperature

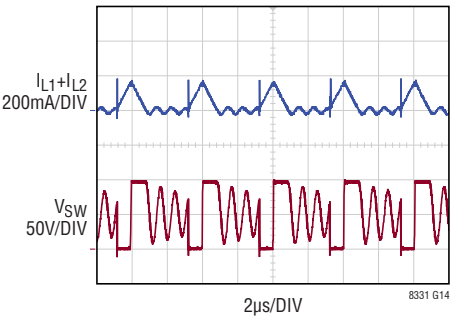


Switching Waveforms (in CCM)



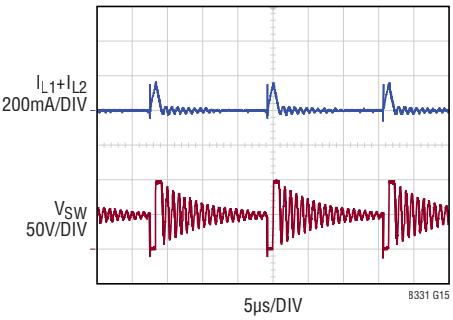
FRONT PAGE APPLICATION
V_{IN} = 48V, V_{OUT} = 48V, I_{LOAD} = 165mA

Switching Waveforms (in DCM/Light Burst Mode)



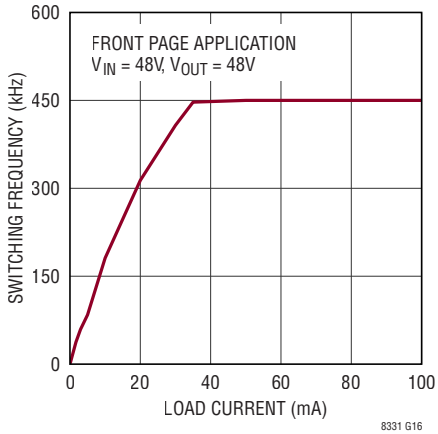
FRONT PAGE APPLICATION
V_{IN} = 48V, V_{OUT} = 48V, I_{LOAD} = 15mA

Switching Waveforms (in Deep Burst Mode)

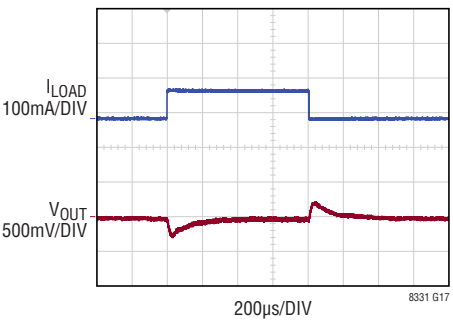


FRONT PAGE APPLICATION
V_{IN} = 48V, V_{OUT} = 48V, I_{LOAD} = 3mA

Burst Frequency vs Load Current

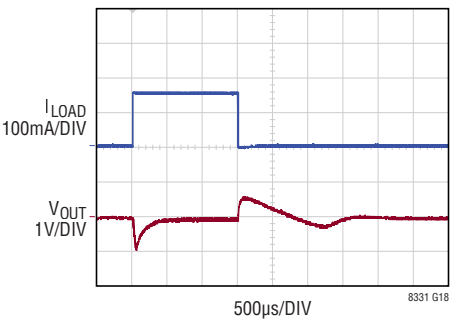


V_{OUT} Transient Response: Load Current Transients from 82.5mA to 165mA to 82.5mA



FRONT PAGE APPLICATION
V_{IN} = 48V, V_{OUT} = 48V

V_{OUT} Transient Response: Load Current Transients from 5mA to 165mA to 5mA



FRONT PAGE APPLICATION
V_{IN} = 48V, V_{OUT} = 48V

PIN FUNCTIONS

EN/UVLO (Pin 1): Shutdown and Undervoltage Detect Pin. The LT8331 is shut down when this pin is low and active when this pin is high. Below an accurate 1.6V threshold, the part enters undervoltage lockout and stops switching. This allows an undervoltage lockout (UVLO) threshold to be programmed for system input voltage by resistively dividing down system input voltage to the EN/UVLO pin. A 140mV pin hysteresis ensures part switching resumes when the pin exceeds 1.74V. EN/UVLO pin voltage below 0.2V reduces V_{IN} current below 1µA. If shutdown and UVLO features are not required, the pin can be tied directly to system input.

V_{IN} (Pin 3): Input Supply. This pin must be locally bypassed. Be sure to place the positive terminal of the input capacitor as close as possible to the V_{IN} pin, and the negative terminal as close as possible to the exposed pad PGND copper (near Pin 1).

$INTV_{CC}$ (Pin 5): Regulated 3.2V Supply for Internal Loads. The $INTV_{CC}$ pin must be bypassed with a minimum 1µF low ESR ceramic capacitor to GND. No additional components or loading is allowed on this pin. $INTV_{CC}$ draws power from the BIAS pin if $4.4V \leq BIAS \leq V_{IN} - 0.4V$, otherwise $INTV_{CC}$ is powered by the V_{IN} pin.

NC (Pins 6, 8): No Internal Connection. Leave these pins open.

BIAS (Pin 7): Second Input Supply for Powering $INTV_{CC}$. Removes the majority of $INTV_{CC}$ current from the V_{IN} pin to improve efficiency when $4.4V \leq BIAS \leq V_{IN} - 0.4V$. If unused, tie the pin to GND copper.

FBX (Pin 9): Voltage Regulation Feedback Pin for Positive or Negative Outputs. Connect this pin to a resistor divider between the output and the exposed pad GND copper (near Pin 9). FBX reduces the switching frequency during start-up and fault conditions when FBX is close to 0V.

RT (Pin 10): A resistor from this pin to the exposed pad GND copper (near Pin 9) programs switching frequency.

SS (Pin 11): Soft-Start Pin. Connect a capacitor from this pin to GND copper (near Pin 9) to control the ramp rate of inductor current during converter start-up. SS pin charging current is 2µA. An internal 250Ω MOSFET discharges this pin during shutdown or fault conditions.

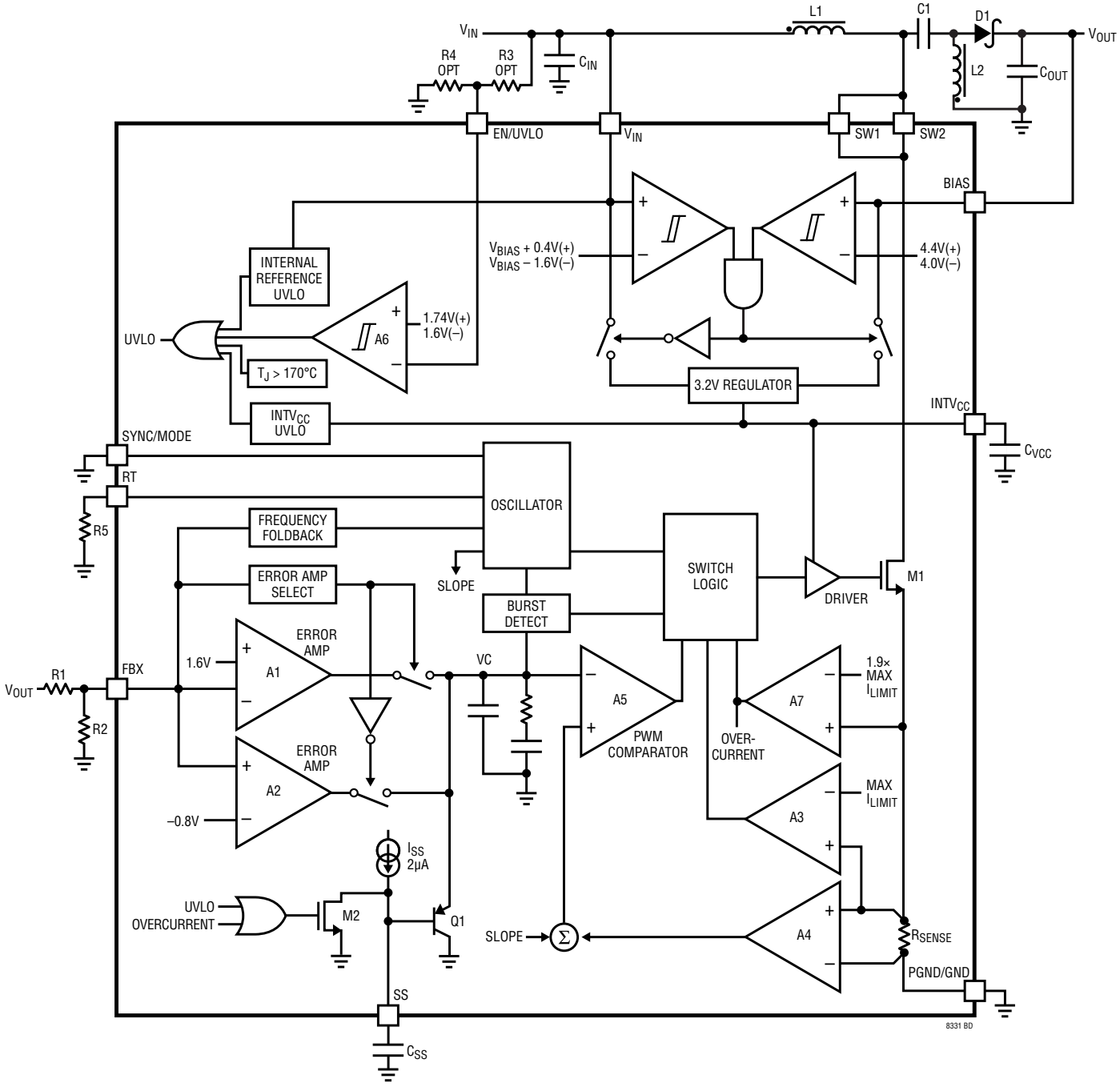
SYNC/MODE (Pin 12): This pin allows three selectable modes for optimization of performance.

1. GND: For Burst Mode operation (low I_Q and low output voltage ripple at light loads).
2. External Clock : For synchronized switching frequency.
3. $INTV_{CC}$: For pulse-skipping mode (at light load or low duty cycle).

SW1, SW2 (Pins 14, 16): Outputs of the Internal Power Switch. Minimize the metal trace area connected to these pins to reduce EMI.

PGND,GND (Pin 17): Power Ground and Signal Ground for the IC. The package has an exposed pad (Pin 17) underneath the IC which is the best path for heat out of the package. Pin 17 should be soldered to a continuous copper ground plane under the device to reduce die temperature and increase the power capability of the LT8331. Connect power ground components to the exposed pad copper exiting near Pins 1, 14 and 16. Connect signal ground components to the exposed pad copper exiting near Pins 8 and 9.

BLOCK DIAGRAM



OPERATION

The LT8331 uses a fixed frequency, current mode control scheme to provide excellent line and load regulation. Operation can be best understood by referring to the Block Diagram. An oscillator (with frequency programmed by a resistor at the RT pin) turns on the internal power switch at the beginning of each clock cycle. Current in the inductor then increases until the current comparator trips and turns off the power switch. The peak inductor current at which the switch turns off is controlled by the voltage on the internal VC node. The error amplifier servos the VC node by comparing the voltage on the FBX pin with an internal reference voltage (1.60V or –0.80V, depending on the chosen topology). When the load current increases it causes a reduction in the FBX pin voltage relative to the internal reference. This causes the error amplifier to increase the VC voltage until the new load current is satisfied. In this manner, the error amplifier sets the correct peak switch current level to keep the output in regulation.

The LT8331 is capable of generating either a positive or negative output voltage with a single FBX pin. It can be configured as a boost, SEPIC or flyback converter to generate a positive output voltage, or as an inverting converter to generate a negative output voltage. When configured as a SEPIC converter, as shown in the Block Diagram, the FBX pin is pulled up to the internal bias voltage of 1.60V by a voltage divider (R1 and R2) connected from V_{OUT} to GND. Amplifier A2 becomes inactive and amplifier A1 performs (inverting) amplification from FBX to VC. When the LT8331 is in an inverting configuration, the FBX pin is pulled down to –0.80V by a voltage divider from V_{OUT} to GND. Amplifier A1 becomes inactive and amplifier A2 performs (non-inverting) amplification from FBX to VC.

If the EN/UVLO pin voltage is below 1.6V, the LT8331 enters undervoltage lockout (UVLO), and stops switching. When the EN/UVLO pin voltage is above 1.74V (typical), the LT8331 resumes switching. If the EN/UVLO pin voltage is below 0.2V, the LT8331 draws less than 1µA from V_{IN}.

For the SYNC/MODE pin tied to ground, the LT8331 provides low output ripple Burst Mode operation with ultra low quiescent current at light loads. For the SYNC/MODE pin tied to $INTV_{CC}$, the LT8331 uses pulse-skipping mode, at the expense of hundreds of microamps, to maintain output voltage regulation at light loads by skipping switch pulses. For the SYNC/MODE pin driven by an external clock, the converter switching frequency is synchronized to that clock and pulse-skipping mode is also enabled.

The LT8331 includes a BIAS pin to improve efficiency across all loads. The $INTV_{CC}$ supply current can be drawn from the BIAS pin instead of the V_{IN} pin for 4.4V ≤ BIAS ≤ V_{IN}.

Protection features ensure the immediate disable of switching and reset of the SS pin for any of the following faults: internal reference UVLO, $INTV_{CC}$ UVLO, switch current > 1.9× maximum limit, EN/UVLO < 1.6V or junction temperature > 170°C.

APPLICATIONS INFORMATION

ACHIEVING ULTRALOW QUIESCENT CURRENT

To enhance efficiency at light loads the LT8331 uses a low ripple Burst Mode architecture. This keeps the output capacitor charged to the desired output voltage while minimizing the input quiescent current and output ripple. In Burst Mode operation, the LT8331 delivers single small pulses of current to the output capacitor followed by sleep periods where the output power is supplied by the output capacitor. While in sleep mode, the LT8331 consumes only 6µA.

As the output load decreases, the frequency of single current pulses decreases (see Figure 1) and the percentage of time the LT8331 is in sleep mode increases, resulting in much higher light load efficiency than for typical converters. To optimize the quiescent current performance at light loads, the current in the feedback resistor divider must be minimized as it appears to the output as load current. In addition, all possible leakage currents from the output should also be minimized as they all add to the equivalent output load. The largest contributor to leakage current can be due to the reverse biased leakage of the Schottky diode (see Diode Selection in the Applications Information section).

While in Burst Mode operation, the current limit of the switch is approximately 140mA resulting in the output voltage ripple shown in Figure 2. Increasing the output capacitance will decrease the output ripple proportionally. As the output load ramps upward from zero the switching frequency will increase but only up to the fixed frequency defined by the resistor at the RT pin as shown in Figure 1. The output load at which the LT8331 reaches the fixed frequency varies based on input voltage, output voltage, and inductor choice.

PROGRAMMING INPUT TURN-ON AND TURN-OFF THRESHOLDS WITH EN/UVLO PIN

The EN/UVLO pin voltage controls whether the LT8331 is enabled or is in a shutdown state. A 1.6V reference and a comparator A6 with built-in hysteresis (typical 140mV) allow the user to accurately program the system input voltage at which the IC turns on and off (see the Block Diagram). The typical input falling and rising threshold voltages can be calculated by the following equations:

$$V_{IN(FALLING,UVLO(-))} = 1.60 \bullet \frac{R3 + R4}{R4}$$

$$V_{IN(RISING,\ UVLO(+))} = 1.74 \bullet \frac{R3 + R4}{R4}$$

V_{IN} current is reduced below 1µA when the EN/UVLO pin voltage is less than 0.2V. The EN/UVLO pin can be connected directly to the input supply V_{IN} for always-enabled operation. A logic input can also control the EN/UVLO pin.

When operating in Burst Mode operation for light load currents, the current through the R3 and R4 network can easily be greater than the supply current consumed by the LT8331. Therefore, R3 and R4 should be large enough to minimize their effect on efficiency at light loads.

$INTV_{CC}$ REGULATOR

A low dropout (LDO) linear regulator, supplied from V_{IN}, produces a 3.2V supply at the $INTV_{CC}$ pin. A minimum 1µF low ESR ceramic capacitor must be used to bypass the $INTV_{CC}$ pin to ground to supply the high transient currents required by the internal power MOSFET gate driver.

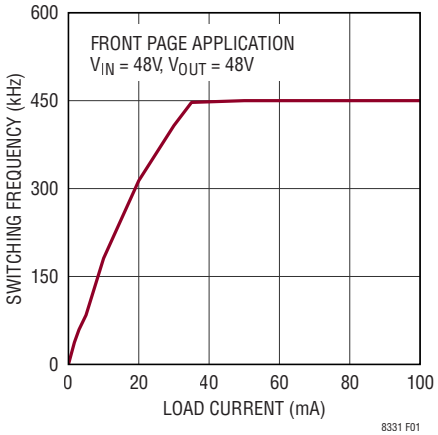


Figure 1. Burst Frequency vs Load Current

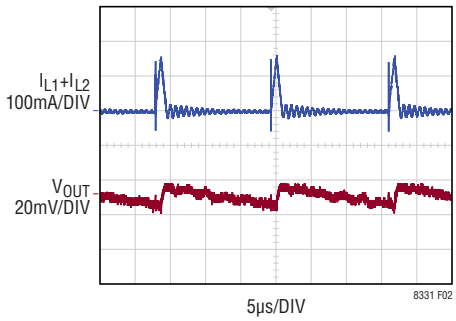


Figure 2. Burst Mode Operation

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No additional components or loading is allowed on this pin. The $INTV_{CC}$ rising threshold (to allow soft-start and switching) is typically 2.6V. The $INTV_{CC}$ falling threshold (to stop switching and reset soft-start) is typically 2.5V.

To improve efficiency across all loads, the majority of $INTV_{CC}$ current can be drawn from the BIAS pin ($4.4V \leq BIAS \leq V_{IN} - 0.4V$) instead of the V_{IN} pin. For flyback or SEPIC applications with V_{IN} often greater than V_{OUT}, the BIAS pin can be directly connected to V_{OUT}. If the BIAS pin is connected to a supply other than V_{OUT}, be sure to bypass the pin with a local ceramic capacitor.

Programming Switching Frequency

The LT8331 uses a constant frequency PWM architecture that can be programmed to switch from 100kHz to 500kHz by using a resistor tied from the RT pin to ground. A table showing the necessary R_T value for a desired switching frequency is in Table 1.

The R_T resistor required for a desired switching frequency can be calculated using:

$$R_T = \frac{32.85}{f_{SW}} - 9.5$$

where R_T is in kΩ and f_{SW} is the desired switching frequency in MHz.

Table 1. SW Frequency vs R_T Value

f_{SW} (MHz)	R_T (kΩ)
0.1	324
0.2	154
0.3	100
0.4	73.2
0.45	63.4
0.5	56.2

Synchronization and Mode Selection

To select low ripple Burst Mode operation, tie the SYNC/MODE pin below 0.6V (this can be ground or a logic low output). To synchronize the LT8331 oscillator to an external frequency connect a square wave (with 20% to 80% duty cycle) to the SYNC pin. The square wave amplitude should have valleys that are below 0.6V and peaks above 2.4V (up to 6V).

The LT8331 will not enter Burst Mode operation at low output loads while synchronized to an external clock, but instead will pulse skip to maintain regulation. The LT8331 may be synchronized over a 100kHz to 625kHz range. The R_T resistor should be chosen to set the LT8331 switching frequency equal to or below the lowest synchronization input. For example, if the synchronization signal will be 500kHz and higher, the R_T should be selected for 500kHz.

For some applications it is desirable for the LT8331 to operate in pulse-skipping mode, offering two major differences from Burst Mode operation. Firstly, the clock stays awake at all times and all switching cycles are aligned to the clock. Secondly, the full switching frequency is reached at lower output load than in Burst Mode operation. These two differences come at the expense of increased quiescent current. To enable pulse-skipping mode, tie the SYNC pin above 2.4V (this can be $INTV_{CC}$ or a logic high output).

DUTY CYCLE CONSIDERATION

The LT8331 minimum on-time, minimum off-time and switching frequency (f_{OSC}) define the allowable minimum and maximum duty cycles of the converter (see Minimum On-Time, Minimum Off-Time, and Switching Frequency in the Electrical Characteristics table).

$$\text{Minimum Allowable Duty Cycle} = \text{Minimum On-Time}_{(MAX)} \bullet f_{OSC(MAX)}$$

$$\text{Maximum Allowable Duty Cycle} = 1 - \text{Minimum Off-Time}_{(MAX)} \bullet f_{OSC(MAX)}$$

The required switch duty cycle range for a Boost converter operating in continuous conduction mode (CCM) can be calculated as:

$$D_{MIN} = 1 - \frac{V_{IN(MAX)}}{(V_{OUT} + V_D)}$$

$$D_{MAX} = 1 - \frac{V_{IN(MIN)}}{(V_{OUT} + V_D)}$$

where V_D is the diode forward voltage drop. If the above duty cycle calculations for a given application violate

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the minimum and/or maximum allowed duty cycles for the LT8331, operation in discontinuous conduction mode (DCM) might provide a solution. For the same V_{IN} and V_{OUT} levels, operation in DCM does not demand as low a duty cycle as in CCM. DCM also allows higher duty cycle operation than CCM. The additional advantage of DCM is the removal of the limitations to inductor value and duty cycle required to avoid sub-harmonic oscillations and the right half plane zero (RHPZ). While DCM provides these benefits, the trade-off is higher inductor peak current, lower available output power and reduced efficiency.

SETTING THE OUTPUT VOLTAGE

The output voltage is programmed with a resistor divider from the output to the FBX pin. Choose the resistor values for a positive output voltage according to:

$$R1 = R2 \bullet \left(\frac{V_{OUT}}{1.60V} - 1\right)$$

Choose the resistor values for a negative output voltage according to:

$$R1 = R2 \bullet \left(\frac{|V_{OUT}|}{0.80V} - 1\right)$$

The locations of R1 and R2 are shown in the Block Diagram. 1% resistors are recommended to maintain output voltage accuracy.

Higher-value FBX divider resistors result in the lowest input quiescent current and highest light-load efficiency. FBX divider resistors R1 and R2 are usually in the range from 25k to 1M.

SOFT-START

The LT8331 contains several features to limit peak switch currents and output voltage (V_{OUT}) overshoot during start-up or recovery from a fault condition. The primary purpose of these features is to prevent damage to external components or the load.

High peak switch currents during start-up may occur in switching regulators. Since V_{OUT} is far from its final value, the feedback loop is saturated and the regulator tries to charge the output capacitor as quickly as possible, resulting in large peak currents. A large surge current may cause inductor saturation or power switch failure.

The LT8331 addresses this mechanism with a programmable soft-start function. As shown in the Block Diagram, the soft-start function controls the ramp of the power switch current by controlling the ramp of VC through Q1. This allows the output capacitor to be charged gradually toward its final value while limiting the start-up peak currents. Figure 3 shows the output voltage and supply current for the first page Typical Applications. It can be seen that both the output voltage and supply current come up gradually.

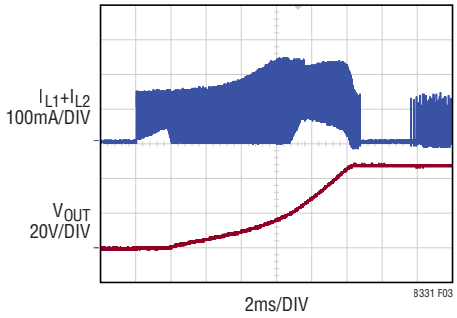


Figure 3. Soft-Start Waveforms

FAULT PROTECTION

An inductor overcurrent fault (> 1.15A) and/or $INTV_{CC}$ undervoltage ($INTV_{CC}$ < 2.5V) and/or thermal lockout (T_J > 170°C) will immediately prevent switching, will reset the SS pin and will pull down VC. Once all faults are removed, the LT8331 will soft-start VC and hence inductor peak current.

FREQUENCY FOLDBACK

During start-up or fault conditions in which V_{OUT} is very low, extremely small duty cycles may be required to maintain control of inductor peak current. The minimum on-time limitation of the power switch might prevent these low duty cycles from being achievable. In this scenario inductor current rise will exceed inductor current fall during each cycle, causing inductor current to "walk up" beyond the switch current limit. The LT8331 provides protection from this by folding back switching frequency whenever FBX pin is close to GND (low V_{OUT} levels). This

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frequency foldback provides a larger switch-off time, allowing inductor current to fall enough each cycle (see Normalized Switching Frequency vs FBX Voltage in the Typical Performance Characteristics section).

THERMAL LOCKOUT

If the LT8331 die temperature reaches 170°C (typical), the part will stop switching and go into thermal lockout. When the die temperature has dropped by 5°C (nominal), the part will resume switching with a soft-started inductor peak current.

COMPENSATION

The LT8331 is internally compensated. The decision to use either low ESR (ceramic) capacitors or the higher ESR (tantalum or OS-CON) capacitors, for the output capacitor, can affect the stability of the overall system. The ESR of any capacitor, along with the capacitance itself, contributes a zero to the system. For the tantalum and OS-CON capacitors, this zero is located at a lower frequency due to the higher value of the ESR, while the zero of a ceramic capacitor is at a much higher frequency and can generally be ignored.

A phase lead zero can be intentionally introduced by placing a capacitor in parallel with the resistor between V_{OUT} and FBX. By choosing the appropriate values for the resistor and capacitor, the zero frequency can be designed to improve the phase margin of the overall converter. The typical target value for the zero frequency is between 5kHz to 20kHz.

A practical approach to compensation is to start with one of the circuits in this data sheet that is similar to your application. Optimize performance by adjusting the output capacitor and/or the feed forward capacitor (connected across the feedback resistor from output to FBX pin).

THERMAL CONSIDERATIONS

Care should be taken in the layout of the PCB to ensure good heat sinking of the LT8331. The package has an exposed pad (Pin 17) underneath the IC which is the best path for heat out of the package. Pin 17 should be soldered to a continuous copper ground plane under the device to reduce die temperature and increase the power capability of the LT8331. The ground plane should be connected to large copper layers to spread heat dissipated by the LT8331. Power dissipation within the LT8331 (P_{DISS_LT8331}) can be estimated by subtracting the inductor and Schottky diode power losses from the total power losses calculated in an efficiency measurement. The junction temperature of LT8331 can then be estimated by:

$$T_J(LT8331) = T_A + \theta_{JA} \bullet P_{DISS_LT8331}$$

APPLICATION CIRCUITS

The LT8331 can be configured for different topologies. The first topology to be analyzed will be the boost converter, followed by the flyback, SEPIC and inverting converters.

Boost Converter: Switch Duty Cycle

The LT8331 can be configured as a boost converter for the applications where the converter output voltage is higher than the input voltage. Remember that boost converters are not short-circuit protected. Under a shorted output condition, the inductor current is limited only by the input supply capability. For applications requiring a step-up converter that is short-circuit protected, please refer to the Applications Information section covering SEPIC converters.

The conversion ratio as a function of duty cycle is:

$$\frac{V_{OUT}}{V_{IN}} = \frac{1}{1 - D}$$

in continuous conduction mode (CCM).

For a boost converter operating in CCM, the duty cycle of the main switch can be calculated based on the output voltage (V_{OUT}) and the input voltage (V_{IN}). The maximum duty cycle (D_{MAX}) occurs when the converter has the minimum input voltage:

$$D_{MAX} = \frac{V_{OUT} - V_{IN(MIN)}}{V_{OUT}}$$

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Discontinuous conduction mode (DCM) provides higher conversion ratios at a given frequency at the cost of reduced efficiencies, higher switching currents, and lower available output power.

Boost Converter: Maximum Output Current Capability and Inductor Selection

For the boost topology, the maximum average inductor current is:

$$I_{L(MAX)(AVE)} = I_{O(MAX)} \bullet \frac{1}{1 - D_{MAX}} \bullet \frac{1}{\eta}$$

where η (< 1.0) is the converter efficiency.

Due to the current limit of its internal power switch, the LT8331 should be used in a boost converter whose maximum output current ($I_{O(MAX)}$) is:

$$I_{O(MAX)} \leq \frac{V_{IN(MIN)}}{V_{OUT}} \bullet \left(0.5A - 0.5 \bullet \Delta I_{SW}\right) \bullet \eta$$

Minimum possible inductor value and switching frequency should also be considered since they will increase inductor ripple current ΔI_{SW}.

The inductor ripple current ΔI_{SW} has a direct effect on the choice of the inductor value and the converter's maximum output current capability. Choosing smaller values of ΔI_{SW} increases output current capability, but requires large inductances and reduces the current loop gain (the converter will approach voltage mode). Accepting larger values of ΔI_{SW} provides fast transient response and allows the use of low inductances, but results in higher input current ripple and greater core losses, and reduces output current capability. It is recommended to choose a ΔI_{SW} of approximately 0.2A to 0.3A.

Given an operating input voltage range, and having chosen the operating frequency and ripple current in the inductor, the inductor value of the boost converter can be determined using the following equation:

$$L = \frac{V_{IN(MIN)}}{\Delta I_{SW} \bullet f_{OSC}} \bullet D_{MAX}$$

The peak inductor current is the switch current limit (maximum 0.7A), and the RMS inductor current is approximately equal to $I_{L(MAX)(AVE)}$.

Choose an inductor that can handle at least 0.7A without saturating, and ensure that the inductor has a low DCR (copper-wire resistance) to minimize I^2R power losses. Note that in some applications, the current handling requirements of the inductor can be lower, such as in the SEPIC topology where each inductor only carries one-half of the total switch current. For better efficiency, use similar valued inductors with a larger volume. Many different sizes and shapes are available from various manufacturers (see Table 2). Choose a core material that has low losses at the programmed switching frequency, such as a ferrite core. The final value chosen for the inductor should not allow peak inductor currents to exceed 0.5A in steady state at maximum load. Due to tolerances, be sure to account for minimum possible inductance value, switching frequency and converter efficiency.

Table 2. Inductor Manufacturers

Sumida	(847) 956-0666	www.sumida.com
TDK	(847) 803-6100	www.tdk.com
Murata	(714) 852-2001	www.murata.com
Coilcraft	(847) 639-6400	www.coilcraft.com
Wurth	(605) 886-4385	www.we-online.com

BOOST CONVERTER: INPUT CAPACITOR SELECTION

Bypass the input of the LT8331 circuit with a ceramic capacitor of X7R or X5R type placed as close as possible to the V_{IN} and GND pins. Y5V types have poor performance over temperature and applied voltage, and should not be used. A 4.7µF to 10µF ceramic capacitor is adequate to bypass the LT8331 and will easily handle the ripple current. If the input power source has high impedance, or there is significant inductance due to long wires or cables, additional bulk capacitance may be necessary. This can be provided with a low performance electrolytic capacitor.

A precaution regarding the ceramic input capacitor concerns the maximum input voltage rating of the LT8331. A ceramic input capacitor combined with trace or cable

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inductance forms a high quality (under damped) tank circuit. If the LT8331 circuit is plugged into a live supply, the input voltage can ring to twice its nominal value, possibly exceeding the LT8331's voltage rating. This situation is easily avoided (see Application Note 88).

BOOST CONVERTER: OUTPUT CAPACITOR SELECTION

Low ESR (equivalent series resistance) capacitors should be used at the output to minimize the output ripple voltage. Multilayer ceramic capacitors are an excellent choice, as they are small and have extremely low ESR. Use X5R or X7R types. This choice will provide low output ripple and good transient response. A 10µF to 47µF output capacitor is sufficient for most applications, but systems with very low output currents may need only a 1µF or 2.2µF output capacitor. Solid tantalum or OS-CON capacitor can be used, but they will occupy more board area than a ceramic and will have a higher ESR. Always use a capacitor with a sufficient voltage rating.

Contributions of ESR (equivalent series resistance), ESL (equivalent series inductance) and the bulk capacitance must be considered when choosing the correct output capacitors for a given output ripple voltage. The effect of these three parameters (ESR, ESL and bulk C) on the output voltage ripple waveform for a typical boost converter is illustrated in Figure 4.

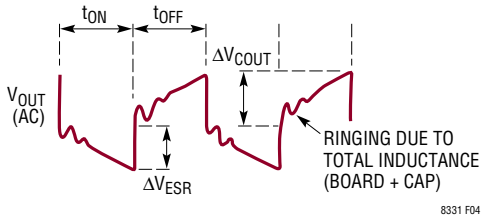


Figure 4. The Output Ripple Waveform of a Boost Converter

The choice of component(s) begins with the maximum acceptable ripple voltage (expressed as a percentage of the output voltage), and how this ripple should be divided between the ESR step ΔV_{ESR} and the charging/discharging ΔV_{COUT}. For the purpose of simplicity, we will choose 2% for the maximum output ripple, to be divided equally between ΔV_{ESR} and ΔV_{COUT}. This percentage ripple will change, depending on the requirements of the application, and the following equations can easily be modified. For a 1% contribution to the total ripple voltage, the ESR of the output capacitor can be determined using the following equation:

$$ESR_{COUT} \leq \frac{0.01 \bullet V_{OUT}}{I_{D(PEAK)}}$$

For the bulk C component, which also contributes 1% to the total ripple:

$$C_{OUT} \geq \frac{I_{O(MAX)}}{0.01 \bullet V_{OUT} \bullet f_{OSC}}$$

The output capacitor in a boost regulator experiences high RMS ripple currents, as shown in Figure 4. The RMS ripple current rating of the output capacitor can be determined using the following equation:

$$I_{RMS(COUT)} \geq I_{O(MAX)} \bullet \sqrt{\frac{D_{MAX}}{1 - D_{MAX}}}$$

Multiple capacitors are often paralleled to meet ESR requirements. Typically, once the ESR requirement is satisfied, the capacitance is adequate for filtering and has the required RMS current rating. Additional ceramic capacitors in parallel are commonly used to reduce the effect of parasitic inductance in the output capacitor, which reduces high frequency switching noise on the converter output.

CERAMIC CAPACITORS

Ceramic capacitors are small, robust and have very low ESR. However, ceramic capacitors can cause problems when used with the LT8331 due to their piezoelectric nature. When in Burst Mode operation, the LT8331's switching frequency depends on the load current, and at very light loads the LT8331 can excite the ceramic capacitor at audio frequencies, generating audible noise. Since the LT8331 operates at a lower current limit during Burst Mode operation, the noise is typically very quiet to a casual ear. If this is unacceptable, use a high performance

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tantalum or electrolytic capacitor at the output. Low noise ceramic capacitors are also available.

Table 3. Ceramic Capacitor Manufacturers

Taiyo Yuden	(408) 573-4150	www.t-yuden.com
AVX	(803) 448-9411	www.avxcorp.com
Murata	(714) 852-2001	www.murata.com

BOOST CONVERTER: DIODE SELECTION

A Schottky diode is recommended for use with the LT8331. Low leakage Schottky diodes are necessary when low quiescent current is desired at low loads. The diode leakage appears as an equivalent load at the output and should be minimized. Choose Schottky diodes with sufficient reverse voltage ratings for the target applications.

Table 4. Recommended Schottky Diodes

PART NUMBER	AVERAGE FORWARD CURRENT (mA)	REVERSE VOLTAGE (V)	REVERSE CURRENT (µA)	MANUFACTURER
DFLS1100	1000	100	1.0	Diodes, Inc.
RB558VA150TR	500	150	0.5	ROHM
RB068L150TE25	2000	150	3.0	ROHM
RF101L2STE25	1000	200	10	ROHM
BAV21W	200	200	0.1	Vishay

BOOST CONVERTER: LAYOUT HINTS

The high speed operation of the LT8331 demands careful attention to board layout. Careless layout will result in performance degradation. Figure 5 shows the recommended component placement for a boost converter. Note the vias under the exposed pad. These should connect to a local ground plane for better thermal performance.

FLYBACK CONVERTER APPLICATIONS

The LT8331 can be configured as a flyback converter for the applications where the converters have multiple outputs, high output voltages or isolated outputs. Figure 6 shows a simplified flyback converter.

The flyback converter has a very low parts count for multiple outputs, and with prudent selection of turns ratio, can have high output/input voltage conversion ratios with a desirable duty cycle. However, it has low efficiency due to the high peak currents, high peak voltages and consequent power loss.

The flyback converter can be designed to operate either in continuous or discontinuous mode. Compared to continuous mode, discontinuous mode has the advantage of

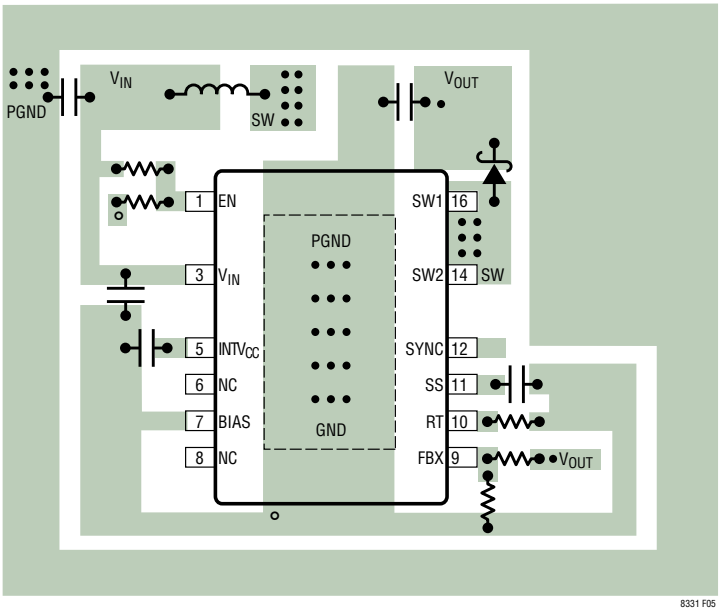


Figure 5. Suggested Boost Converter Layout

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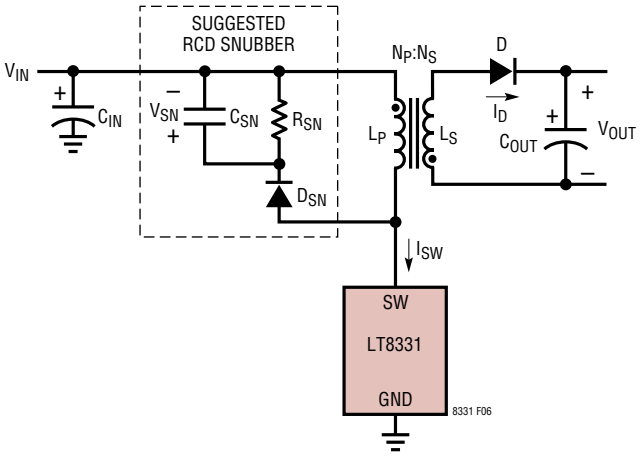


Figure 6. A Simplified Flyback Converter

smaller transformer inductances and easy loop compensation, and the disadvantage of higher peak-to-average current and lower efficiency.

Flyback Converter: Switch Duty Cycle and Turns Ratio

The flyback converter conversion ratio in the continuous mode operation is:

$$\frac{V_{OUT}}{V_{IN}} = \frac{N_S}{N_P} \bullet \frac{D}{1 - D}$$

where N_S/N_P is the second to primary turns ratio. D is duty cycle.

Figure 7 shows the waveforms of the flyback converter in discontinuous mode operation. During each switching period T_S, three subintervals occur: DT_S, $D2T_S$, $D3T_S$. During DT_S, M is on, and D is reverse-biased. During $D2T_S$, M is off, and L_S is conducting current. Both L_P and L_S currents are zero during $D3T_S$.

The flyback converter conversion ratio in the discontinuous mode operation is:

$$\frac{V_{OUT}}{V_{IN}} = \frac{N_S}{N_P} \bullet \frac{D}{D2}$$

According to Figure 6, the peak SW voltage is:

$$V_{SW(PEAK)} = V_{IN(MAX)} + V_{SN}$$

where V_{SN} is the snubber capacitor voltage. A smaller V_{SN} results in a larger snubber loss. A reasonable V_{SN} is 1.5 to 2 times of the reflected output voltage:

$$V_{SN} = k \bullet \frac{V_{OUT} \bullet N_P}{N_S}$$

$$k = 1.5 \sim 2$$

According to the Absolute Maximum Ratings table, the SW voltage Absolute Maximum value is 140V. Therefore, the maximum primary to secondary turns ratio (for both the continuous and the discontinuous operation) should be:

$$\frac{N_P}{N_S} \leq \frac{140V - V_{IN(MAX)}}{k \bullet V_{OUT}}$$

According to the preceding equations, the user has relative freedom in selecting the switch duty cycle or turns ratio to suit a given application. The selections of the duty cycle and the turns ratio are somewhat iterative processes, due to the number of variables involved. The user can choose either a duty cycle or a turns ratio as the start point. The following trade-offs should be considered when selecting the switch duty cycle or turns ratio, to optimize

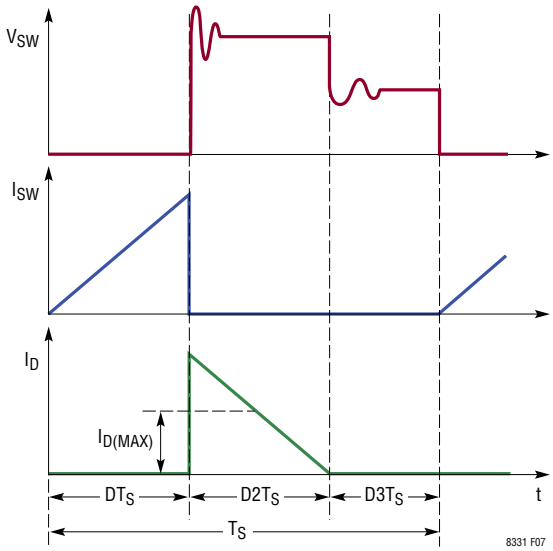


Figure 7. Waveforms of the Flyback Converter in Discontinuous Mode Operation

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the converter performance. A higher duty cycle affects the flyback converter in the following aspects:

- Lower switch RMS current $I_{SW(RMS)}$, but higher switch V_{SW} peak voltage
- Lower diode peak reverse voltage, but higher diode RMS current $I_{D(RMS)}$
- Higher transformer turns ratio (N_P/N_S)

It is recommended to choose a duty cycle between 20% and 80%.

Flyback Converter: Maximum Output Current Capability and Transformer Design

The maximum output current capability and transformer design for continuous conduction mode (CCM) is chosen as presented here.

The maximum duty cycle (D_{MAX}) occurs when the converter has the minimum V_{IN}:

$$D_{MAX} = \frac{V_{OUT} \bullet \left(\frac{N_P}{N_S}\right)}{V_{OUT} \bullet \left(\frac{N_P}{N_S}\right) + V_{IN(MIN)}}$$

Due to the current limit of its internal power switch, the LT8331 should be used in a flyback converter whose maximum output current ($I_{O(MAX)}$) is:

$$I_{O(MAX)} \leq \frac{V_{IN(MIN)}}{V_{OUT}} \bullet D_{MAX} \bullet (0.5A - 0.5 \bullet \Delta I_{SW}) \bullet \eta$$

where η (< 1.0) is the converter efficiency. Minimum possible inductor value and switching frequency should also be considered since they will increase inductor ripple current ΔI_{SW}.

The transformer ripple current ΔI_{SW} has a direct effect on the design/choice of the transformer and the converter's output current capability. Choosing smaller values of ΔI_{SW} increases the output current capability, but requires large primary and secondary inductances and reduces the current loop gain (the converter will approach voltage mode). Accepting larger values of ΔI_{SW} allows the use of low primary and secondary inductances, but results in higher input current ripple, greater core losses, and reduces the output current capability. It is recommended to choose a ΔI_{SW} of approximately 0.2A to 0.3A.

Given an operating input voltage range, and having chosen the operating frequency and ripple current in the primary winding, the primary winding inductance can be calculated using the following equation:

$$L = \frac{V_{IN(MIN)}}{\Delta I_{SW} \bullet f_{OSC}} \bullet D_{MAX}$$

The primary winding peak current is the switch current limit (maximum 0.7A). The primary and secondary maximum RMS currents are:

$$I_{LP(RMS)} \approx \frac{P_{OUT(MAX)}}{D_{MAX} \bullet V_{IN(MIN)} \bullet \eta}$$

$$I_{LS(RMS)} \approx \frac{I_{OUT(MAX)}}{1 - D_{MAX}}$$

Based on the preceding equations, the user should design/choose the transformer having sufficient saturation and RMS current ratings.

Flyback Converter: Snubber Design

Transformer leakage inductance (on either the primary or secondary) causes a voltage spike to occur after the MOSFET turn-off. This is increasingly prominent at higher load currents, where more stored energy must be dissipated. In some cases a snubber circuit will be required to avoid overvoltage breakdown at the MOSFET's drain node. There are different snubber circuits (such as RC snubber, RCD snubber, etc.) and Application Note 19 is a good reference on snubber design. An RCD snubber is shown in Figure 6.

The snubber resistor value (R_{SN}) can be calculated by the following equation:

$$R_{SN} = 2 \bullet \frac{V^2_{SN} - V_{SN} \bullet V_{OUT} \bullet \frac{N_P}{N_S}}{I^2_{SW(PEAK)} \bullet L_{LK} \bullet f_{OSC}}$$

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L_{LK} is the leakage inductance of the primary winding, which is usually specified in the transformer characteristics. L_{LK} can be obtained by measuring the primary inductance with the secondary windings shorted. The snubber capacitor value (C_{SN}) can be determined using the following equation:

$$C_{SN} = \frac{V_{SN}}{\Delta V_{SN} \bullet R_{SN} \bullet f_{OSC}}$$

where ΔV_{SN} is the voltage ripple across C_{SN}. A reasonable ΔV_{SN} is 5% to 10% of V_{SN}. The reverse voltage rating of D_{SN} should be higher than the sum of V_{SN} and $V_{IN(MAX)}$.

Flyback Converter: Output Diode Selection

The output diode in a flyback converter is subject to large RMS current and peak reverse voltage stresses. A fast switching diode with a low forward drop and a low reverse leakage is desired. Schottky diodes are recommended if the output voltage is below 100V.

Approximate the required peak repetitive reverse voltage rating V_{RRM} using:

$$V_{RRM} > \frac{N_S}{N_P} \bullet V_{IN(MAX)} + V_{OUT}$$

The power dissipated by the diode is:

$$P_D = I_{O(MAX)} \bullet V_D$$

and the diode junction temperature is:

$$T_J = T_A + P_D \bullet R\theta_{JA}$$

The $R_{\theta JA}$ to be used in this equation normally includes the $R_{\theta JC}$ for the device, plus the thermal resistance from the board to the ambient temperature in the enclosure. T_J must not exceed the diode maximum junction temperature rating.

Flyback Converter: Output Capacitor Selection

The output capacitor of the flyback converter has a similar operation condition as that of the boost converter. Refer to the Boost Converter: Output Capacitor Selection section for the calculation of C_{OUT} and ESR_{COUT}.

The RMS ripple current rating of the output capacitors in continuous operation can be determined using the following equation:

$$I_{RMS(COUT),CONTINUOUS} \approx I_{O(MAX)} \bullet \sqrt{\frac{D_{MAX}}{1 - D_{MAX}}}$$

Flyback Converter: Input Capacitor Selection

The input capacitor in a flyback converter is subject to a large RMS current due to the discontinuous primary current. To prevent large voltage transients, use a low ESR input capacitor sized for the maximum RMS current. The RMS ripple current rating of the input capacitors in continuous operation can be determined using the following equation:

$$I_{RMS(CIN),CONTINUOUS} \approx \frac{P_{OUT(MAX)}}{V_{IN(MIN)} \bullet \eta} \bullet \sqrt{\frac{1-D_{MAX}}{D_{MAX}}}$$

SEPIC CONVERTER APPLICATIONS

The LT8331 can be configured as a SEPIC (single-ended primary inductance converter), as shown in Figure 8. This topology allows for the input to be higher, equal, or lower than the desired output voltage. The conversion ratio as a function of duty cycle is:

$$\frac{V_{OUT} + V_D}{V_{IN}} = \frac{D}{1 - D}$$

in continuous conduction mode (CCM).

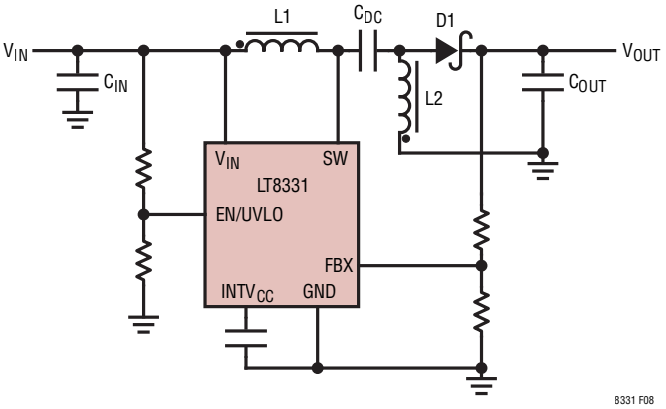


Figure 8. LT8331 Configured in a SEPIC Topology

APPLICATIONS INFORMATION

In a SEPIC converter, no DC path exists between the input and output. This is an advantage over the boost converter for applications requiring the output to be disconnected from the input source when the circuit is in shutdown.

SEPIC Converter: Switch Duty Cycle and Frequency

For a SEPIC converter operating in CCM, the duty cycle of the main switch can be calculated based on the output voltage (V_{OUT}), the input voltage (V_{IN}) and the diode forward voltage (V_D).

The maximum duty cycle (D_{MAX}) occurs when the converter operates at the minimum input voltage:

$$D_{MAX} = \frac{V_{OUT} + V_D}{V_{IN(MIN)} + V_{OUT} + V_D}$$

Conversely, the minimum duty cycle (D_{MIN}) occurs when the converter operates at the maximum input voltage:

$$D_{MIN} = \frac{V_{OUT} + V_D}{V_{IN(MAX)} + V_{OUT} + V_D}$$

Be sure to check that D_{MAX} and D_{MIN} obey:

$$D_{MAX} < 1 - \text{Minimum Off-Time}_{(MAX)} \bullet f_{OSC(MAX)}$$

and

$$D_{MIN} > \text{Minimum On-Time}_{(MAX)} \bullet f_{OSC(MAX)}$$

where Minimum Off-Time, Minimum On-Time and f_{OSC} are specified in the Electrical Characteristics table.

SEPIC Converter: The Maximum Output Current Capability and Inductor Selection

As shown in Figure 8, the SEPIC converter contains two inductors: L1 and L2. L1 and L2 can be independent, but can also be wound on the same core, since identical voltages are applied to L1 and L2 throughout the switching cycle.

For the SEPIC topology, the current through L1 is the converter input current. Based on the fact that, ideally, the output power is equal to the input power, the maximum average inductor currents of L1 and L2 are:

$$I_{L1(MAX)(AVE)} = I_{IN(MAX)(AVE)} = I_{O(MAX)} \bullet \frac{D_{MAX}}{1 - D_{MAX}}$$

$$I_{L2(MAX)(AVE)} = I_{O(MAX)}$$

In a SEPIC converter, the switch current is equal to $I_{L1} + I_{L2}$ when the power switch is on, therefore, the maximum average switch current is defined as:

$$I_{SW(MAX)(AVE)} = I_{L1(MAX)(AVE)} + I_{L2(MAX)(AVE)}$$

$$= I_{O(MAX)} \bullet \frac{1}{1 - D_{MAX}}$$

and the peak switch current is:

$$I_{SW(PEAK)} = \left(1 + \frac{\chi}{2}\right) \bullet I_{O(MAX)} \bullet \frac{1}{1 - D_{MAX}}$$

The constant χ in the preceding equations represents the percentage peak-to-peak ripple current in the switch, relative to $I_{SW(MAX)(AVE)}$, as shown in Figure 9. Then, the switch ripple current ΔI_{SW} can be calculated by:

$$\Delta I_{SW} = \chi \bullet I_{SW(MAX)(AVE)}$$

The inductor ripple currents ΔI_{L1} and ΔI_{L2} are identical:

$$\Delta I_{L1} = \Delta I_{L2} = 0.5 \bullet \Delta I_{SW}$$

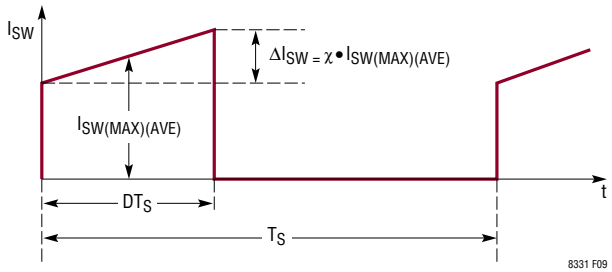


Figure 9. The Switch Current Waveform of the SEPIC Converter

APPLICATIONS INFORMATION

The inductor ripple current has a direct effect on the choice of the inductor value. Choosing smaller values of ΔI_L requires large inductances and reduces the current loop gain (the converter will approach voltage mode). Accepting larger values of ΔI_L allows the use of low inductances, but results in higher input current ripple and greater core losses. It is recommended that χ falls in the range of 0.5 to 0.8.

Due to the current limit of its internal power switch, the LT8331 should be used in a SEPIC converter whose maximum output current ($I_{O(MAX)}$) is:

$$I_{O(MAX)} < (1 - D_{MAX}) \bullet (0.5A - 0.5 \bullet \Delta I_{SW}) \bullet \eta$$

where η (< 1.0) is the converter efficiency. Minimum possible inductor value and switching frequency should also be considered since they will increase inductor ripple current ΔI_{SW}.

Given an operating input voltage range, and having chosen ripple current in the inductor, the inductor value (L1 and L2 are independent) of the SEPIC converter can be determined using the following equation:

$$L1 = L2 = \frac{V_{IN(MIN)}}{0.5 \bullet \Delta I_{SW} \bullet f_{OSC}} \bullet D_{MAX}$$

For most SEPIC applications, the equal inductor values will fall in the range of 4.7µH to 220µH.

By making L1 = L2, and winding them on the same core, the value of inductance in the preceding equation is replaced by 2L, due to mutual inductance:

$$L = \frac{V_{IN(MIN)}}{\Delta I_{SW} \bullet f_{OSC}} \bullet D_{MAX}$$

This maintains the same ripple current and energy storage in the inductors. The peak inductor currents are:

$$I_{L1(PEAK)} = I_{L1(MAX)} + 0.5 \bullet \Delta I_{L1}$$

$$I_{L2(PEAK)} = I_{L2(MAX)} + 0.5 \bullet \Delta I_{L2}$$

The maximum RMS inductor currents are approximately equal to the maximum average inductor currents.

Based on the preceding equations, the user should choose the inductors having sufficient saturation and RMS current ratings.

SEPIC Converter: Output Diode Selection

To maximize efficiency, a fast switching diode with a low forward drop and low reverse leakage is desirable. The average forward current in normal operation is equal to the output current.

It is recommended that the peak repetitive reverse voltage rating V_{RRM} is higher than $V_{OUT} + V_{IN(MAX)}$ by a safety margin (a 10V safety margin is usually sufficient).

The power dissipated by the diode is:

$$P_D = I_{O(MAX)} \bullet V_D$$

where V_D is diode's forward voltage drop, and the diode junction temperature is:

$$T_J = T_A + P_D \bullet R\theta_{JA}$$

The $R_{\theta JA}$ used in this equation normally includes the $R_{\theta JC}$ for the device, plus the thermal resistance from the board, to the ambient temperature in the enclosure. T_J must not exceed the diode maximum junction temperature rating.

SEPIC Converter: Output and Input Capacitor Selection

The selections of the output and input capacitors of the SEPIC converter are similar to those of the boost converter.

SEPIC Converter: Selecting the DC Coupling Capacitor

The DC voltage rating of the DC coupling capacitor (C_{DC}, as shown in Figure 10) should be larger than the maximum input voltage:

$$V_{CDC} > V_{IN(MAX)}$$

APPLICATIONS INFORMATION

C_{DC} has nearly a rectangular current waveform. During the switch off-time, the current through C_{DC} is I_{IN}, while approximately $-I_O$ flows during the on-time. The RMS rating of the coupling capacitor is determined by the following equation:

$$I_{RMS(CDC)} > I_{O(MAX)} \bullet \sqrt{\frac{V_{OUT} + V_D}{V_{IN(MIN)}}}$$

A low ESR and ESL, X5R or X7R ceramic capacitor works well for C_{DC}.

INVERTING CONVERTER APPLICATIONS

The LT8331 can be configured as a dual-inductor inverting topology, as shown in Figure 10. The V_{OUT} to V_{IN} ratio is:

$$\frac{|V_{OUT} + V_D|}{V_{IN}} = \frac{D}{1-D}$$

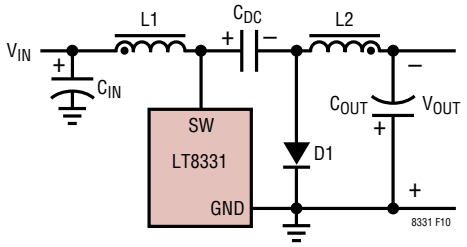


Figure 10. A Simplified Inverting Converter

in continuous conduction mode (CCM).

Inverting Converter: Switch Duty Cycle and Frequency

For an inverting converter operating in CCM, the duty cycle of the main switch can be calculated based on the negative output voltage (V_{OUT}) and the input voltage (V_{IN}).

The maximum duty cycle (D_{MAX}) occurs when the converter has the minimum input voltage:

$$D_{MAX} = \frac{|V_{OUT}| + V_D}{|V_{OUT}| + V_D + V_{IN(MIN)}}$$

Conversely, the minimum duty cycle (D_{MIN}) occurs when the converter operates at the maximum input voltage :

$$D_{MIN} = \frac{|V_{OUT}| + V_D}{|V_{OUT}| + V_D + V_{IN(MAX)}}$$

Be sure to check that D_{MAX} and D_{MIN} obey :

$$D_{MAX} < 1 - \text{Minimum Off-Time}_{(MAX)} \bullet f_{OSC(MAX)}$$

and

$$D_{MIN} > \text{Minimum On-Time}_{(MAX)} \bullet f_{OSC(MAX)}$$

where Minimum Off-Time, Minimum On-Time and f_{OSC} are specified in the Electrical Characteristics table.

Inverting Converter: Inductor, Output Diode and Input Capacitor Selections

The selections of the inductor, output diode and input capacitor of an inverting converter are similar to those of the SEPIC converter. Please refer to the corresponding SEPIC converter sections.

Inverting Converter: Output Capacitor Selection

The inverting converter requires much smaller output capacitors than those of the boost, flyback and SEPIC converters for similar output ripples. This is due to the fact that, in the inverting converter, the inductor L2 is in series with the output, and the ripple current flowing through the output capacitors are continuous. The output ripple voltage is produced by the ripple current of L2 flowing through the ESR and bulk capacitance of the output capacitor:

$$\Delta V_{OUT(P-P)} = \Delta I_{L2} \bullet \left(ESR_{COUT} + \frac{1}{8 \bullet f_{OSC} \bullet C_{OUT}} \right)$$

After specifying the maximum output ripple, the user can select the output capacitors according to the preceding equation.

APPLICATIONS INFORMATION

The ESR can be minimized by using high quality X5R or X7R dielectric ceramic capacitors. In many applications, ceramic capacitors are sufficient to limit the output voltage ripple.

The RMS ripple current rating of the output capacitor needs to be greater than:

$$I_{RMS(COUT)} > 0.3 \bullet \Delta I_{L2}$$

Inverting Converter: Selecting the DC Coupling Capacitor

The DC voltage rating of the DC coupling capacitor (C_{DC}, as shown in Figure 10) should be larger than the maximum input voltage minus the output voltage (negative voltage):

$$V_{CDC} > V_{IN(MAX)} - V_{OUT}$$

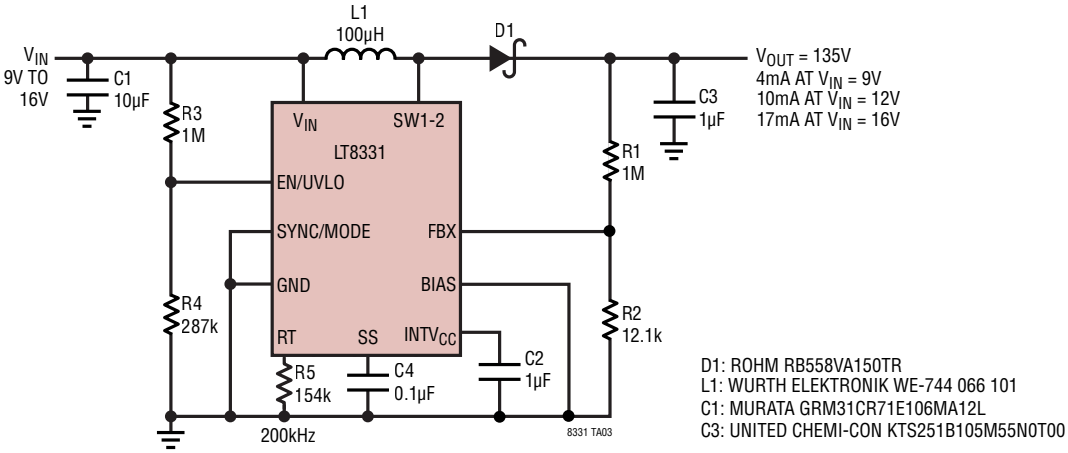
C_{DC} has nearly a rectangular current waveform. During the switch off-time, the current through C_{DC} is I_{IN}, while approximately $-I_O$ flows during the on-time. The RMS rating of the coupling capacitor is determined by the following equation:

$$I_{RMS(CDC)} > I_{O(MAX)} \bullet \sqrt{\frac{D_{MAX}}{1 - D_{MAX}}}$$

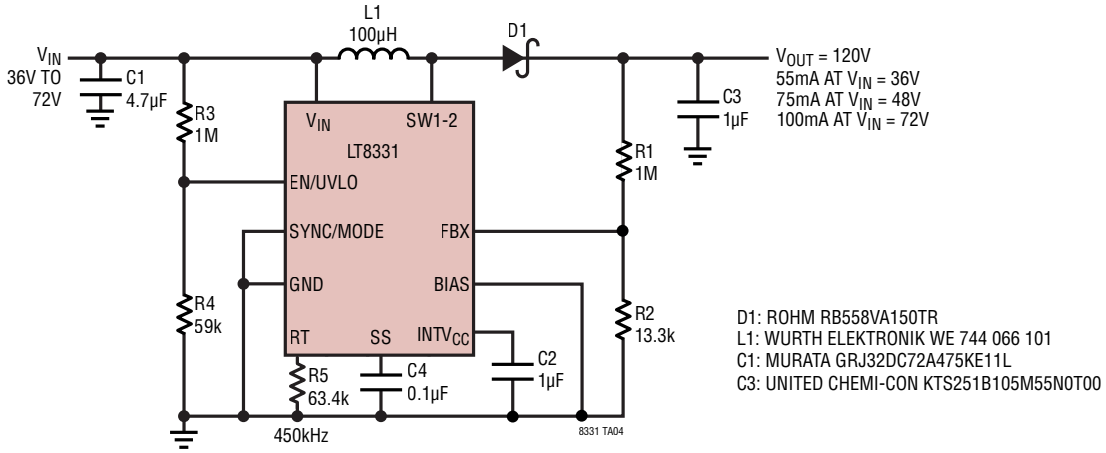
A low ESR and ESL, X5R or X7R ceramic capacitor works well for C_{DC}.

TYPICAL APPLICATIONS

9V to 16V Input, 135V Boost Converter

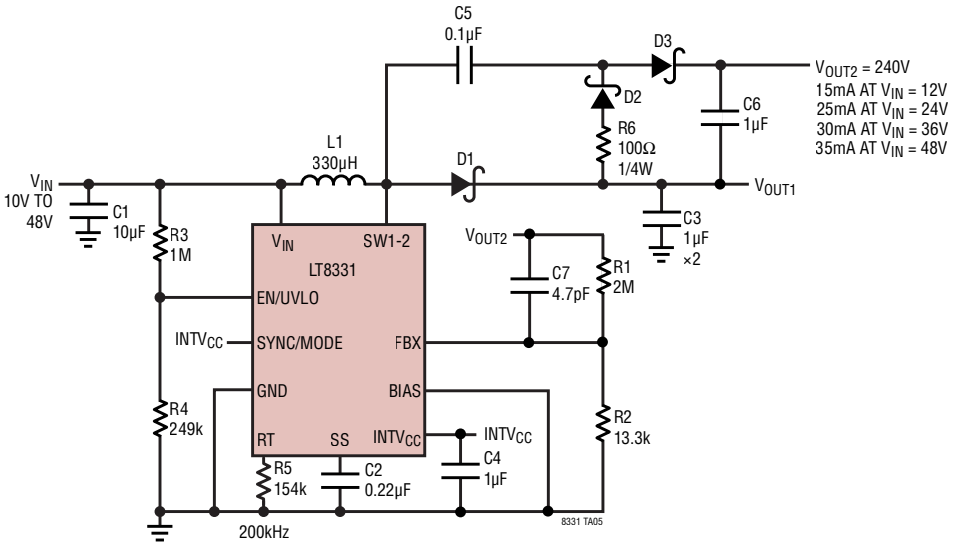


36V to 72V Input,120V Boost Converter



TYPICAL APPLICATIONS

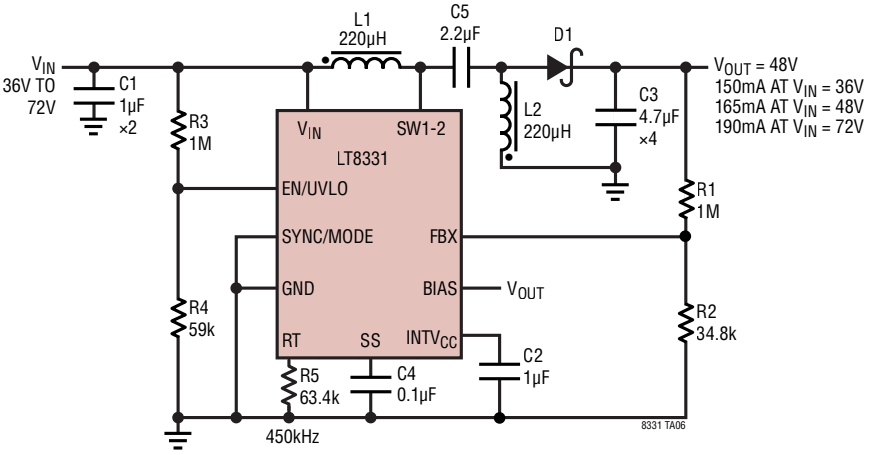
10V to 48V Input, 240V Boost Converter



D1, D2, D3: DIODES INC. BAV21W
L1: SUMIDA CDRH8D43RT125NP-331MC
C1: MURATA GRM31CR61H106KA12L

C3, C6: MURATA GRM55DR72E105KW01L
C5: MURATA GRM31CR72D104KW03L
C7: MURATA GQM2195C2E4R7CB12J

36V to 72V Input, 48V SEPIC Converter

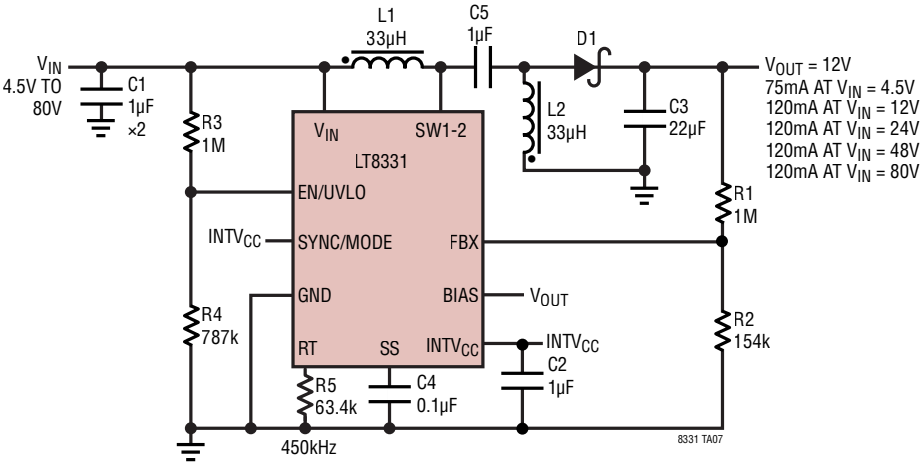


D1: ROHM RB558VA150TR
L1, L2: COILTRONICS DRQ127-221
C1: MURATA GRM32ER72A105KA01L

C3: MURATA GRJ32DC72A475KE11L
C5: MURATA GRM31CR72A225KA73L

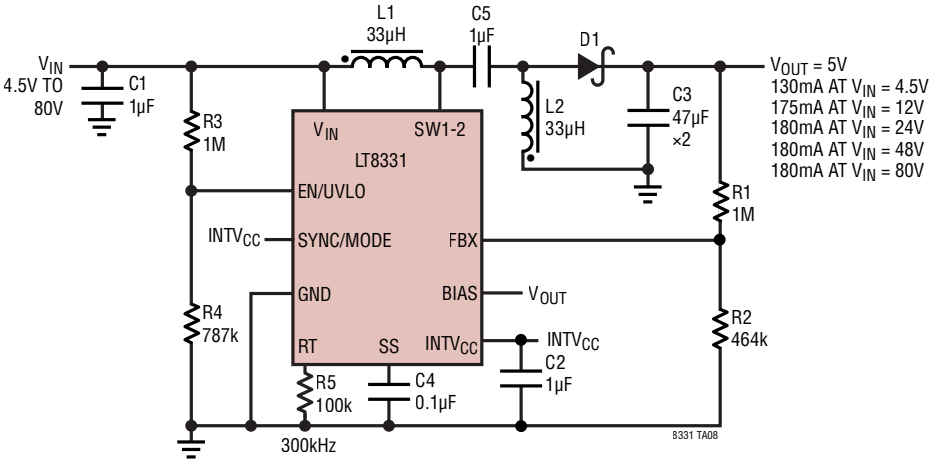
TYPICAL APPLICATIONS

4.5V to 80V Input, 12V SEPIC Converter



D1: ROHM RB578VAM100TR
L1, L2: COILTRONICS DRQ74-330
C1: MURATA GRM32ER72A105KA01L
C3: MURATA GRM32ER71E226KE15L
C5: MURATA GRM31CR72A105KA01L

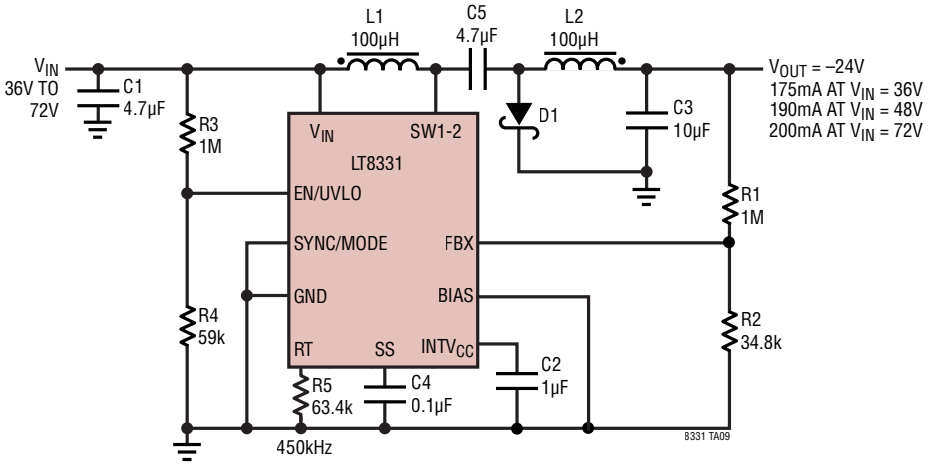
4.5V to 80V Input, 5V SEPIC Converter



D1: ROHM RB578VAM100TR
L1, L2: COILTRONICS DRQ74-330
C1: MURATA GRM32ER72A105KA01L
C3: MURATA GRM31CR61A476ME15L
C5: MURATA GRM31CR72A105KA01L

TYPICAL APPLICATIONS

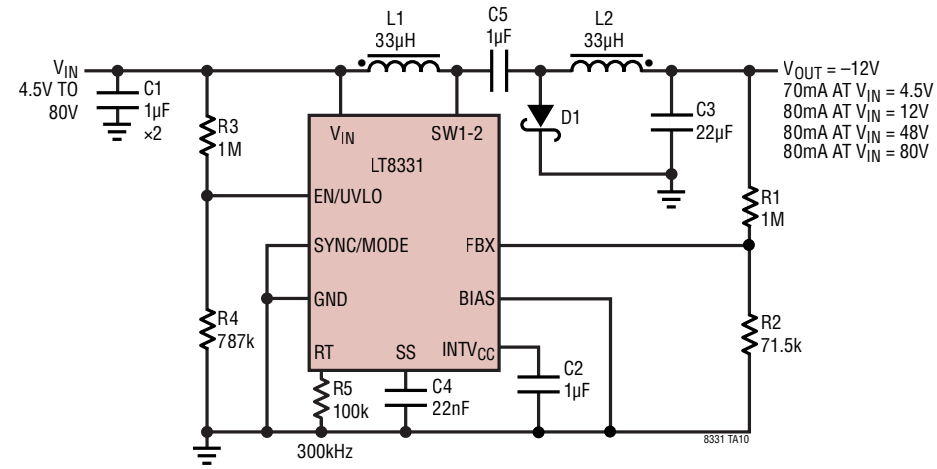
36V to 72V Input, –24V Inverting Converter



D1: ROHM RB558VA150TR
L1, L2: COILTRONICS DRQ127-101
C1: MURATA GRM32DC72A475K11L

C3: MURATA GRM31CR61H106KA12L
C5: MURATA GRM32DC72A475K11L

4.5V to 80V Input, –12V Inverting Converter

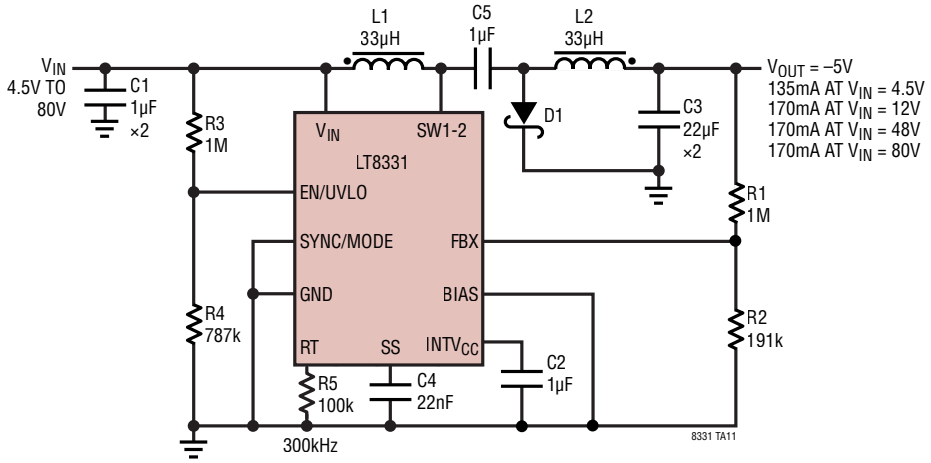


D1: DIODES INC. DFLS1100
L1, L2: COILTRONICS DRQ74-330
C1: MURATA GRM32ER72A105KA01L

C3: MURATA GRM32ER61A226KE20L
C5: MURATA GRM31CR72A105KA01L

TYPICAL APPLICATIONS

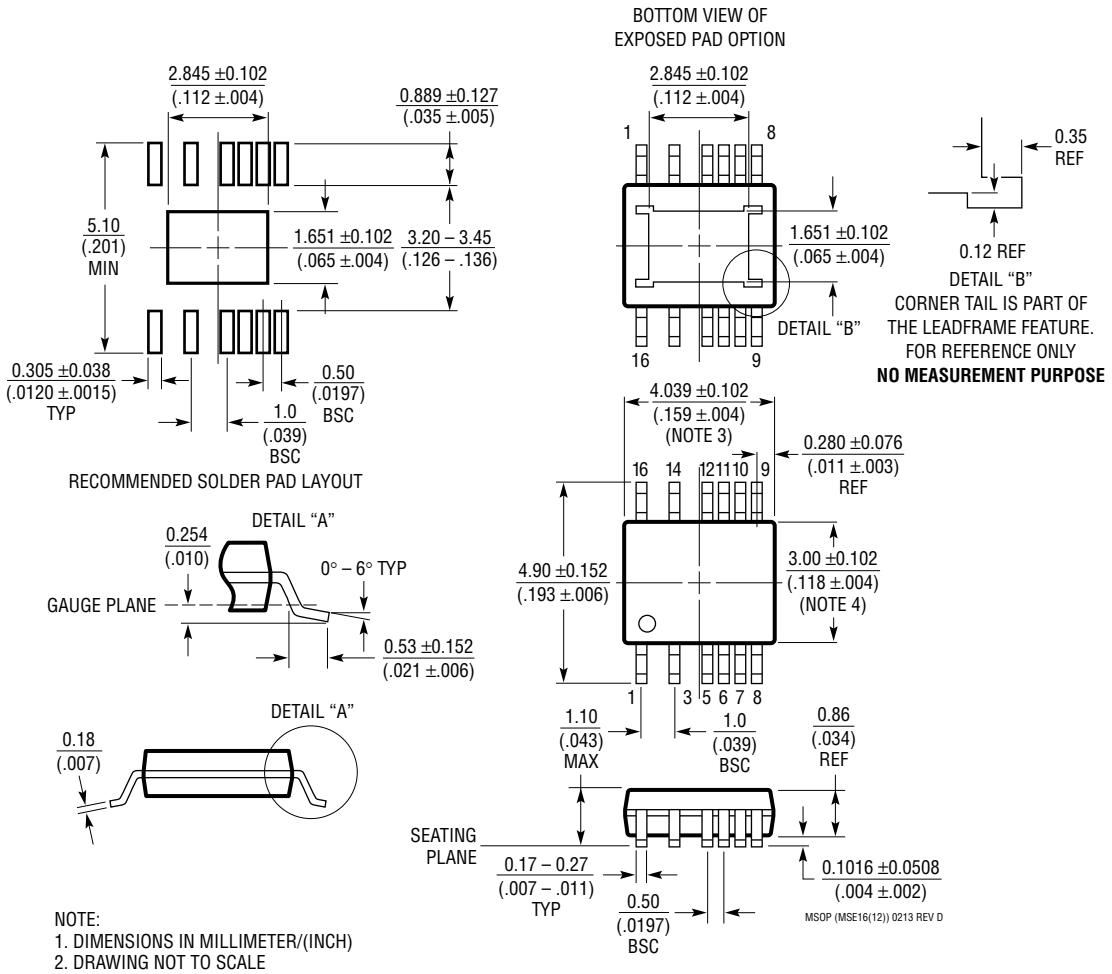
4.5V to 80V Input, –5V Inverting Converter



D1: DIODES INC. DFLS1100
L1, L2: COILTRONICS DRQ74-330
C1: MURATA GRM32ER72A105KA01L
C3: MURATA GRM32ER61A226KE20L
C5: MURATA GRM31CR72A105KA01L

PACKAGE DESCRIPTION

MSE Package
Variation: MSE16 (12)
16-Lead Plastic MSOP with 4 Pins Removed
Exposed Die Pad
(Reference LTC DWG # 05-08-1871 Rev D)



NOTE:
1. DIMENSIONS IN MILLIMETER/(INCH)
2. DRAWING NOT TO SCALE
3. DIMENSION DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS.
   MOLD FLASH, PROTRUSIONS OR GATE BURRS SHALL NOT EXCEED 0.152mm (.006") PER SIDE
4. DIMENSION DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSIONS.
   INTERLEAD FLASH OR PROTRUSIONS SHALL NOT EXCEED 0.152mm (.006") PER SIDE
5. LEAD COPLANARITY (BOTTOM OF LEADS AFTER FORMING) SHALL BE 0.102mm (.004") MAX
6. EXPOSED PAD DIMENSION DOES INCLUDE MOLD FLASH. MOLD FLASH ON E-PAD SHALL
   NOT EXCEED 0.254mm (.010") PER SIDE.

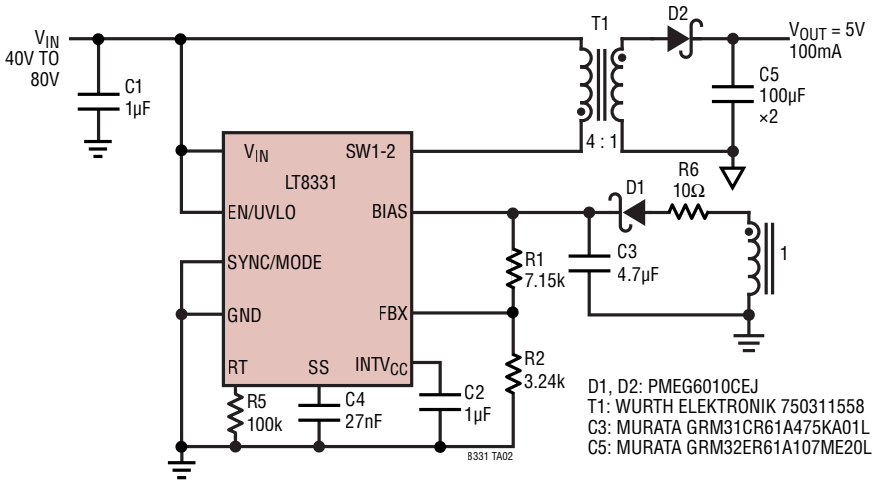
REVISION HISTORY

REV	DATE	DESCRIPTION	PAGE NUMBER
A	08/16	Updated 10V to 48V Input schematic.	24
B	05/19	Corrected Typo in V_{IN} Quiescent Current.	2
C	03/20	Added to Features Section. Added Automotive Products. Corrected D_{MIN} equation.	1, 2, 21

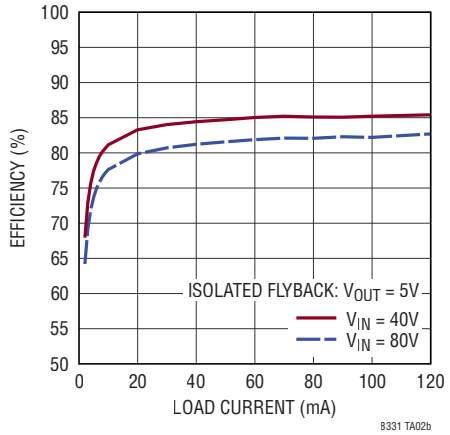
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TYPICAL APPLICATION

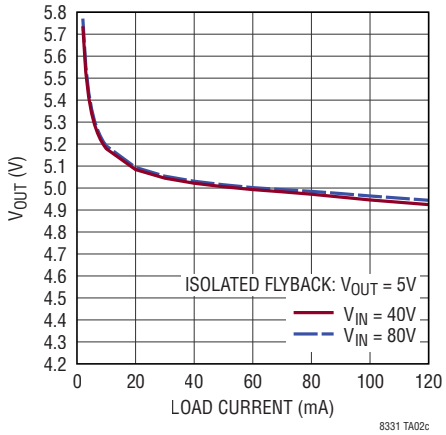
40V to 80V Input, 5V Isolated Output Converter



Efficiency



Load Regulation



RELATED PARTS

PART NUMBER	DESCRIPTION	COMMENTS
LT8300	100V_{IN} Micropower Isolated Flyback Converter with 150V/260mA Switch	V_{IN} = 6V to 100V, Low I_Q Monolithic No-Opto Flyback, 5-Lead TSOT-23
LT8330	60V, 1A, Low I_Q Boost/SEPIC/Inverting Converter	V_{IN} = 3V to 40V, $V_{OUT(MAX)}$ = 60V, I_Q = 6µA (Burst Mode Operation), 6-Lead TSOT-23, 3mm × 2mm DFN packages
LT8494	70V, 2A Boost/SEPIC 1.5MHz High Efficiency Step-Up DC/DC Converter	V_{IN} = 1V to 60V (2.5V to 32V Start-Up), $V_{OUT(MAX)}$ = 70V, I_Q = 3µA (Burst Mode Operation), I_{SD} = <1µA, 20-Lead TSSOP
LT8570/LT8570-1	65V, 500mA/250mA Boost/Inverting DC/DC Converter	$V_{IN(MIN)}$ = 2.55V, $V_{IN(MAX)}$ = 40V, $V_{OUT(MAX)}$ = ±60V, I_Q = 1.2mA, I_{SD} = <1mA, 3mm × 3mm DFN-8, MSOP-8E
LT8580	1A (I_{SW}), 65V, 1.5MHz, High Efficiency Step-Up DC/DC Converter	V_{IN}: 2.55V to 40V, $V_{OUT(MAX)}$ = 65V, I_Q = 1.2mA, I_{SD} = <1µA, 3mm × 3mm DFN-8, MSOP-8E

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