# 600$V_{IN}$ Micropower No-Opto Isolated Flyback Controller

## FEATURES

- **Wide Input Voltage Range: 16V to 600V**
- **No Opto-Isolator Required for Regulation**
- **Quasi-Resonant Boundary Mode Operation**
- **Constant-Current and Constant-Voltage Regulation**
- Low-Ripple Light Load Burst Mode® Operation
- Low Quiescent Current: 75µA
- Programmable Current Limit and Soft-Start
- TSSOP Package with High-Voltage Spacing

## APPLICATIONS

- Isolated Telecom, Automotive, Industrial, Medical Power Supplies
- Isolated Off-Line Housekeeping Power Supplies
- Electric Vehicles and Battery Stacks
- Multioutput Isolated Power Supplies for Inverter Gate Drives

## DESCRIPTION

The LT®8316 is a micropower, high voltage flyback controller. No opto-isolator is needed for regulation. The device samples the output voltage from the isolated flyback waveform appearing across a third winding on the transformer. Quasi-resonant boundary mode operation improves load regulation, reduces transformer size, and maintains high efficiency.

At start-up, the LT8316 charges its $INTV_{CC}$ capacitor via a high voltage current source. During normal operation, the current source turns off and the device draws its power from a third winding on the transformer minimizing standby power dissipation.

The LT8316 operates from a wide range of input supply voltages and can deliver up to 100W of power. It is available in a thermally enhanced 20-pin TSSOP package with four pins removed for high-voltage spacing.

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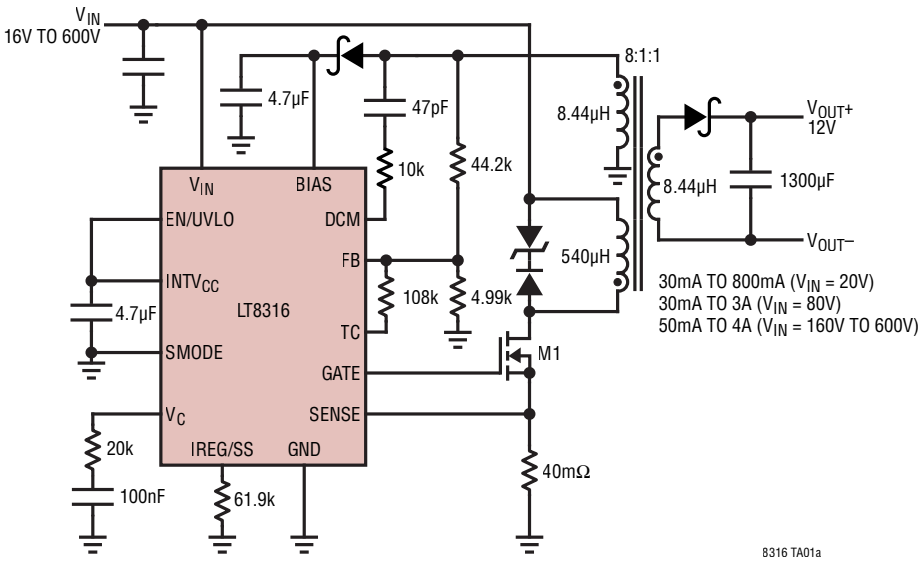
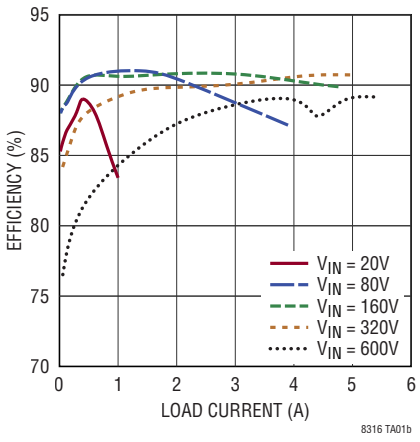
## TYPICAL APPLICATION

**16$V_{IN}$ to 600$V_{IN}$ Isolated 12$V_{OUT}$ Supply**




**Efficiency**

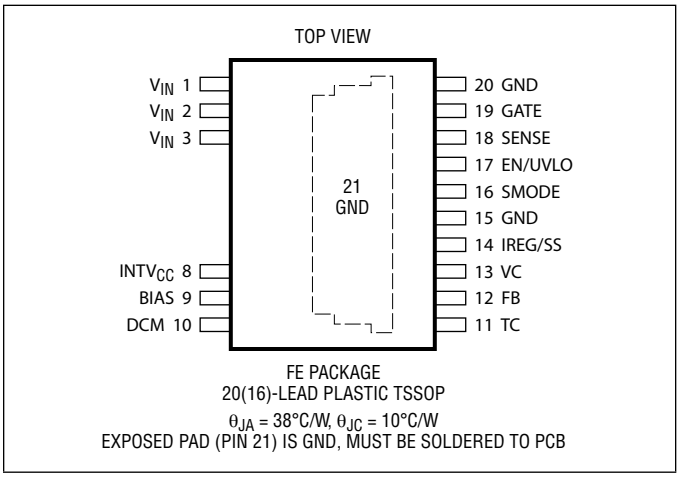


## ABSOLUTE MAXIMUM RATINGS

**(Note 1)**

$V_{IN}$ .....600V
BIAS, EN/UVLO.....40V
$INTV_{CC}$.....15V
SMODE, GATE..... $INTV_{CC}$
SENSE, TC, FB, $V_C$, IREG/SS.....4V
DCM.....±100mA
Operating Junction Temperature (Note 2)
LT8316E, LT8316I ..... –40°C to 125°C
Storage Temperature Range ..... –65°C to 150°C
Lead Temperature (Soldering, 10 sec).....300°C

## PIN CONFIGURATION




FE PACKAGE
20(16)-LEAD PLASTIC TSSOP
$\theta_{JA}$ = 38°C/W, $\theta_{JC}$ = 10°C/W
EXPOSED PAD (PIN 21) IS GND, MUST BE SOLDERED TO PCB

## ORDER INFORMATION

| LEAD FREE FINISH | TAPE AND REEL | PART MARKING* | PACKAGE DESCRIPTION | TEMPERATURE RANGE |
|---|---|---|---|---|
| LT8316EFE#PBF | LT8316EFE#TRPBF | LT8316FE | 20-Lead Plastic TSSOP | –40°C to 125°C |
| LT8316IFE#PBF | LT8316IFE#TRPBF | LT8316FE | 20-Lead Plastic TSSOP | –40°C to 125°C |

Contact the factory for parts specified with wider operating temperature ranges. *The temperature grade is identified by a label on the shipping container.

Tape and reel specifications. Some packages are available in 500 unit reels through designated sales channels with #TRMPBF suffix.

## ELECTRICAL CHARACTERISTICS

**The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at $T_A$ = 25°C. BIAS = 30V, $V_{EN/UVLO}$ = 30V unless otherwise noted.**

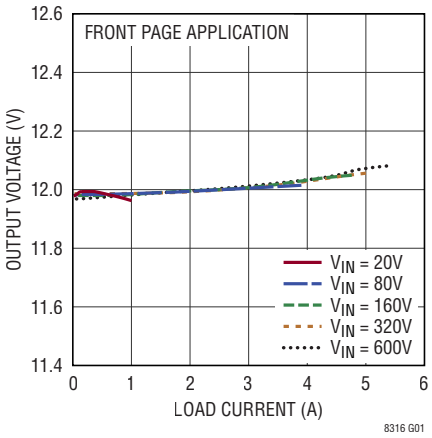
| SYMBOL | PARAMETER | CONDITIONS | | MIN | TYP | MAX | UNITS |
|---|---|---|---|---|---|---|---|
| BIAS | Chip Bias Voltage Supply Range | After Startup | | 9.5 | | | V |
| $I_Q$ | BIAS Quiescent Current | Burst Mode Operation<br>Active | | | 75<br>470 | 150<br>700 | µA |
| $I_{CLAMP(MAX)}$ | BIAS Clamp Maximum Current | | | | | 15 | mA |
| $V_{CLAMP}$ | BIAS Clamping Voltage | $I_{CLAMP}$ = 200µA<br>$I_{CLAMP}$ = 15mA | | 34<br>35 | | 38<br>39 | V<br>V |
| $I_{SHDN}$ | $V_{IN}$ Shutdown Current | $V_{EN/UVLO}$ < 0.3V, BIAS = Floating | | | 12 | 20 | µA |
| $V_{IN(MIN)}$ | Minimum Input Voltage for Startup | BIAS = Floating | ● | | | 16 | V |
| $I_{STARTUP}$ | Startup Current Out of $INTV_{CC}$ | $V_{IN}$ = 16V, BIAS = Floating | ● | 100 | 300 | | µA |
| $V_{UVLO}$ | EN/UVLO Threshold<br>EN/UVLO Hysteresis | $V_{EN/UVLO}$ Falling<br>$V_{EN/UVLO}$ Rising | | 1.18<br>30 | 1.22<br>65 | 1.26<br>120 | V<br>mV |
| | $INTV_{CC}$ UVLO Rising Threshold | Startup Current through Depletion FET | | 11.1 | 12 | 13.1 | V |
| | $INTV_{CC}$ UVLO Falling Threshold | | | 7.6 | 8.1 | 8.6 | V |
| | $INTV_{CC}$ Regulation Voltage | Drawing 20mA from $INTV_{CC}$ | | 9.5 | 10 | 10.5 | V |
| | $INTV_{CC}$ LDO Dropout Voltage | Drawing 20mA from $INTV_{CC}$ | | | | 1 | V |
| | Gate Driver Rise Time | $C_{GATE}$ = 3.3nF, 10% to 90% | | | 30 | | ns |
| | Gate Driver Fall Time | $C_{GATE}$ = 3.3nF, 90% to 10% | | | 8 | | ns |
| $V_{REG}$ | FB Regulation Voltage | | ● | 1.18 | 1.22 | 1.25 | V |
| $G_M$ | Voltage Error Amplifier Transconductance | $V_{FB}$ = 1.22V ± 5mV | | 245 | 350 | 455 | µS |
| $V_{TC}$ | TC Voltage<br>TC Voltage Temperature Coefficient | $T_A$ = 25°C | | | 1.22<br>+4.1 | | V<br>mV/°C |
| $I_{TC}$ | TC Sinking/Sourcing Current | | | ±100 | | | µA |
| $I_{IREG/SS}$ | IREG/SS Current | Current Out-of-Pin | | 9.7 | 10 | 10.3 | µA |
| $I_{DCM}$ | Flyback Collapse Detection Threshold<br>Resonant Valley Detection Threshold | $I_{DCM}$ Rising<br>$I_{DCM}$ Falling | | | –170<br>–85 | | µA<br>µA |
| $V_{SENSE(MIN)}$ | Minimum Current Voltage Threshold | | | 14 | 20 | 26 | mV |
| $V_{SENSE(MAX)}$ | Maximum Current Voltage Threshold | | | 90 | 100 | 110 | mV |
| | SENSE Input Bias Current | Current Out-of-Pin | | | 35 | | µA |
| $F_{SW(MIN)}$ | Minimum Switching Frequency | Burst Mode<br>Standby Mode | | 3<br>187 | 3.5<br>220 | 4<br>250 | kHz<br>Hz |
| $F_{SW(MAX)}$ | Maximum Switching Frequency | | | 138 | 140 | 142 | kHz |

**Note 1:** Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to any Absolute Maximum Rating condition for extended periods may affect device reliability and lifetime.

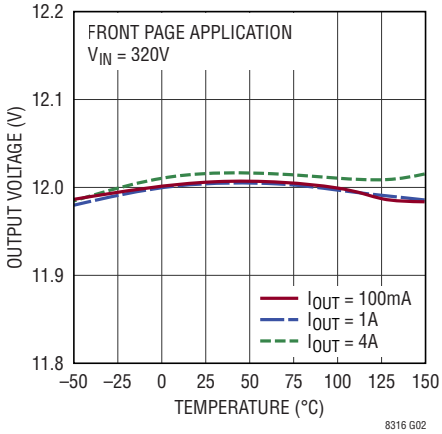
**Note 2:** The LT8316E is guaranteed to meet performance specifications from 0°C to 125°C junction temperature. Specifications over the –40°C to 125°C operating junction temperature range are assured by design characterization and correlation with statistical process controls. The LT8316I is guaranteed over the full –40°C to 125°C operating junction temperature range. High junction temperatures degrade operating lifetimes. Operating lifetime is derated at junction temperatures greater than 125°C.

## TYPICAL PERFORMANCE CHARACTERISTICS $T_A$ = 25°C, unless otherwise noted.

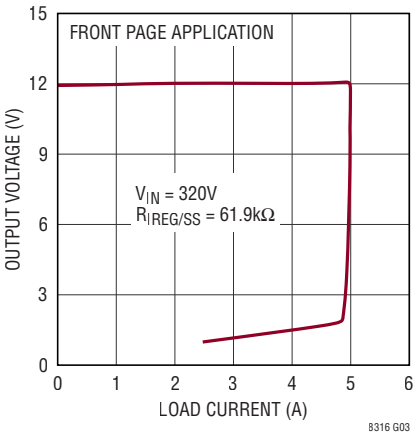
### Load and Line Regulation



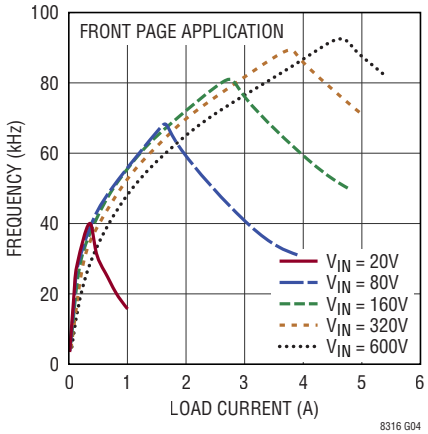

### Output Voltage vs Temperature



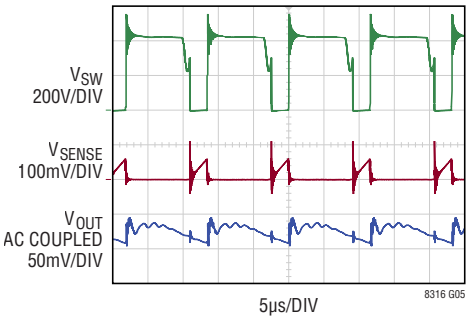

### CV/CC Operation




### Switching Frequency

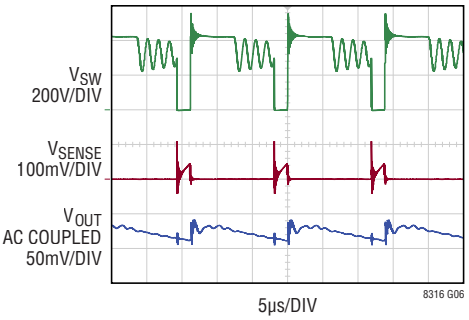



### Boundary Mode Waveforms



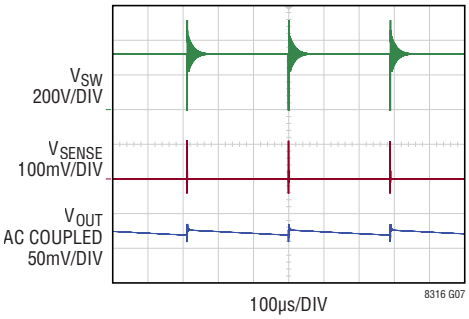

FRONT PAGE APPLICATION
$V_{IN}$ = 320V, $I_{OUT}$ = 4A

### Discontinuous Mode Waveforms




FRONT PAGE APPLICATION
$V_{IN}$ = 320V, $I_{OUT}$ = 2A

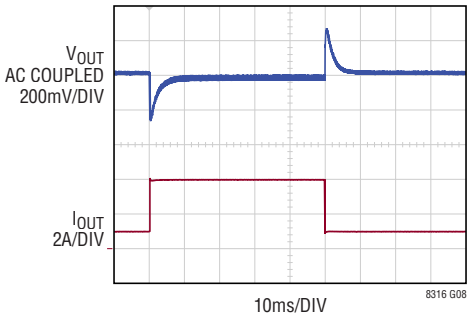
### Burst Mode Waveforms



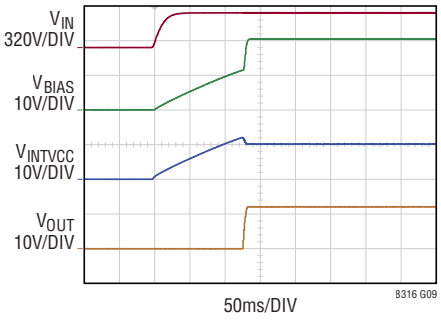

FRONT PAGE APPLICATION
$V_{IN}$ = 320V, $I_{OUT}$ = 30mA

## TYPICAL PERFORMANCE CHARACTERISTICS $T_A$ = 25°C, unless otherwise noted.

### Load Transient Response

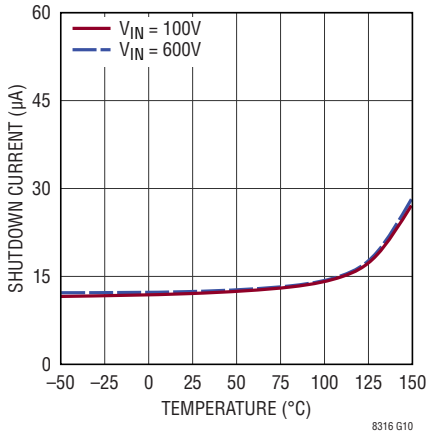



### Startup Waveforms

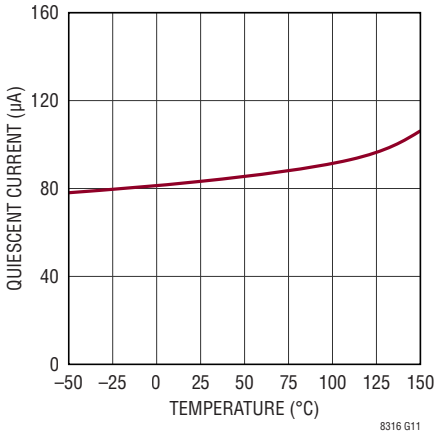



FRONT PAGE APPLICATION
$V_{IN}$ = 320V, $R_{OUT}$= 3Ω

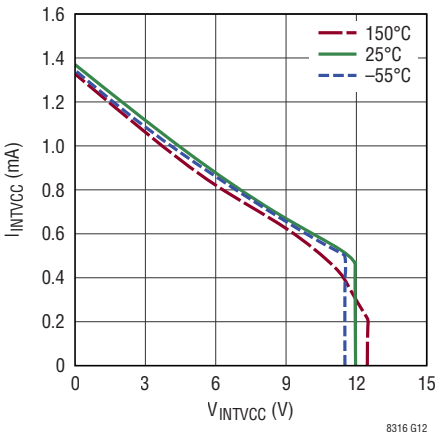
### $V_{IN}$ Pin Shutdown Current



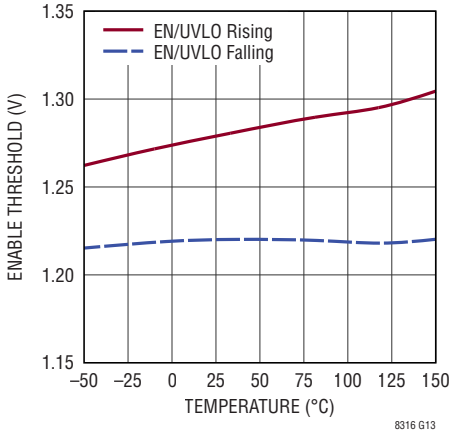

### BIAS Pin Quiescent Current



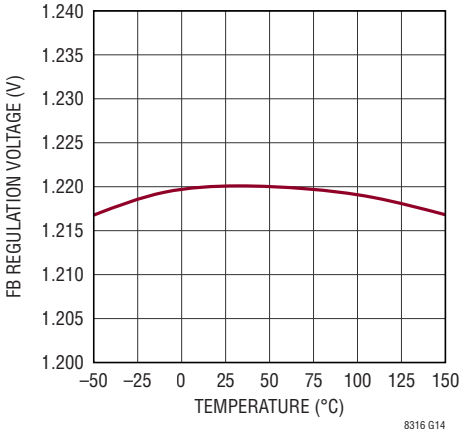

### Depletion Startup Current



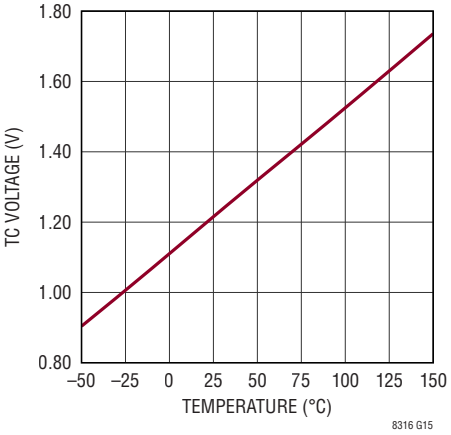

### ULVO Threshold




### FB Regulation Voltage

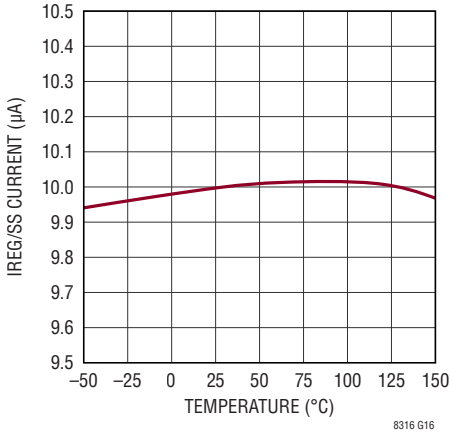



### TC Pin Voltage

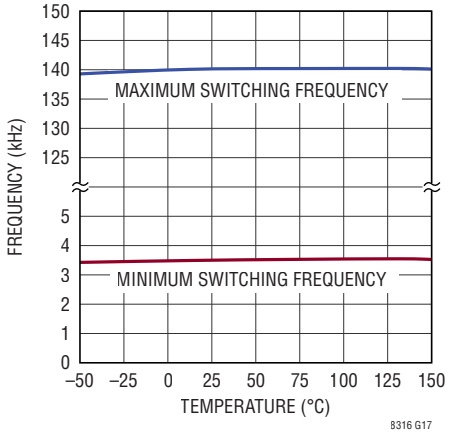


## TYPICAL PERFORMANCE CHARACTERISTICS $T_A$ = 25°C, unless otherwise noted.

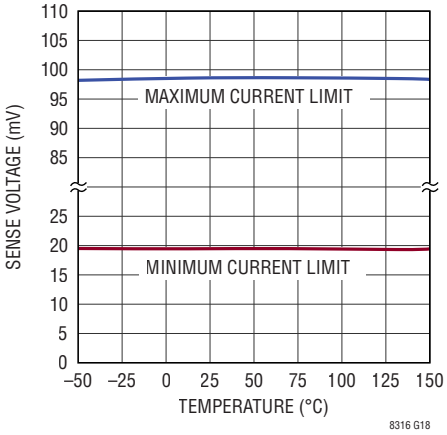
### IREG/SS Pin Current



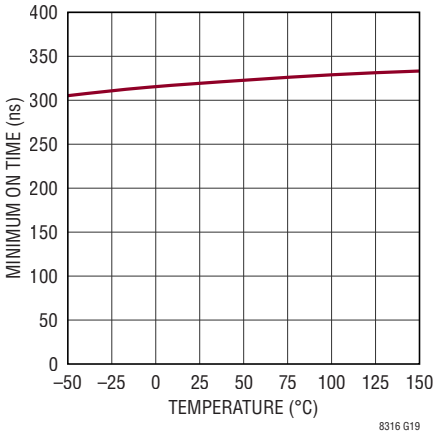

### Switching Frequency Limit



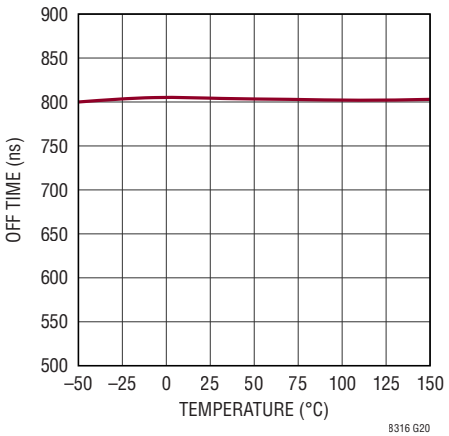

### Switch Current Limit



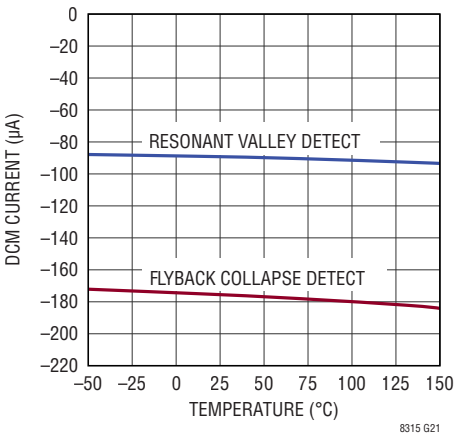

### Minimum Switch-On Time




### Minimum Switch-Off Time




### DCM Pin Threshold



## PIN FUNCTIONS

**$V_{IN}$ (Pins 1, 2, 3):** Drain of the 600V Internal Startup FET. During startup, an internal depletion MOSFET draws power from this pin to charge the $INTV_{CC}$ capacitor.

**$INTV_{CC}$ (Pin 8):** Internal Gate Driver Bias Voltage. During start-up, current from the $V_{IN}$ pin charges this pin to 12V. During operation, a linear regulator from BIAS maintains this voltage at 10V. Bypass locally with a ≥2.2µF ceramic ≥15V rated capacitor.

**BIAS (Pin 9):** Unregulated Input Voltage for the IC. This pin derives power from a third winding on the transformer to provide power to $INTV_{CC}$. Bypass locally with a ≥100nF capacitor.

**DCM (Pin 10):** Discontinuous Conduction Mode Detector. This pin detects the dV/dt of the switching waveform, ensuring accurate output voltage sampling and quasi-resonant boundary-mode switching. Connect a capacitor with series resistance from this pin to the third winding. See Boundary Mode Detection section.

**TC (Pin 11):** Temperature Compensation Pin. This pin presents a proportional-to-absolute-temperature (PTAT) voltage, which is equal to the internal 1.22V reference voltage at 25°C and rises with temperature by 4.1mV/°C, to compensate for the output rectifier diode. Connect an appropriate resistor from this pin to FB.

**FB (Pin 12):** Feedback Pin. The voltage appearing on this pin is sampled and regulated to equal the internal 1.22V reference voltage. Connect this pin to a resistor divider from the third winding to regulate the output voltage.

**VC (Pin 13):** Loop Compensation Pin. An internal $G_M$ transconductance amplifier feeds this pin with an error current depending on the sampled FB voltage. The resulting voltage determines the switching frequency and peak current limit for power delivery. Connect a series R-C network to stabilize the regulator. See Loop Compensation section.

**IREG/SS (Pin 14):** Current Regulation/Soft-Start Pin. A 10µA current flows out of this pin. The resulting voltage sets the output current regulation point, as determined by an internal current regulation loop. Program the current with a resistor to GND, or connect a capacitor to implement soft-start.

**SMODE (Pin 16):** Standby Mode Pin. Connect this pin to $INTV_{CC}$ to enable Standby Mode, which reduces the minimum switching frequency to 220Hz for ultralow quiescent power consumption. Connect to GND to disable.

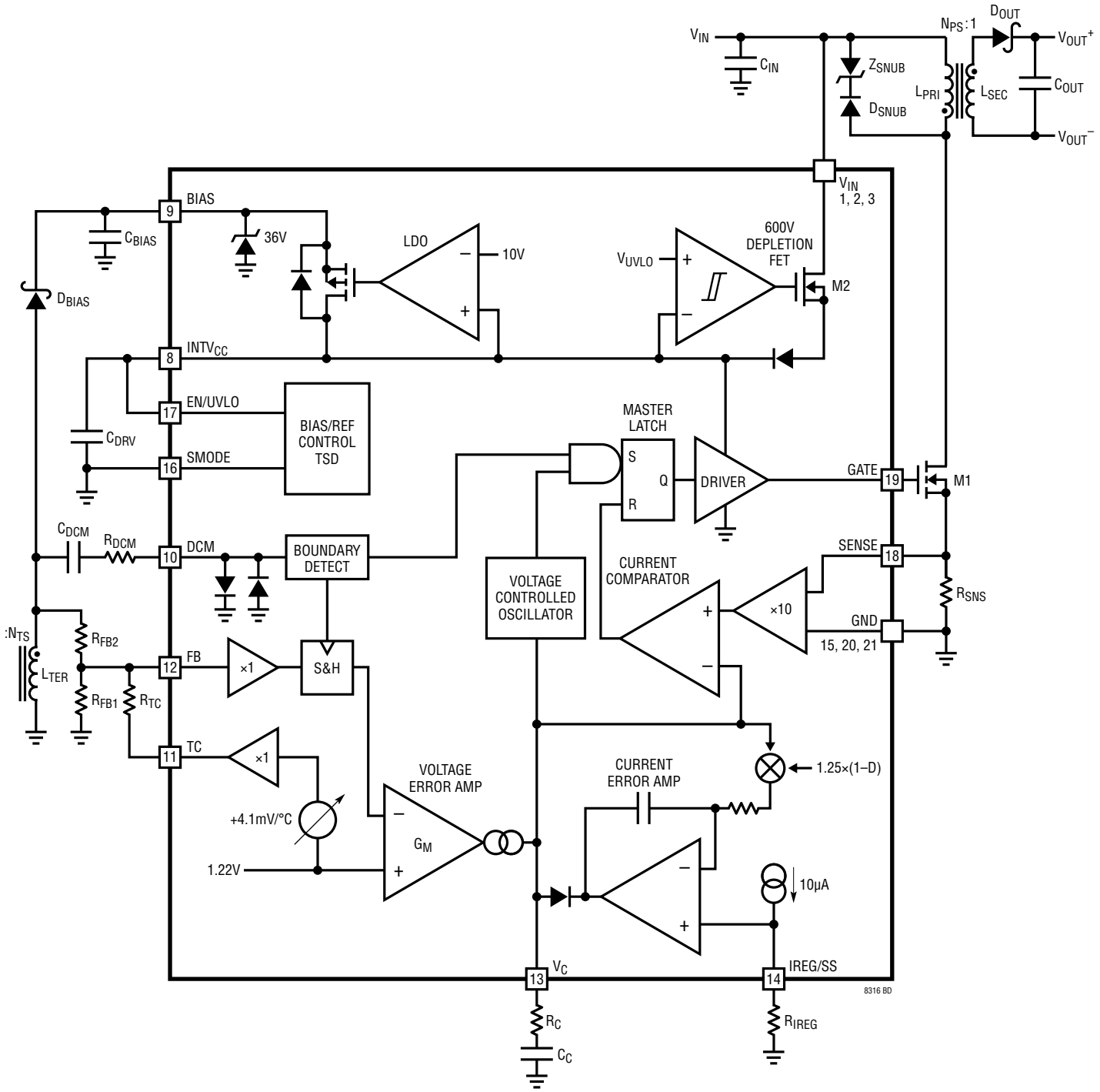
**EN/UVLO (Pin 17):** Enable/Undervoltage Lockout Pin. The chip will operate only if the voltage on this pin is greater than the internal 1.22V reference voltage. Connect to a resistor divider as desired, or connect to BIAS or $INTV_{CC}$ if UVLO functionality is not desired.

**SENSE (Pin 18):** Current Sense Pin. The voltage appearing on this pin is used for peak current-mode control and current limiting. Connect a current-sensing resistor from the main power MOSFET to GND to program the current limit. Utilize a compact layout with the transformer and input capacitor to reduce EMI and voltage spikes.

**GATE (Pin 19):** Gate Driver Output. Connect this pin to the gate of the main power MOSFET for the flyback converter.

**GND (Pins 15, 20, 21):** Ground. **Solder the exposed pad (Pin 21) to a ground plane for heat sinking.**

## BLOCK DIAGRAM



# OPERATION

The LT8316 is a high-voltage current-mode switching controller designed for the isolated flyback topology. The problem normally encountered in such circuits is that information relating to the output voltage on the isolated secondary side of the transformer must be communicated to the primary side in order to achieve regulation. This is often performed by opto-isolator circuits, which waste output power, require extra components that increase the cost and physical size of the power supply, and exhibit trouble due to limited dynamic response, nonlinearity, unit-to-unit variation, and aging over their life.

The LT8316 does not need an opto-isolator because it derives information about the isolated output voltage by examining the flyback pulse waveform appearing on a tertiary winding on the transformer. The output voltage is easily programmed with two resistors.

The LT8316 features a boundary mode control method (also called critical conduction mode), where the part operates at the boundary between continuous conduction mode and discontinuous conduction mode. Due to boundary mode operation, the output voltage can be determined from the tertiary winding's voltage when the secondary current is almost zero. This method improves load regulation without extra resistors and capacitors.

The Block Diagram shows an overall view of the system. Many of the blocks are similar to those found in traditional switching regulators, including a current comparator, internal reference, LDO, logic, timers and a MOSFET gate driver. The novel sections include a special sampling error amplifier, a temperature compensation circuit, an output current regulator, and a depletion-mode startup FET.

### Depletion Startup FET

The LT8316 features an internal depletion mode MOSFET. At startup, this transistor charges the $INTV_{CC}$ capacitor so that the LT8316 has power to begin switching. This removes the need for an external bleeder resistor or other components.

### Boundary Mode Operation

Boundary mode is a variable frequency, current-mode switching scheme. The external N-channel MOSFET turns on and the inductor current increases until it reaches the limit determined by the voltage on the $V_C$ pin and the sense resistor's value. After the MOSFET turns off, the voltage on the tertiary winding rises to the output voltage multiplied by the transformer tertiary-to-secondary turns ratio. After the current through the output diode falls to zero, the voltage on the tertiary winding falls. A boundary mode detection comparator on the DCM pin detects the negative dV/dt associated with the falling voltage and triggers the sample-and-hold circuit to sample the FB voltage. When the tertiary voltage reaches its minimum and stops falling, the boundary mode comparator turns the internal MOSFET back on for minimal switching energy loss.

Boundary mode operation returns the secondary current to zero every cycle, so parasitic resistive voltage drops do not cause load regulation errors. Boundary mode also allows the use of a smaller transformer compared to continuous conduction mode and does not exhibit subharmonic oscillation.

### Discontinuous Conduction Mode Operation

As the load gets lighter, the peak switch current decreases. Maintaining boundary mode requires the switching frequency to increase. An excessive switching frequency increases switching and gate charge losses. To limit these losses, the LT8316 features an internal oscillator which limits the maximum switching frequency to 140kHz. Once the switching frequency hits this limit, the part starts to reduce its switching frequency and operates in discontinuous conduction mode.

### Low Ripple Burst Mode Operation

Unlike traditional flyback converters, the MOSFET has to turn on and off to generate a flyback pulse in order to update the sampled output voltage. The duration of a well-formed flyback pulse must exceed the minimum-off time for proper sampling. To this end, a minimum switch turn-off current is necessary to ensure a flyback pulse of sufficient duration.

## OPERATION

As the load gets very light, the LT8316 reduces switching frequency while maintaining the minimum current limit in order to reduce current delivery while still properly sampling the output voltage. Because flyback pulses must be generated to regulate the output, a minimum switching frequency of 3.5kHz is enforced. The minimum switching frequency determines how often the output voltage is sampled and introduces a minimum load requirement of approximately 1% of the maximum load power.

Tying the SMODE pin to $INTV_{CC}$ enables Standby Mode, which reduces the minimum switching frequency to 220Hz, reducing the minimum load requirement at the expense of a longer period between samples.

### CV/CC Regulation

Like a traditional voltage regulator, the LT8316 implements a $G_M$ transconductance amplifier that regulates the output voltage. In addition, the LT8316 includes a current regulation loop which regulates the estimated output current to a point set by the voltage on the IREG/SS pin. Below the current setpoint, the output voltage is regulated for constant-voltage (CV) regulation. Below the voltage setpoint, the the output current is regulated for constant-current (CC) regulation.

## APPLICATIONS INFORMATION

The LT8316 is designed to be an easy-to-use, yet fully-featured flyback controller. With proper technique, it is simple to build an efficient and robust power solution.

However, the voltage and power levels involved can be lethal. **Milliamperes from a high voltage power supply can cause heart fibrillation and death.** Never touch conductive nodes while the circuit is active, and keep one hand behind your back while probing.

### Depletion Startup FET

The LT8316 features an internal depletion-mode FET, which has a negative threshold voltage and is therefore normally on. At startup, this FET charges the $INTV_{CC}$ capacitor to 12V so that the LT8316 has power to begin switching. This removes the need for an external bleeder resistor or other startup components. Once $INTV_{CC}$ is charged, the depletion-mode FET turns off.

The depletion FET is current-limited to avoid destructive power levels. To ensure start-up, do not load $INTV_{CC}$ or BIAS with excessive current while the chip is starting.

### ENABLE and Undervoltage Lockout (UVLO)

A resistive divider from $V_{IN}$ to the EN/UVLO pin implements undervoltage lockout (UVLO). The EN/UVLO pin threshold is set at 1.22V. Upon startup, the EN/UVLO pin exhibits a ~65mV hysteresis voltage to prevent oscillations.

The EN/UVLO pin can also be driven with logic levels and set by the output pin of a digital controller. Otherwise, EN/UVLO can also be tied to BIAS or $INTV_{CC}$ to keep the chip enabled.

### Output Voltage

The output voltage is programmed by the $R_{FB1}$ and $R_{FB2}$ resistors depicted in the Block Diagram. The LT8316 operates similarly to traditional current-mode switchers, except in its use of a unique sample-and-hold error amplifier, which regulates the isolated output voltage from the sampled flyback pulse.

Operation is as follows: when the power switch M1 turns off, the voltage across the tertiary winding rises. The amplitude of the flyback pulse is given as:

$$V_{FLBK} = (V_{OUT} + V_F + I_{SEC} \bullet ESR) \bullet N_{TS},$$

## APPLICATIONS INFORMATION

where

$V_F$ = Output diode ($D_{OUT}$) forward-biased voltage

$I_{SEC}$ = Transformer secondary current

ESR = Parasitic resistance of secondary circuit

$N_{TS}$ = Transformer tertiary-to-secondary turns ratio

The voltage divider formed by $R_{FB1}$ and $R_{FB2}$ feeds a scaled version of the flyback pulse to the FB pin, where it is sampled and fed to the error amplifier. Because the sample-and-hold circuit samples the voltage when the secondary current is nearly zero, the ($I_{SEC}$ • ESR) term in the $V_{FLBK}$ equation can be ignored.

The internal 1.22V reference voltage feeds the non-inverting input of the error amplifier. The high gain of the overall loop causes the FB voltage to be nearly equal to the reference voltage. The resulting flyback voltage $V_{FLBK}$ can be expressed as:

$$V_{FLBK} = \left(1 + \frac{R_{FB2}}{R_{FB1}}\right) \bullet 1.22V$$

Combining with the previous $V_{FLBK}$ equation and solving for $V_{OUT}$ yields:

$$V_{OUT} = \left(1 + \frac{R_{FB2}}{R_{FB1}}\right) \bullet \frac{1.22V}{N_{TS}} - V_F$$

Due to the fast nature of the flyback pulse, it is recommended to keep $R_{FB1}$ between 1kΩ and 10kΩ in order to preserve the resistor divider's dynamic response.

### Selecting the $R_{FB2}$ Resistor Value

The LT8316 uses a unique sampling scheme to regulate the isolated output voltage. Due to its sampling nature, the scheme exhibits repeatable delays and error sources, which will affect the output voltage and force a re-evaluation of the resistor values.

With a fixed value for $R_{FB1}$ (such as 10kΩ) chosen, rearrangement of the expression for $V_{OUT}$ yields the starting value for $R_{FB2}$:

$$R_{FB2} = R_{FB1} \bullet \left(\frac{V_{OUT} + V_F}{1.22V} \bullet N_{TS} - 1\right)$$

where

$V_{OUT}$ = Desired output voltage

$V_F$ = Output diode ($D_{OUT}$) forward voltage ≈ 300mV

$N_{TS}$ = Transformer tertiary-to-secondary turns ratio

Power up the application with the final power components installed and the starting $R_{FB2}$ value, and measure the regulated output voltage, $V_{OUT(MEAS)}$. The final $R_{FB2}$ value can be adjusted to:

$$R_{FB2(FINAL)} \approx (R_{FB2} + R_{FB1}) \bullet \frac{V_{OUT}}{V_{OUT(MEAS)}} - R_{FB1}$$

Once the final $R_{FB2}$ value is selected, the regulation accuracy from board to board for a given application will be very consistent, typically within ±5% when including device variation of all the components in the system (assuming resistor tolerances and transformer windings matching within ±1%). However, if the transformer or the output diode is changed, or the layout is dramatically altered, there may be some change in $V_{OUT}$.

Example: Consider a 12V output supply with an output diode whose forward voltage at nearly zero current is 300mV at room temperature. If the tertiary-to-secondary ratio $N_{TS}$ is 1 and $R_{FB1}$ is 10kΩ, then $R_{FB2}$ is calculated as 90.9kΩ. The application is powered up and the output is slightly high at 12.2V, so $R_{FB2}$ is adjusted to 88.7kΩ.

### Output Diode Temperature Compensation

Reiterating the equation for $V_{OUT}$,

$$V_{OUT} = \left(1 + \frac{R_{FB2}}{R_{FB2}}\right) \bullet \frac{1.22V}{N_{TS}} - V_F$$

The first term in the $V_{OUT}$ equation is insensitive to temperature, but the output diode forward voltage $V_F$ has a significant negative temperature coefficient (from –1mV/°C to –2mV/°C). Such a temperature coefficient produces approximately 200mV to 400mV output voltage variation across operating temperature.

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At higher output voltages, the resulting variation may be unimportant as it represents a small fraction of the total output. However, for lower output voltages, the diode temperature coefficient accounts for a large output voltage error.

To correct this error, the TC pin provides a buffered proportional-to-absolute-temperature (PTAT) voltage. At room temperature, this voltage is equal to the internal 1.22V reference, and it has a +4.1mV/°C temperature coefficient.

The output diode's temperature coefficient $TC_F$ can easily be found experimentally by applying a uniform temperature to both the output diode and the LT8316. First, $R_{FB1}$ and $R_{FB2}$ are adjusted to give the desired output voltage at room temperature. The temperature is then raised or lowered by a known amount to a new temperature, and the diode temperature coefficient is found as:

$$TC_F = \frac{V_{OUT(25°C)} - V_{OUT(TNEW)}}{T_{NEW} - 25°C}$$

where

$V_{OUT(25°C)}$ = $V_{OUT}$ measured at room temperature

$V_{OUT(TNEW)}$ = $V_{OUT}$ measured at new temperature

$T_{NEW}$ = New temperature in Celsius

Alternatively, $TC_F$ can be found more accurately by measuring $V_{OUT}$ at two extremes of temperature and computing:

$$TC_F = -\frac{\Delta V_{OUT}}{\Delta T}$$

It should be noted that for this measurement, it is critical that the entire board be heated or cooled uniformly, for example by an oven. A heat gun or freeze spray will not suffice, since the heating and cooling will not be uniform, and dramatic temperature mismatch between the LT8316 and the output diode will cause significant error.

If no method is available to apply uniform heat or cooling, extrapolating data from the diode's data sheet or assuming a nominal $TC_F$ value (such as –1.5mV/°C) may yield a satisfactory result.

With the output diode's temperature coefficient known, a resistor $R_{TC}$ is then attached from the TC pin to the FB pin. Its value can be calculated as:

$$R_{TC} = \frac{-R_{FB2} \bullet 4.1mV / °C}{TC_F \bullet N_{TS}}$$

Example: If the output diode's temperature coefficient $TC_F$ is found experimentally to be –1.9mV/°C, then with $R_{FB2}$ = 88.7kΩ, a $R_{TC}$ value of 191kΩ will yield a temperature-invariant output voltage.

### Sense Resistor Selection

The resistor $R_{SNS}$ between the power MOSFET and GND should be selected to provide an adequate switch current to drive the application without exceeding the current limit threshold.

At maximum current delivery, current limit occurs when the SENSE pin voltage is 100mV. In boundary mode, the maximum output current will depend on the duty cycle D and is given by:

$$I_{OUT(MAX)} \approx \frac{100mV}{2 \bullet R_{SNS}} \bullet (1 - D) \bullet N_{PS}$$

where

$N_{PS}$ = Transformer primary-to-secondary turns ratio

$$D \approx \frac{(V_{OUT} + V_F) \bullet N_{PS}}{(V_{OUT} + V_F) \bullet N_{PS} + V_{IN}}$$

$V_{IN}$ = Power supply voltage.

It should be noted that the worst-case occurs at minimum $V_{IN}$, so $D_{VIN(MIN)}$ should be calculated assuming $V_{IN}$ = $V_{IN(MIN)}$. Solving for the sense resistor value:

$$R_{SNS} = \frac{1 - D_{VIN(MIN)}}{I_{OUT(MAX)}} \bullet 50mV \bullet N_{PS} \bullet 80\%$$

A factor of 80% is introduced to compensate for system delays and tolerances, but it may need adjustment for the final application.

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Example: A 12V output voltage is generated from a $V_{IN}$ = 400V input that can drop as low as $V_{IN(MIN)}$ = 250V. If a transformer with primary-to-secondary turns ratio $N_{PS}$ = 10 is selected to supply a maximum output current $I_{OUT(MAX)}$ = 2A, then the duty cycle is $D_{VIN(MIN)} \approx 33\%$ and the sense resistor is calculated $R_{SNS}$ = 133mΩ. A 120mΩ resistor is selected.

A more accurate value for $R_{SNS}$ can be obtained by finding D experimentally with an oscilloscope and electronic load.

### Output Power

Compared with a buck or a boost converter, a flyback converter has a complicated relationship between the input and output currents. Boost converters have relatively constant maximum input current regardless of input voltage, while buck converters have relatively constant maximum output current regardless of input voltage, owing to the fact that they have continuous input and output currents respectively. A flyback converter, however, has both discontinuous input and output currents. The duty cycle affects both input and output currents, making it hard to predict maximum output power.

The following equation calculates output power:

$$P_{OUT} = 0.5 \bullet \eta \bullet V_{IN} \bullet D \bullet I_{SW(MAX)}$$

where

$\eta$ = Efficiency ≈ 80%

$$D \approx \frac{(V_{OUT} + V_F) \bullet N_{PS}}{(V_{OUT} + V_F) \bullet N_{PS} + V_{IN}}$$

$I_{SW(MAX)}$ = Max. switch current limit = 100mV/$R_{SNS}$

The calculated power is approximate, and does not take into account timing variations caused by circuit parasitics. The actual output power must be evaluated on the bench.

Example: Consider a 12V output converter with a $V_{IN(MIN)}$ of 250V and a $V_{IN(MAX)}$ of 500V. With a ten-to-one primary-to-secondary winding ratio ($N_{PS}$ = 10) and a sense resistor $R_{SNS}$ = 120mΩ, the maximum power output is 33W at $V_{IN(MAX)}$ = 500V but lowers to 28W at $V_{IN(MIN)}$ = 250V.

### Selecting a Transformer

Transformer specification and design is possibly the most critical part of successfully applying the LT8316. In addition to the usual list of guidelines dealing with high-frequency isolated power supply transformer design, the following information should be carefully considered.

Analog Devices has worked with several leading magnetic component manufacturers to produce pre-designed flyback transformers for use with the LT8316. Table 1 shows the details of these transformers.

**Table 1. Predesigned Transformers — Typical Specifications**

| TRANSFORMER PART NUMBER | $L_{PRI}$ (µH) | $N_P$:$N_S$:$N_T$ | ISOLATION | VENDOR | TARGET APPLICATIONS |
|---|---|---|---|---|---|
| 11328-T078 | 670 | 8:1:1 | Reinforced | Sumida | 100V–600V to 12V/3A |
| 11328-T080 | 670 | 4:1:0.5 | Reinforced | Sumida | 100V–600V to 24V/1.5A |
| 11328-T073 | 670 | 2:1:0.25 | Reinforced | Sumida | 100V–600V to 54V/0.7A |
| 11328-T061 | 600 | 5:1:1 | Basic | Sumida | 200V–450V to 15V/2A |
| 11338-T195 | 1000 | 14:1:1.7 | Basic | Sumida | 100V–400V to 7V/2A |
| 11328-T074 | 500 | 8:1:1 | Reinforced | Sumida | 100V–450V to 12V/3A |
| 15364-T008 | 1500 | 20:1:2.4 | Reinforced | Sumida | 25V–450V to 5V/1A |
| 11328-T086 | 70 | 4:1:0.5 | Reinforced | Sumida | 30V–260V to 24V/3A |
| 00399-T239 | 2800 | 6:1:0.7 | Functional | Sumida | 90V–500V to 16.8V/0.4A |
| 750317463 | 440 | 8:1:1 | Reinforced | Wurth Elektronik | 100V–600V to 12V/4A |
| 750317589 | 670 | 8:1:1 | Reinforced | Wurth Elektronik | 100V–600V to 12V/3A |
| 750317464 | 440 | 4:1:0.5 | Reinforced | Wurth Elektronik | 100V–600V to 24V/2A |
| 11328-T060 | 800 | 18:1:3 | Reinforced | Sumida | 140V–450V to 5V/7A |

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### Flyback Transformer Modeling

A flyback transformer can be thought of as an ideal transformer with a parallel magnetizing inductance and series leakage inductances, as shown in Figure 1.

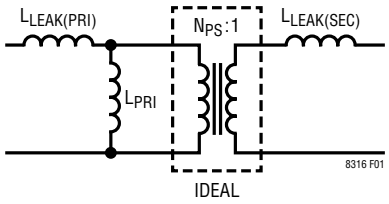


**Figure 1. Transformer Model**

The magnetizing inductance, which is the mutual inductance shared by both primary and secondary windings, is essential for absorbing energy and delivering it to the load. It stores energy in magnetic flux lines that pass through both primary and secondary windings.

If the leakage inductances are small, the magnetizing inductance can be measured by leaving the secondary open-circuited and measuring the inductance of the primary, resulting in an inductance $L_{PRI}$. The magnetizing inductance can also be measured from the secondary by leaving the primary open-circuited and measuring the secondary inductance $L_{SEC}$. The relationship between the primary-referred magnetizing inductance and secondary-referred magnetizing inductance is given by the primary-to-secondary turns ratio $N_{PS}$ as:

$$L_{PRI} = L_{SEC} \bullet N_{PS}^2$$

The transformer also has leakage inductances, which are parasitic inductances associated with each winding. These inductances store energy in magnetic flux lines which "leak" out of the magnetic core and do not pass through both windings, and therefore represent self-inductances whose energy cannot be transferred through the transformer. As such, they contribute to energy loss and reduced converter efficiency.

If the leakage inductances are small, the combined leakage inductance can be measured by short-circuiting the secondary and measuring the primary inductance. This results in a primary-referred inductance,

$$L_{LEAK} = L_{LEAK(PRI)} + L_{LEAK(SEC)} \bullet N_{PS}^2$$

The leakage inductance and magnetizing inductance are related by the coupling coefficient k according to the relation:

$$k = \frac{L_{PRI}}{L_{PRI} + L_{LEAK} / 2}$$

Coupling coefficients of k=99% are common, and are a function of transformer construction and materials. Increased voltage isolation between primary and secondary is often desired for safety purposes, but generally reduces the coupling coefficient and increases leakage inductance. Bifilar windings maximize the coupling coefficient, but are often undesirable because of their minimal isolation and increased primary-to-secondary capacitance. In the end, a reasonable trade-off between isolation and coupling coefficient must be made.

### Magnetizing Inductance Requirement

The appropriate magnetizing inductance depends on the LT8316's minimum switch-on time, its minimum switch-off time, and output power.

The conduction of secondary current reflects the output voltage onto the tertiary winding during the flyback pulse. The LT8316 obtains output voltage information from the reflected output voltage on the FB pin. The sample-and-hold error amplifier needs a minimum of 800ns to settle and sample the reflected output voltage. In order to ensure proper sampling, the secondary winding needs to conduct current for at least 800ns.

The minimum value for primary-side magnetizing inductance is given by:

$$L_{PRI} \geq \frac{t_{OFF(MIN)} \bullet N_{PS} \bullet (V_{OUT} + V_F)}{I_{SW(MIN)}}$$

where

$t_{OFF(MIN)}$ = Minimum switch-off time = 800ns

$I_{SW(MIN)}$ = Minimum switch current limit = $20mV/R_{SNS}$

The LT8316 has a minimum switch-on time that prevents the chip from turning on the power switch for a period shorter than 300ns in order to blank the initial switch

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turn-on current spike. If the inductor current exceeds the minimum switch current limit during that time, the minimum load current will increase. Therefore, the following equation must also be observed:

$$L_{PRI} \geq \frac{t_{ON(MIN)} \bullet V_{IN(MAX)}}{I_{SW(MIN)}}$$

where

$t_{ON(MIN)}$ = Minimum Switch-On Time = 300ns

Additionally, the magnetizing inductance must be large enough to provide sufficient power to the output when the LT8316 operates at maximum frequency. This creates a third requirement for magnetizing inductance:

$$L_{PRI} \geq \frac{2 \bullet (V_{OUT} + V_F) \bullet I_{OUT(MAX)}}{\eta \bullet I_{SW(MAX)}^2 \bullet f_{SW(MAX)}}$$

where

$I_{SW(MAX)}$ = Maximum switch current = 100mV/$R_{SNS}$

$I_{OUT(MAX)}$ = Maximum load current

$f_{SW(MAX)}$ = Maximum switching frequency = 140kHz

$\eta$ = Efficiency ≈ 80%

In general, choose a transformer with its primary magnetizing inductance about 20% to 50% larger than the minimum values calculated above.

In addition to these minimum values, the magnetizing inductance has a maximum value. To avoid a stuck output-low state, the LT8316 has a 50µs backup timer that turns the switch on if the secondary diode turn-off has not been detected. As a result, the magnetizing inductance must not be so large as to cause secondary diode conduction to exceed this time. This creates a final requirement for maximum magnetizing inductance:

$$L_{PRI} < \frac{0.8 \bullet (V_{OUT} + V_F) \bullet N_{PS} \bullet t_{BU}}{I_{SW(MAX)}}$$

where

$t_{BU}$ = Backup time = 50µs

Example: For a 12V/2A output converter with $V_{IN(MAX)}$ = 500V, $V_F$ = 300mV, $N_{PS}$ = 10, and $R_{SNS}$ = 120mΩ, the first equation requires $L_{PRI} \geq$ 590µH, the second equation requires $L_{PRI} \geq$ 900µH, and the third equation requires $L_{PRI} \geq$ 633µH. A reasonable standard value for primary inductance is $L_{PRI}$ = 1.2mH. If a larger minimum load at high $V_{IN}$ can be tolerated, 820µH is acceptable. The fourth equation dictates that $L_{PRI}$ must be less than 5.9mH; this requirement is easily satisfied by both options.

### Saturation Current

The current in the transformer windings should not exceed its rated saturation current. Beyond its saturation value, the inductance drops and the current rises to an uncontrolled value, causing extra power dissipation and possible failure. Choose a transformer whose primary saturation current is at least 30% greater than $I_{SW(MAX)}$, which is 100mV/$R_{SNS}$.

### Turns Ratios

Typically, choose the transformer primary-to-secondary turns ratio $N_{PS}$ to maximize available output power. For low output voltages, a larger $N_{PS}$ ratio can be used to maximize the transformer's current gain. However, remember that the MOSFET's drain sees a voltage that is equal to $V_{IN}$ plus the output voltage multiplied by $N_{PS}$. Additionally, leakage inductance will cause a voltage spike ($V_{LEAKAGE}$) that adds to this reflected voltage. This total quantity needs to remain below the absolute maximum rating of the MOSFET's drain to prevent breakdown. Together these conditions place an upper limit on the turns ratio $N_{PS}$ for a given application. Choose a turns ratio low enough to ensure:

$$N_{PS} < \frac{V_{BR} - V_{IN(MAX)} - V_{LEAKAGE}}{V_{OUT} + V_F}$$

where

$V_{BR}$ = MOSFET breakdown voltage.

For producing high output voltages, a low ratio $N_{PS}$ may be used. However, the multiplied capacitance presented to the transformer primary may cause ringing that exceeds

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the 300ns $t_{ON(MIN)}$, causing light-load instability. Fully evaluate these applications before use with the LT8316.

During operation, the LT8316 derives its power from a tertiary winding through its BIAS pin. BIAS must be maintained between 10V and 30V for proper operation. This dictates a tertiary-to-secondary turns ratio $N_{TS}$ of:

$$\frac{10V}{V_{OUT}} < N_{TS} < \frac{30V}{V_{OUT}}$$

Example: For $V_{OUT}$ = 12V, $N_{TS}$ must lie between 0.83 and 2.5, or a 5:6 and 5:2 tertiary-to-secondary ratio respectively.

Due to leakage inductance ringing on the tertiary winding, BIAS will rise above its nominal value. To prevent BIAS pin breakdown, an internal clamp circuit activates at 36V and shunts the excess current to ground. This current must not exceed 15mA; evaluate at maximum load current and minimum $V_{IN}$ to verify proper operation.

Because the output voltage is measured through the voltage appearing on the third winding, $N_{TS}$ directly affects the output voltage regulation accuracy. For best results, make sure the transformer is manufactured with a precise turns ratio specified within ±1%.

### Leakage Inductance and Snubbers

Any leakage inductance on either the primary or secondary windings causes a voltage spike to appear on the primary after the power switch turns off. This spike is increasingly prominent at higher load currents where more energy is stored in the leakage inductance. This energy cannot be delivered to the load, and must be dissipated as heat. It is thus very important to minimize transformer leakage inductance.

When designing an application, adequate margin should be kept for the worst-case leakage voltage spikes even under overload conditions. In most cases, the reflected output voltage on the primary plus $V_{IN}$ should be kept below 80% of $V_{BR}$, as shown in Figure 2. This leaves 20% margin for the leakage spike across line and load conditions. A larger voltage margin will be required for poorly wound transformers with excessive leakage inductance.

In addition to the voltage spikes, the leakage inductance also causes the switching node to ring for a while after the power switch turns off. To prevent the voltage ringing from falsely triggering the boundary mode detector, the LT8316 internally blanks the boundary mode detector for 800ns. Any ringing after 800ns may trigger the power switch to turn back on again before the secondary current falls to zero, so the leakage inductance spike and associated ringing should be limited to less than 800ns.

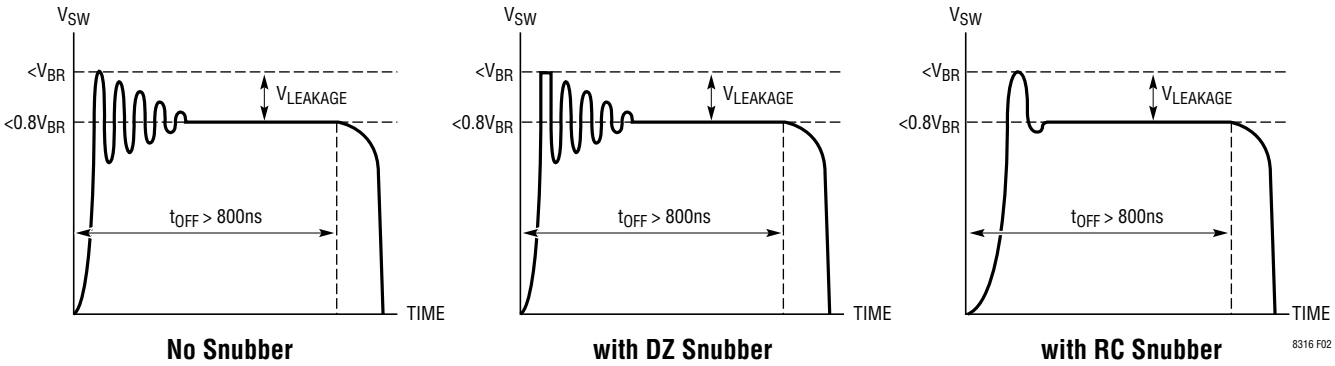


**Figure 2. Maximum Voltages for SW Pin Flyback Waveform**

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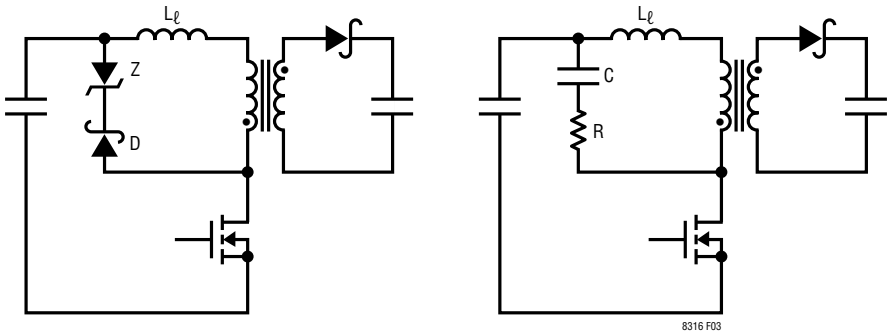


**DZ Snubber** **RC Snubber**

**Figure 3. Snubber Circuits**

A snubber circuit is recommended for most applications. Figure 3 shows two types of snubber circuits that can protect the internal power switch: the DZ (diode-Zener) snubber and the RC (resistor-capacitor) snubber. The DZ snubber ensures a well-defined and consistent clamping voltage and has slightly higher power efficiency, while the RC snubber quickly damps the voltage spike ringing and provides better load regulation and EMI performance. Figure 2 shows the flyback waveforms with the DZ and RC snubbers.

For the DZ snubber, proper care must be taken when choosing both the diode and the Zener diode. Choose a fast-recovery diode that has a reverse-voltage rating higher than the maximum DRAIN pin voltage.

The Zener diode breakdown voltage should be chosen to balance power loss and switch voltage protection. The best compromise is to choose the largest voltage breakdown. Use the following equation to make the proper choice:

$$V_{ZENER(MAX)} \leq V_{BR} - V_{IN(MAX)}$$

Multiple Zener diodes may be placed in series to attain the required voltage and power dissipation.

The Zener diode must be rated to absorb the power loss in the clamp, which is due to energy storage in the leakage inductance and the primary-to-secondary commutation time, which decreases with higher clamp voltage. A 500mW Zener is typically recommended. Design the metal of the $V_{IN}$ trace for sufficient heat removal.

For the RC snubber, the recommended design approach is to power up at low voltage to avoid overvoltage stress, measure the period of the ringing on the MOSFET's drain when the power switch turns off without the snubber ($T_{RING}$), and then add capacitance $C_{SNUBBER}$ (starting with 100pF) until the period of the ringing is 1.5 to 2 times longer ($T_{RING(SNUBBED)}$). The change in period will determine the value of the parasitic capacitance $C_{SW}$, from which the parasitic inductance $L_{LEAK}$ can also be determined, according to the equations:

$$C_{SW} = \frac{C_{SNUBBER}}{\left(\frac{T_{RING(SNUBBED)}}{T_{RING}}\right)^2 - 1}$$

$$L_{LEAK} = \left(\frac{T_{RING}}{2\pi}\right)^2 \bullet \frac{1}{C_{SW}}$$

With the value of the switching node capacitance and leakage inductance known, a resistor can be added in series with the snubber capacitor to dissipate power and critically dampen the ringing. The equation for deriving the optimal series resistance is:

$$R_{SNUBBER} = \sqrt{\frac{L_{LEAK}}{C_{SW}}}$$

Energy absorbed by the RC snubber will be converted to heat and will not be delivered to the load. In high power applications, the snubber resistor may need to be sized for thermal dissipation.

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Note that the switching node capacitance is sometimes dominated by transformer interwinding capacitance. Also note that oscilloscope probes present considerable loading capacitance. Use of low-capacitance, high-voltage 100× probes is recommended.

### Leakage Inductance and Output Diode Stress

The output diode may also see increased reverse voltage stresses from leakage inductance. While it nominally sees a reverse voltage of the input voltage divided by $N_{PS}$ plus the output voltage when the MOSFET power switch turns on, the capacitance on the output diode and the leakage inductance form an LC tank which may ring beyond that expected reverse voltage. A snubber or clamp may be implemented to reduce the voltage spike if it is desired to use a lower reverse voltage diode.

### Secondary Leakage Inductance

Leakage inductance on the secondary forms an inductive divider that effectively reduces the size of the tertiary-referred flyback pulse used for voltage feedback. This will increase the output voltage by a similar percentage. Note that, unlike leakage spike behavior, this phenomenon is load independent. To the extent that the secondary leakage inductance is a constant percentage of mutual inductance (over manufacturing variations), this can be accommodated by adjusting the $R_{FB2}/R_{FB1}$ resistor ratio.

### Winding Resistance

Resistance in either the primary or secondary will reduce conversion efficiency. Good output voltage regulation will be maintained despite winding resistance due to the boundary/discontinuous conduction mode operation of the LT8316.

### Boundary Mode Detection

Boundary mode is a variable frequency switching scheme that always returns the secondary current to zero with every cycle.

The DCM pin uses a fast, current-input comparator in combination with a small capacitor $C_{DCM}$ to detect when the flyback waveform's dV/dt is negative, indicating that the secondary diode has turned off and the flyback pulse on the tertiary winding is falling. To avoid false tripping due to leakage inductance ringing, a blanking time of 800ns is applied after the switch turns off. The detector triggers when $C_{DCM}$ draws 170µA of current out of the DCM pin. This information is used to set the timing of the FB sample-and-hold and estimate the output current.

This is not the best time to turn the switch on because the MOSFET's drain voltage is still nearly $V_{IN} + (V_{OUT} \bullet N_{PS})$, and turning the switch on would waste all the energy stored in the parasitic capacitance on the switching node. When the secondary current reaches zero, discontinuous ringing begins and the energy in the parasitic capacitance on the switch node resonates with the transformer's magnetizing inductance, delivering this energy back to $V_{IN}$. The minimum voltage of the switching node during this discontinuous ring is $V_{IN} – (V_{OUT} \bullet N_{PS})$. This is the optimal moment to turn the switch back on, and the LT8316 does this by sensing when current drawn out of DCM falls to 85µA. This switching technique increases efficiency by up to 5%.

Typical $C_{DCM}$ values range from 10pF to 100pF. A good starting value is 47pF. If the LT8316 is observed not to run in boundary mode, then increasing this capacitor will help. An unnecessarily large $C_{DCM}$ value can cause premature switch turn-on and increased power loss.

Excessive current delivered to the DCM pin can cause erratic behavior. To avoid this, a resistor $R_{DCM}$ can be added in series with $C_{DCM}$ to limit the current. Typical values range from 5kΩ to 50kΩ.

### Output Capacitor Selection

The output capacitor should be chosen to minimize the output voltage ripple while considering the increase in size and cost of a larger capacitor. The following equation provides an estimate of the maximum output voltage ripple at steady-state:

$$V_{RIPPLE} \approx \frac{L_{PRI} \bullet I_{LIM}^{2}}{2 \bullet C_{OUT} \bullet V_{OUT}}$$

where

$I_{LIM}$ = Maximum primary current = $100mV/R_{SNS}$

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This is a simplified equation; the actual ripple will depend on load current, duty cycle and capacitor ESR.

The LT8316 samples the output voltage only when switching. As a result, when it is operating at its minimum frequency, a load transient may discharge the output capacitor before the device can respond. The output capacitor must be sufficient to prevent the load from brown-out in this event. Additional bulk capacitance may be desirable for this purpose.

### Operation Under Light Output Loads

The LT8316 detects the output voltage from the flyback pulse appearing on the tertiary winding, which requires delivering power to the output. Thus, the LT8316 delivers a minimum amount of energy even during light load conditions to ensure accurate output voltage information. The minimum operating frequency at minimum load is approximately 3.5kHz. The minimum delivery of energy creates a minimum load requirement on the output of approximately 1% of the maximum load power.

A Zener diode sufficiently rated to handle the minimum load power can be used to provide a minimum load without decreasing efficiency in normal operation. In selecting a Zener diode for this purpose, the Zener voltage should be high enough that the diode does not become the load path during transient conditions but the voltage must still be low enough that the MOSFET and output voltage ratings are not exceeded when the Zener functions as the minimum load.

### Standby Mode Operation

For extremely low no-load power dissipation, the LT8316 features a standby mode which is enabled by tying the SMODE pin to $INTV_{CC}$. When the load current has dropped to zero, the LT8316 reduces its minimum switching frequency by a factor of 16 from 3.5kHz to 220Hz.

This reduces the minimum load current by a factor of 16, at the cost of slower transient response. Because the output voltage is sampled only once every 4.6ms, the LT8316 will be unable to respond to load steps for up to this period.

### Output Current Regulation and Soft-Start

Using duty cycle information and the current limit set by the $V_C$ pin, the LT8316 estimates the output current and regulates it to a setpoint determined by the voltage on the IREG/SS pin. The output current is regulated according to the equation:

$$I_{OUT} = \frac{N_{PS} \bullet V_{IREG/SS}}{25 \bullet R_{SNS}}$$

where

$V_{IREG/SS}$ = Voltage on IREG/SS pin.

A trimmed 10µA current flows out of the IREG/SS pin, so that a resistor tied from this pin to GND programs the output current according to the equation:

$$R_{IREG/SS} = \frac{2.5M\Omega \bullet I_{OUT} \bullet R_{SNS}}{N_{PS}}$$

Example: For an application with $R_{SNS}$ = 120mΩ, $N_{PS}$ = 10, and a desired regulated output current $I_{OUT}$ = 2A, an $I_{REG/SS}$ resistor is selected $R_{IREG/SS}$ = 60.4kΩ.

Circuit parasitics, especially transformer capacitance, will influence the accuracy of output current regulation due to energy delivery to the parasitics. Although this effect is usually small, some iteration may be necessary if accuracy better than 5% is required. In this case, $R_{IREG/SS}$ can be implemented with a rheostat and adjusted until the desired output current is realized, and then replaced with a fixed-value resistor for production. When the rheostat is present, a small bypass capacitor is helpful to attenuate switching interference pickup by the rheostat. Additionally, an RC snubber placed across the secondary rectifier can improve current regulation accuracy.

Soft-start functionality can also be implemented by connecting a capacitor from the IREG/SS pin to GND. The 10µA current will act to charge the external soft-start capacitor. At startup, the regulated output current will rise monotonically until reaching voltage regulation. The soft-start capacitor then charges entirely and the output current regulation loop will not interfere with voltage regulation.

## APPLICATIONS INFORMATION

In order to avoid an undervoltage condition which causes the chip to shut down, the combined capacitance on the $INTV_{CC}$ and BIAS pins must be sufficient to power the LT8316 until the output achieves regulation.

If power at $V_{IN}$ is removed, over-temperature protection is engaged, undervoltage lockout trips, or overcurrent in the sense resistor is detected, a 20Ω pull-down switch to GND discharges any capacitance on the IREG/SS pin for the duration of the fault plus 640µs.

### Protection from Shorted Output Conditions

During a shorted output condition, the LT8316 operates at the minimum operating frequency. In normal operation, the tertiary winding provides power to the IC, but the tertiary winding voltage collapses during a shorted condition. This causes the part's $INTV_{CC}$ UVLO of 8.1V (typical) to shutdown switching and charge through the depletion startup current source. The part starts switching again when $INTV_{CC}$ has reached its turn-on voltage of 12V.

To protect the output diode from excessive power dissipation during overload conditions, it is advised to program the regulated output current with a resistor $R_{IREG/SS}$. For voltage regulators, the programmed current should be 120% to 150% of the maximum load current to ensure current regulation does not interfere with voltage regulation.

### Loop Compensation

The LT8316 is compensated using an external resistor-capacitor network on the $V_C$ pin. Typical values are in the range of $R_C$ = 20kΩ and $C_C$ = 220nF. If too large an $R_C$ value is used, the part will be more susceptible to high frequency noise and jitter. If too small of an $R_C$ value is used, the transient performance will suffer. The value choice for $C_C$ is somewhat the inverse of the $R_C$ choice: if too small a $C_C$ value is used, the loop may be unstable and if too large a $C_C$ value is used, the transient performance will suffer.

Transient response may be evaluated with a load step box and adjusted with an adjustable RC compensation network. Stability should be confirmed over the full range of load current and input voltage.

### Extending Supply Voltage

The LT8316 is rated to operate from a $V_{IN}$ up to 600V. Operation from a higher supply voltage is made possible by placing a Zener diode in series with the $V_{IN}$ pin, as shown in Figure 4. The voltage dropped across the Zener diode reduces the voltage applied to the chip, allowing the supply voltage to exceed 600V.

For example, a 600V Zener diode will, in principle, allow a supply voltage ranging from 616V to 1200V. It should be noted that 616V is needed only during start-up; after start-up, the LT8316 will continue to operate through transient dips in supply voltage. In practice, the input voltage range must be adjusted according to the Zener diode's voltage tolerance.

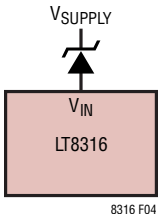



**Figure 4. Increased Supply Voltage with a Zener Diode**

## APPLICATIONS INFORMATION

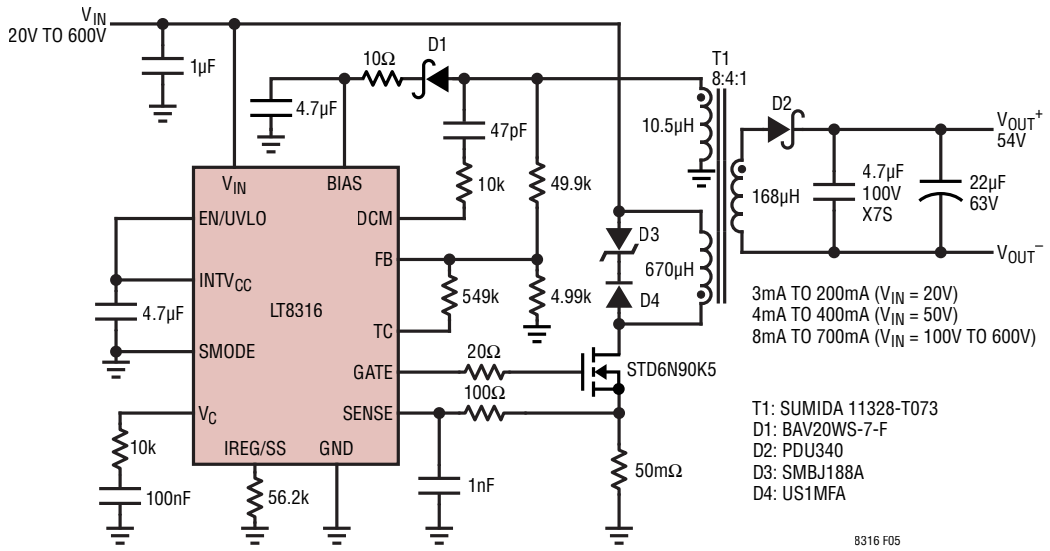



**Figure 5. 94% Efficient Isolated 54V Supply**

## APPLICATIONS INFORMATION

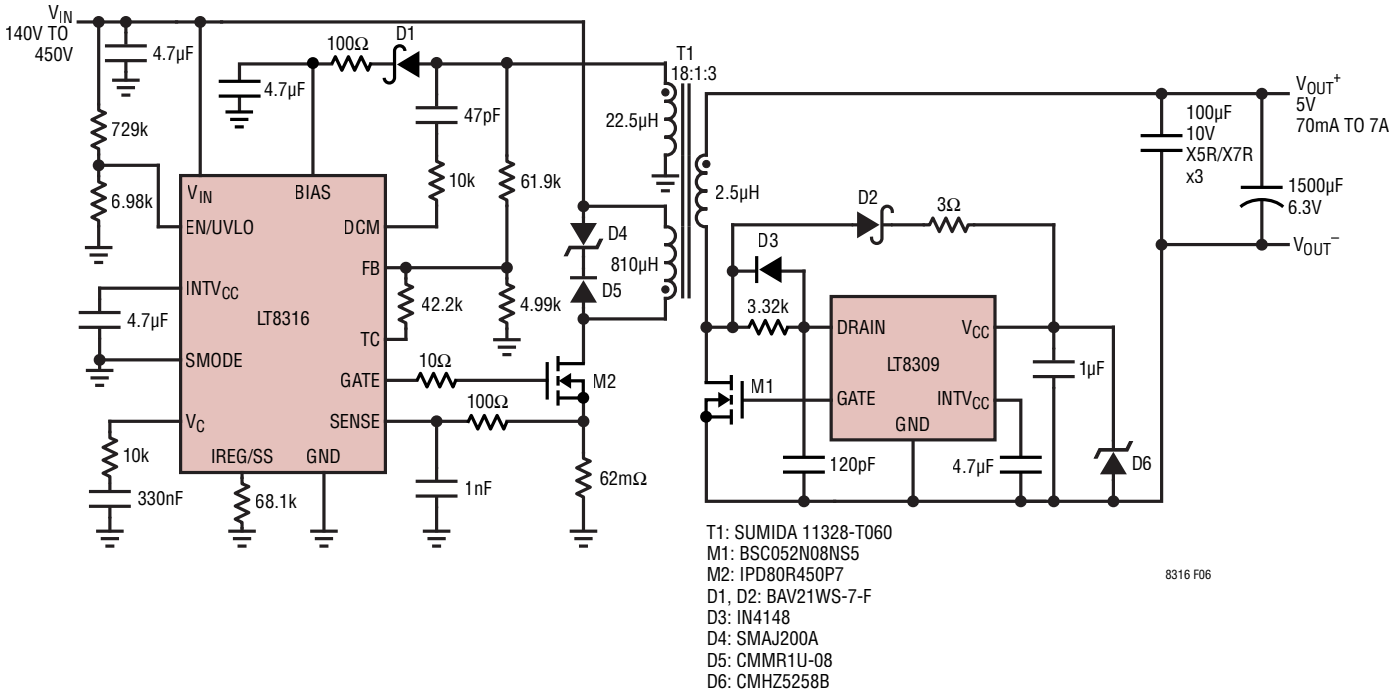



**Figure 6. 91% Efficient Isolated 5V/7A Synchronous Flyback Converter**

# APPLICATIONS INFORMATION

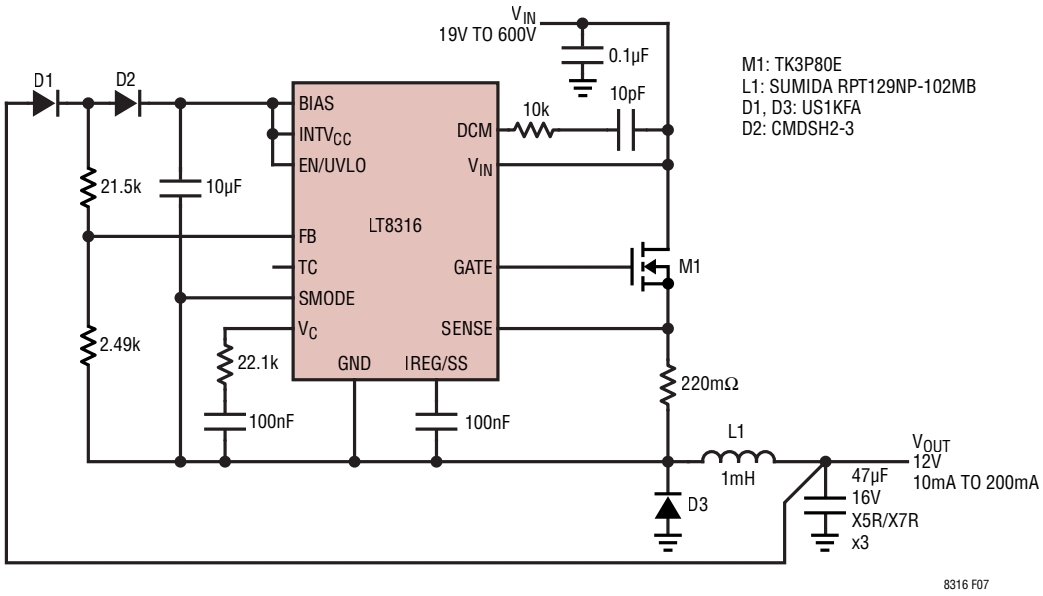



**Figure 7. Ultra-Wide Input Range Non-Isolated 12V Buck Converter**

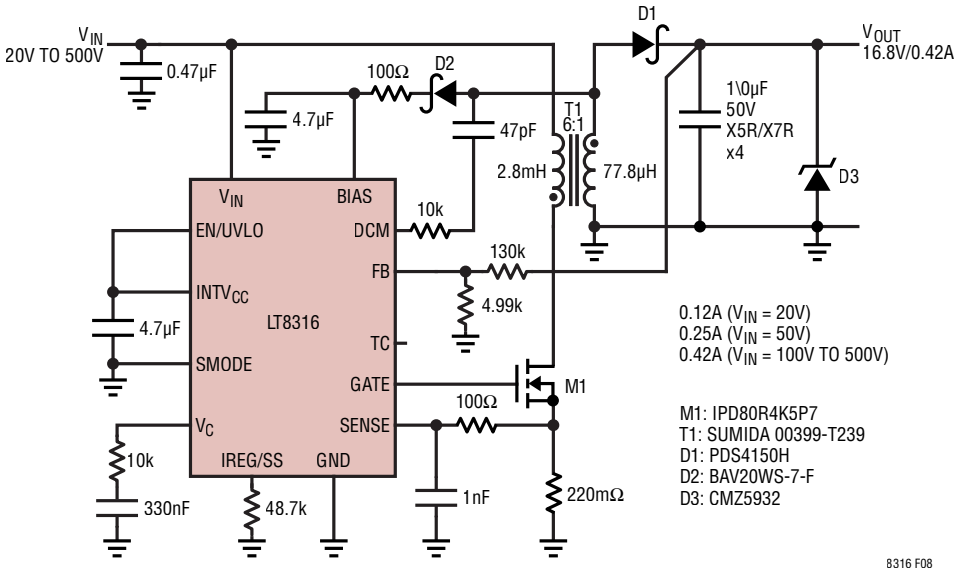



**Figure 8. Non-Isolated 16.8V Gate Drive Supply**

## APPLICATIONS INFORMATION

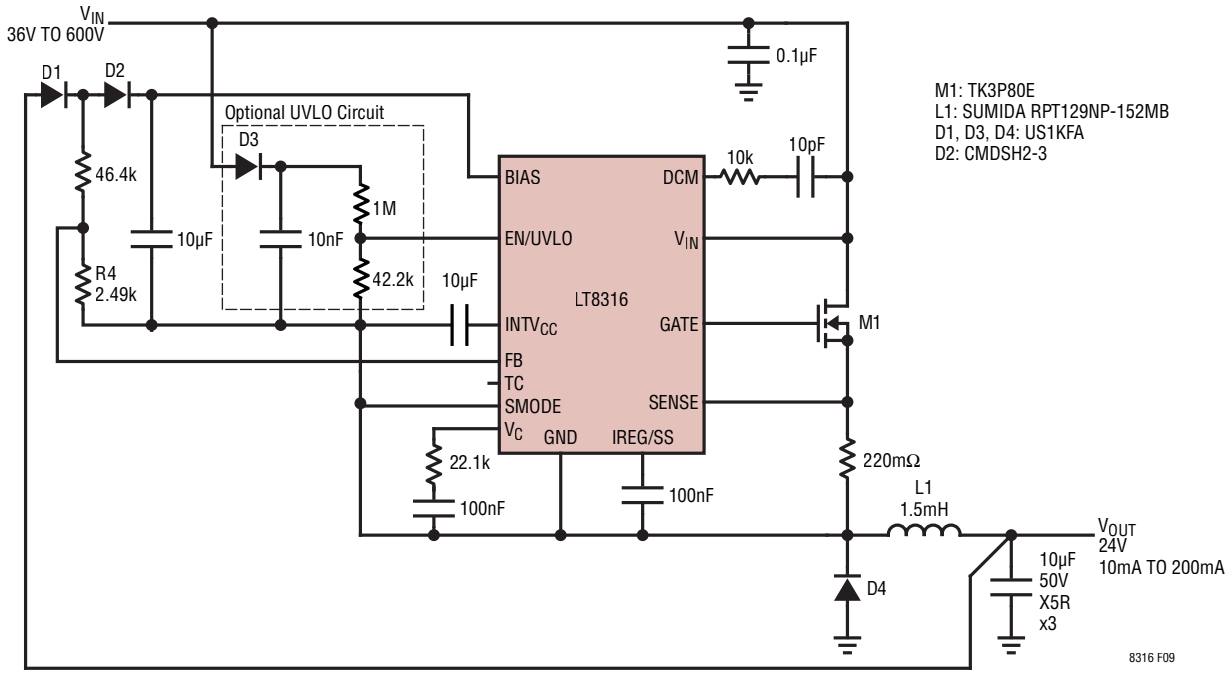
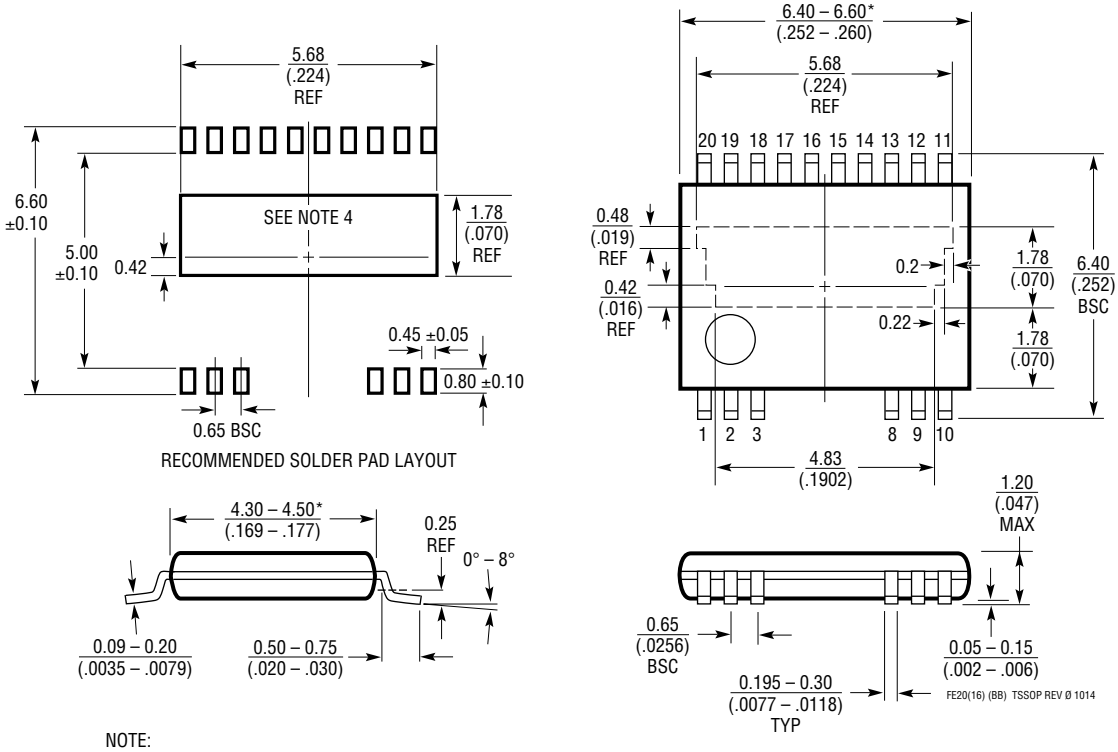



**Figure 9. Nonisolated 24V Buck Converter with Optional Undervoltage Lockout**

# PACKAGE DESCRIPTION

**FE Package**
**Variation: FE20(16)**
**20-Lead Plastic TSSOP (4.4mm)**
(Reference LTC DWG # 05-08-1990 Rev Ø)
**Exposed Pad Variation BB**




NOTE:
1. CONTROLLING DIMENSION: MILLIMETERS
2. DIMENSIONS ARE IN $\frac{\text{MILLIMETERS}}{(\text{INCHES})}$
3. DRAWING NOT TO SCALE
4. RECOMMENDED MINIMUM PCB METAL SIZE FOR EXPOSED PAD ATTACHMENT

*DIMENSIONS DO NOT INCLUDE MOLD FLASH. MOLD FLASH SHALL NOT EXCEED 0.150mm (.006") PER SIDE



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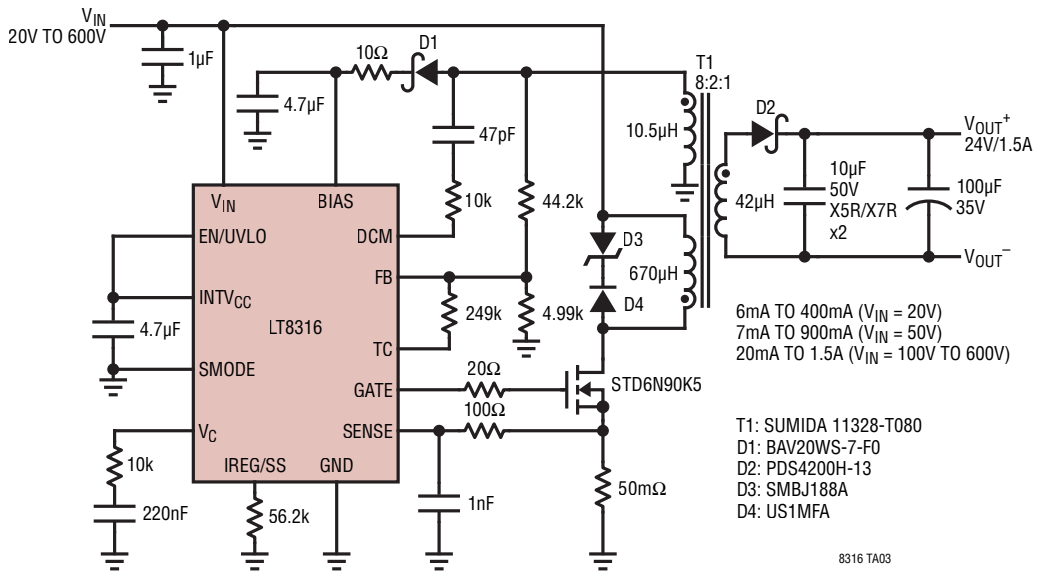
# TYPICAL APPLICATION

**Wide Input Range 24V Flyback Converter**




# RELATED PARTS

| PART NUMBER | DESCRIPTION | COMMENTS |
|---|---|---|
| LT8304/LT8304-1 | 100$V_{IN}$ Micropower Isolated Flyback Converter with 150V/2A Switch | Low $I_Q$ Monolithic No-Opto Flyback, SO-8 Package<br>LT8304-1 Is Recommended for High Output Voltages |
| LT8300 | 100$V_{IN}$ Micropower Isolated Flyback Converter with 150V/260mA Switch | Low $I_Q$ Monolithic No-Opto Flyback, 5-Lead TSOT-23 |
| LT8303 | 100$V_{IN}$ Micropower Isolated Flyback Converter with 150V/0.45A Switch | Low $I_Q$ Monolithic No-Opto Flyback, 5-Lead TSOT-23 |
| LT8301 | 42$V_{IN}$ Micropower Isolated Flyback Converter with 65V/1.2A Switch | Low $I_Q$ Monolithic No-Opto Flyback, 5-Lead TSOT-23 |
| LT8302 | 42$V_{IN}$ Micropower Isolated Flyback Converter with 65V/3.6A Switch | Low $I_Q$ Monolithic No-Opto Flyback, SO-8 Package |
| LT8309 | Secondary-Side Synchronous Rectifier Driver | 4.5V ≤ $V_{CC}$ ≤ 40V, Fast Turn-On and Turn-Off, 5-Lead TSOT-23 |
| LT3748 | 100V Isolated Flyback Controller | 5V ≤ $V_{IN}$ ≤ 100V, No-Opto Flyback, MSOP-16(12) |
| LT3798 | Off-Line Isolated No-Opto Flyback Controller with Active PFC | $V_{IN}$ and $V_{OUT}$ Limited Only by External Components |
| LT8312 | Boost Controller with Power Factor Correction | $V_{IN}$ and $V_{OUT}$ Limited Only by External Components |
| LT8315 | 560$V_{IN}$ Micropower Isolated Flyback Converter with 630V/300mA Switch | Low $I_Q$ Monolithic No-Opto Flyback, TSSOP-20(16) |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