

Dual Micropower, 1.4V/ μ s Precision Rail-to-Rail Output Amplifier

FEATURES

- **Excellent Slew Rate to Power Ratio**
 - **Slew Rate: 1.4V/ μ s**
 - **Maximum Supply Current: 20 μ A/Amplifier**
- **Maximum Offset Voltage: 30 μ V**
- High Dynamic Input Impedance
- Fast Recovery from Shutdown
- Maximum Input Bias Current: 3nA
- No Output Phase Inversion
- Gain Bandwidth Product: 40kHz
- Wide Specified Supply Range: 3V to 30V
- Operating Temperature Range: -40°C to 125°C
- Rail-to-Rail Outputs
- DFN and MS8 Packages

APPLICATIONS

- Precision Signal Processing
- DAC Amplifier
- Multiplexed ADC Applications
- Low Power Portable Systems
- Low Power Wireless Sensor Networks

DESCRIPTION

The **LT[®]6023** is a low power, enhanced slew rate, precision operational amplifier. The proprietary circuit topology of this amplifier gives excellent slew rate at low quiescent power dissipation without compromising precision or settling time. In addition, proprietary input stage circuitry allows the input impedance to remain high during input voltage steps as large as 5V. The combination of precision specs along with fast settling makes this part ideal for MUX applications.

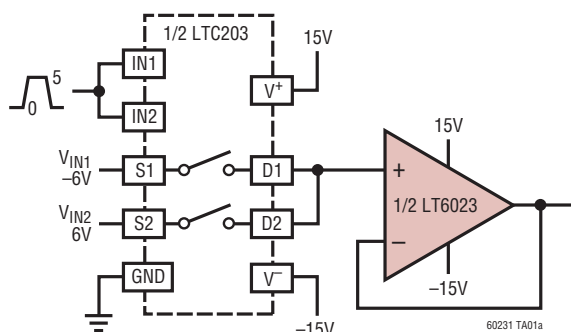
The low quiescent current of the LT6023 along with its ability to operate on supplies as low as 3V make it useful in portable systems. The LT6023-1 features a shutdown mode which reduces the typical supply current to 800nA.

The LT6023 is available in the small 8-lead DFN and 8-lead MSOP packages. The LT6023-1 is available in a 10-lead DFN package.

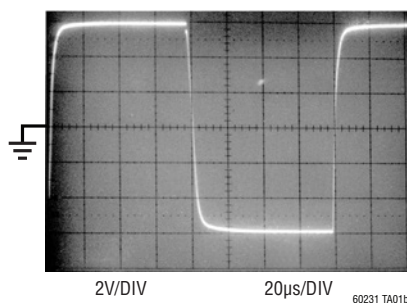
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TYPICAL APPLICATION

$\pm 13.6\text{V}$ Input Range MUX Buffer



MUX Buffer Response, 12V Step



LT6023/LT6023-1

ABSOLUTE MAXIMUM RATINGS

(Note 1)

Total Supply Voltage (V^+ to V^-)	36V	Operating and Specified Temperature Range	
Differential Input Voltage (within Supplies)	36V	I-Grade.....	-40°C to 85°C
Input Voltage (DGND, EN, +IN, -IN)		H-Grade	-40°C to 125°C
(Relative to V^-)	36V	Junction Temperature	150°C
Input Current (+IN, -IN, DGND, EN)	±10mA	Storage Temperature Range	-65°C to 150°C
Output Short-Circuit Duration	Indefinite	Lead Temperature (Soldering, 10 sec).....	300°C

PIN CONFIGURATION

TOP VIEW DD PACKAGE 8-LEAD (3mm × 3mm) PLASTIC DFN $\theta_{JA} = 43^\circ\text{C/W}$, $\theta_{JC} = 5.5^\circ\text{C/W}$ EXPOSED PAD (PIN 9) IS CONNECTED TO V^- (PIN 4) (PCB CONNECTION OPTIONAL)	TOP VIEW DD PACKAGE 10-LEAD (3mm × 3mm) PLASTIC DFN $\theta_{JA} = 43^\circ\text{C/W}$, $\theta_{JC} = 5.5^\circ\text{C/W}$ EXPOSED PAD (PIN 11) IS CONNECTED TO V^- (PIN 4) (PCB CONNECTION OPTIONAL)	TOP VIEW MS8 PACKAGE 8-LEAD PLASTIC MSOP $\theta_{JA} = 163^\circ\text{C/W}$, $\theta_{JC} = 40^\circ\text{C/W}$
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ORDER INFORMATION

LEAD FREE FINISH	TAPE AND REEL	PART MARKING*	PACKAGE DESCRIPTION	TEMPERATURE RANGE
LT6023IDD#PBF	LT6023IDD#TRPBF	LGRS	8-Lead (3mm × 3mm) Plastic DFN	-40°C to 85°C
LT6023HDD#PBF	LT6023HDD#TRPBF	LGRS	8-Lead (3mm × 3mm) Plastic DFN	-40°C to 125°C
LT6023IDD-1#PBF	LT6023IDD-1#TRPBF	LGRV	10-Lead (3mm × 3mm) Plastic DFN	-40°C to 85°C
LT6023HDD-1#PBF	LT6023HDD-1#TRPBF	LGRV	10-Lead (3mm × 3mm) Plastic DFN	-40°C to 125°C
LT6023IMS8#PBF	LT6023IMS8#TRPBF	LTGRT	8-Lead Plastic MSOP	-40°C to 85°C
LT6023HMS8#PBF	LT6023HMS8#TRPBF	LTGRT	8-Lead Plastic MSOP	-40°C to 125°C

Consult LTC Marketing for parts specified with wider operating temperature ranges. *The temperature grade is identified by a label on the shipping container.

For more information on lead free part marking, go to: <http://www.linear.com/leadfree/>

For more information on tape and reel specifications, go to: <http://www.linear.com/tapeandreel/>

ELECTRICAL CHARACTERISTICS The ● denotes the specifications which apply over the specified temperature range, otherwise specifications are at $T_A = 25^\circ\text{C}$, $V_S = \pm 15\text{V}$, $V_{CM} = V_{OUT} = \text{Mid-Supply}$, $V_{DGND} = 0\text{V}$, $V_{EN} = 5\text{V}$. DGND and EN specifications only apply to the LT6023-1.

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
V_{OS}	Input Offset Voltage	DD Packages	●	20	70 160	μV μV
		MS8 Package	●	5	30 160	μV μV
$\frac{\Delta V_{OS}}{\Delta \text{Temp}}$	Input Offset Voltage Drift (Note 2)	DD Packages	●	-3.5	± 0.9	$\mu\text{V}/^\circ\text{C}$
		MS8 Package	●	-2.9	± 0.5	$\mu\text{V}/^\circ\text{C}$
$\frac{\Delta V_{OS}}{\Delta \text{Time}}$	Long Term Input Offset Voltage Stability			± 0.2		$\mu\text{V}/\text{Mo}$
I_B	Input Bias Current	$T_A = -40^\circ$ to 85°C	●	-3	± 0.1	nA
		$T_A = -40^\circ$ to 125°C	●	-3	3	nA
			●	-10	10	nA
I_{OS}	Input Offset Current	$T_A = -40^\circ$ to 85°C	●	-1	± 0.1	nA
		$T_A = -40^\circ$ to 125°C	●	-1	1	nA
			●	-2	2	nA
	Input Noise Voltage	0.1Hz to 10Hz		3		μV_{P-P}
e_n	Input Noise Voltage Density	$f = 1\text{Hz}$		132		$\text{nV}/\sqrt{\text{Hz}}$
		$f = 1\text{kHz}$		132		$\text{nV}/\sqrt{\text{Hz}}$
i_n	Input Noise Current Density	$f = 1\text{kHz}$		12.1		$\text{fA}/\sqrt{\text{Hz}}$
C_{IN}	Input Capacitance	Common Mode		1.5		pF
		Differential Mode		2.5		pF
R_{IN}	Input Resistance	Common Mode		140		G Ω
		Differential Mode		330		M Ω
V_{ICM}	Common Mode Input Range		●	$V^- + 1.2$	$V^+ - 1.4$	V
CMRR	Common Mode Rejection Ratio	$V_{CM} = -13.8\text{V}$ to 13.6V	●	120	136	dB
			●	116		dB
PSRR	Supply Rejection Ratio	$V_S = 3\text{V}$ to 30V	●	120	140	dB
			●	110		dB
A_{VOL}	Large-Signal Voltage Gain	$R_L = 10\text{k}\Omega$, $V_{OUT} = \pm 14\text{V}$	●	110	114	dB
			●	100		dB
		$R_L = 100\text{k}\Omega$, $V_{OUT} = \pm 14.5\text{V}$	●	126	134	dB
V_{OL}	Output Swing Low ($V_{OUT} - V^-$)	$R_L = 10\text{k}\Omega$	●	180	300	mV
		$T_A = -40^\circ$ to 85°C	●		380	mV
		$T_A = -40^\circ$ to 125°C	●		430	mV
V_{OH}	Output Swing High ($V^+ - V_{OUT}$)	$R_L = 10\text{k}\Omega$	●	115	140	mV
		$T_A = -40^\circ$ to 85°C	●		165	mV
		$T_A = -40^\circ$ to 125°C	●		190	mV
I_{SC}	Short-Circuit Current	$V_{OUT} = 0\text{V}$, Sourcing	●	3	5.25	mA
		$T_A = -40^\circ$ to 85°C	●	2.5		mA
		$T_A = -40^\circ$ to 125°C	●	2		mA
		$V_{OUT} = 0\text{V}$, Sinking	●	6.5	15	mA
		$T_A = -40^\circ$ to 85°C	●	4.5		mA
		$T_A = -40^\circ$ to 125°C	●	4		mA

LT6023/LT6023-1

ELECTRICAL CHARACTERISTICS The ● denotes the specifications which apply over the specified temperature range, otherwise specifications are at $T_A = 25^\circ\text{C}$, $V_S = \pm 15\text{V}$, $V_{CM} = V_{OUT} = \text{Mid-Supply}$, $V_{DGND} = 0\text{V}$, $V_{EN} = 5\text{V}$. DGND and EN specifications only apply to the LT6023-1.

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
SR	Slew Rate	$A_{VCL} = 1$, 10V Step	0.85	1.4		V/ μs
		$T_A = -40^\circ$ to 85°C ●	0.7			V/ μs
		$T_A = -40^\circ$ to 125°C ●	0.6			V/ μs
		$A_{VCL} = 1$, 5V Step	0.3	0.65		V/ μs
GBW	Gain-Bandwidth Product	$f = 1\text{kHz}$ ●	29	40		kHz
	Minimum Supply Voltage	Guaranteed by PSRR ●	3			V
I_S	Supply Current per Amplifier	$T_A = -40^\circ$ to 85°C ●		18	20	μA
		$T_A = -40^\circ$ to 125°C ●			28	μA
					40	μA
	Supply Current in Shutdown	$V_{EN} = 0.8\text{V}$ $T_A = -40^\circ$ to 85°C ● $T_A = -40^\circ$ to 125°C ●		0.8	3	μA μA μA
t_s	Settling Time ($A_V = 1$)	0.1% 5V Output Step		40		μs
		0.01% 5V Output Step		60		μs
		0.0015% 5V Output Step		124		μs
		0.0015% 10V Output Step		132		μs
t_{ON}	Enable Time	$A_V = 1$		480		μs
V_{DGND}	DGND Pin Voltage Range	●	V^-		$V^+ - 3$	V
I_{DGND}	DGND Pin Current	●			-200	nA
I_{EN}	EN Pin Current	●			-200	nA
V_{ENL}	EN Pin Input Low Voltage	Relative to DGND ●			0.8	V
V_{ENH}	EN Pin Input High Voltage	Relative to DGND ●	1.7			V

ELECTRICAL CHARACTERISTICS The ● denotes the specifications which apply over the specified temperature range, otherwise specifications are at $T_A = 25^\circ\text{C}$, $V_S = 3\text{V}$, $V_{CM} = V_{OUT} = \text{Mid-Supply}$, $V_{DGND} = 0\text{V}$, $V_{EN} = 3\text{V}$. DGND and EN pin specifications only apply to the LT6023-1.

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
V_{OS}	Input Offset Voltage	DD Packages ●		20	100 190	μV μV
		MS8 Package ●		5	45 175	μV μV
$\frac{\Delta V_{OS}}{\Delta \text{Temp}}$	Input Offset Voltage Drift (Note 2)	DD Packages ●	-3.5	± 0.9	3.5	$\mu\text{V}/^\circ\text{C}$
		MS8 Package ●	-2.9	± 0.5	2.9	$\mu\text{V}/^\circ\text{C}$
$\frac{\Delta V_{OS}}{\Delta \text{Time}}$	Long Term Input Offset Voltage Stability			± 0.2		$\mu\text{V}/\text{Mo}$
I_B	Input Bias Current			± 1		nA
I_{OS}	Input Offset Current			± 0.1		nA
	Input Noise Voltage	0.1Hz to 10Hz		3		μV_{P-P}
e_n	Input Noise Voltage Density	$f = 1\text{Hz}$		132		$\text{nV}/\sqrt{\text{Hz}}$
		$f = 1\text{kHz}$		132		$\text{nV}/\sqrt{\text{Hz}}$
i_n	Input Noise Current Density	$f = 1\text{kHz}$		12.1		$\text{fA}/\sqrt{\text{Hz}}$
C_{IN}	Input Capacitance	Common Mode		1.5		pF
		Differential Mode		2.5		pF
R_{IN}	Input Resistance	Common Mode		140		G Ω
		Differential Mode		400		M Ω
V_{ICM}	Common Mode Input Range	●	$V^- + 1.2$		$V^+ - 1.4$	V
CMRR	Common Mode Rejection Ratio	$V_{CM} = 1.2\text{V to } 1.6\text{V}$		125		dB
PSRR	Supply Rejection Ratio	$V_S = 3\text{V to } 30\text{V}$ ●	120	140		dB
			110			dB
A_{VOL}	Large-Signal Voltage Gain	$R_L = 10\text{k}\Omega$, $V_{OUT} = 0.5\text{V to } 2.5\text{V}$ ●	98	108		dB
		●	95			dB
		$R_L = 100\text{k}\Omega$, $V_{OUT} = 0.5\text{V to } 2.5\text{V}$		136		dB
V_{OL}	Output Swing Low ($V_{OUT} - V^-$)	$R_L = 10\text{k}\Omega$		60	100	mV
		$T_A = -40^\circ\text{ to } 85^\circ\text{C}$ ●			150	mV
		$T_A = -40^\circ\text{ to } 125^\circ\text{C}$ ●			170	mV
V_{OH}	Output Swing High ($V^+ - V_{OUT}$)	$R_L = 10\text{k}\Omega$		60	80	mV
		$T_A = -40^\circ\text{ to } 85^\circ\text{C}$ ●			90	mV
		$T_A = -40^\circ\text{ to } 125^\circ\text{C}$ ●			100	mV
I_{SC}	Short-Circuit Current	$V_{OUT} = 1.5\text{V}$, Sourcing	2.5	3.5		mA
		$T_A = -40^\circ\text{ to } 85^\circ\text{C}$ ●	2.25			mA
		$T_A = -40^\circ\text{ to } 125^\circ\text{C}$ ●	2			mA
	$V_{OUT} = 1.5\text{V}$, Sinking	$T_A = -40^\circ\text{ to } 85^\circ\text{C}$ ●	3.5	5		mA
		$T_A = -40^\circ\text{ to } 85^\circ\text{C}$ ●	2			mA
		$T_A = -40^\circ\text{ to } 125^\circ\text{C}$ ●	2			mA
SR	Slew Rate (Note 3)	$A_{VCL} = -1$, 2V Step		0.05		V/ μs
GBW	Gain-Bandwidth Product	$f = 1\text{kHz}$		40		kHz
	Minimum Supply Voltage	Guaranteed by PSRR ●	3			V

LT6023/LT6023-1

ELECTRICAL CHARACTERISTICS The ● denotes the specifications which apply over the specified temperature range, otherwise specifications are at $T_A = 25^\circ\text{C}$, $V_S = 3\text{V}$, $V_{CM} = V_{OUT} = \text{Mid-Supply}$, $V_{DGND} = 0\text{V}$, $V_{EN} = 3\text{V}$. DGND and EN pin specifications only apply to the LT6023-1.

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
I_S	Supply Current per Amplifier	$T_A = -40^\circ$ to 85°C	●	15	20	μA
		$T_A = -40^\circ$ to 125°C	●		25	μA
					35	μA
I_S	Supply Current in Shutdown	$V_{EN} = 0.8\text{V}$		0.2	1.1	μA
		$T_A = -40^\circ$ to 85°C	●		1.5	μA
		$T_A = -40^\circ$ to 125°C	●		3	μA
t_s	Settling Time ($A_V = -1$)	0.1% 2.4V Output Step		85		μs
		0.01% 2.4V Output Step		100		μs
		0.0015% 2.4V Output Step		250		μs
t_{ON}	Enable Time	$A_V = 1$		580		μs
V_{DGND}	DGND Pin Voltage Range		●	V^-	$V^+ - 3$	V
I_{DGND}	DGND Pin Current			-75		nA
I_{EN}	EN Pin Current			-75		nA
V_{ENL}	EN Pin Input Low Voltage	Relative to DGND	●		0.8	V
V_{ENH}	EN Pin Input High Voltage	Relative to DGND	●	1.7		V

Note 1: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to any Absolute Maximum Rating condition for extended periods may affect device reliability and lifetime.

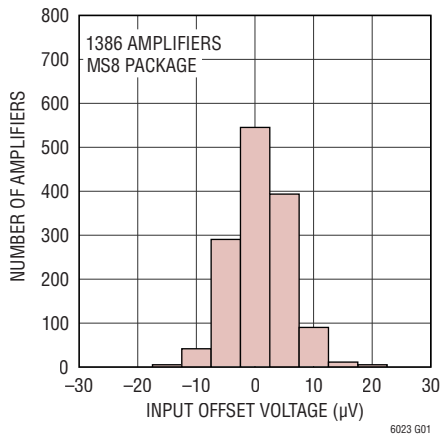
Note 2: Guaranteed by design.

Note 3: The slew rate of the LT6023 increases with the size of the input step. At lower supplies, the input step size is limited by the input common mode range. This trend can be seen in the Typical Performance Characteristics.

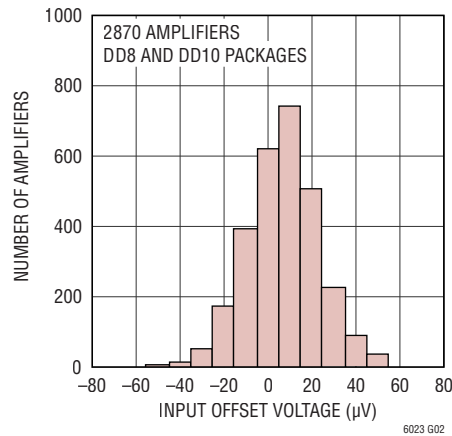
TYPICAL PERFORMANCE CHARACTERISTICS

$T_A = 25^\circ\text{C}$, $V_S = \pm 15\text{V}$, $R_L = 100\text{k}\Omega$, unless otherwise specified.

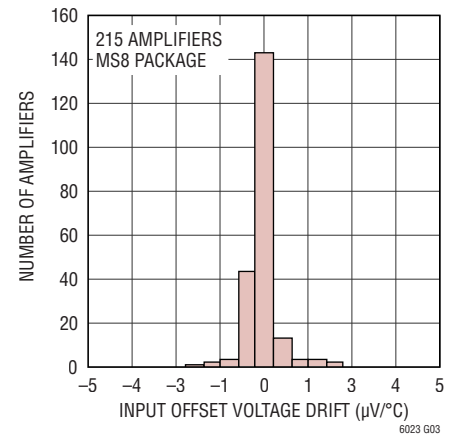
Typical Distribution of Input Offset Voltage



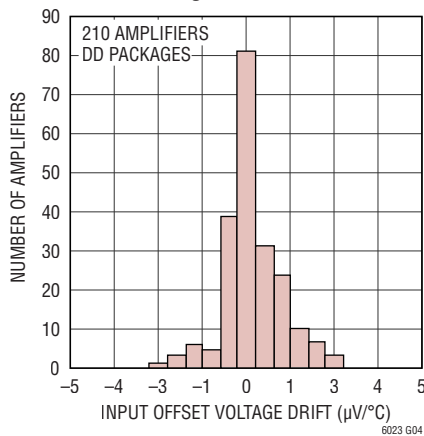
Typical Distribution of Input Offset Voltage



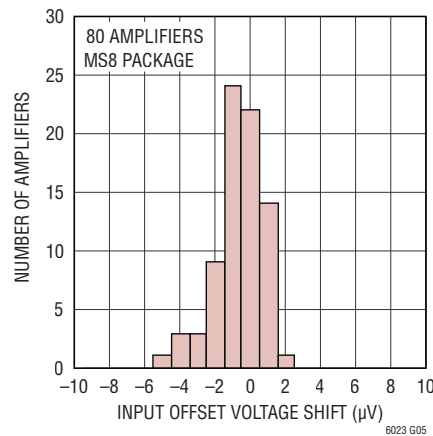
Typical Distribution of Input Offset Voltage Drift



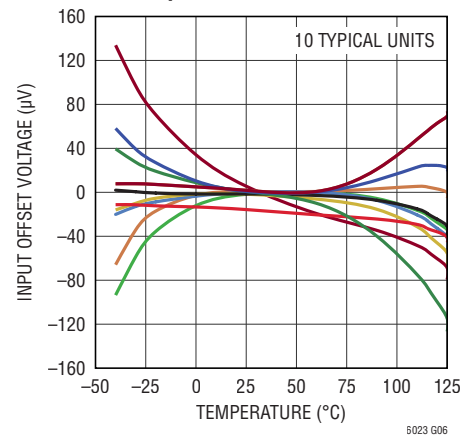
Typical Distribution of Input Offset Voltage Drift



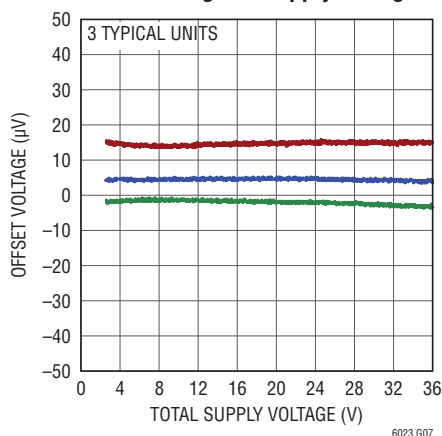
Offset Voltage Shift vs Lead Free IR Reflow



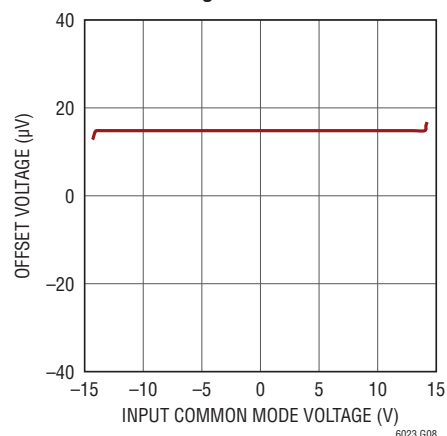
Typical Input Offset Voltage vs Temperature



Offset Voltage vs Supply Voltage

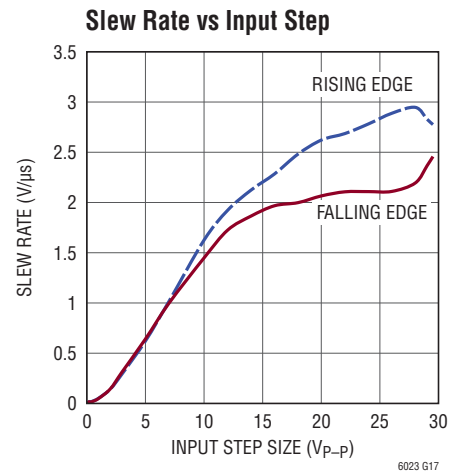
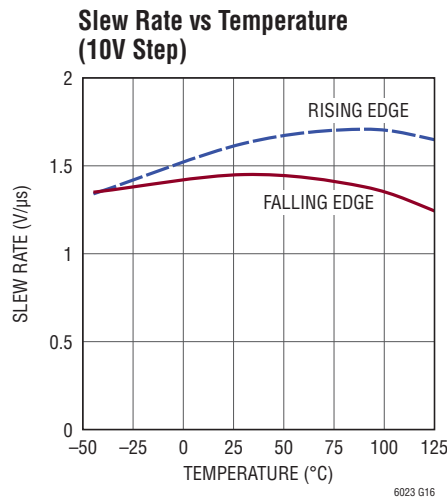
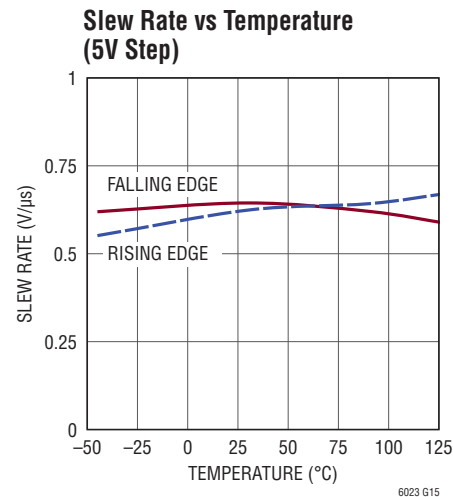
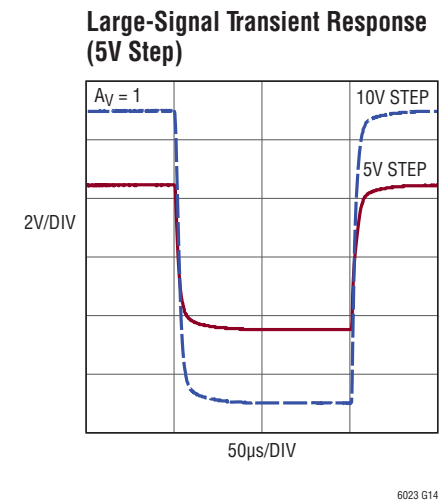
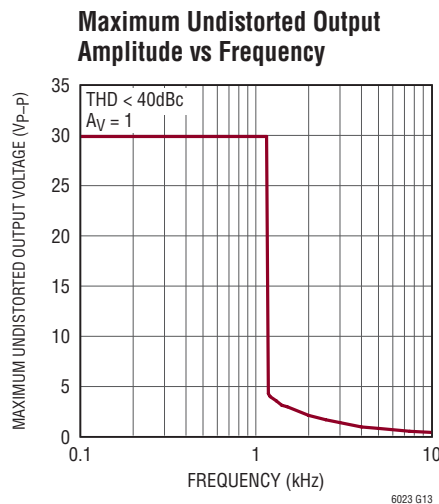
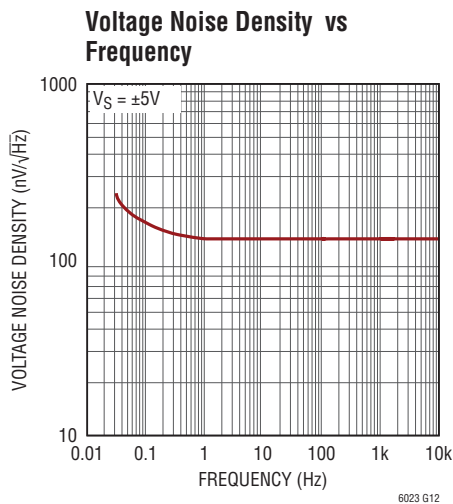
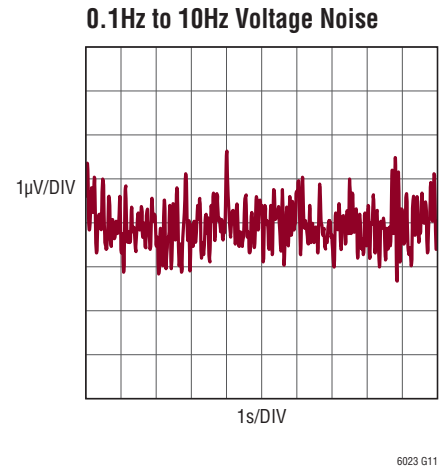
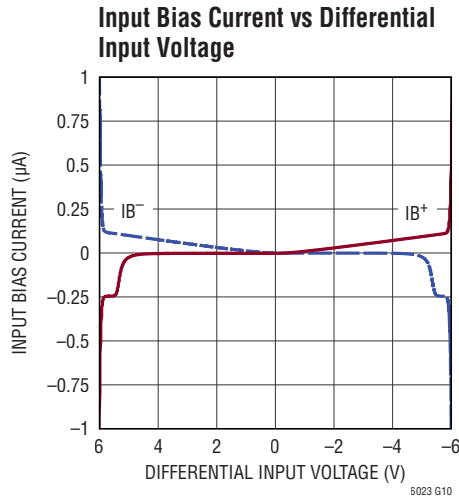
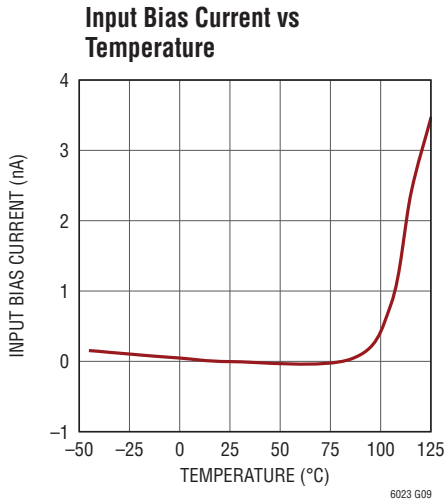


Offset Voltage vs Input Common Mode Voltage



TYPICAL PERFORMANCE CHARACTERISTICS

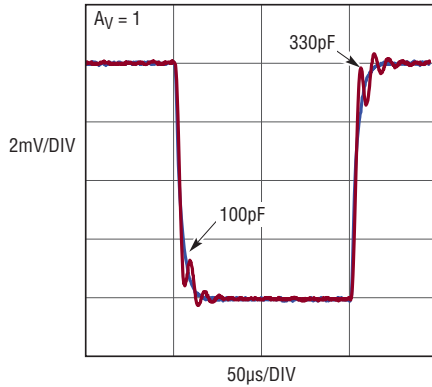
$T_A = 25^\circ\text{C}$, $V_S = \pm 15\text{V}$, $R_L = 100\text{k}\Omega$, unless otherwise specified.



TYPICAL PERFORMANCE CHARACTERISTICS

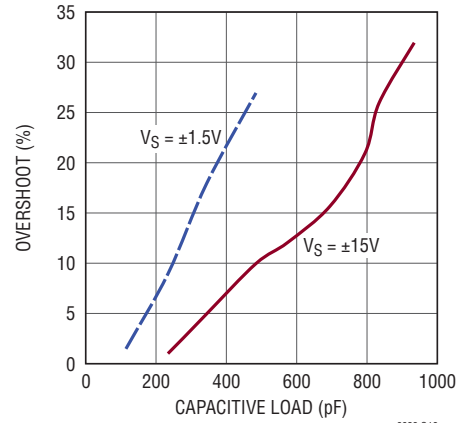
$T_A = 25^\circ\text{C}$, $V_S = \pm 15\text{V}$, $R_L = 100\text{k}\Omega$ unless otherwise specified.

Small-Signal Transient Response



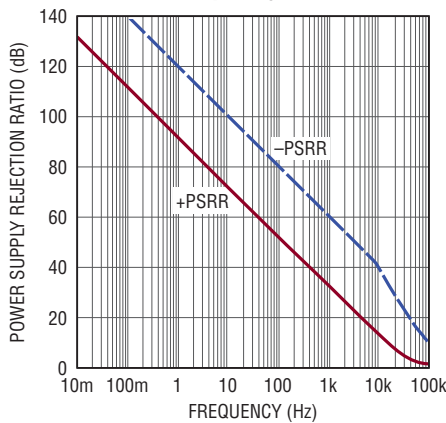
6023 G18

Overshoot vs Capacitive Load



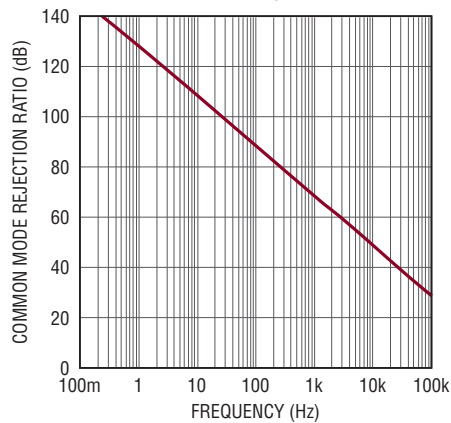
6023 G19

PSRR vs Frequency



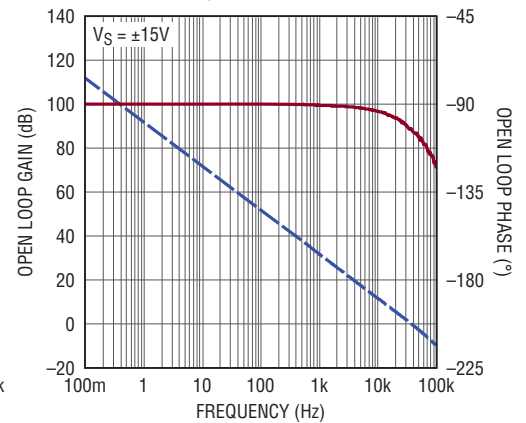
6023 G20

CMRR vs Frequency



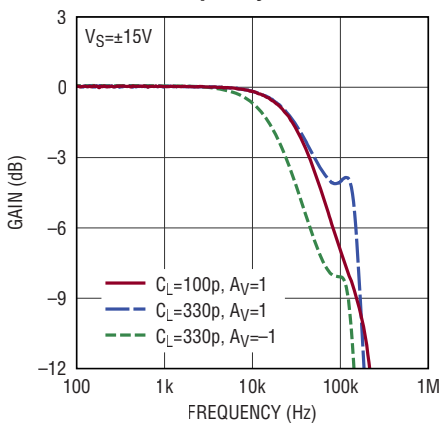
6023 G21

Open-Loop Gain and Phase vs Frequency



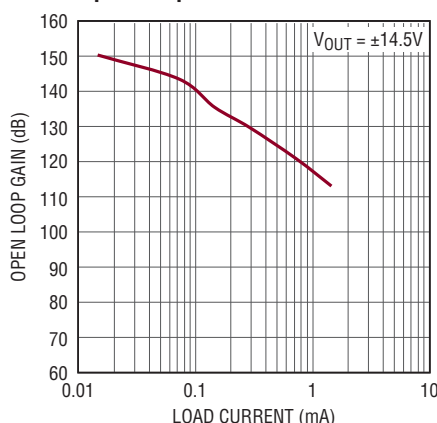
6023 G22

Gain vs Frequency



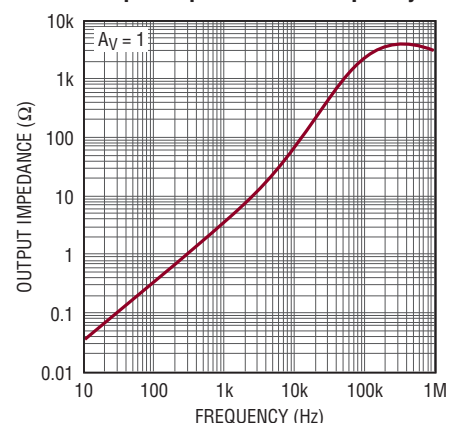
6023 G23

Open Loop Gain vs Load



6023 G24

Output Impedance vs Frequency

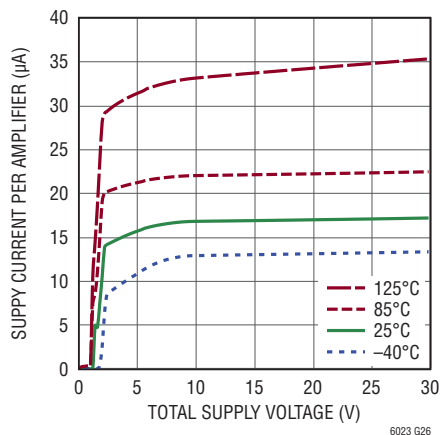


6023 G25

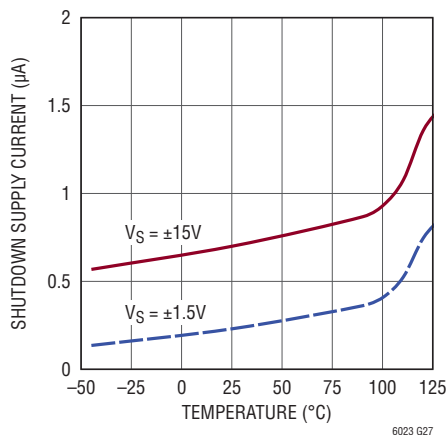
TYPICAL PERFORMANCE CHARACTERISTICS

$T_A = 25^\circ\text{C}$, $V_S = \pm 15\text{V}$, $R_L = 100\text{k}\Omega$ unless otherwise specified.

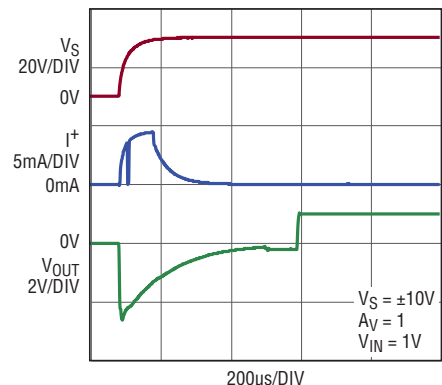
Supply Current vs Supply Voltage



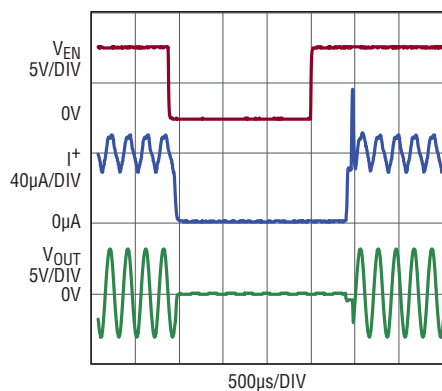
Shutdown Supply Current vs Temperature



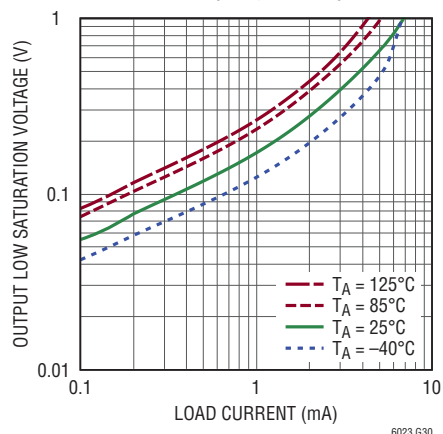
Start-Up Response



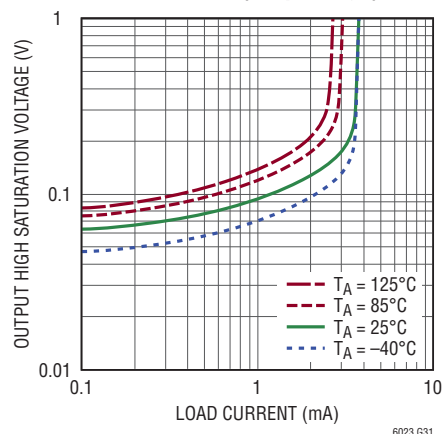
Enable/Disable Response



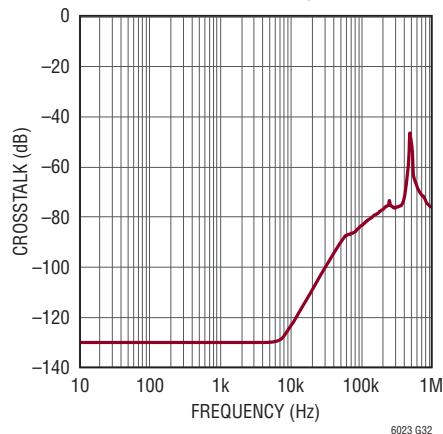
Output Saturation Voltage vs Sink Current (Output Low)



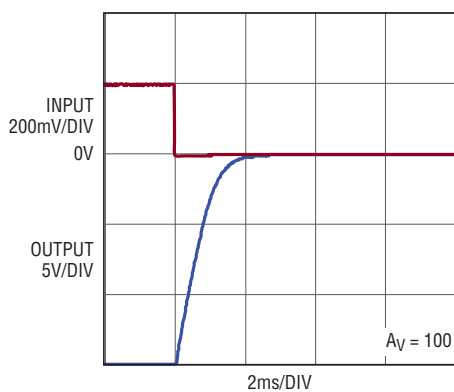
Output Saturation Voltage vs Source Current (Output High)



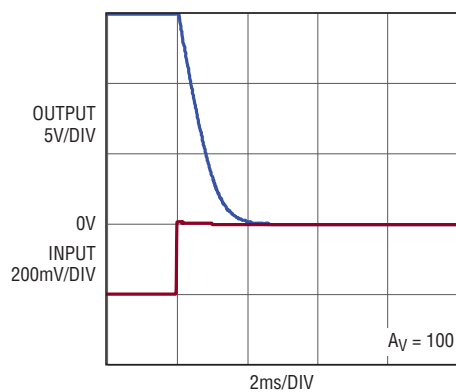
Crosstalk vs Frequency



Positive Output Overdrive Recovery



Negative Output Overdrive Recovery



PIN FUNCTIONS

OUT: Amplifier Output.

-IN: Inverting Input of the Amplifier.

+IN: Noninverting Input of the Amplifier.

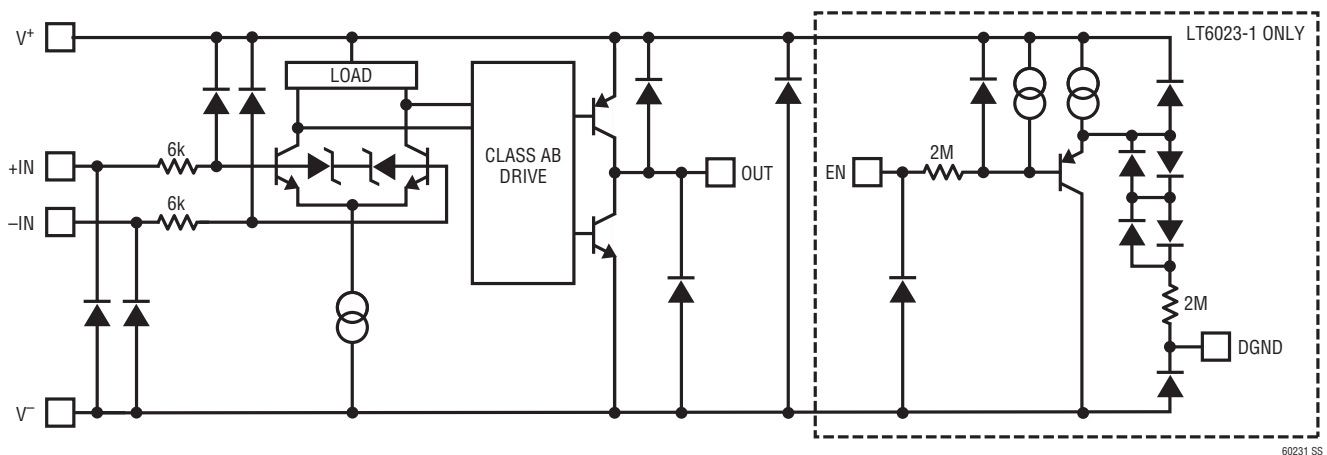
V⁻: Negative Power Supply. A bypass capacitor should be used between supply pins and ground. Additional bypass capacitance may be used between the power supply pins.

DGND (LT6023-1 Only): Reference for EN Pin. It is normally tied to ground. DGND must be in the range from V⁻ to V⁺ -3V. If grounded, V⁺ must be $\geq 3V$. The EN pin threshold is specified with respect to the voltage on the DGND pin. DGND cannot be floated.

EN (LT6023-1 Only): Enable Input. This pin must be connected high, normally to V⁺, for the amplifiers to be functional. EN is active high with the threshold approximately two diodes above DGND. EN cannot be floated. The shutdown threshold voltage is specified with respect to the voltage on the DGND pin.

V⁺: Positive Power Supply. A bypass capacitor should be used between supply pins and ground. Additional bypass capacitance may be used between the power supply pins.

SIMPLIFIED SCHEMATIC



60231 SS

APPLICATIONS INFORMATION

Preserving Low Power Operation

The proprietary circuitry used in the LT6023 provides an excellent combination of low power, low offset and enhanced slew rate. Normally an amplifier with higher supply current would be required to achieve this combination of slew rate and precision. Special care must be taken to ensure that the low power operation is preserved.

The choice of feedback resistor values impacts several op-amp parameters as noted in the feedback components section. It should also be noted that the output of the amplifier must drive this network. For example, in a gain of two with a total feedback resistance of 10k Ω and an output voltage of 14V, the amplifier's output will need to supply 1.4mA of current. This current will ultimately come from a supply.

The supply current of the LT6023 increases with large differential input voltages. Normally, this does not impact the low power nature of the LT6023 because the amplifier is forcing the two inputs to be at the same potential. Conditions which cause differential input voltage to appear should be avoided in order to preserve the low power dissipation of the LT6023. This includes but is not limited to: operation as a comparator, excessive loading on the output and overdriving the input.

Enhanced Slew Rate

The LT6023 uses a proprietary input stage which provides an enhanced slew rate without sacrificing input precision specs such as input offset voltage, common mode rejection and noise. The unique input stage of the LT6023 allows the output to quickly slew to its final value when large signal input steps are applied. This enhanced slew characteristic allows the LT6023 to quickly settle the output to 0.0015% independent of input step size as shown in Figure 1. Typical micropower amplifiers cannot process large amplitude signals with this speed. As shown in the Typical Performance curves, when the LT6023 is configured in unity gain and a 10V step is applied to the input the output will slew at 1.4V/ μ s. In this same configuration, a 5V input step will slew the output at 0.65V/ μ s. Furthermore, a 0.7V input step

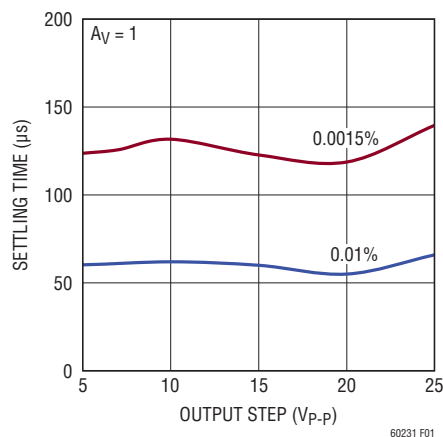


Figure 1. Settling Time Is Essentially Flat

will lower the slew rate to 0.02V/ μ s. Note that for these smaller inputs the LT6023 slew rate approaches the slew rate more common in traditional micropower amplifiers.

Input Bias Current

The design of the input stage of the LT6023 is more sophisticated than that shown in the Simplified Schematic. It uses both NPN and PNP input differential amplifiers to sense the input differential voltage. As a result the specified input bias current may flow in or out of the input pins.

Multiplexer Applications/High Dynamic Input Impedance

The LT6023 has features which make it desirable for multiplexer applications, such as the application featured on the front page of this data sheet. When the channels of the multiplexer are cycled, the output of the multiplexer can produce large voltage transitions. Normally, bipolar amplifiers have back-to-back diodes between the inputs, which will turn on when the input transient voltage exceeds 0.7V, causing a large transient current to be conducted from the amplifier output stage back into the input driving circuitry. The driving circuitry then needs to absorb this current and settle before the amplifier can settle. The LT6023 uses 5.5V Zener diodes to protect its inputs which dramatically increases its input impedance with input steps as large as 5V.

APPLICATIONS INFORMATION

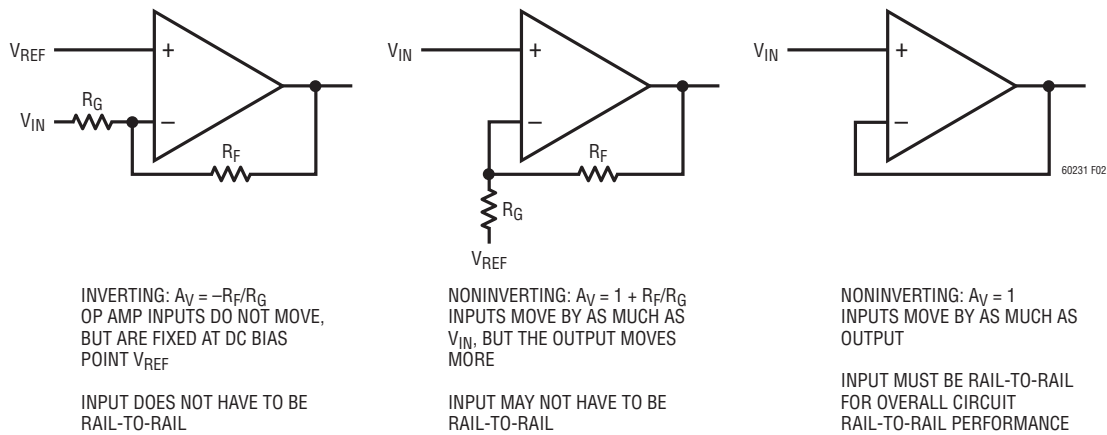


Figure 2. Some Op Amp Configurations Do Not Require Rail-to-Rail Inputs to Achieve Rail-to-Rail Outputs

Achieving Rail-to-Rail Operation without Rail-to-Rail Inputs

The LT6023 output is able to swing close to each power supply rail, but the input stage is limited to operating between $V^- + 1.2V$ and $V^+ - 1.4V$. For many inverting applications and noninverting gain applications, this is largely inconsequential. Figure 2 shows the basic op amp configurations, what happens to the op amp inputs and whether or not the op amp must have rail-to-rail inputs.

The circuit of Figure 3 shows an extreme example of the inverting case. The input voltage at the 100k resistor can swing $\pm 13.5V$ and the LT6023 will output an inverted, divided-by-ten version of the input voltage. The output

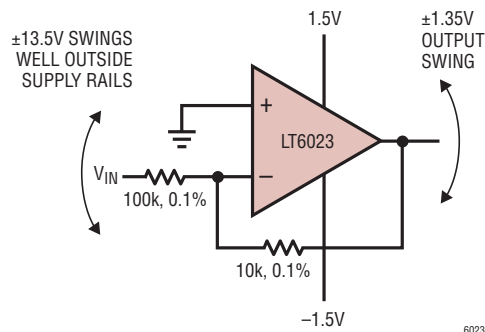


Figure 3. Extreme Inverting Case: Circuit Operates Properly with Input Voltage Swing Well Outside Op Amp Supply Rails

accuracy is limited by the resistors shown to 0.2%. Output referred, this error becomes 2.7mV. The 30 μV input offset voltage contribution, plus the additional error due to input bias current times the $\sim 10k$ effective source impedance, contribute only negligibly to error.

Phase Inversion

The LT6023 input stage is limited to operating between $V^- + 1.2V$ and $V^+ - 1.4V$. Exceeding this common mode range will cause the open loop gain to drop significantly. For a unity gain amplifier, the output roughly tracks the input well beyond the specified input voltage range as shown in Figure 4.

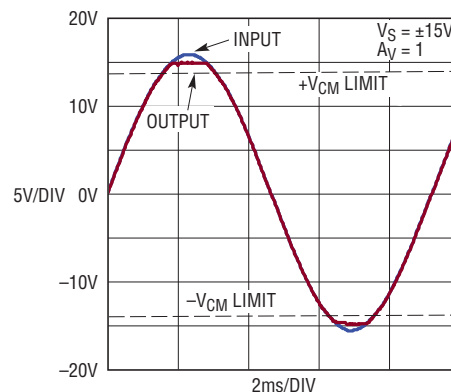


Figure 4. No Phase Inversion

APPLICATIONS INFORMATION

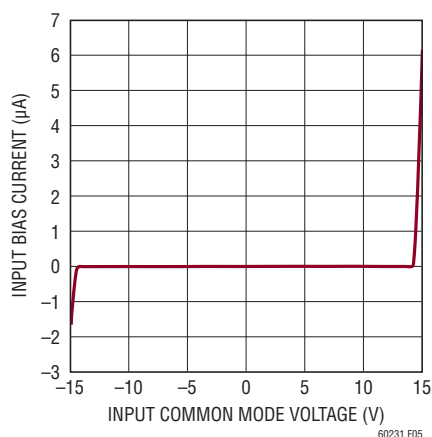


Figure 5. Increased I_b Beyond VICM

However the open loop gain is significantly reduced. While the output roughly tracks the input, the reduction in open loop gain degrades the accuracy of the LT6023 in this region. Exceeding the input common mode range also causes a significant increase in input bias current as shown in Figure 5. The output of the LT6023 is guaranteed over the specified temperature range not to phase invert as long as the input voltage does not exceed the supply voltage.

Preserving Input Precision

Preserving the input accuracy of the LT6023 requires that the application circuit and PC board layout do not introduce errors comparable to or greater than the offset of the amplifiers. Temperature differentials across the input connections can generate thermocouple voltages of tens of microvolts so the connections of the input leads should be short, close together and away from heat dissipating components. Air currents across the board can also generate temperature differentials.

As is the case with all amplifiers, a change in load current changes the finite open loop gain. Increased load current reduces the open loop gain as seen in the Typical Performance Characteristics section. This results in a

change in input offset voltage. Under large signal conditions with load currents of $\pm 1\text{mA}$ the effective change in input error is just tens of microvolts. In precision applications it is important to consider amplifier loading when selecting feedback resistor values as well as the loads on the device.

Feedback Components

Care must be taken to ensure that the phase shift formed by the feedback resistors and the parasitic capacitance at the inverting input does not degrade stability. For example, in a gain of +2 configuration, with 1M feedback resistors and a poorly designed circuit board layout with parasitic capacitance of 10pF (amplifier + PC board) at the amplifier's inverting input will cause the amplifier to have poor phase margin due to a pole formed at 32kHz. An additional capacitor of 10pF across the feedback resistor as shown in Figure 6 will eliminate any ringing or oscillation.

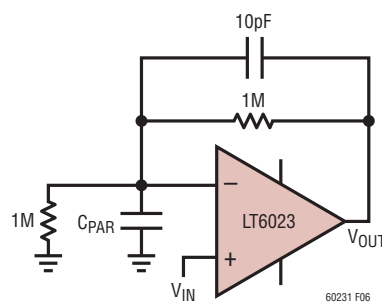


Figure 6. Stability with Parasitic Input Capacitance

Capacitive Loads

The LT6023 can drive capacitive loads up to 100pF in unity gain. The capacitive load driving capability increases as the amplifier is used in higher gain configurations. A small series resistance between the output and the load will further increase the amount of capacitance that the amplifier can drive.

APPLICATIONS INFORMATION

Shutdown Operation (LT6023-1)

The LT6023-1 shutdown function has been designed to be easily controlled from single supply logic or microcontrollers. To enable the LT6023-1 when $V_{DGND} = 0V$ the enable pin must be driven above 1.7V. Conversely, to enter the low power shutdown mode the enable pin must be driven below 0.8V. In a $\pm 15V$ dual supply application where $V_{DGND} = -15V$, the enable pin must be driven above $\sim -13.3V$ to enable the LT6023-1. If the enable pin is driven below $-14.2V$ the LT6023-1 enters the low power shutdown mode. Note that to enable the LT6023-1 the enable pin voltage can range from $-13.3V$ to $15V$ whereas

to disable the LT6023-1 the enable pin can range from $-15V$ to $-14.2V$. Figure 7 shows examples of enable pin control. While in shutdown, the outputs of the LT6023-1 are high impedance.

The LT6023-1 is typically capable of coming out of shutdown within $480\mu s$. This is useful in power sensitive applications where duty cycled operation is employed such as wireless mesh networks. In these applications the system is in low power mode the majority of the time, but then needs to wake up quickly and settle for an acquisition before being powered back down to save power.

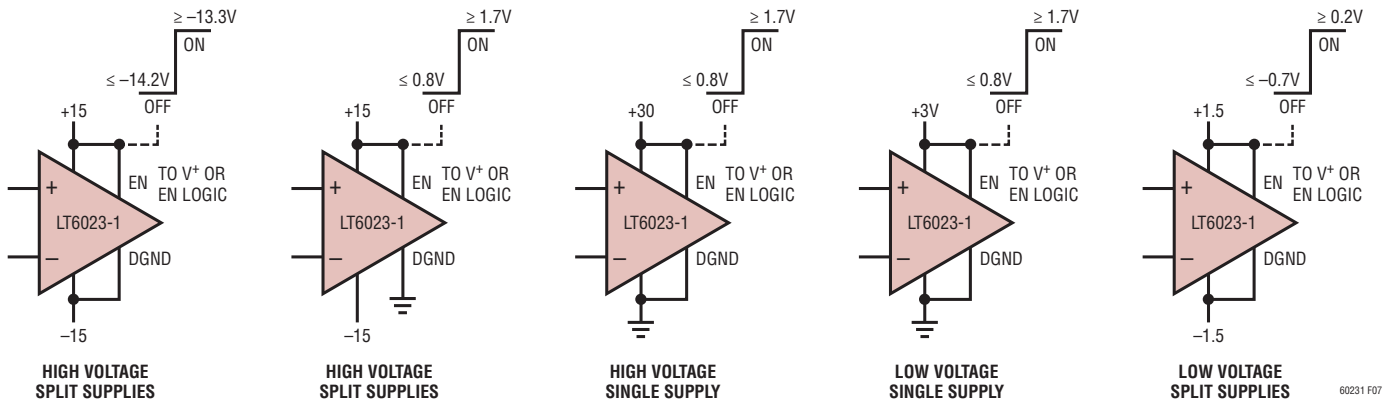
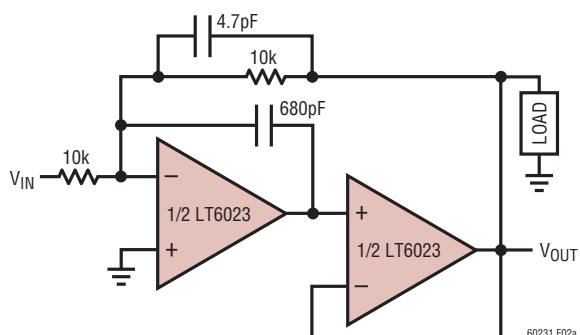


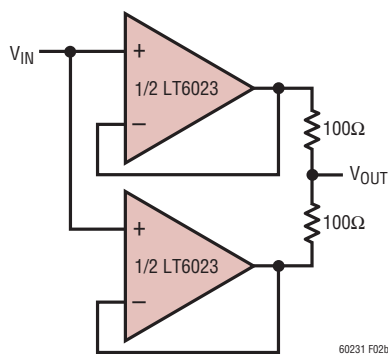
Figure 7. LT6023-1 Enable Pin Control Examples

TYPICAL APPLICATIONS

High Open-Loop Gain Composite Amplifier



Parallel Amplifiers Achieves 93nV/ $\sqrt{\text{Hz}}$ Noise, Doubles Output Drive and Lowers Offset

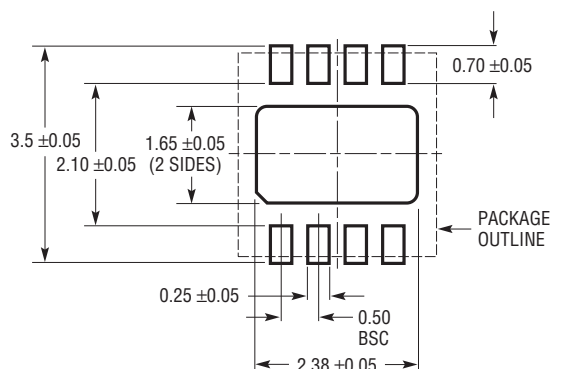


The circuit diagram illustrates a two-stage precision rectifier. The first stage uses an LT6656-4.096 precision centred zero-crossing detector. Its input (IN) is connected to a 12V supply through capacitor C1 (0.1µF). The output (OUT) is connected to the non-inverting input (+) of the first 1/2 LT6023 op-amp through capacitor C2 (1µF). The op-amp's inverting input (-) is connected to ground through resistor R1* (100k) and to the output through a feedback network consisting of resistor R2* (100k) and capacitor C5 (0.1µF). The output of the first stage is connected to the non-inverting input (+) of the second 1/2 LT6023 op-amp through resistor R5 (49.9kΩ). The second op-amp's inverting input (-) is connected to ground through resistor R3* (100k) and to the output through a feedback network consisting of resistor R4* (100k) and capacitor C3 (0.1µF). The final output of the circuit is connected to the output of the second op-amp through resistor R7 (49.9kΩ) and is filtered by capacitor C4 (10µF). The output voltage is 2.048V. The first stage output voltage is 4.096V. The circuit is powered by a 12V supply. The op-amps are identified as 1/2 LT6023. The resistors R1*, R2*, R3*, and R4* are specified as *LT5400-2.

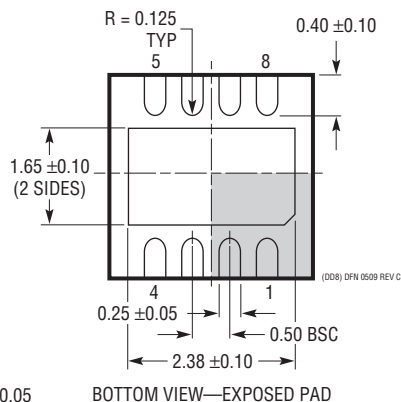
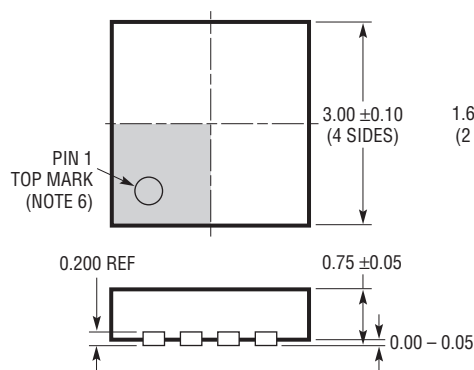
PACKAGE DESCRIPTION

Please refer to <http://www.linear.com/designtools/packaging/> for the most recent package drawings.

DD Package 8-Lead Plastic DFN (3mm × 3mm) (Reference LTC DWG # 05-08-1698 Rev C)



RECOMMENDED SOLDER PAD PITCH AND DIMENSIONS
APPLY SOLDER MASK TO AREAS THAT ARE NOT SOLDERED



NOTE:

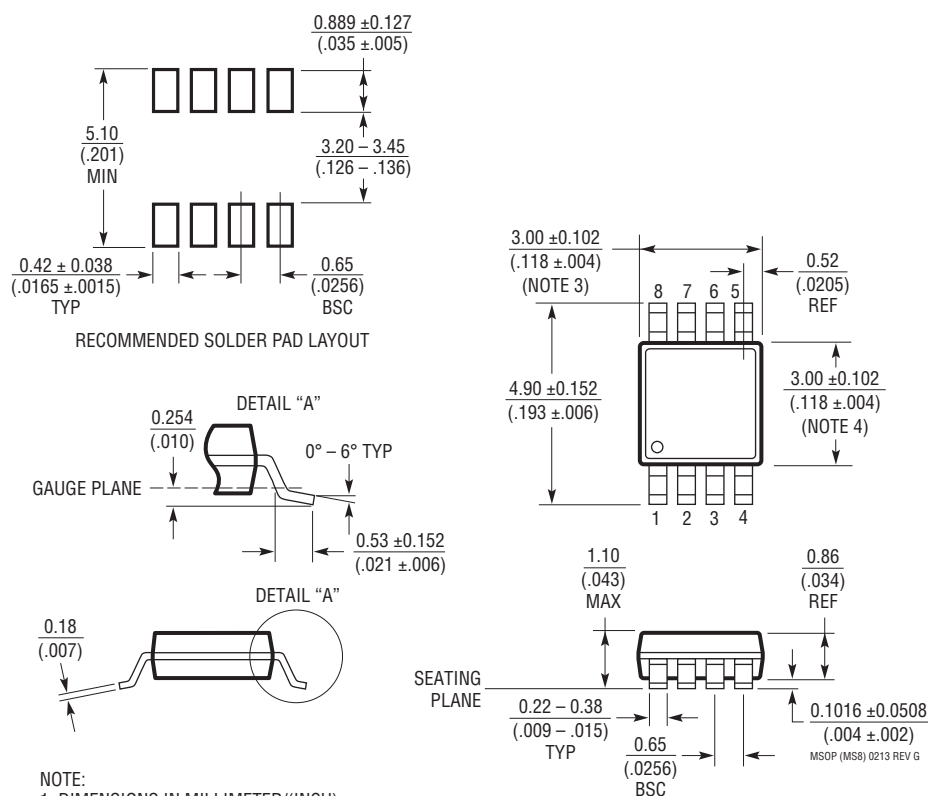
1. DRAWING TO BE MADE A JEDEC PACKAGE OUTLINE MO-229 VARIATION OF (WEED-1)
2. DRAWING NOT TO SCALE
3. ALL DIMENSIONS ARE IN MILLIMETERS
4. DIMENSIONS OF EXPOSED PAD ON BOTTOM OF PACKAGE DO NOT INCLUDE MOLD FLASH. MOLD FLASH, IF PRESENT, SHALL NOT EXCEED 0.15mm ON ANY SIDE
5. EXPOSED PAD SHALL BE SOLDER PLATED
6. SHADED AREA IS ONLY A REFERENCE FOR PIN 1 LOCATION ON TOP AND BOTTOM OF PACKAGE

PACKAGE DESCRIPTION

Please refer to <http://www.linear.com/designtools/packaging/> for the most recent package drawings.

MS8 Package 8-Lead Plastic MSOP

(Reference LTC DWG # 05-08-1660 Rev G)



REVISION HISTORY

REV	DATE	DESCRIPTION	PAGE NUMBER
A	04/15	Updated typical slew rate to be consistent throughout the data sheet	1, 4
		Corrected negative supply voltage on front page circuit	1
		Corrected Input Bias Current vs. Differential Input Voltage graph	8

R1 TO R4: FOR HIGH DC CMRR USE LT5400-3

60231 TA03a

The diagram shows an LT6023 op-amp configured as a Class AB output stage. The non-inverting input (+) is connected to V_{IN} , and the inverting input (-) is connected to the output V_{OUT} . The op-amp's output is connected to the bases of a 2N3904 (NPN) and a 2N3906 (PNP) transistor. The emitters of both transistors are connected to ground (V^-). The collector of the 2N3904 is connected to V^+ through a 1k resistor. The collector of the 2N3906 is connected to the output V_{OUT} . A load is connected between V_{OUT} and ground. The LT6023 is labeled with '60231 TA09b'.

[illegible]

PART NUMBER	DESCRIPTION	COMMENTS
LT6004	2kHz, 1μA RRIO Op Amp	V_{OS} : 500μV, GBW: 2kHz, SR: 0.8V/ms, e_n : 325nV/√Hz, I_S : 1μA
LT1490A	200kHz, 50μA RRIO Op Amp	V_{OS} : 500μV, GBW: 200kHz, SR: 0.06V/μs, e_n : 50nV/√Hz, I_S : 50μA
LTC6256	6.5MHz, 65μA RRIO Op Amp	V_{OS} : 350μV, GBW: 6.5MHz, SR: 1.8V/μs, e_n : 20nV/√Hz, I_S : 65μA
LT6020	400kHz, 100μA, 5V/μs Op Amp	V_{OS} : 30μV, GBW: 400kHz, SR: 5V/μs, e_n : 46nV/√Hz, I_S : 100μA
LTC2055	500kHz, 150μA Zero-Drift Op Amp	V_{OS} : 3μV, GBW: 500kHz, SR: 0.5V/μs, I_S : 150μA
LT1783	1.2MHz, 230μA Over-The-Top RRIO Op Amp	V_{OS} : 600μV, GBW: 1.2MHz, SR: 0.4V/μs, e_n : 20nV/√Hz, I_S : 230μA
LT1352	3MHz, 200V/μs Op Amp	V_{OS} : 600μV, GBW: 3MHz, SR: 200V/μs, e_n : 14nV/√Hz, I_S : 330μA
LT1492	5MHz, 3V/μs Op Amp	V_{OS} : 180μV, GBW: 5MHz, SR: 3V/μs, e_n : 16.5nV/√Hz, I_S : 550μA
LTC5800	SmartMesh® Wireless Sensor Network IC	Wireless Mesh Networks
LT5400	Quad Matched Resistor Network	0.01% Matching