# 40V, 5A, 2MHz Step-Down Switching Regulator with 3.3µA Quiescent Current

## FEATURES

- **Ultralow Quiescent Current:**
  **3.3µA $I_Q$ at $12V_{IN}$ to $3.3V_{OUT}$**
- **Low Ripple Burst Mode® Operation**
  **Output Ripple < $15mV_{P-P}$**
- **Wide Input Range: Operation from 4.3V to 40V**
- **5A Maximum Output Current**
- **Excellent Start-Up and Dropout Performance**
- **Adjustable Switching Frequency: 200kHz to 2MHz**
- **Synchronizable Between 250kHz to 2MHz**
- Accurate Programmable Undervoltage Lockout
- Low Shutdown Current: $I_Q$ = 700nA
- Power Good Flag
- Soft-Start Capability
- Thermal Shutdown Protection
- Current Limit Foldback with Soft-Start Override
- Saturating Switch Design: 75mΩ On-Resistance
- Small, Thermally Enhanced 16-Lead MSOP and 24-Lead 3mm × 5mm QFN Packages

## APPLICATIONS

- Automotive Battery Regulation
- Portable Products
- Industrial Supplies

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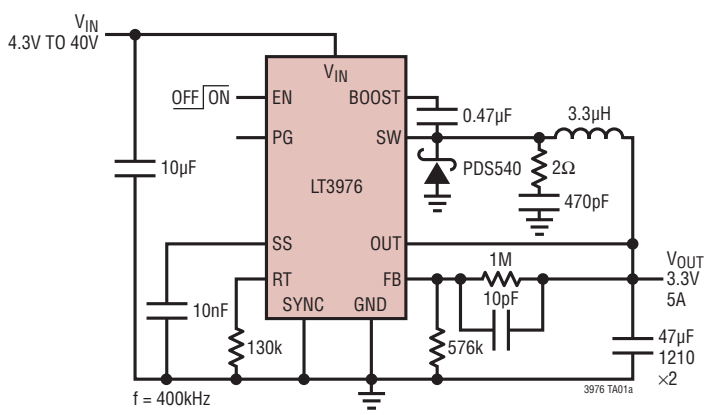
## DESCRIPTION

The LT®3976 is an adjustable frequency monolithic buck switching regulator that accepts a wide input voltage range up to 40V. Low quiescent current design consumes only 3.3µA of supply current while regulating with no load. Low ripple Burst Mode operation maintains high efficiency at low output currents while keeping the output ripple below 15mV in a typical application. The LT3976 can supply up to 5A of load current and has current limit foldback to limit power dissipation during short-circuit. A low dropout voltage of 500mV is maintained when the input voltage drops below the programmed output voltage, such as during automotive cold crank.

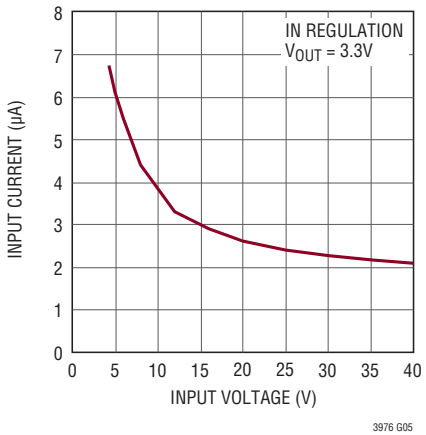
An internally compensated current mode topology is used for fast transient response and good loop stability. A high efficiency 75mΩ switch is included on the die along with a boost Schottky diode. An accurate 1.02V threshold enable pin can be driven directly from a microcontroller or used as a programmable undervoltage lockout. A capacitor on the SS pin provides a controlled inrush current (soft-start). A power good flag signals when $V_{OUT}$ reaches 91.6% of the programmed output voltage. The LT3976 is available in small 16-lead MSOP and 24-lead 3mm × 5mm QFN packages with exposed pad for low thermal resistance.

## TYPICAL APPLICATION

**3.3V Step-Down Converter**




**No-Load Supply Current**



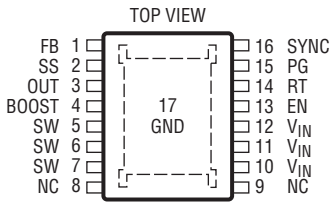
## ABSOLUTE MAXIMUM RATINGS

**(Note 1)**

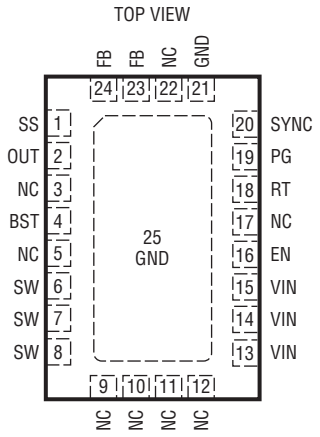
$V_{IN}$, EN Voltage (Note 3) .....40V
BOOST Pin Voltage .....55V
BOOST Pin Above SW Pin.....30V
FB, RT, SYNC, SS Voltage .....6V
PG Voltage .....30V
OUT Voltage.....16V

Operating Junction Temperature Range (Note 2)
LT3976E..... –40°C to 125°C
LT3976I ..... –40°C to 125°C
LT3976H ..... –40°C to 150°C
Storage Temperature Range ..... –65°C to 150°C
Lead Temperature (Soldering, 10 sec).....300°C

## PIN CONFIGURATION




MSE PACKAGE
16-LEAD PLASTIC MSOP
$\theta_{JA}$ = 40°C/W
EXPOSED PAD (PIN 17) IS GND, MUST BE SOLDERED TO PCB




UDD PACKAGE
24-LEAD (3mm × 5mm) PLASTIC QFN
$\theta_{JA}$ = 46°C/W
EXPOSED PAD (PIN 25) IS GND, MUST BE SOLDERED TO PCB

## ORDER INFORMATION

| LEAD FREE FINISH | TAPE AND REEL | PART MARKING* | PACKAGE DESCRIPTION | TEMPERATURE RANGE |
|---|---|---|---|---|
| LT3976EMSE#PBF | LT3976EMSE#TRPBF | 3976 | 16-Lead Plastic MSOP | –40°C to 125°C |
| LT3976IMSE#PBF | LT3976IMSE#TRPBF | 3976 | 16-Lead Plastic MSOP | –40°C to 125°C |
| LT3976HMSE#PBF | LT3976HMSE#TRPBF | 3976 | 16-Lead Plastic MSOP | –40°C to 150°C |
| LT3976EUDD#PBF | LT3976EUDD#TRPBF | LGHV | 24-Lead (3mm × 5mm) Plastic QFN | –40°C to 125°C |
| LT3976IUDD#PBF | LT3976IUDD#TRPBF | LGHV | 24-Lead (3mm × 5mm) Plastic QFN | –40°C to 125°C |

Consult LTC Marketing for parts specified with wider operating temperature ranges. *The temperature grade is identified by a label on the shipping container.Consult LTC Marketing for information on non-standard lead based finish parts.

For more information on lead free part marking, go to: http://www.linear.com/leadfree/
For more information on tape and reel specifications, go to: http://www.linear.com/tapeandreel/

## ELECTRICAL CHARACTERISTICS

**The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at $T_A$ = 25°C. (Note 2)**

| PARAMETER | CONDITIONS | | MIN | TYP | MAX | UNITS |
|---|---|---|---|---|---|---|
| Minimum Input Voltage | (Note 3) | ● | | 4 | 4.3 | V |
| Dropout Comparator Threshold | ($V_{IN}$ – OUT) Falling | | 430 | 500 | 570 | mV |
| Dropout Comparator Threshold Hysteresis | | | | 25 | | mV |
| Quiescent Current from $V_{IN}$ | $V_{EN}$ Low<br>$V_{EN}$ High, $V_{SYNC}$ Low<br>$V_{EN}$ High, $V_{SYNC}$ Low | <br><br>● | | 0.7<br>1.6 | 1.3<br>2.7<br>30 | µA<br>µA<br>µA |
| FB Pin Current | $V_{FB}$ = 1.5V | ● | | 0.1 | 12 | nA |
| Feedback Voltage | | <br>● | 1.183<br>1.173 | 1.197<br>1.197 | 1.212<br>1.222 | V<br>V |
| FB Voltage Line Regulation | 4.3V < $V_{IN}$ < 40V (Note 3) | | | 0.0003 | 0.01 | %/V |
| Switching Frequency | $R_T$ = 11.8k<br>$R_T$ = 41.2k<br>$R_T$ = 294k | | 1.8<br>0.8<br>160 | 2.25<br>1<br>200 | 2.7<br>1.2<br>240 | MHz<br>MHz<br>kHz |
| Minimum Switch On-Time | | | | 120 | | ns |
| Minimum Switch Off-Time (Note 4) | | | | 150 | 200 | ns |
| Switch Current Limit | $V_{FB}$ = 1V | | 7.5 | 10 | 12.5 | A |
| Foldback Switch Current Limit | $V_{FB}$ = 0V | | | 4.8 | | A |
| Switch $V_{CESAT}$ | $I_{SW}$ = 1A | | | 80 | | mV |
| Switch Leakage Current | | | | 0.02 | 1 | µA |
| Boost Schottky Forward Voltage | $I_{SH}$ = 100mA | | | 730 | | mV |
| Boost Schottky Reverse Leakage | $V_{REVERSE}$ = 12V | | | 0.02 | 2 | µA |
| Minimum Boost Voltage (Note 5) | | ● | | 1.3 | 1.8 | V |
| BOOST Pin Current | $I_{SW}$ = 1A, $V_{BOOST}$ – $V_{SW}$ = 3V | | | 20 | 32 | mA |
| EN Voltage Threshold | EN Falling, $V_{IN}$ ≥ 4.3V | ● | 0.92 | 1.02 | 1.12 | V |
| EN Voltage Hysteresis | | | | 60 | | mV |
| EN Pin Current | | | | 0.2 | 20 | nA |
| PG Threshold Offset from $V_{FB}$ | $V_{FB}$ Falling | | 5 | 8.4 | 13 | % |
| PG Hysteresis as % of Output Voltage | | | | 1.7 | | % |
| PG Leakage | $V_{PG}$ = 3V | | | 0.02 | 1 | µA |
| PG Sink Current | $V_{PG}$ = 0.4V | ● | 125 | 480 | | µA |
| SYNC Low Threshold | | | 0.6 | 1.0 | | V |
| SYNC High Threshold | | | | 1.18 | 1.5 | V |
| SYNC Pin Current | $V_{SYNC}$ = 6V | | | 0.1 | | nA |
| SS Source Current | $V_{SS}$ = 0.5V | | 0.9 | 1.8 | 2.6 | µA |

**Note 1:** Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to any Absolute Maximum Rating condition for extended periods may affect device reliability and lifetime.

**Note 2:** The LT3976E is guaranteed to meet performance specifications from 0°C to 125°C junction temperature. Specifications over the –40°C to 125°C operating junction temperature range are assured by design, characterization, and correlation with statistical process controls. The LT3976I is guaranteed over the full –40°C to 125°C operating junction temperature range. The LT3976H is guaranteed over the full –40°C to 150°C operating junction temperature range. High junction temperatures degrade operating lifetimes. Operating lifetime is derated at junction temperatures greater than 125°C. The junction temperature ($T_J$, in °C) is calculated from the ambient temperature ($T_A$, in °C) and power dissipation ($P_D$, in Watts) according to the formula:

$$T_J = T_A + (P_D \bullet \theta_{JA})$$

where $\theta_{JA}$ (in °C/W) is the package thermal impedance.

## ELECTRICAL CHARACTERISTICS

**Note 3:** Minimum input voltage depends on application circuit.

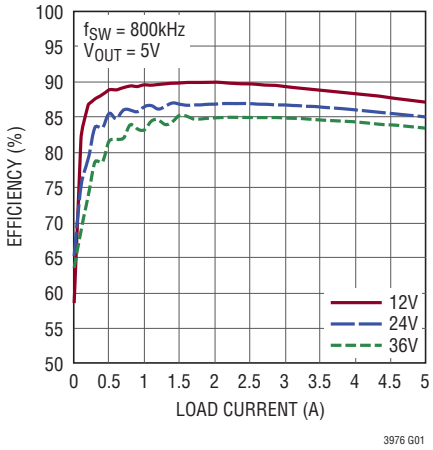
**Note 4:** The LT3976 contains circuitry that extends the maximum duty cycle if there is sufficient voltage across the boost capacitor. See the Application Information section for more details.

**Note 5:** This is the minimum voltage across the boost capacitor needed to guarantee full saturation of the switch.

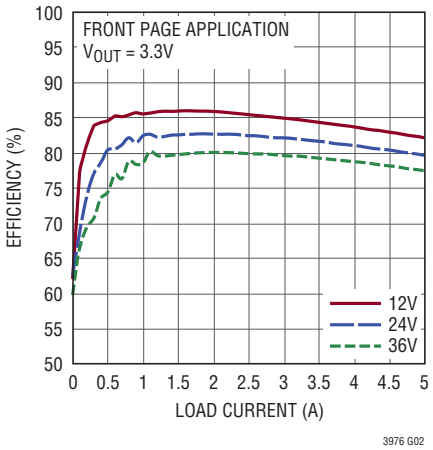
**Note 6:** This IC includes overtemperature protection that is intended to protect the device during momentary overload conditions. Junction temperature will exceed the maximum operating junction temperature when overtemperature protection is active. Continuous operation above the specified maximum operating junction temperature may impair device reliability or permanently damage the device.

## TYPICAL PERFORMANCE CHARACTERISTICS $T_A$ = 25°C, unless otherwise noted.

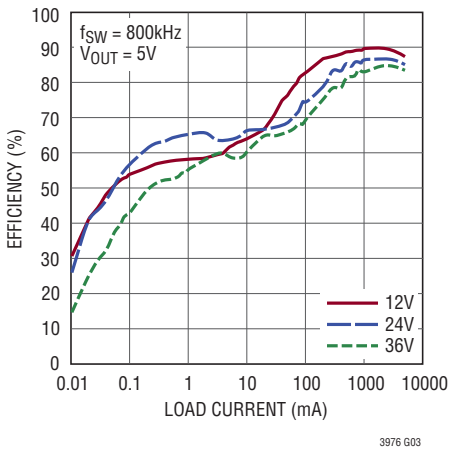
**Efficiency at $5V_{OUT}$**



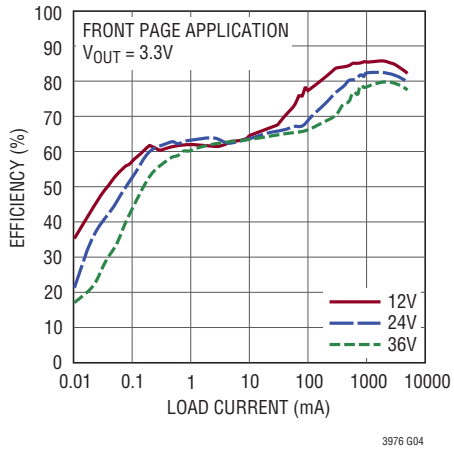

**Efficiency at $3.3V_{OUT}$**



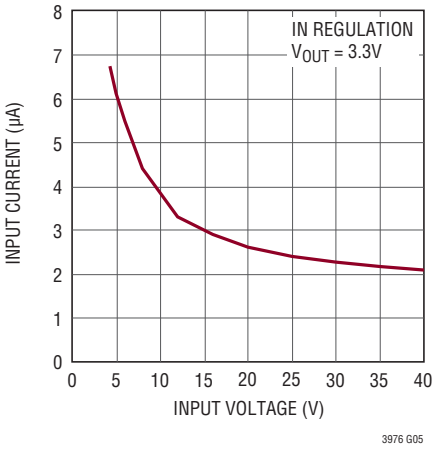

**Efficiency at $5V_{OUT}$**



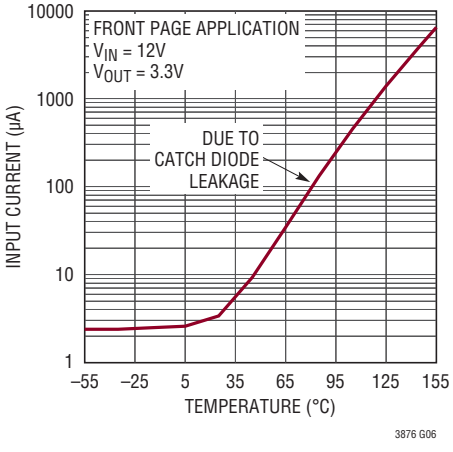

**Efficiency at $3.3V_{OUT}$**




**No-Load Supply Current**

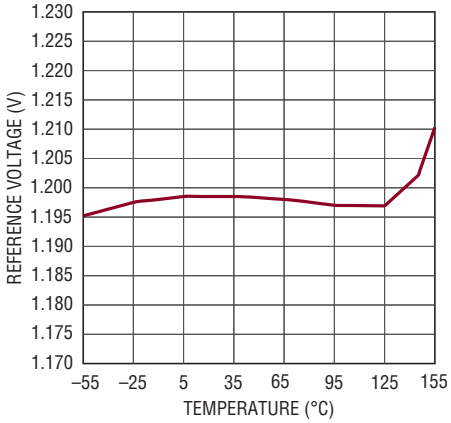



**No-Load Supply Current**



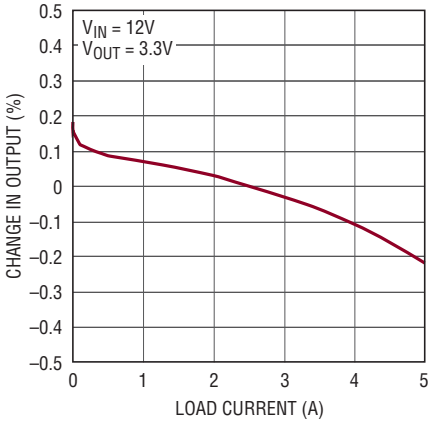
## TYPICAL PERFORMANCE CHARACTERISTICS $T_A$ = 25°C, unless otherwise noted.

### Reference Voltage



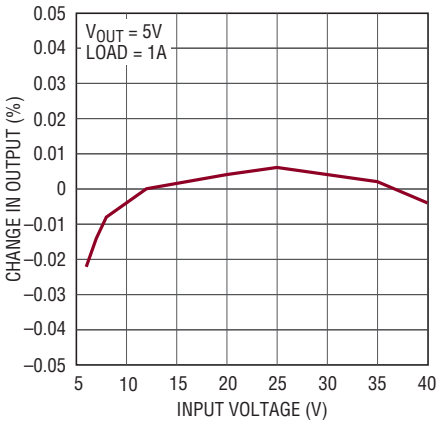

3976 G07

### Load Regulation



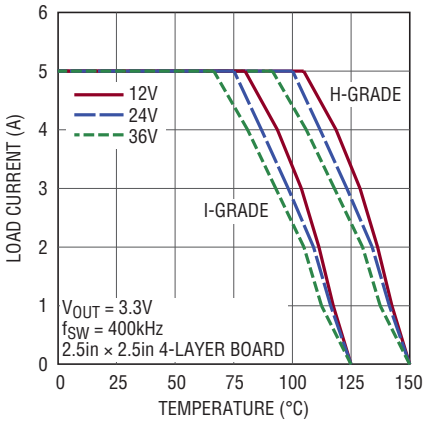

3976 G08

### Line Regulation




3976 G09

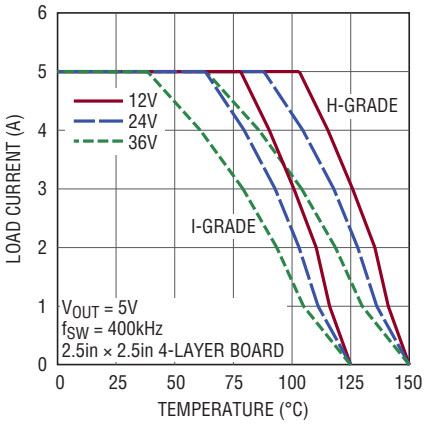
### Thermal Derating




LIMITED BY MAXIMUM
JUNCTION TEMPERATURE
$\Theta_{JA}$ = 40°C/W

3976 G10

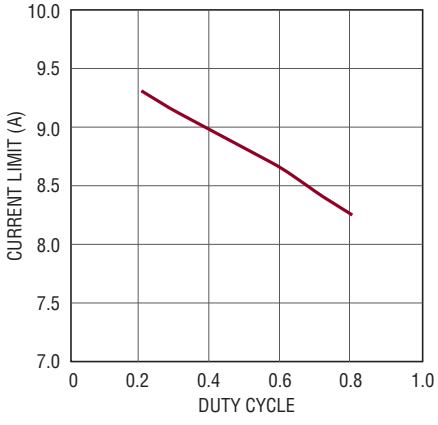
### Thermal Derating




LIMITED BY MAXIMUM
JUNCTION TEMPERATURE
$\Theta_{JA}$ = 40°C/W

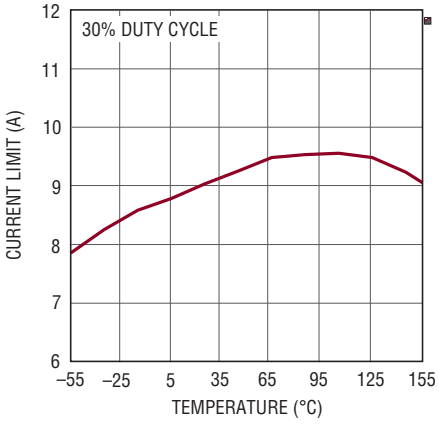
3976 G11

### Switch Current Limit



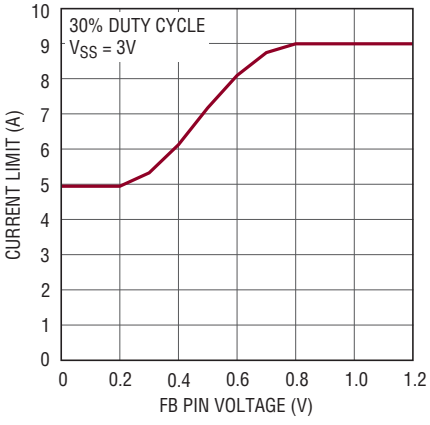

3976 G12

### Switch Current Limit



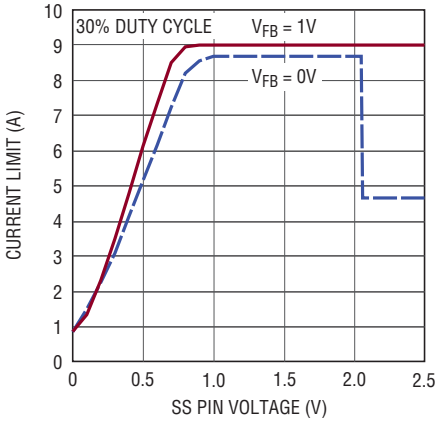

3976 G13

### Current Limit Foldback




3976 G14

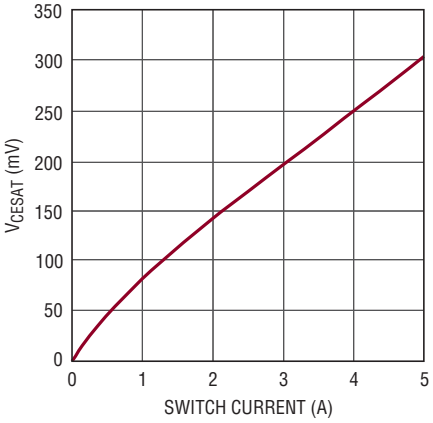
### Soft-Start



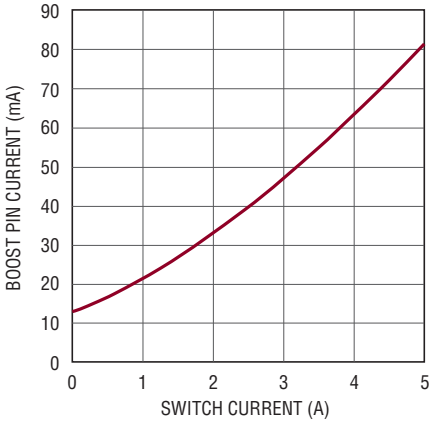

3976 G15

## TYPICAL PERFORMANCE CHARACTERISTICS $T_A$ = 25°C, unless otherwise noted.

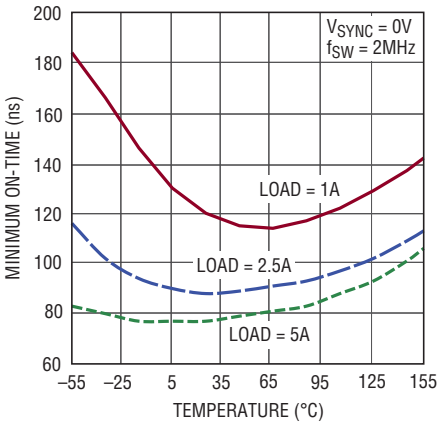
### Switch $V_{CESAT}$



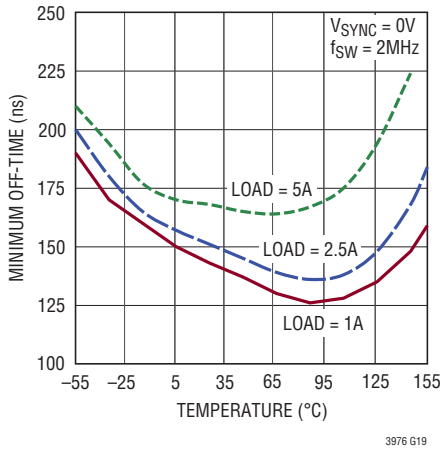

### BOOST Pin Current



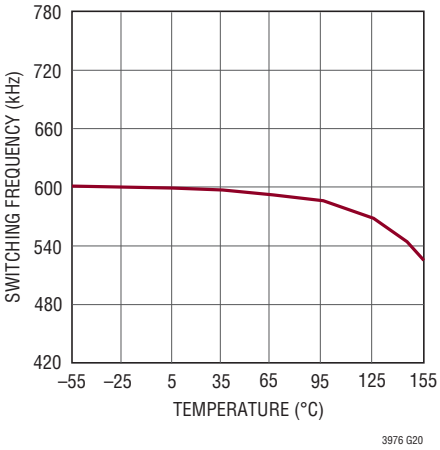

### Minimum On-Time



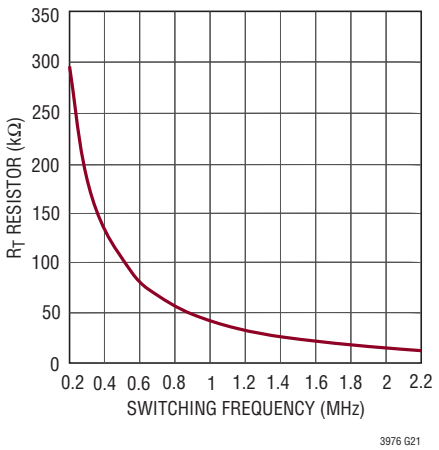

### Minimum Off-Time



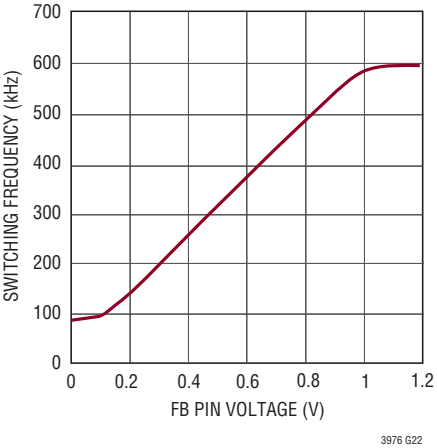

### Switching Frequency



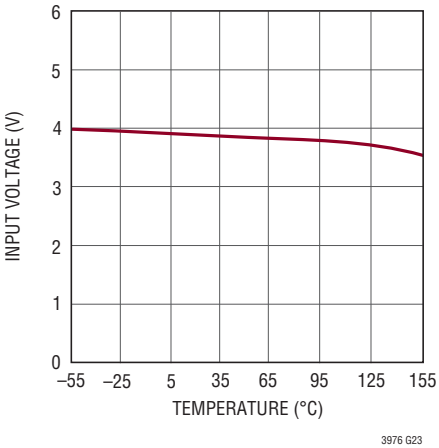

### $R_T$ Programmed Switching Frequency



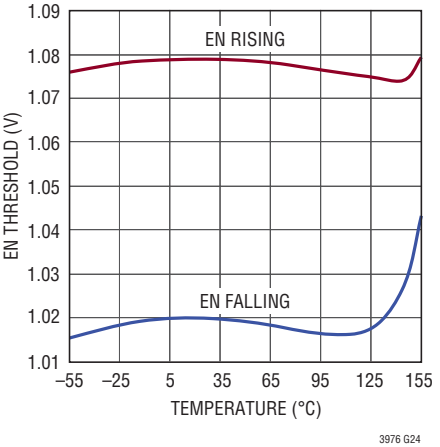

### Frequency Foldback




### Internal Undervoltage Lockout (UVLO)

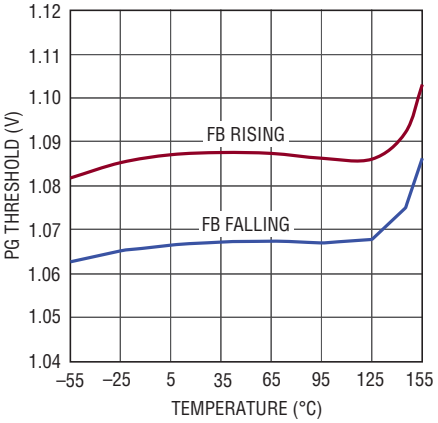



### EN Thresholds



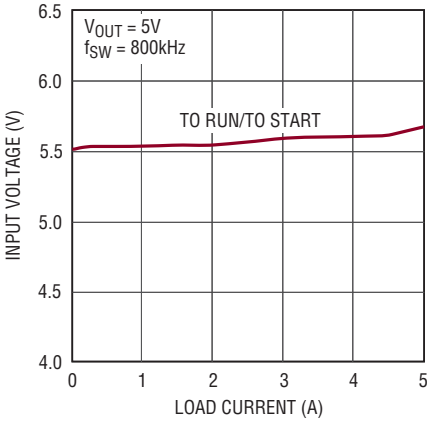
## TYPICAL PERFORMANCE CHARACTERISTICS $T_A$ = 25°C, unless otherwise noted.

### PG Thresholds



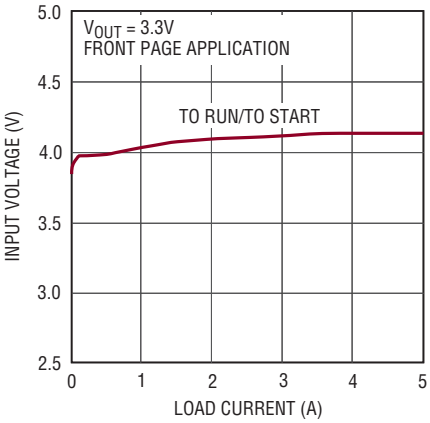

3976 G25

### Minimum Input Voltage, $V_{OUT}$ = 5V



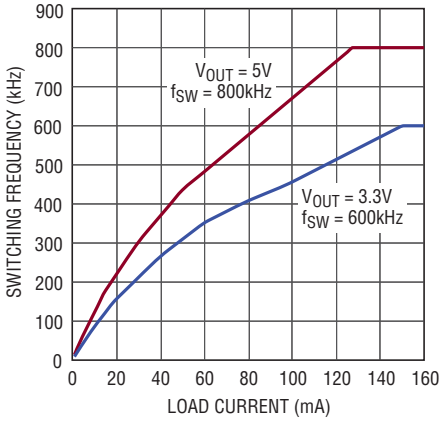

3976 G26

### Minimum Input Voltage, $V_{OUT}$ = 3.3V



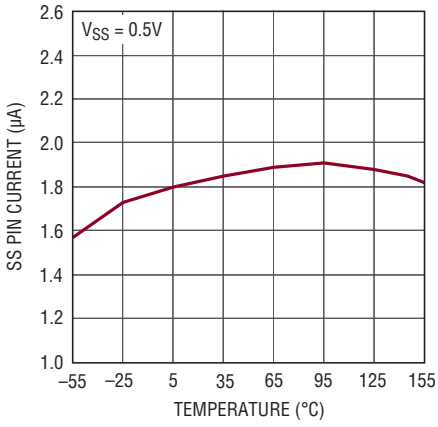

3976 G27

### Burst Frequency



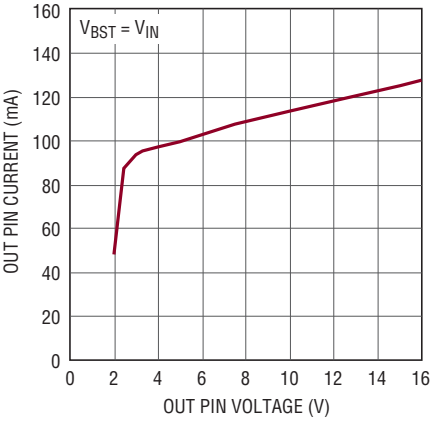

3976 G28

### SS Pin Current



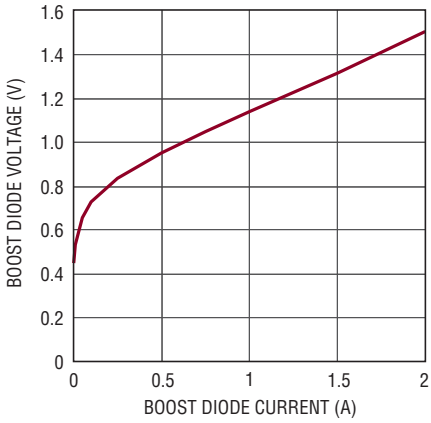

3976 G29

### Boost Capacitor Charger



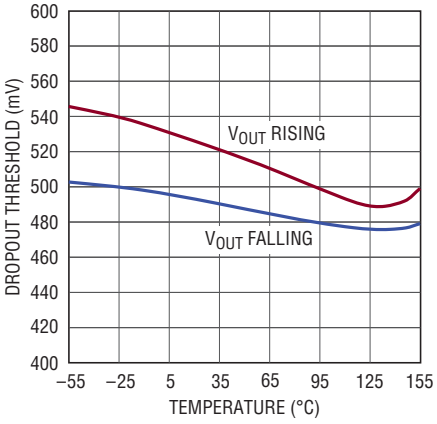

3976 G30

### Boost Diode Forward Voltage




3976 G31

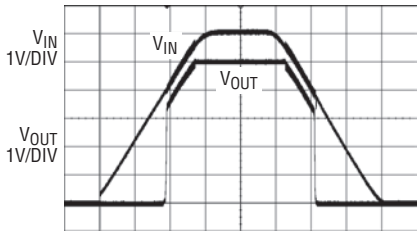
### Dropout Comparator Thresholds




3976 G32

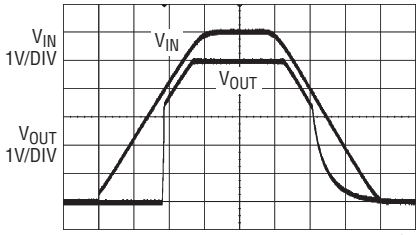
## TYPICAL PERFORMANCE CHARACTERISTICS $T_A$ = 25°C, unless otherwise noted.

### Start-Up/Dropout Performance



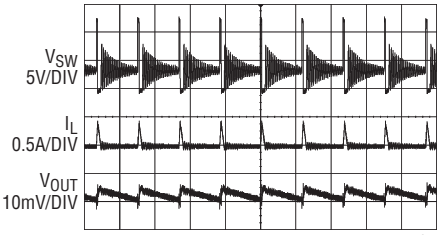

2.5Ω LOAD 100ms/DIV
(2A IN REGULATION)

### Start-Up/Dropout Performance



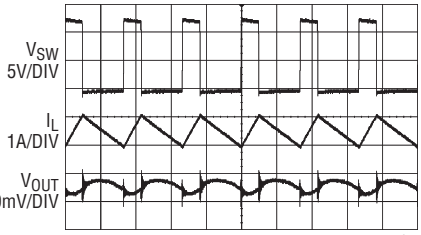

1kΩ LOAD 100ms/DIV
(5mA IN REGULATION)

### Burst Mode Switching Waveforms



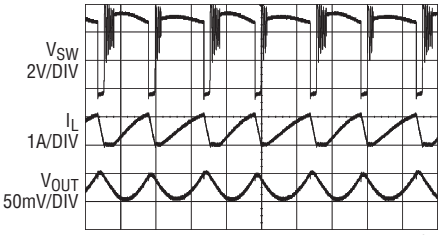

$V_{IN}$ = 12V 5µs/DIV
$V_{OUT}$ = 3.3V
$I_{LOAD}$ = 20mA
$C_{OUT}$ = 47µF

### Full Frequency Switching Waveforms



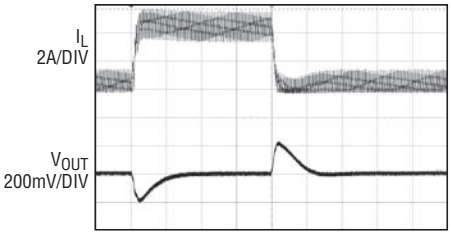

$V_{IN}$ = 12V 1µs/DIV
$V_{OUT}$ = 3.3V
$I_{LOAD}$ = 1A
$C_{OUT}$ = 47µF

### Dropout Switching Waveforms



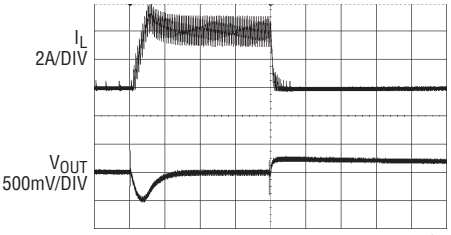

$V_{IN}$ = 5V 5µs/DIV
$V_{OUT}$ SET FOR 5V
$I_{LOAD}$ = 0.5A
$C_{OUT}$ = 47µF

### Load Transient: 0.5A to 4.5A




$12V_{IN}$ 50µs/DIV
$3.3V_{OUT}$
$C_{OUT}$ = 2 × 47µF

### Load Transient: 10mA to 4A




$12V_{IN}$ 50µs/DIV
$3.3V_{OUT}$
$C_{OUT}$ = 2 × 47µF

## PIN FUNCTIONS (MSE/UDD)

**FB (Pin 1/Pins 23, 24):** The LT3976 regulates the FB pin to 1.197V. Connect the feedback resistor divider tap to this pin. Also, connect a phase lead capacitor between FB and the output. Typically, this capacitor is 10pF.

**SS (Pin 2/Pin 1):** A capacitor is tied between SS and ground to slowly ramp up the peak current limit of the LT3976 on start-up. There is an internal 1.8µA pull-up on this pin. The soft-start capacitor is actively discharged when the EN pin goes low, during undervoltage lockout or thermal shutdown. Float this pin to disable soft-start.

**OUT (Pin 3/Pin 2):** This pin is an input to the dropout comparator which maintains a minimum dropout of 500mV between $V_{IN}$ and OUT. The OUT pin connects to the anode of the internal boost diode. This pin also supplies the current to the LT3976's internal regulator when OUT is above 3.2V. Connect this pin to the output when the programmed output voltage is less than 16V.

**BOOST (Pin 4/Pin 4):** This pin is used to provide a drive voltage, higher than the input voltage, to the internal bipolar NPN power switch.

**SW (Pins 5, 6, 7/Pins 6, 7, 8):** The SW pin is the output of an internal power switch. Connect these pins to the inductor, catch diode, and boost capacitor. An R-C snubber to GND is needed to ensure robustness under all conditions. Typical values are 2Ω and 470pF.

**NC (Pins 8, 9/Pins 3, 5, 9-12, 17, 22):** No Connects. These pins are not connected to internal circuitry.

**$V_{IN}$ (Pins 10, 11, 12/Pins 13, 14, 15):** The $V_{IN}$ pin supplies current to the LT3976's internal circuitry and to the internal power switch. These pins must be locally bypassed.

**EN (Pin 13/Pin 16):** The part is in shutdown when this pin is low and active when this pin is high. The hysteretic threshold voltage is 1.08V going up and 1.02V going down. The EN threshold is only accurate when $V_{IN}$ is above 4.3V. If $V_{IN}$ is lower than 3.9V, internal UVLO will place the part in shutdown. Tie to $V_{IN}$ if shutdown feature is not used.

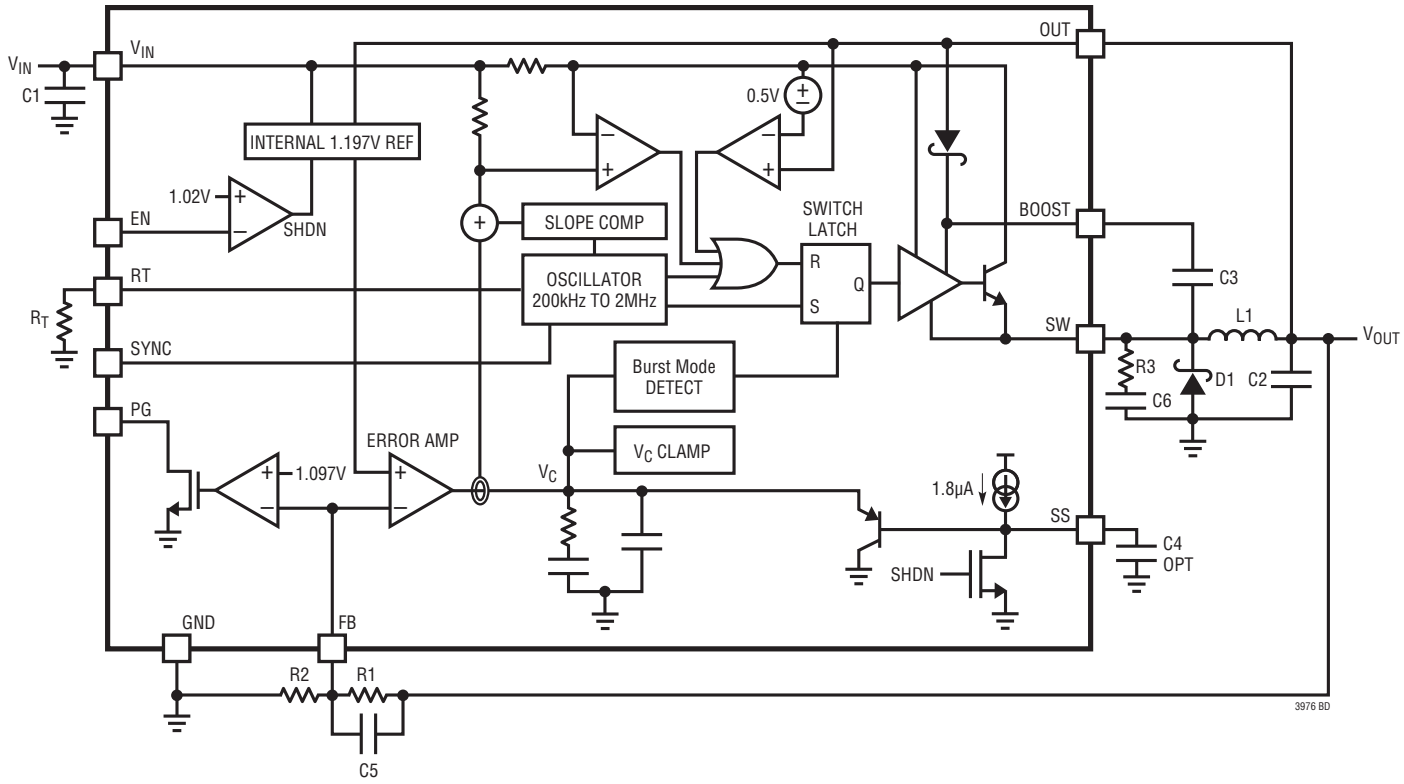
**RT (Pin 14/Pin 18):** A resistor is tied between RT and ground to set the switching frequency.

**PG (Pin 15/Pin 19):** The PG pin is the open-drain output of an internal comparator. PGOOD remains low until the FB pin is within 8.4% of the final regulation voltage. PGOOD is valid when $V_{IN}$ is above 2V.

**SYNC (Pin 16/Pin 20):** This is the external clock synchronization input. Ground this pin for low ripple Burst Mode operation at low output loads. Tie to a clock source for synchronization, which will include pulse skipping at low output loads. When in pulse-skipping mode, quiescent current increases to 11µA in a typical application at no load. Do not float this pin.

**GND (Exposed Pad Pin 17/Pin 21, Exposed Pad Pin 25):** Ground. The exposed pad must be soldered to the PCB.

## BLOCK DIAGRAM



## OPERATION

The LT3976 is a constant frequency, current mode step-down regulator. An oscillator, with frequency set by RT, sets an RS flip-flop, turning on the internal power switch. An amplifier and comparator monitor the current flowing between the $V_{IN}$ and SW pins, turning the switch off when this current reaches a level determined by the voltage at $V_C$ (see Block Diagram). An error amplifier measures the output voltage through an external resistor divider tied to the FB pin and servos the $V_C$ node. If the error amplifier's output increases, more current is delivered to the output; if it decreases, less current is delivered. An active clamp on the $V_C$ pin provides current limit. The $V_C$ pin is also clamped by the voltage on the SS pin; soft-start is implemented by generating a voltage ramp at the SS pin using an external capacitor.

An internal regulator provides power to the control circuitry. The bias regulator normally draws power from the $V_{IN}$ pin, but if the OUT pin is connected to an external voltage higher than 3.2V, bias power will be drawn from the external source (typically the regulated output voltage). This improves efficiency.

If the EN pin is low, the LT3976 is shut down and draws 700nA from the input. When the EN pin falls below 1.02V, the switching regulator will shut down, and when the EN pin rises above 1.08V, the switching regulator will become active. This accurate threshold allows programmable undervoltage lockout.

The switch driver operates from either $V_{IN}$ or from the BOOST pin. An external capacitor is used to generate a voltage at the BOOST pin that is higher than the input supply. This allows the driver to fully saturate the internal bipolar NPN power switch for efficient operation.

To further optimize efficiency, the LT3976 automatically switches to Burst Mode operation in light load situations. Between bursts, all circuitry associated with controlling the output switch is shut down reducing the input supply current to 1.7µA. In a typical application, 3.3µA will be consumed from the supply when regulating with no load.

The oscillator reduces the LT3976's operating frequency when the voltage at the FB pin is low. This frequency foldback helps to control the output current during start-up and overload.

The LT3976 can provide up to 5A of output current. A current limit foldback feature throttles back the current limit during overload conditions to limit the power dissipation. When SS is below 2V, the LT3976 overrides the current limit foldback circuit to avoid interfering with start-up. Thermal shutdown further protects the part from excessive power dissipation, especially in elevated ambient temperature environments.

If the input voltage decreases towards the programmed output voltage, the LT3976 will start to skip switch-off times and decrease the switching frequency to maintain output regulation. As the input voltage decreases below the programmed output voltage, the output voltage will be regulated 500mV below the input voltage. This enforced minimum dropout voltage limits the duty cycle and keeps the boost capacitor charged during dropout conditions. Since sufficient boost voltage is maintained, the internal switch can fully saturate yielding low dropout performance.

The LT3976 contains a power good comparator which trips when the FB pin is at 91.6% of its regulated value. The PG output is an open-drain transistor that is off when the output is in regulation, allowing an external resistor to pull the PG pin high. Power good is valid when $V_{IN}$ is above 2V. When the LT3976 is shut down the PG pin is actively pulled low.

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### Achieving Ultralow Quiescent Current

To enhance efficiency at light loads, the LT3976 operates in low ripple Burst Mode operation, which keeps the output capacitor charged to the desired output voltage while minimizing the input quiescent current. In Burst Mode operation the LT3976 delivers single pulses of current to the output capacitor followed by sleep periods where the output power is supplied by the output capacitor. When in sleep mode the LT3976 consumes 1.7µA, but when it turns on all the circuitry to deliver a current pulse, the LT3976 consumes several mA of input current in addition to the switch current. Therefore, the total quiescent current will be greater than 1.7µA when regulating.

As the output load decreases, the frequency of single current pulses decreases (see Figure 1) and the percentage of time the LT3976 is in sleep mode increases, resulting in much higher light load efficiency. By maximizing the time between pulses, the converter quiescent current gets closer to the 1.7µA ideal. Therefore, to optimize the quiescent current performance at light loads, the current in the feedback resistor divider and the reverse current in the catch diode must be minimized, as these appear to the output as load currents. Use the largest possible feedback resistors and a low leakage Schottky catch diode in applications utilizing the ultralow quiescent current performance of the LT3976. The feedback resistors should preferably be on the order of MΩ and the Schottky catch diode should have less than a few µA of typical reverse leakage at room temperature. These two considerations are reiterated in the FB Resistor Network and Catch Diode Selection sections.

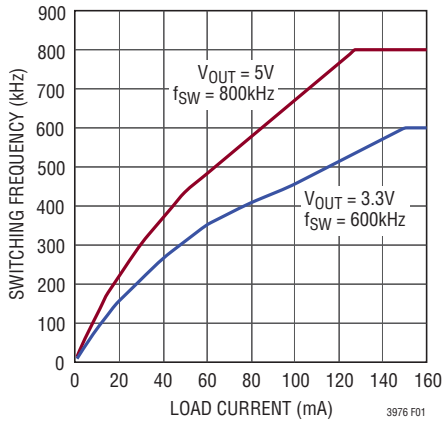


**Figure 1. Switching Frequency in Burst Mode Operation**

It is important to note that another way to decrease the pulse frequency is to increase the magnitude of each single current pulse. However, this increases the output voltage ripple because each cycle delivers more power to the output capacitor. The magnitude of the current pulses was selected to ensure less than 15mV of output ripple in a typical application. See Figure 2.

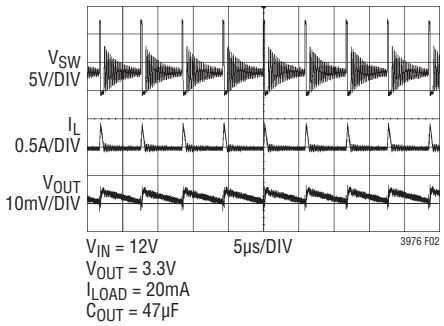


**Figure 2. Burst Mode Operation**

While in Burst Mode operation, the burst frequency and the charge delivered with each pulse will not change with output capacitance. Therefore, the output voltage ripple will be inversely proportional to the output capacitance. In a typical application with a 22µF output capacitor, the output ripple is about 10mV, and with a 47µF output capacitor the output ripple is about 5mV. The output voltage ripple can continue to be decreased by increasing the output capacitance, though care must be taken to minimize the effects of output capacitor ESR and ESL.

At higher output loads (above 150mA for the front page application) the LT3976 will be running at the frequency programmed by the $R_T$ resistor, and will be operating in standard PWM mode. The transition between PWM and low ripple Burst Mode operation is seamless, and will not disturb the output voltage.

To ensure proper Burst Mode operation, the SYNC pin must be grounded. When synchronized with an external clock, the LT3976 will pulse skip at light loads. At very

## APPLICATIONS INFORMATION

light loads, the part will go to sleep between groups of pulses, so the quiescent current of the part will still be low, but not as low as in Burst Mode operation. The quiescent current in a typical application when synchronized with an external clock is 11µA at no load. Holding the SYNC pin DC high yields no advantages in terms of output ripple or minimum load to full frequency, so is not recommended.

### FB Resistor Network

The output voltage is programmed with a resistor divider between the output and the FB pin. Choose the resistor values according to:

$$R1 = R2\left(\frac{V_{OUT}}{1.197V} - 1\right)$$

Reference designators refer to the Block Diagram. 1% resistors are recommended to maintain output voltage accuracy.

The total resistance of the FB resistor divider should be selected to be as large as possible to enhance low current performance. The resistor divider generates a small load on the output, which should be minimized to optimize the low supply current at light loads.

When using large FB resistors, a 10pF phase lead capacitor should be connected from $V_{OUT}$ to FB.

### Setting the Switching Frequency

The LT3976 uses a constant frequency PWM architecture that can be programmed to switch from 200kHz to 2MHz by using a resistor tied from the RT pin to ground. A table showing the necessary $R_T$ value for a desired switching frequency is in Table 1.

To estimate the necessary $R_T$ value for a desired switching frequency, use the equation:

$$R_T = \frac{51.1}{\left(f_{SW}\right)^{1.09}} - 9.27$$

where $R_T$ is in kΩ and $f_{SW}$ is in MHz.

**Table 1. Switching Frequency vs $R_T$ Value**

| SWITCHING FREQUENCY (MHz) | $R_T$ VALUE (kΩ) |
|---|---|
| 0.2 | 294 |
| 0.3 | 182 |
| 0.4 | 130 |
| 0.6 | 78.7 |
| 0.8 | 54.9 |
| 1.0 | 41.2 |
| 1.2 | 32.4 |
| 1.4 | 26.1 |
| 1.6 | 21.5 |
| 1.8 | 17.8 |
| 2.0 | 14.7 |
| 2.2 | 12.4 |

### Operating Frequency Trade-Offs

Selection of the operating frequency is a trade-off between efficiency, component size, minimum dropout voltage, and maximum input voltage. The advantage of high frequency operation is that smaller inductor and capacitor values may be used. The disadvantages are lower efficiency, and lower maximum input voltage. The highest acceptable switching frequency ($f_{SW(MAX)}$) for a given application can be calculated as follows:

$$f_{SW(MAX)} = \frac{V_{OUT} + V_D}{t_{ON(MIN)}\left(V_{IN} - V_{SW} + V_D\right)}$$

where $V_{IN}$ is the typical input voltage, $V_{OUT}$ is the output voltage, $V_D$ is the catch diode drop (~0.5V), and $V_{SW}$ is the internal switch drop (~0.3V at max load). This equation shows that slower switching frequency is necessary to safely accommodate high $V_{IN}/V_{OUT}$ ratio. This is due to the limitation on the LT3976's minimum on-time. The minimum on-time is a strong function of temperature. Use the typical minimum on-time curve to design for an application's maximum temperature, while adding about 30% for part-to-part variation. The minimum duty cycle that can be achieved taking minimum on time into account is:

$$DC_{MIN} = f_{SW} \bullet t_{ON(MIN)}$$

where $f_{SW}$ is the switching frequency, the $t_{ON(MIN)}$ is the minimum switch on-time.

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A good choice of switching frequency should allow adequate input voltage range (see next two sections) and keep the inductor and capacitor values small.

### Maximum Input Voltage Range

The LT3976 can operate from input voltages of up to 40V. Often the highest allowed $V_{IN}$ during normal operation ($V_{IN(OP-MAX)}$) is limited by the minimum duty cycle rather than the absolute maximum ratings of the $V_{IN}$ pin. It can be calculated using the following equation:

$$V_{IN(OP-MAX)} = \frac{V_{OUT} + V_D}{f_{SW} \bullet t_{ON(MIN)}} - V_D + V_{SW}$$

where $t_{ON(MIN)}$ is the minimum switch on-time. A lower switching frequency can be used to extend normal operation to higher input voltages.

The circuit will tolerate inputs above the maximum operating input voltage and up to the absolute maximum ratings of the $V_{IN}$ and BOOST pins, regardless of chosen switching frequency. However, during such transients where $V_{IN}$ is higher than $V_{IN(OP-MAX)}$, the LT3976 will enter pulse-skipping operation where some switching pulses are skipped to maintain output regulation. The output voltage ripple and inductor current ripple will be higher than in typical operation. Do not overload when $V_{IN}$ is greater than $V_{IN(OP-MAX)}$.

During start-up or overload, the switch node slews very fast due to the 10A peak current limit. At high voltages during these conditions, an R-C snubber on the switch node is required to ensure robustness of the LT3976. Typical values for the snubber are 2Ω and 470pF. See the Typical Applications section to see how the snubber is connected.

### Minimum Input Voltage Range

The minimum input voltage is determined by either the LT3976's minimum operating voltage of 4.3V, its maximum duty cycle, or the enforced minimum dropout voltage. See the Typical Performance Characteristics section for the minimum input voltage across load for outputs of 3.3V and 5V.

The duty cycle is the fraction of time that the internal switch is on during a clock cycle. Unlike many fixed frequency regulators, the LT3976 can extend its duty cycle by remaining on for multiple clock cycles. The LT3976 will not switch off at the end of each clock cycle if there is sufficient voltage across the boost capacitor (C3 in the Block Diagram). Eventually, the voltage on the boost capacitor falls and requires refreshing. When this occurs, the switch will turn off, allowing the inductor current to recharge the boost capacitor. This places a limitation on the maximum duty cycle as follows:

$$DC_{MAX} = \frac{\beta_{SW}}{\beta_{SW} + 1}$$

where $\beta_{SW}$ is equal to the beta of the internal power switch. The beta of the power switch is typically about 50, which leads to a $DC_{MAX}$ of about 98%. This leads to a minimum input voltage of approximately:

$$V_{IN(MIN1)} = \frac{V_{OUT} + V_D}{DC_{MAX}} - V_D + V_{SW}$$

where $V_{OUT}$ is the output voltage, $V_D$ is the catch diode drop, $V_{SW}$ is the internal switch drop and $DC_{MAX}$ is the maximum duty cycle.

The final factor affecting the minimum input voltage is the minimum dropout voltage. When the OUT pin is tied to the output, the LT3976 regulates the output such that it stays 500mV below $V_{IN}$. This enforced minimum dropout voltage is due to reasons that are covered in the next section. This places a limitation on the minimum input voltage as follows:

$$V_{IN(MIN2)} = V_{OUT} + V_{DROPOUT(MIN)}$$

where $V_{OUT}$ is the programmed output voltage and $V_{DROPOUT(MIN)}$ is the minimum dropout voltage of 500mV.

Combining these factors leads to the overall minimum input voltage:

$$V_{IN(MIN)} = \text{Max}\ (V_{IN(MIN1)}, V_{IN(MIN2)}, 4.3V)$$

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### Minimum Dropout Voltage

To achieve a low dropout voltage, the internal power switch must always be able to fully saturate. This means that the boost capacitor, which provides a base drive higher than $V_{IN}$, must always be able to charge up when the part starts up and then must also stay charged during all operating conditions.

During start-up if there is insufficient inductor current, such as during light load situations, the boost capacitor will be unable to charge. When the LT3976 detects that the boost capacitor is not charged, it activates a 100mA (typical) pull-down on the OUT pin. If the OUT pin is connected to the output, the extra load will increase the inductor current enough to sufficiently charge the boost capacitor. When the boost capacitor is charged, the current source turns off, and the part may re-enter Burst Mode operation.

To keep the boost capacitor charged regardless of load during dropout conditions, a minimum dropout voltage is enforced. When the OUT pin is tied to the output, the LT3976 regulates the output such that:

$$V_{IN} - V_{OUT} > V_{DROPOUT(MIN)}$$

where $V_{DROPOUT(MIN)}$ is 500mV. The 500mV dropout voltage limits the duty cycle and forces the switch to turn off regularly to charge the boost capacitor. Since sufficient voltage across the boost capacitor is maintained, the switch is allowed to fully saturate and the internal switch drop stays low for good dropout performance. Figure 3 shows the overall $V_{IN}$ to $V_{OUT}$ performances during start-up and dropout conditions.

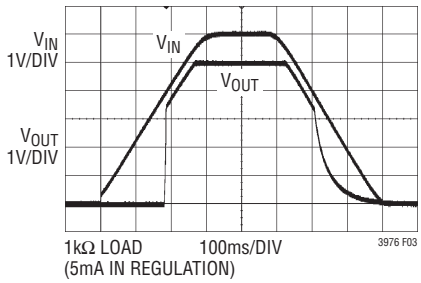


**Figure 3. $V_{IN}$ to $V_{OUT}$ Performance**

It is important to note that the 500mV dropout voltage specified is the minimum difference between $V_{IN}$ and $V_{OUT}$. When measuring $V_{IN}$ to $V_{OUT}$ with a multimeter, the measured value will be higher than 500mV because you have to add half the ripple voltage on the input and half the ripple voltage on the output. With the normal ceramic capacitors specified in the data sheet, this measured dropout voltage can be as high as 650mV at high load. If some bulk electrolytic capacitance is added to the input and output the voltage ripple, and subsequently the measured dropout voltage, can be significantly reduced. Additionally, when operating in dropout at high currents, high ripple voltage on the input and output can generate audible noise. This noise can also be significantly reduced by adding bulk capacitance to the input and output to reduce the voltage ripple.

### Inductor Selection and Maximum Output Current

For a given input and output voltage, the inductor value and switching frequency will determine the ripple current. The ripple current increases with higher $V_{IN}$ or $V_{OUT}$ and decreases with higher inductance and faster switching frequency. A good first choice for the inductor value is:

$$L = \frac{V_{OUT} + V_D}{2f_{SW}}$$

where $f_{SW}$ is the switching frequency in MHz, $V_{OUT}$ is the output voltage, $V_D$ is the catch diode drop (~0.5V) and L is the inductor value is µH.

The inductor's RMS current rating must be greater than the maximum load current and its saturation current should be about 30% higher. For robust operation in fault conditions (start-up or overload) and high input voltage (>30V), the saturation current should be above 13A. To keep the efficiency high, the series resistance (DCR) should be less than 0.1Ω, and the core material should be intended for high frequency applications. Table 2 lists several inductor vendors.

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**Table 2. Inductor Vendors**

| VENDOR | URL |
|---|---|
| Coilcraft | www.coilcraft.com |
| Sumida | www.sumida.com |
| Toko | www.tokoam.com |
| Würth Elektronik | www.we-online.com |
| Coiltronics | www.cooperet.com |
| Murata | www.murata.com |

The inductor value must be sufficient to supply the desired maximum output current ($I_{OUT(MAX)}$), which is a function of the switch current limit ($I_{LIM}$) and the ripple current.

$$I_{OUT(MAX)} = I_{LIM} - \frac{\Delta I_L}{2}$$

The LT3976 limits its peak switch current in order to protect itself and the system from overload and short-circuit faults. The LT3976's switch current limit ($I_{LIM}$) is typically 10A at low duty cycles and decreases linearly to 8A at DC = 0.8.

When the switch is off, the potential across the inductor is the output voltage plus the catch diode drop. This gives the peak-to-peak ripple current in the inductor:

$$\Delta I_L = \frac{(1-DC) \bullet (V_{OUT} + V_D)}{L \bullet f_{SW}}$$

where $f_{SW}$ is the switching frequency of the LT3976, DC is the duty cycle and L is the value of the inductor. Therefore, the maximum output current that the LT3976 will deliver depends on the switch current limit, the inductor value, and the input and output voltages. The inductor value may have to be increased if the inductor ripple current does not allow sufficient maximum output current ($I_{OUT(MAX)}$) given the switching frequency, and maximum input voltage used in the desired application.

The optimum inductor for a given application may differ from the one indicated by this simple design guide. A larger value inductor provides a higher maximum load current and reduces the output voltage ripple. If your load is lower than the maximum load current, than you can relax the value of the inductor and operate with higher ripple current. This allows you to use a physically smaller inductor, or one with a lower DCR resulting in higher efficiency. Be aware that if the inductance differs from the simple rule above, then the maximum load current will depend on the input voltage. In addition, low inductance may result in discontinuous mode operation, which further reduces maximum load current. For details of maximum output current and discontinuous operation, see Linear Technology's Application Note 44. Finally, for duty cycles greater than 50% ($V_{OUT}/V_{IN} > 0.5$), a minimum inductance is required to avoid sub-harmonic oscillations, see Application Note 19.

One approach to choosing the inductor is to start with the simple rule given above, look at the available inductors, and choose one to meet cost or space goals. Then use the equations above to check that the LT3976 will be able to deliver the required output current. Note again that these equations assume that the inductor current is continuous. Discontinuous operation occurs when $I_{OUT}$ is less than $\Delta I_L/2$.

### Current Limit Foldback and Thermal Protection

The LT3976 has a large peak current limit to ensure a 5A max output current across duty cycle and current limit distribution, as well as allowing a reasonable inductor ripple current. During a short-circuit fault, having a large current limit can lead to excessive power dissipation and temperature rise in the LT3976, as well as the inductor and catch diode. To limit this power dissipation, the LT3976 starts to fold back the current limit when the FB pin falls below 0.8V. The LT3976 typically lowers the peak current limit about 50% from 10A to 5A.

During start-up, when the output voltage and FB pin are low, current limit foldback could hinder the LT3976's ability to start up into a large load. To avoid this potential problem, the LT3976's current limit foldback will be disabled until the SS pin has charged above 2V. Therefore, the use of a soft-start capacitor will keep the current limit foldback feature out of the way while the LT3976 is starting up.

The LT3976 has thermal shutdown to further protect the part during periods of high power dissipation, particularly in high ambient temperature environments. The thermal shutdown feature detects when the LT3976 is too hot and shuts the part down, preventing switching. When the thermal event passes and the LT3976 cools, the part will restart and resume switching. A thermal shutdown event actively discharges the soft-start capacitor.

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### Input Capacitor

Bypass the input of the LT3976 circuit with a ceramic capacitor of X7R or X5R type. Y5V types have poor performance over temperature and applied voltage, and should not be used. A 4.7µF to 10µF ceramic capacitor is adequate to bypass the LT3976 and will easily handle the ripple current. Note that larger input capacitance is required when a lower switching frequency is used (due to longer on times). If the input power source has high impedance, or there is significant inductance due to long wires or cables, additional bulk capacitance may be necessary. This can be provided with a low performance electrolytic capacitor.

Step-down regulators draw current from the input supply in pulses with very fast rise and fall times. The input capacitor is required to reduce the resulting voltage ripple at the LT3976 and to force this very high frequency switching current into a tight local loop, minimizing EMI. A 10µF capacitor is capable of this task, but only if it is placed close to the LT3976 (see the PCB Layout section). A second precaution regarding the ceramic input capacitor concerns the maximum input voltage rating of the LT3976. A ceramic input capacitor combined with trace or cable inductance forms a high quality (under damped) tank circuit. If the LT3976 circuit is plugged into a live supply, the input voltage can ring to twice its nominal value, possibly exceeding the LT3976's voltage rating. If the input supply is poorly controlled or the user will be plugging the LT3976 into an energized supply, the input network should be designed to prevent this overshoot. See Linear Technology Application Note 88 for a complete discussion.

### Output Capacitor and Output Ripple

The output capacitor has two essential functions. Along with the inductor, it filters the square wave generated by the LT3976 to produce the DC output. In this role it determines the output ripple, so low impedance (at the switching frequency) is important. The second function is to store energy in order to satisfy transient loads and stabilize the LT3976's control loop. Ceramic capacitors have very low equivalent series resistance (ESR) and provide the best ripple performance. A good starting value is:

$$C_{OUT} = \frac{300}{V_{OUT} \bullet f_{SW}}$$

where $f_{SW}$ is in MHz, and $C_{OUT}$ is the recommended output capacitance in µF. Use X5R or X7R types. This choice will provide low output ripple and good transient response. Transient performance can be improved with a higher value capacitor if combined with a phase lead capacitor (typically 10pF) between the output and the feedback pin. A lower value of output capacitor can be used to save space and cost but transient performance will suffer.

When choosing a capacitor, look carefully through the data sheet to find out what the actual capacitance is under operating conditions (applied voltage and temperature). A physically larger capacitor or one with a higher voltage rating may be required. Table 3 lists several capacitor vendors.

**Table 3. Recommended Ceramic Capacitor Vendors**

| MANUFACTURER | URL |
|---|---|
| AVX | www.avxcorp.com |
| Murata | www.murata.com |
| Taiyo Yuden | www.t-yuden.com |
| Vishay Siliconix | www.vishay.com |
| TDK | www.tdk.com |

### Ceramic Capacitors

When in dropout, the LT3976 can excite ceramic capacitors at audio frequencies. At high load, this could be unacceptable. Simply adding bulk input capacitance to the input and output will significantly reduce the voltage ripple and the audible noise generated at these nodes to acceptable levels.

A final precaution regarding ceramic capacitors concerns the maximum input voltage rating of the LT3976. As previously mentioned, a ceramic input capacitor combined with trace or cable inductance forms a high quality (under damped) tank circuit. If the LT3976 circuit is plugged into a live supply, the input voltage can ring to twice its nominal value, possibly exceeding the LT3976's rating. If the input supply is poorly controlled or the user will be plugging the LT3976 into an energized supply, the input network should be designed to prevent this overshoot. See Linear Technology Application Note 88 for a complete discussion.

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### Catch Diode Selection

The catch diode (D1 from the Block Diagram) conducts current only during the switch off time. Average forward current in normal operation can be calculated from:

$$I_{D(AVG)} = I_{OUT}\left(\frac{V_{IN} - V_{OUT}}{V_{IN}}\right)$$

where $I_{OUT}$ is the output load current. The current rating of the diode should be selected to be greater than or equal to the application's output load current, so that the diode is robust for a wide input voltage range. A diode with even higher current rating can be selected for the worst-case scenario of overload, where the max diode current can then increase to the typical peak switch current. Short circuit is not the worst-case condition due to current limit foldback. Peak reverse voltage is equal to the regulator input voltage. For inputs up to 40V, a 40V diode is adequate.

An additional consideration is reverse leakage current. When the catch diode is reversed biased, any leakage current will appear as load current. When operating under light load conditions, the low supply current consumed by the LT3976 will be optimized by using a catch diode with minimum reverse leakage current. Low leakage Schottky diodes often have larger forward voltage drops at a given current, so a trade-off can exist between low load and high load efficiency. Often Schottky diodes with larger reverse bias ratings will have less leakage at a given output voltage than a diode with a smaller reverse bias rating. Therefore, superior leakage performance can be achieved at the expense of diode size. Table 4 lists several Schottky diodes and their manufacturers.

**Table 4. Schottky Diodes. The Reverse Current Values Listed Are Estimates Based Off of Typical Curves for Reverse Current vs Reverse Voltage at 25°C**

| PART NUMBER | $V_R$ (V) | $I_{AVE}$ (A) | $V_F$ at 5A TYP 25°C (mV) | $V_F$ at 5A MAX 25°C (mV) | $I_R$ at $V_R$ = 20V 25°C (µA) |
|---|---|---|---|---|---|
| **On Semiconductor** | | | | | |
| MBRS540T3 | 40 | 5 | 450 | 500 | 120 |
| **Diodes Inc.** | | | | | |
| B540C | 40 | 5 | 510 | 550 | 2 |
| PDS540 | 40 | 5 | 480 | 520 | 4 |
| PDS560 | 60 | 5 | 610 | 670 | 0.9 |
| SBR8A45SP5 | 45 | 8 | 450 | — | 18 |
| SBR8AU60P5 | 60 | 8 | 400 | — | 60 |

### BOOST and OUT Pin Considerations

Capacitor C3 and the internal boost Schottky diode (see the Block Diagram) are used to generate a boost voltage that is higher than the input voltage. In most cases a 0.47µF capacitor will work well. The BOOST pin must be more than 1.8V above the SW pin for best efficiency and more than 2.6V above the SW pin to allow the LT3976 to skip off times to achieve very high duty cycles. For outputs between 3.2V and 16V, the standard circuit with the OUT pin connected to the output (Figure 4a) is best. Below 3.2V the internal Schottky diode may not be able to sufficiently charge the boost capacitor. Above 16V, the OUT pin abs max is violated. For outputs between 2.5V and 3.2V, an external Schottky diode to the output is sufficient because an external Schottky will have much lower forward voltage drop than the internal boost diode.

For output voltages less than 2.5V, there are two options. An external Schottky diode can charge the boost capacitor from the input (Figure 4c) or from an external voltage source (Figure 4d). Using an external voltage source is the better option because it is more efficient than charging the boost capacitor from the input. However, such a voltage rail is not always available in all systems. For output voltages greater than 16V, an external Schottky diode from an external voltage source should be used to charge the boost capacitor (Figure 4e). In applications using an external voltage source, the supply should be between 3.1V and 16V. When using the input, the input voltage may not exceed 27V. In all cases, the maximum voltage rating of the BOOST pin must not be exceeded.

When the output is above 16V, the OUT pin can not be tied to the output or the OUT pin abs max will be violated. It should instead be tied to GND (Figure 4e). This is to prevent the dropout circuitry from interfering with switching behavior and to prevent the 100mA active pull-down from drawing power. It is important to note that when the output is above 16V and the OUT pin is grounded, the dropout circuitry is not connected, so the minimum dropout will be about 1.5V, rather than 500mV. If the output is less than 3.2V and an external Schottky is used

## APPLICATIONS INFORMATION

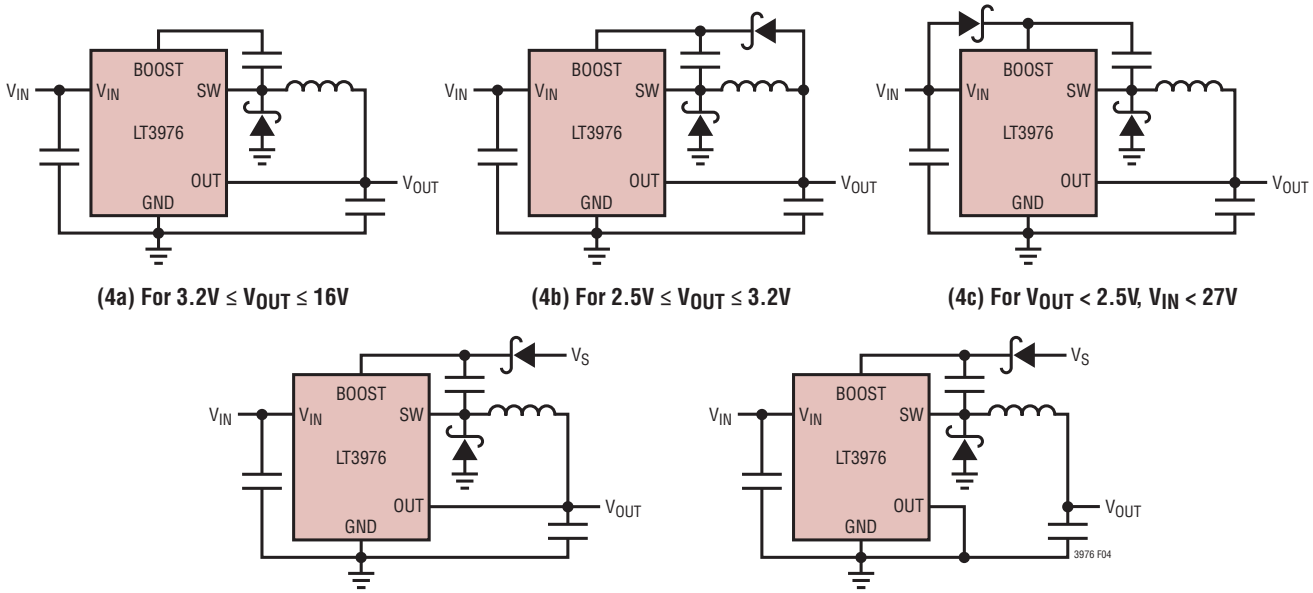
to charge the boost capacitor, the OUT pin should still be tied to the output even though the minimum input voltage of the LT3976 will be limited by the 4.3V minimum rather than the minimum dropout voltage.

With the OUT pin connected to the output, a 100mA active load will charge the boost capacitor during light load start-up and an enforced 500mV minimum dropout voltage will keep the boost capacitor charged across operating conditions (see Minimum Dropout Voltage section). This yields excellent start-up and dropout performance. Figure 5 shows the minimum input voltage for 3.3V and 5V outputs.

### Enable and Undervoltage Lockout

The LT3976 is in shutdown when the EN pin is low and active when the pin is high. The falling threshold of the EN comparator is 1.02V, with 60mV of hysteresis. The EN pin can be tied to $V_{IN}$ if the shutdown feature is not used.

Undervoltage lockout (UVLO) can be added to the LT3976 as shown in Figure 6. Typically, UVLO is used in situations where the input supply is current limited, or has a relatively high source resistance. A switching regulator draws constant power from the source, so source current increases as source voltage drops. This looks like a




(4a) For 3.2V ≤ $V_{OUT}$ ≤ 16V

(4b) For 2.5V ≤ $V_{OUT}$ ≤ 3.2V

(4c) For $V_{OUT}$ < 2.5V, $V_{IN}$ < 27V

(4d) For $V_{OUT}$ < 2.5V, 3.1V ≤ $V_S$ ≤ 16V

(4e) For $V_{OUT}$ > 16V, 3.1V ≤ $V_S$ ≤ 16V

**Figure 4. Five Circuits for Generating the Boost Voltage**

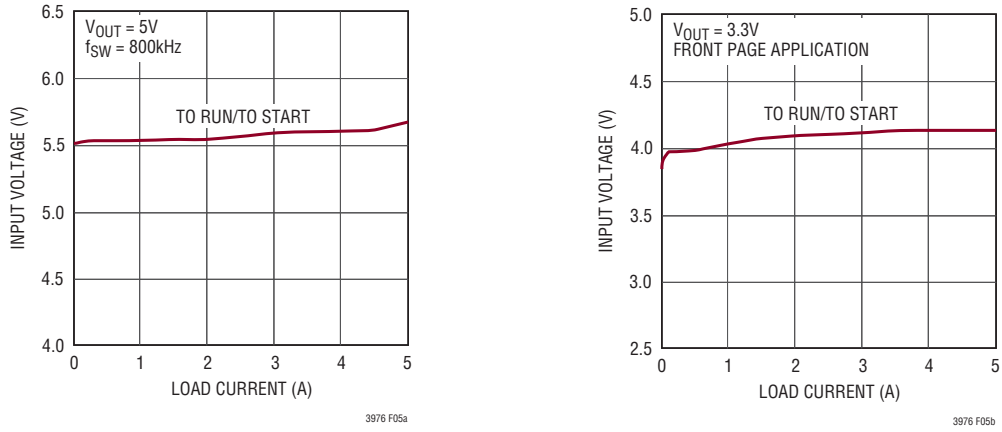



**Figure 5. The Minimum Input Voltage Depends on Output Voltage and Load Current**

## APPLICATIONS INFORMATION

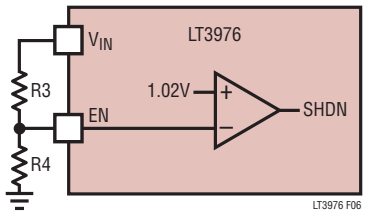



**Figure 6. Undervoltage Lockout**

negative resistance load to the source and can cause the source to current limit or latch low under low source voltage conditions. UVLO prevents the regulator from operating at source voltages where the problems might occur. The UVLO threshold can be adjusted by setting the values R3 and R4 such that they satisfy the following equation:

$$V_{UVLO} = V_{EN(THRESH)}\left(\frac{R3+R4}{R4}\right)$$

where $V_{EN(THRESH)}$ is the falling threshold of the EN pin, which is approximately 1.02V, and where switching should stop when $V_{IN}$ falls below $V_{UVLO}$. Note that due to the comparator's hysteresis, switching will not start until the input is about 6% above $V_{UVLO}$.

When operating in Burst Mode operation for light load currents, the current through the UVLO resistor network can easily be greater than the supply current consumed by the LT3976. Therefore, the UVLO resistors should be large to minimize their effect on efficiency at low loads.

### Soft-Start

The SS pin can be used to soft start the LT3976 by throttling the maximum input current during start-up and reset. An internal 1.8µA current source charges an external capacitor generating a voltage ramp on the SS pin. The SS pin clamps the internal $V_C$ node, which slowly ramps up the current limit. Maximum current limit is reached when the SS pin is about 1.5V or higher. By selecting a large enough capacitor, the output can reach regulation without overshoot. Figure 7 shows start-up waveforms for a typical application with a 10nF capacitor on SS for a 1.65Ω load when the EN pin is pulsed high for 7ms.

The external SS capacitor is actively discharged when the EN pin is low, or during thermal shutdown. The active pull-down on the SS pin has a resistance of about 150Ω.

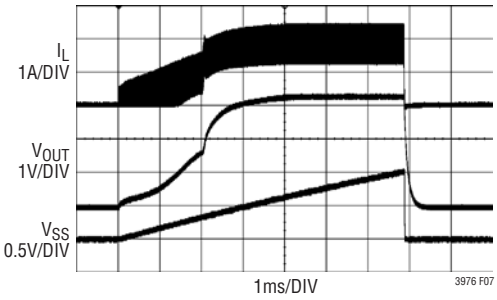



**Figure 7. Soft-Start Waveforms for the Front-Page Application with a 10nF Capacitor on SS. EN Is Pulsed High for About 7ms with a 1.65Ω Load Resistor**

### Synchronization

To select low ripple Burst Mode operation, tie the SYNC pin below 0.5V (this can be ground or a logic output).

Synchronizing the LT3976 oscillator to an external frequency can be done by connecting a square wave (with 20% to 80% duty cycle) to the SYNC pin. The square wave amplitude should have valleys that are below 0.5V and peaks above 1.5V (up to 6V).

The LT3976 will pulse skip at low output loads while synchronized to an external clock to maintain regulation. At very light loads, the part will go to sleep between groups of pulses, so the quiescent current of the part will still be low, but not as low as in Burst Mode operation. The quiescent current in a typical application when synchronized with an external clock is 11µA at no load. Holding the SYNC pin DC high yields no advantages in terms of output ripple or minimum load to full frequency, so is not recommended. Never float the SYNC pin.

The LT3976 may be synchronized over a 250kHz to 2MHz range. The $R_T$ resistor should be chosen to set the LT3976 switching frequency 20% below the lowest synchronization input. For example, if the synchronization signal will be 250kHz and higher, the $R_T$ should be selected for 200kHz. To assure reliable and safe operation the LT3976 will only synchronize when the output voltage is near regulation as indicated by the PG flag. It is therefore necessary to choose a large enough inductor value to supply the required output current at the frequency set by the $R_T$ resistor (see Inductor Selection section). The slope compensation is set by the $R_T$ value, while the minimum slope compensation required to avoid subharmonic oscillations is established

## APPLICATIONS INFORMATION

by the inductor size, input voltage and output voltage. Since the synchronization frequency will not change the slopes of the inductor current waveform, if the inductor is large enough to avoid subharmonic oscillations at the frequency set by $R_T$, than the slope compensation will be sufficient for all synchronization frequencies.

### Power Good Flag

The PG pin is an open-drain output which is used to indicate to the user when the output voltage is within regulation. When the output is lower than the regulation voltage by more than 8.4%, as determined from the FB pin voltage, the PG pin will pull low to indicate the power is not good. Otherwise, the PG pin will go high impedance and can be pulled logic high with a resistor pull-up. The PG pin is only comparing the output voltage to an accurate reference when the LT3976 is enabled and $V_{IN}$ is above 4.3V. When the part is shutdown, the PG is actively pulled low to indicate that the LT3976 is not regulating the output. The input voltage must be greater than 1.4V to fully turn-on the active pull-down device. Figure 8 shows the status of the PG pin as the input voltage is increased.

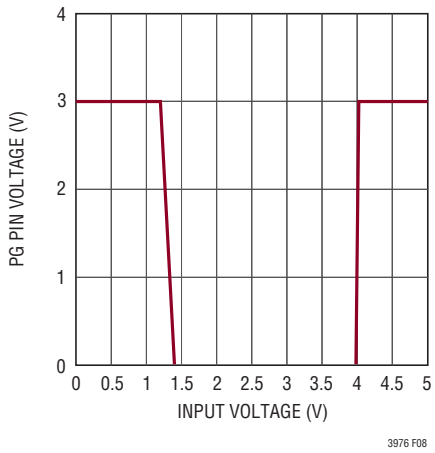



**Figure 8. PG Pin Voltage Versus Input Voltage when PG Is Connected to 3V Through a 150k Resistor. The FB Pin Voltage Is 1.15V**

### Shorted and Reversed Input Protection

If the inductor is chosen so that it won't saturate excessively, a LT3976 buck regulator will tolerate a shorted output and the power dissipation will be limited by current limit foldback (see Current Limit Foldback and Thermal Protection section). There is another situation to consider in systems where the output will be held high when the input to the LT3976 is absent. This may occur in battery charging applications or in battery backup systems where a battery or some other supply is diode ORed with the LT3976's output. If the $V_{IN}$ pin is allowed to float and the EN/UVLO pin is held high (either by a logic signal or because it is tied to $V_{IN}$), then the LT3976's internal circuitry will pull its quiescent current through its SW pin. This is fine if your system can tolerate a few µA in this state. If you ground the EN pin, the SW pin current will drop to essentially zero. However, if the $V_{IN}$ pin is grounded while the output is held high, regardless of EN, parasitic diodes inside the LT3976 can pull current from the output through the SW pin and the $V_{IN}$ pin. Figure 9 shows a circuit that will run only when the input voltage is present and that protects against a shorted or reversed input.

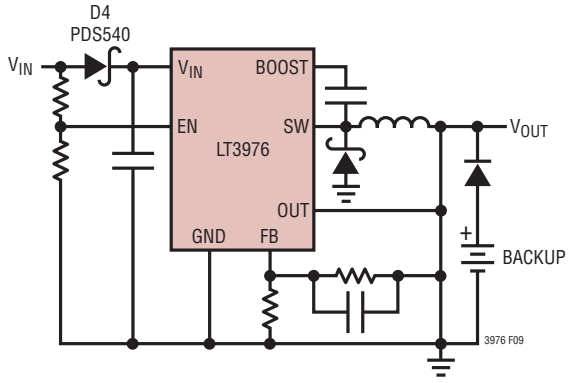



**Figure 9. Diode D4 Prevents a Shorted Input from Discharging a Backup Battery Tied to the Output. It Also Protects the Circuit from a Reversed Input. The LT3976 Runs Only When the Input Is Present**

### PCB Layout

For proper operation and minimum EMI, care must be taken during printed circuit board layout. Figure 10 shows a sample component placement with trace, ground plane and via locations, which serves as a good PCB layout example. Note that large, switched currents flow in the LT3976's $V_{IN}$ and SW pins, the catch diode (D1), and the input capacitor (C1). The loop formed by these components should be as small as possible. These components, along with the inductor and output capacitor, should be placed on the same side of the circuit board, and their connections should be made on that layer. Place a local,

## APPLICATIONS INFORMATION

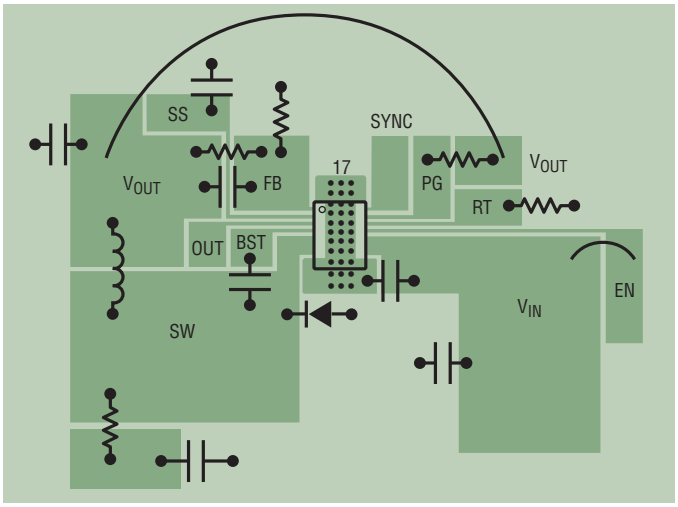



**Figure 10. Layout Showing a Good PCB Design**

unbroken ground plane below these components. The SW and BOOST nodes should be as small as possible. Finally, keep the FB and RT nodes small so that the ground traces will shield it from the SW and BOOST nodes. The exposed pad on the bottom of the package must be soldered to ground so that the pad acts as a heat sink. To keep thermal resistance low, extend the ground plane as much as possible, and add thermal vias under and near the LT3976 to additional ground planes within the circuit board and on the bottom side.

### High Temperature Considerations

For higher ambient temperatures, care should be taken in the layout of the PCB to ensure good heat sinking of the LT3976. The exposed pad on the bottom of the package must be soldered to a ground plane. This ground should be tied to large copper layers below with thermal vias; these layers will spread the heat dissipated by the LT3976. Placing additional vias can reduce the thermal resistance further. When operating at high ambient temperatures, the maximum load current should be derated as the ambient temperature approaches the maximum junction rating. (See Thermal Derating curve in the Typical Performance Characteristics section.)

Power dissipation within the LT3976 can be estimated by calculating the total power loss from an efficiency measurement and subtracting the catch diode loss and inductor loss. The die temperature is calculated by multiplying the LT3976 power dissipation by the thermal resistance from junction to ambient. The temperature rise of the LT3976 for a 3.3V and 5V application was measured using a thermal camera and is shown in Figure 11.

Also keep in mind that the leakage current of the power Schottky diode goes up exponentially with junction temperature. When the power switch is off, the power Schottky diode is in parallel with the power converter's output filter stage. As a result, an increase in a diode's leakage current results in an effective increase in the load, and a corresponding increase in the input quiescent current. Therefore, the catch Schottky diode must be selected with care to avoid excessive increase in light load supply current at high temperatures.

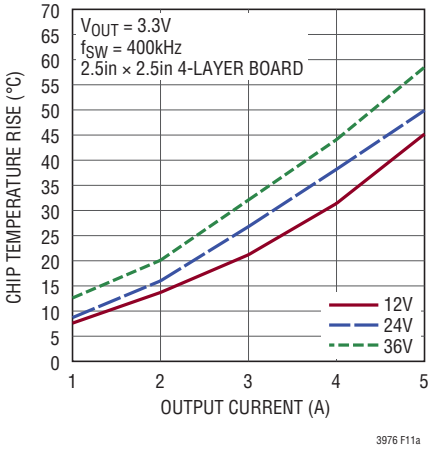



**Figure 11a. Temperature Rise of the LT3976 in the Front Page Application**

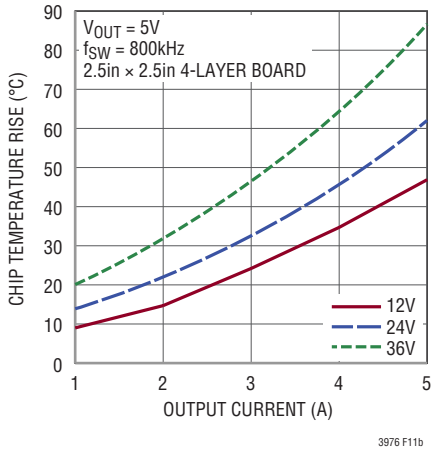



**Figure 11b. Temperature Rise of the LT3976 in a $5V_{OUT}$ Application**

## APPLICATIONS INFORMATION

### Fault Tolerance of QFN Package

The QFN package is designed to tolerate single fault conditions. Shorting two adjacent pins together or leaving one single pin floating does not raise the output voltage or cause damage to the LT3976 regulator. However, the application circuit must meet a few requirements discussed in this section in order to achieve this fault tolerance.

Tables 5 and 6 show the effects that result from shorting adjacent pins or from a floating pin, respectively.

There are three items which require consideration in terms of the application circuit to achieve fault tolerance: SS-OUT pin short, RT-PG pin short, and PG-SYNC pin short.

If the output voltage is less than 6V, then the application circuit can be setup normally (see Figure 12a) because a SS to OUT short will not violate the SS pin 6V absolute maximum and a PG short to either RT or SYNC will not violate the 6V absolute maximum on each of those pins.

If the output voltage is greater than 6V, the best way to solve the problem of violating the SS absolute maximum when shorted to OUT is to tie the OUT pin to GND. Note that grounding the OUT pin will compromise the dropout performance of the LT3976. When OUT is grounded, an external Schottky diode to either the output, $V_{IN}$, or another voltage source must be used to charge the boost capacitor. The PG pull-up resistor must be increased

**Table 5. Effects of Pin Shorts**

| PINS | EFFECT |
|---|---|
| SS-OUT | $V_{OUT}$ may fall below regulation voltage for $V_{OUT}$ less than or equal to 6V. For outputs above 6V, the absolute maximum of the SS pin would be violated, so the OUT pin must be tied to GND (see discussion in the Fault Tolerance section) |
| $V_{IN}$-EN | No effect. In most applications, EN is tied to $V_{IN}$. If EN is driven with a logic signal, the customer must ensure that the circuit generating that signal can withstand the maximum $V_{IN}$ |
| RT-PG | No effect if PG is floated. $V_{OUT}$ will fall below regulation if PG is connected to the output with a resistor pull-up as long as the resister divider formed by the PG pin pull-up and the RT resistor prevents the RT pin absolute maximum from being violated (see discussion in the Fault Tolerance section). In both cases, the switching frequency will be significantly increased if the output goes below regulation, which may cause the LT3976 to go into pulse-skipping mode if the minimum on-time is violated. |
| PG-SYNC | No effect if PG is floated. No effect if PG is connected to the output with a resistor pull-up as long as there is a resistor to GND on the SYNC pin or the SYNC pin is tied to GND. This is to ensure that the resistor divider formed by the PG pin pull-up and the SYNC pin resistor to GND prevents the SYNC pin Absolute Maximum from being violated (see discussion in the Fault Tolerance section). |

**Table 6. Effects of Floating Pins**

| PIN | EFFECT |
|---|---|
| SS | No effect; soft-start feature will not function. |
| OUT | $V_{OUT}$ may fall below regulation voltage. With the OUT pin disconnected, the boost capacitor cannot be charged and thus the power switch cannot fully saturate, which increases power dissipation. |
| BOOST | $V_{OUT}$ may fall below regulation voltage. With the BOOST pin disconnected, the boost capacitor cannot be charged and thus the power switch cannot fully saturate, which increases power dissipation. |
| SW | No effect; there are several SW pins. |
| $V_{IN}$ | No effect; there are several $V_{IN}$ pins. |
| EN | $V_{OUT}$ may fall below regulation voltage. Part may work normally or be shutdown depending on how the application circuit couples to the floating EN pin. |
| RT | $V_{OUT}$ may fall below regulation voltage. |
| PG | No effect. |
| SYNC | No effect. The LT3976 may be in Burst Mode operation or pulse-skipping mode depending on how the application circuit couples to the floating SYNC pin. |
| FB | No effect; there are two FB pins. |
| GND | No effect; there are several GND connections. If Exposed Pad is floated, thermal performance will be degraded. |

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and a SYNC pin resistor to GND added, so that a PG pin short to either SYNC or RT will form resistor dividers to keep the voltage on the SYNC and RT pins below their rated absolute maximum. This application is shown in Figure 12b. The external Schottky must be connected such that the absolute maximum of the BOOST pin is not violated. The SYNC pin resistor can be removed if the SYNC pin is grounded or PG is left floating both of which also result in fault tolerant circuits.

### Other Linear Technology Publications

Application Notes 19, 35 and 44 contain more detailed descriptions and design information for buck regulators and other switching regulators. The LT1376 data sheet has a more extensive discussion of output ripple, loop compensation and stability testing. Design Note 318 shows how to generate a bipolar output supply using a buck regulator.

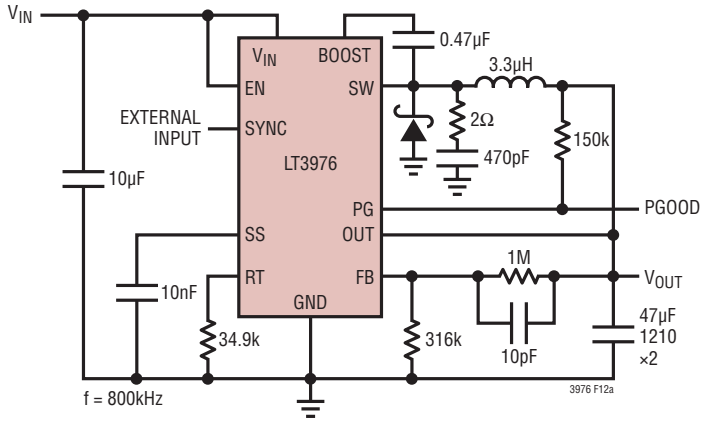



**Figure 12a. Fault Tolerant for $V_{OUT}$ < 6V (Note: For $V_{OUT}$ < 3.3V External Boost Schottky Diode Is Needed)**

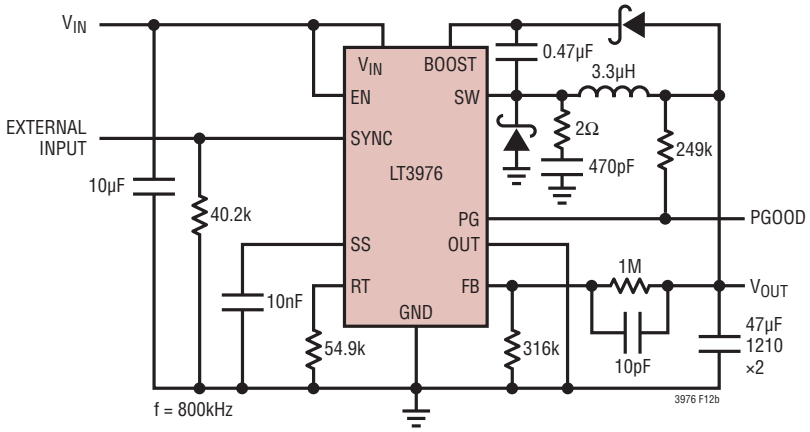
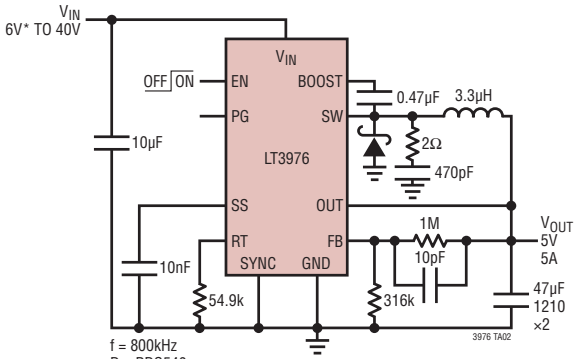



**Figure 12b. Fault Tolerant for $V_{OUT}$ < 27V (Note: For $V_{OUT}$ < 3V External Boost Schottky Diode Should Be Connected to the Input)**

**Figure 12. Two Example Circuits to Achieve Fault Tolerance (FMEA) with the LT3976 QFN Package**

# TYPICAL APPLICATIONS

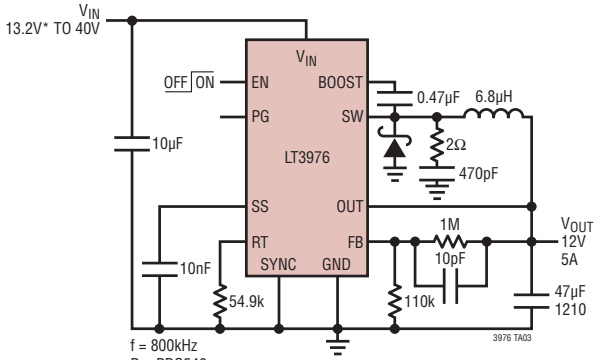
### 5V Step-Down Converter




f = 800kHz
D = PDS540
L = IHLP-2525CZ-01

* MINIMUM $V_{IN}$ CAN BE LOWERED WITH ADDITIONAL INPUT AND OUTPUT CAPACITANCE.

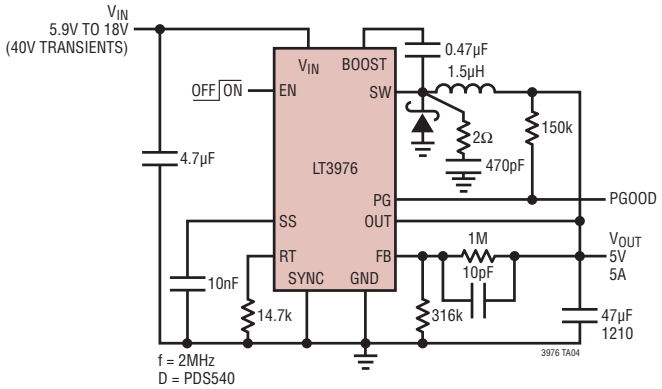
### 12V Step-Down Converter




f = 800kHz
D = PDS540
L = IHLP-4040DZ-01

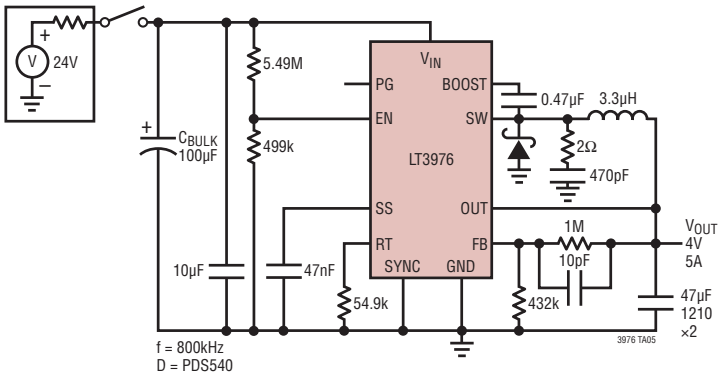
* MINIMUM $V_{IN}$ CAN BE LOWERED WITH ADDITIONAL INPUT AND OUTPUT CAPACITANCE.

### 5V, 2MHz Step-Down Converter with Power Good



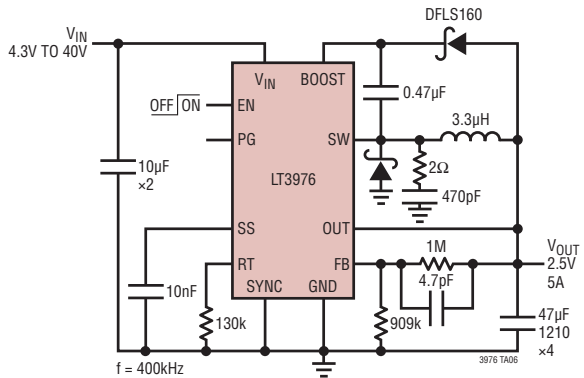

f = 2MHz
D = PDS540
L = IHLP-2525CZ-01

### 4V Step-Down Converter with a High Impedance Input Source



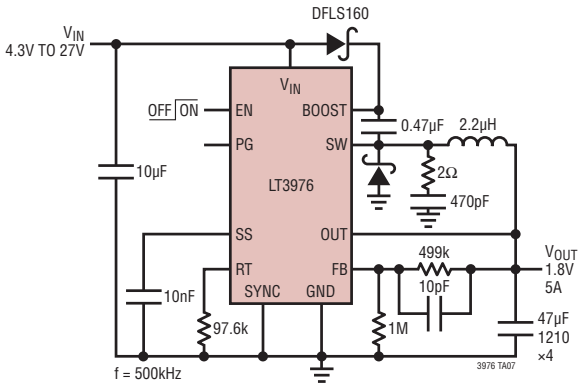

f = 800kHz
D = PDS540
L = IHLP-2525CZ-01

### 2.5V Step-Down Converter




f = 400kHz
D = PDS540
L = IHLP-2525CZ-01

### 1.8V Step-Down Converter

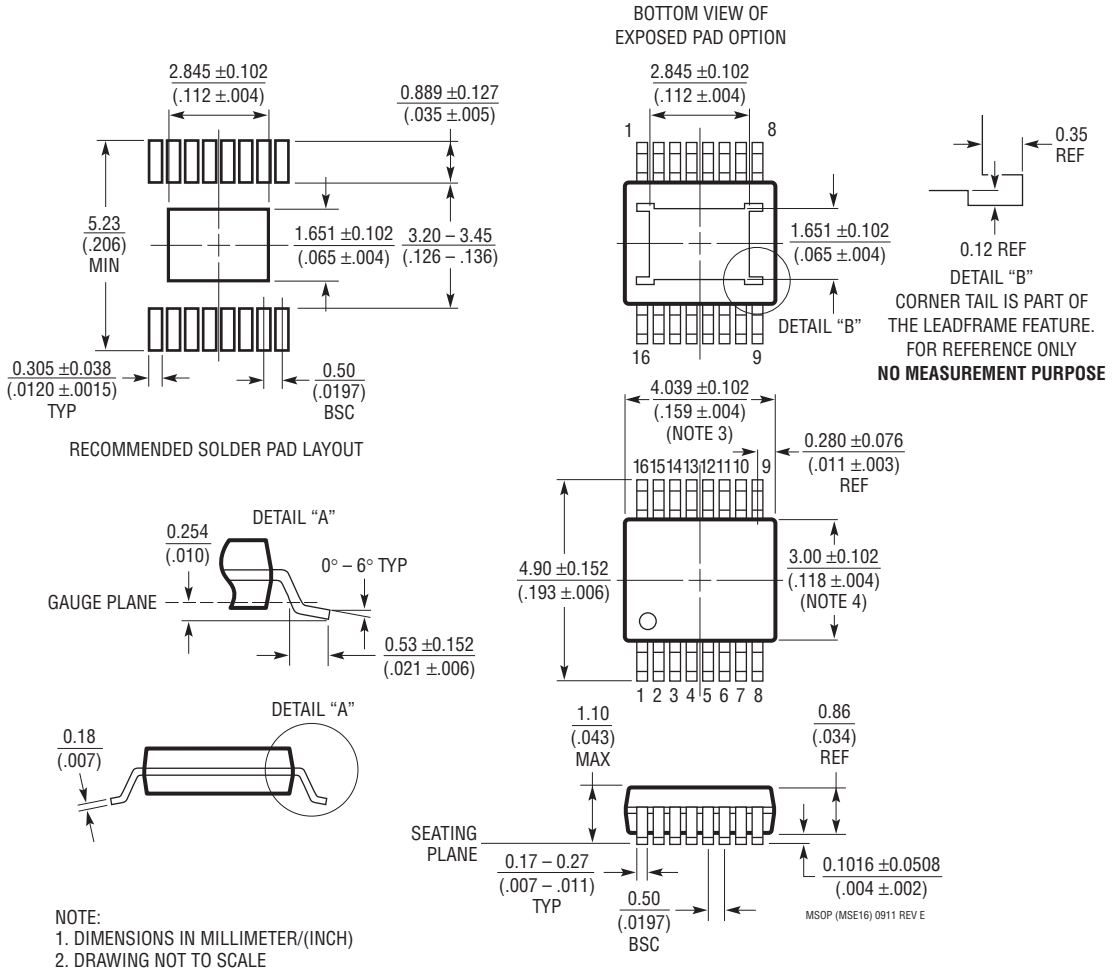



f = 500kHz
D = PDS540
L = IHLP-2525CZ-01

# PACKAGE DESCRIPTION

**Please refer to http://www.linear.com/designtools/packaging/ for the most recent package drawings.**

**MSE Package**
**16-Lead Plastic MSOP, Exposed Die Pad**
(Reference LTC DWG # 05-08-1667 Rev E)

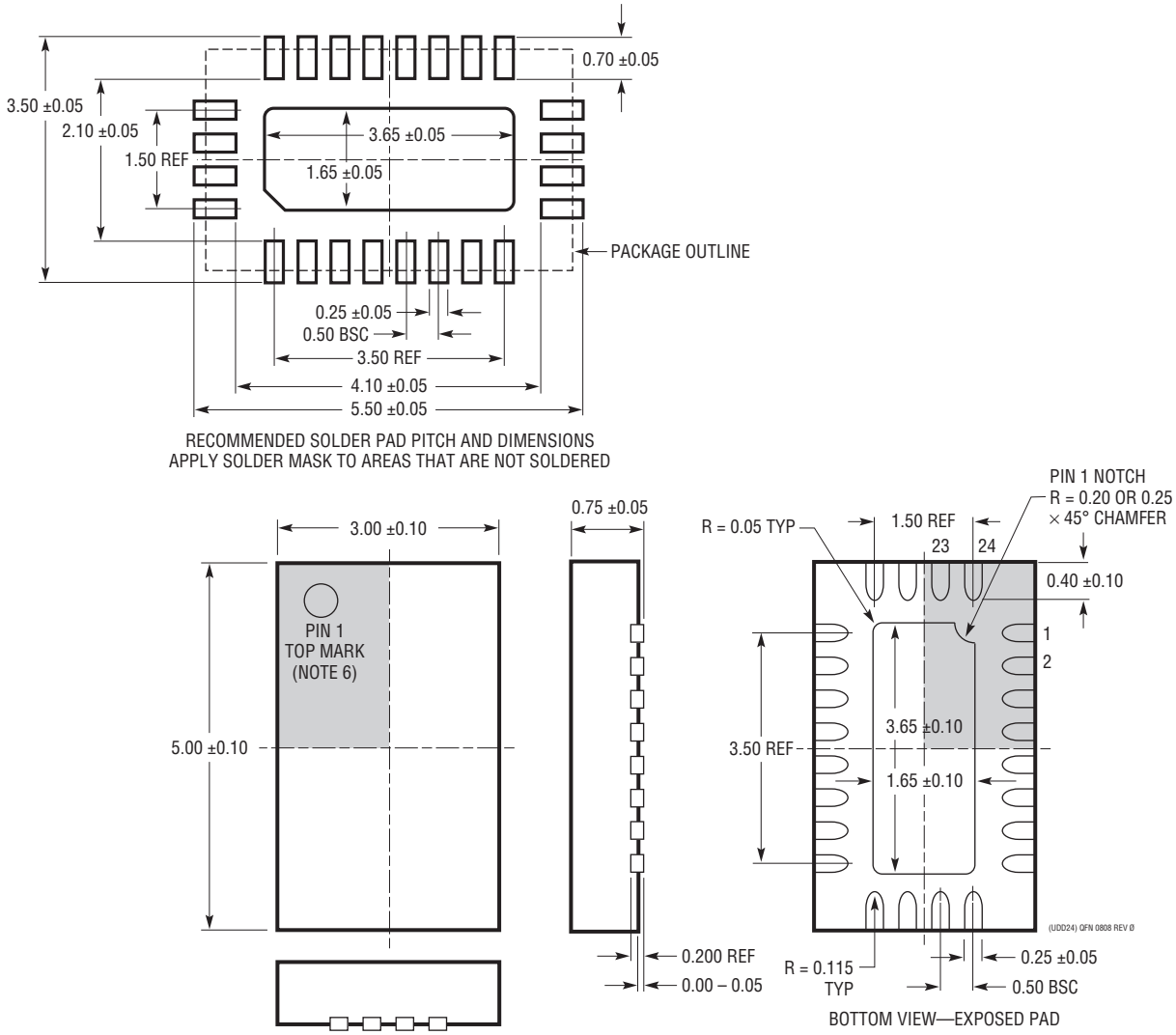



NOTE:
1. DIMENSIONS IN MILLIMETER/(INCH)
2. DRAWING NOT TO SCALE
3. DIMENSION DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS.
   MOLD FLASH, PROTRUSIONS OR GATE BURRS SHALL NOT EXCEED 0.152mm (.006") PER SIDE
4. DIMENSION DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSIONS.
   INTERLEAD FLASH OR PROTRUSIONS SHALL NOT EXCEED 0.152mm (.006") PER SIDE
5. LEAD COPLANARITY (BOTTOM OF LEADS AFTER FORMING) SHALL BE 0.102mm (.004") MAX
6. EXPOSED PAD DIMENSION DOES INCLUDE MOLD FLASH. MOLD FLASH ON E-PAD SHALL
   NOT EXCEED 0.254mm (.010") PER SIDE.

# PACKAGE DESCRIPTION

**Please refer to http://www.linear.com/designtools/packaging/ for the most recent package drawings.**

**UDD Package**
**24-Lead Plastic QFN (3mm × 5mm)**
(Reference LTC DWG # 05-08-1833 Rev Ø)



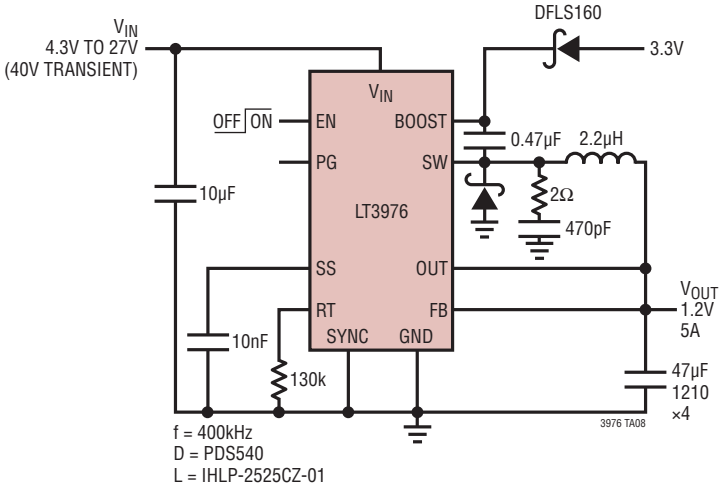

NOTE:
1. DRAWING IS NOT A JEDEC PACKAGE OUTLINE
2. DRAWING NOT TO SCALE
3. ALL DIMENSIONS ARE IN MILLIMETERS
4. DIMENSIONS OF EXPOSED PAD ON BOTTOM OF PACKAGE DO NOT INCLUDE MOLD FLASH. MOLD FLASH, IF PRESENT, SHALL NOT EXCEED 0.15mm ON ANY SIDE
5. EXPOSED PAD SHALL BE SOLDER PLATED
6. SHADED AREA IS ONLY A REFERENCE FOR PIN 1 LOCATION ON THE TOP AND BOTTOM OF PACKAGE



Information furnished by Linear Technology Corporation is believed to be accurate and reliable. However, no responsibility is assumed for its use. Linear Technology Corporation makes no representation that the interconnection of its circuits as described herein will not infringe on existing patent rights.

## TYPICAL APPLICATION

**1.2V Step-Down Converter**




## RELATED PARTS

| PART NUMBER | DESCRIPTION | COMMENTS |
|---|---|---|
| LT3480 | 36V with Transient Protection to 60V, 2A ($I_{OUT}$), 2.4MHz, High Efficiency Step-Down DC/DC Converter with Burst Mode® Operation | $V_{IN}$ = 3.6V to 38V, Transients to 60V, $V_{OUT(MIN)}$ = 0.78V, $I_Q$ = 70µA, $I_{SD}$ < 1µA, 3mm × 3mm DFN-10, MSOP-10E |
| LT3980 | 58V with Transient Protection to 80V, 2A ($I_{OUT}$), 2.4MHz, High Efficiency Step-Down DC/DC Converter with Burst Mode Operation | $V_{IN}$ = 3.6V to 58V, Transients to 80V, $V_{OUT(MIN)}$ = 0.79V, $I_Q$ = 75µA, $I_{SD}$ < 1µA, 3mm × 4mm DFN-16, MSOP-16E |
| LT3971 | 38V, 1.2A ($I_{OUT}$), 2MHz, High Efficiency Step-Down DC/DC Converter with Only 2.8µA of Quiescent Current | $V_{IN}$ = 4.2V to 38V, $V_{OUT(MIN)}$ = 1.2V, $I_Q$ = 2.8µA, $I_{SD}$ < 1µA, 3mm × 3mm DFN-10, MSOP-10E |
| LT3991 | 55V, 1.2A ($I_{OUT}$), 2MHz, High Efficiency Step-Down DC/DC Converter with Only 2.8µA of Quiescent Current | $V_{IN}$ = 4.2V to 55V, $V_{OUT(MIN)}$ = 1.2V, $I_Q$ = 2.8µA, $I_{SD}$ < 1µA, 3mm × 3mm DFN-10, MSOP-10E |
| LT3970 | 40V, 350mA ($I_{OUT}$), 2MHz, High Efficiency Step-Down DC/DC Converter with Only 2.5µA of Quiescent Current | $V_{IN}$ = 4.2V to 40V, $V_{OUT(MIN)}$ = 1.2V, $I_Q$ = 2.5µA, $I_{SD}$ < 0.7µA, 2mm × 3mm DFN-10, MSOP-10E |
| LT3990 | 62V, 350mA ($I_{OUT}$), 2.2MHz, High Efficiency Step-Down DC/DC Converter with Only 2.5µA of Quiescent Current | $V_{IN}$ = 4.2V to 62V, $V_{OUT(MIN)}$ = 1.2V, $I_Q$ = 2.5µA, $I_{SD}$ < 0.7µA, 3mm × 3mm DFN-10, MSOP-16E |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LT 0113 • PRINTED IN USA
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