16-Channel 50mA LED Driver with Buck Controller

FEATURES

- **6V to 55V Power Input Voltage Range**
- **16 Independent LED Outputs Up to 75mA/36V**
- **±3% LED Current Matching at 50mA (Typ ±1%)**
- **6-Bit Dot Correction Current Adjustment**
- **12-Bit Grayscale PWM Dimming**
- **0.5µs Minimum LED On-Time**
- **Adaptive LED Bus Voltage for High Efficiency**
- **Cascadable 30MHz Serial Data Interface**
- Full Diagnostic and Protection: Individual Open/Short LED and Overtemperature Fault
- 40-Lead 6mm × 6mm QFN Package

APPLICATIONS

- Large Screen Display LED Backlighting
- Mono-, Multi-, Full-Color LED Displays
- LED Billboards and Signboards

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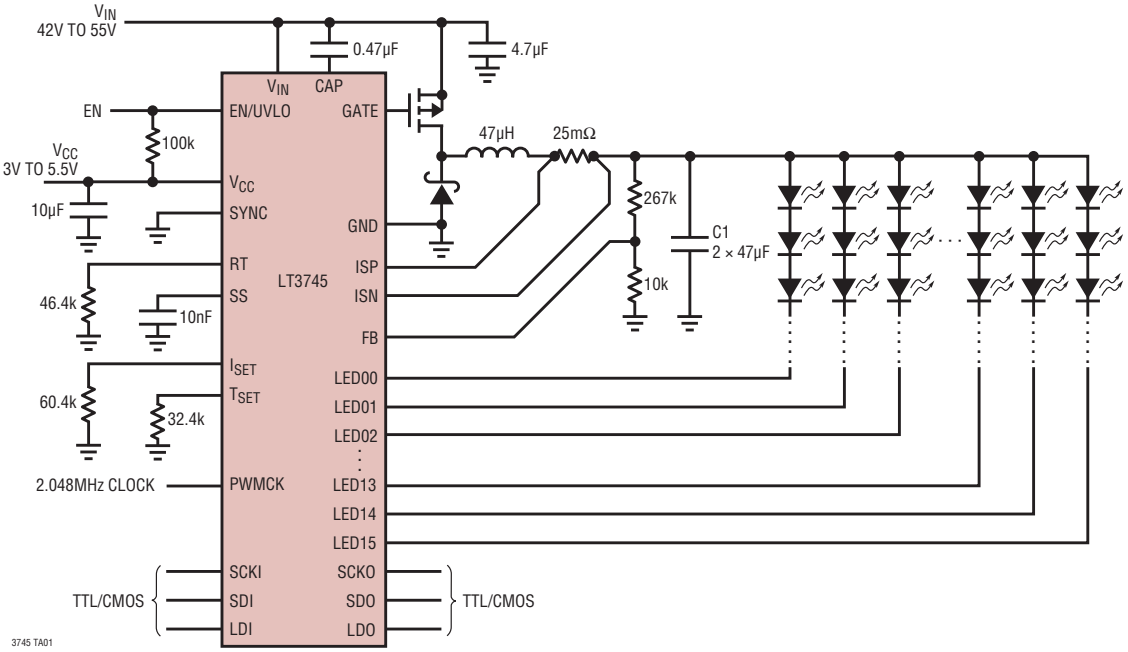
DESCRIPTION

The LT®3745 integrates a 16-channel LED driver with a 55V buck controller. The LED driver lights up to 75mA/36V of LEDs in series per channel, and the buck controller generates an adaptive bus voltage supplying the parallel LED strings. Each channel has individual 6-bit dot correction current adjustment and 12-bit grayscale PWM dimming. Both dot correction and grayscale are accessible via a serial data interface in TTL/CMOS logic. A ±3% LED current matching and a 0.5µs minimum LED on-time can be achieved at 50mA per channel.

The LT3745 performs full diagnostic and protection against open/short LED and overtemperature fault. The fault status is sent back through the serial data interface. The 30MHz fully-buffered, skew-balanced, cascadable serial data interface makes the chip extremely suitable for large screen LCD dynamic backlighting and mono-, multi-, full-color LED displays.

TYPICAL APPLICATION

16-Channel LED Driver, 1MHz Buck, 10 LEDs, 25mA to 75mA per Channel, 500Hz 12-Bit Dimming

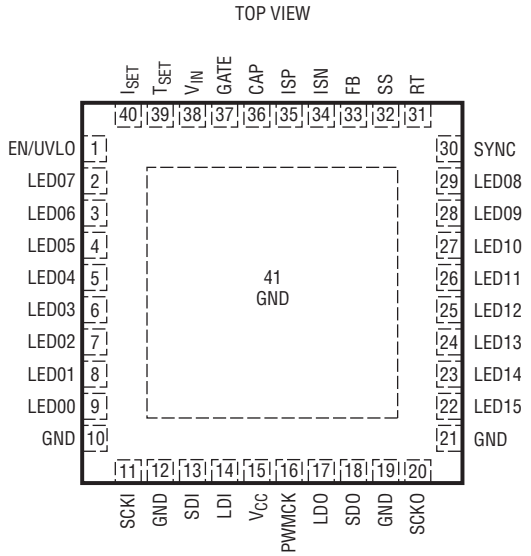


ABSOLUTE MAXIMUM RATINGS

(Note 1)

V_{IN} 57V
CAP ..... V_{IN} – 8V to V_{IN}
GATE ..... CAP to V_{IN}
LED00 to LED15, ISP, ISN 40V
ISP ..... ISN – 1V to ISN + 1V
FB, RT, T_{SET}, I_{SET} 2V
V_{CC} ..... –0.3V to 6V
SCKI, SCKO, SDI, SDO, LDI, LDO, PWMCK, SYNC,
SS, EN/UVLO ..... –0.3V to V_{CC}
Operating Junction Temperature Range
(Notes 2, 3)
LT3745E ..... –40°C to 125°C
LT3745I ..... –40°C to 125°C
Storage Temperature Range ..... –65°C to 125°C

PIN CONFIGURATION



UJ PACKAGE
40-LEAD (6mm × 6mm) PLASTIC QFN

T_{JMAX} = 125°C, θ_{JA} = 34°C/W, θ_{JC} = 2.5°C/W
EXPOSED PAD (PIN 41) IS GND, MUST BE SOLDERED TO PCB

ORDER INFORMATION

LEAD FREE FINISH	TAPE AND REEL	PART MARKING*	PACKAGE DESCRIPTION	TEMPERATURE RANGE
LT3745EUJ#PBF	LT3745EUJ#TRPBF	3745	40-Lead (6mm × 6mm) Plastic QFN	–40°C to 125°C
LT3745IUJ#PBF	LT3745IUJ#TRPBF	3745	40-Lead (6mm × 6mm) Plastic QFN	–40°C to 125°C

Consult LTC Marketing for parts specified with wider operating temperature ranges. *The temperature grade is identified by a label on the shipping container.

Consult LTC Marketing for information on nonstandard lead based finish parts.

For more information on lead free part marking, go to: http://www.linear.com/leadfree/
For more information on tape and reel specifications, go to: http://www.linear.com/tapeandreel/

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. V_{IN} = 12V, V_{CC} = 3.3V, $V_{EN/UVLO}$ = 1.5V, V_{FB} = 1.5V, V_{ISP} = V_{ISN} = 0V, R_T = 105k, R_{ISET} = 60.4k, C_{CAP} = 0.47µF to V_{IN}, unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Supply							
V_{IN}	V_{IN} Operating Voltage		●	6		55	V
I_{VIN}	V_{IN} Supply Current	$V_{EN/UVLO}$ = 0V No Switching			0.2 0.4	2 0.55	µA mA
V_{CC}	V_{CC} Operating Voltage		●	3		5.5	V
I_{VCC}	V_{CC} Supply Current (Note 4)	$V_{EN/UVLO}$ = 0V LED Channel Off, 30MHz Data Off LED Channel On, 30MHz Data Off LED Channel On, 30MHz Data On			0.1 3.1 7 16	1 3.6	µA mA mA mA
Undervoltage Lockout (UVLO)							
	V_{CC} UVLO Threshold	V_{CC} Rising V_{CC} Falling		2.82 2.61	2.89 2.68	2.96 2.75	V V
	EN/UVLO Shutdown Threshold UVLO Threshold	I_{VCC} <20µA $V_{EN/UVLO}$ Rising $V_{EN/UVLO}$ Falling		0.35 1.28 1.19	 1.31 1.22	 1.34 1.25	V V V
$I_{EN/UVLO}$	EN/UVLO Bias Current	$V_{EN/UVLO}$ = V_{CC} = 3.3V			0.1	1	µA
	(V_{IN} – V_{CAP}) UVLO Threshold	(V_{IN} – V_{CAP}) Rising (V_{IN} – V_{CAP}) Falling		4.6 4.2	4.9 4.5	5.2 4.8	V V
Soft-Start (SS)							
I_{SS}	Soft-Start Charge Current	V_{SS} = 1V		–16	–12	–8	µA
	Soft-Start Discharge Current	V_{SS} = V_{CC}, $V_{EN/UVLO}$ = 1V			330		µA
$V_{SS(TH)}$	Soft-Start Reset Threshold				0.35		V
Oscillator							
V_{RT}	RT Pin Voltage			1.186	1.205	1.224	V
I_{RT}	RT Pin Current Limit	V_{RT} = 0V			–80		µA
f_{OSC}	Oscillator Frequency	R_T = 280k R_T = 105k R_T = 46.4k		188 475 965	200 500 1015	212 525 1065	kHz kHz kHz
f_{SYNC}	Sync Frequency Range (Note 5)	R_T = 348k		200		1000	kHz
	SYNC LOGIC High Level Voltage Low Level Voltage	V_{CC} = 3V to 5.5V		 2.4 0		 V_{CC} 0.6	 V V
Error Amplifiers and Loop Dynamics							
V_{FB}	FB Regulation Voltage	V_{ISN} = 5V	●	1.186	1.210	1.234	V
I_{FB}	FB Input Bias Current	V_{ISN} = 5V, V_{FB} Regulated			–120		nA
	LED Regulation Voltage	V_{ISN} = 5V, V_{FB} = 1V		0.63	0.715	0.8	V
$T_{OFF(MIN)}$	Minimum GATE Off-Time	V_{ISP} = V_{ISN} = 5V, V_{FB} = 1V			120		ns
$T_{ON(MIN)}$	Minimum GATE On-Time	(V_{ISP} – V_{ISN}) = 60mV, V_{ISN} = 5V, V_{FB} = 1V			200		ns
Current Sense Amplifier							
	ISP/ISN Pin Common Mode	V_{ISP} = V_{ISN}	●	0		36	V
	V_{IN} to ISN Dropout Voltage (V_{IN} – V_{ISN})	V_{ISP} = V_{ISN}, V_{FB} = 1V	●		1.7	2.1	V
	Current Limit Sense Threshold (V_{ISP} – V_{ISN})	V_{FB} = 1V		34	46.5	59	mV
I_{ISP}	ISP Input Bias Current				–24		µA
I_{ISN}	ISN Input Bias Current				–48		µA

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. V_{IN} = 12V, V_{CC} = 3.3V, $V_{EN/UVLO}$ = 1.5V, V_{FB} = 1.5V, V_{ISP} = V_{ISN} = 0V, R_T = 105k, R_{ISET} = 60.4k, C_{CAP} = 0.47µF to V_{IN}, unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Gate Driver							
V_{BIAS}	CAP Bias Voltage (V_{IN} – V_{CAP})	7V < V_{IN} < 55V		6.5	6.8	7.1	V
I_{CAP}	CAP Bias Current Limit	(V_{IN} – V_{CAP}) = V_{BIAS} – 0.5V			22		mA
	GATE High Level (V_{IN} – V_{GATE})	I_{GATE} = –100mA			0.4		V
	GATE Low Level (V_{GATE} – V_{CAP})	I_{GATE} = 100mA			0.3		V
	GATE Rise Time	C_{GATE} = 3.3nF to V_{IN}			30		ns
	GATE Fall Time	C_{GATE} = 3.3nF to V_{IN}			30		ns
LED Driver							
V_{ISET}	Trimmed I_{SET} Pin Voltage		●	1.181	1.205	1.229	V
	LEDxx Operating Voltage	V_{IN} = 48V, V_{ISP} = V_{ISN} = V_{LEDxx}	●			36	V
	LEDxx Leakage Current	LED Channel Off, V_{IN} = 48V, V_{ISP} = V_{ISN} = 36V, V_{LEDxx} = 24V				0.2	µA
I_{LED}	LED Constant Sink Current	V_{ISP} = V_{ISN} = 5V, V_{LEDxx} = 1V					
		REG_{DC} = 0x00	●	23.5	25.3	27	mA
		REG_{DC} = 0x20	●	48	50.5	53	mA
		REG_{DC} = 0x3F	●	71	74	77	mA
ΔI_{LEDC}	Current Mismatch Between Channels	V_{ISP} = V_{ISN} = 5V, V_{LEDxx} = 1V, REG_{DC} = 0x20 (Note 6)	●		±1	±3	%
ΔI_{LEDD}	Current Mismatch Between Devices	V_{ISP} = V_{ISN} = 5V, V_{LEDxx} = 1V, REG_{DC} = 0x20 (Note 7)	●		±1	±3	%
ΔI_{LINE}	LED Current Line Regulation	V_{ISP} = V_{ISN} = 5V, V_{LEDxx} = 1V, REG_{DC} = 0x20, V_{CC} = 3V to 5.5V (Note 8)			0.1	0.2	%/V
ΔI_{LOAD}	LED Current Load Regulation	V_{ISP} = V_{ISN} = 5V, REG_{DC} = 0x20, V_{LEDxx} = 1V to 3V (Note 9)			0.1	0.2	%/V
V_{OPEN}	Open LED Threshold	V_{ISP} = V_{ISN} = 5V, V_{LEDxx} Falling			0.35		V
V_{SHT}	Short LED Threshold	V_{ISP} = V_{ISN} = 5V, V_{LEDxx} Rising		3.7	3.9	4.1	V
T_{LEDON}	Minimum LED On-Time	V_{ISP} = V_{ISN} = 5V, REG_{GS} = 0x001			0.5		µs
	PWMCK LOGIC	V_{CC} = 3V to 5.5V					
	High Level Voltage			2.4		V_{CC}	V
	Low Level Voltage			0		0.6	V
Thermal Protection							
I_{TSET}	T_{SET} Output Current	V_{TSET} = 1V	●	19.0	19.8	20.6	µA
	T_{SET} Over Temperature Threshold	T_A = 25°C			510		mV
Serial Data Interface							
	Single-Ended Input (Note 10)	V_{CC} = 3V to 5.5V					
V_{SIH}	High Level Voltage			2.4		V_{CC}	V
V_{SIL}	Low Level Voltage			0		0.6	V
I_{SI}	Single-Ended Input Current	V_{CC} = 3V to 5.5V, SI = V_{CC} or GND		–0.2		0.2	µA
	Single-Ended Output (Note 10)	V_{CC} = 3V to 5.5V					V
V_{SOH}	High Level Voltage	I_{SO} = –1mA		V_{CC} – 0.1			V
V_{SOL}	Low Level Voltage	I_{SO} = 1mA				0.1	V

TIMING CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. V_{IN} = 12V, V_{CC} = 3V to 5.5V, $V_{EN/UVLO}$ = 1.5V, V_{FB} = 1.5V, V_{ISP} = V_{ISN} = 5V, V_{LEDxx} = 1V, R_T = 105k, R_{ISET} = 60.4k, C_{CAP} = 0.47µF to V_{IN}, C_{SCKO} = C_{SDO} = C_{LDO} = 15pF to GND, unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
f_{SCKI}	Data Shift Clock Frequency		●			30	MHz
f_{PWMCK}	PWMCK Clock Frequency		●			25	MHz
t_{WH-CKI} t_{WL-CKI}	SCKI Pulse Duration	SCKI = H (Figure 3) SCKI = L (Figure 3)	● ●	16 16			ns ns
t_{WH-PWM} t_{WL-PWM}	PWMCK Pulse Duration	PWMCK = H (Figure 4) PWMCK = L (Figure 4)	● ●	20 20			ns ns
t_{WH-LDI}	LDI Pulse Duration	LDI = H (Figure 3)	●	20			ns
t_{SU-SDI}	SDI-SCKI Setup Time	SDI – SCKI ↑ (Figure 3)	●	2			ns
t_{HD-SDI}	SCKI-SDI Hold Time	SCKI ↑ – SDI (Figure 3)	●	2			ns
t_{SU-LDI}	SCKI-LDI Setup Time	SCKI ↓ – LDI ↑ (Figure 3)	●	5			ns
t_{HD-LDI}	LDI-SCKI Hold Time	LDI ↓ – SCKI ↑ (Figure 3)	●	15			ns
$t_{PD-SCK↑}$	SCKI-SCKO Propagation Delay (Rising)	SCKI ↑ – SCKO ↑ (Figure 3)	●		17	35	ns
$t_{PD-SCK↓}$	SCKI-SCKO Propagation Delay (Falling)	SCKI ↓ – SCKO ↓ (Figure 3)	●		20	40	ns
Δt_{PD-SCK}	SCK Duty Cycle Change	$\Delta t_{PD-SCK} = t_{PD-SCK↑} - t_{PD-SCK↓}$			–3		ns
t_{PD-SD}	SCKO-SDO Propagation Delay	SCKO ↑ – SDO (Figure 3)	●	2.2	4.5	7	ns
$t_{PD-LD↑}$	LDI-LDO Propagation Delay (Rising)	LDI ↑ – LDO ↑ (Figure 3)	●		17	35	ns
$t_{PD-LD↓}$	LDI-LDO Propagation Delay (Falling)	LDI ↓ – LDO ↓ (Figure 3)	●		20	40	ns
Δt_{PD-LD}	LD Duty Cycle Change	$\Delta t_{PD-LD} = t_{PD-LD↑} - t_{PD-LD↓}$			–3		ns
t_{PD-PWM}	PWMCK-LED Propagation Delay	PWMCK ↑ – I_{LED} (Figure 4)			80		ns
t_{R-SO}	SCKO/SDO/LDO Rise Time	C_{LOAD} = 15pF, 10% to 90%			4		ns
t_{F-SO}	SCKO/SDO/LDO Fall Time	C_{LOAD} = 15pF, 90% to 10%			4		ns

Table 1. Test Parameter Equations

$\Delta I_{LEDC}(\%) = \frac{I_{OUTn} - I_{OUTavg(0-15)}}{I_{OUTavg(0-15)}} \bullet 100$	(1)
$\Delta_{LEDD}(\%) = \frac{I_{OUTavg(0-15)} - I_{OUTcal}}{I_{OUTcal}} \bullet 100$	(2)
$I_{OUTcal} = 2500 \bullet \left(\frac{1.205V}{R_{ISET}}\right)$	(3)
$\Delta I_{LINE}(\%/V) = \frac{I_{OUTn}\left\|V_{CC} = 5.5V - I_{OUTn}\right\|V_{CC} = 3V}{I_{OUTn}\left\|V_{CC} = 3V\right.} \bullet \frac{100}{2.5V}$	(4)
$\Delta I_{LOAD}(\%/V) = \frac{I_{OUTn}\left\|V_{OUTn} = 3V - I_{OUTn}\right\|V_{OUTn} = 1V}{I_{OUTn}\left\|V_{OUTn} = 1V\right.} \bullet \frac{100}{2V}$	(5)

ELECTRICAL CHARACTERISTICS

Note 1: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to any Absolute Maximum Rating condition for extended periods may affect device reliability and lifetime.

Note 2: The LT3745E is guaranteed to meet performance specifications from 0°C to 125°C junction temperature. Specifications over the –40°C to 125°C operating junction temperature range are assured by design, characterization and correlation with statistical process controls. The LT3745I is guaranteed over the full –40°C to 125°C operating junction temperature range.

Note 3: This IC includes thermal shutdown protection that is intended to protect the device during momentary overload conditions. Junction temperature will exceed 125°C when thermal shutdown protection is active. Continuous operation above the specified maximum operating junction temperature may impair device reliability.

Note 4: The V_{CC} supply current with LED channel on highly depends on the LED current setting and LEDxx pin voltage; its test condition is R_{ISET} = 60.4k, REG_{DC} = 0x3F, REG_{GS} = 0xFFF, V_{ISP} = V_{ISN} = 5V, V_{LEDxx} = 1V. The V_{CC} supply current with serial data interface on highly depends on V_{CC} supply voltage, serial data interface clock frequency, SCKO/SDO/LDO loading capacitance, and PWMCK clock frequency; its test condition is V_{CC} = 3.3V, f_{SCKI} = 30MHz, C_{SCKO} = C_{SDO} = C_{LDO} = 15pF, f_{PWMCK} = 409.6KHz.

Note 5: The SYNC frequency must be higher than the RT programmed oscillator frequency, and is suggested to be around 20% higher. Any SYNC frequency higher than the suggested value may introduce sub-harmonic oscillation in the converter due to insufficient slope compensation. See Application Information section.

Note 6: The Current Mismatch between Channels is calculated as Equation 1 in Table 1.

Note 7: The Current Mismatch between Devices is calculated as Equations 2 and 3 in Table 1.

Note 8: The LED Current Line Regulation is calculated as Equation 4 in Table 1.

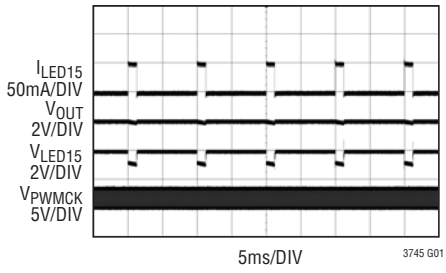
Note 9: The LED Current Load Regulation is calculated as Equation 5 in Table 1.

Note 10: The specifications of single-ended input SI apply to SCKI, SDI, and LDI pins; the specifications of single-ended output SO apply to SCKO, SDO, and LDO pins.

TYPICAL PERFORMANCE CHARACTERISTICS

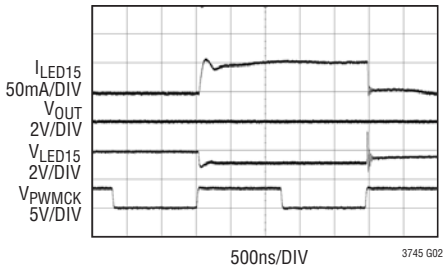
T_A = 25°C, unless otherwise noted.

100Hz 8:1 GS Dimming



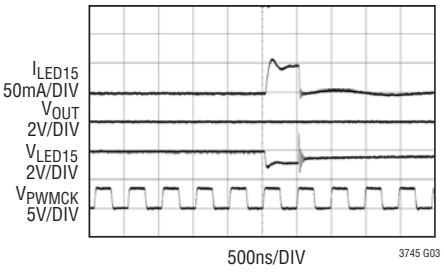
CIRCUIT OF FIGURE 7:
DC_{15} = 0×20
GS_{15} = 0×200

100Hz 4096:1 GS Dimming



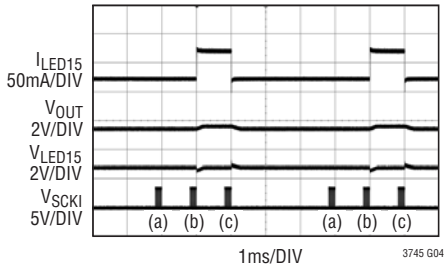
CIRCUIT OF FIGURE 7:
DC_{15} = 0×20
GS_{15} = 0×001

500Hz 4096:1 GS Dimming



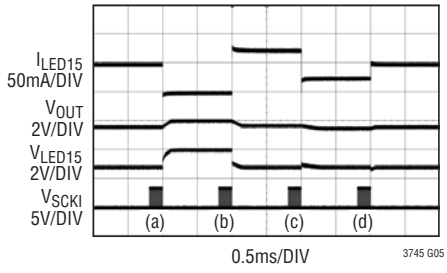
CIRCUIT OF FIGURE 7:
DC_{15} = 0×20
GS_{15} = 0×001

200Hz Two-Level DC Dimming



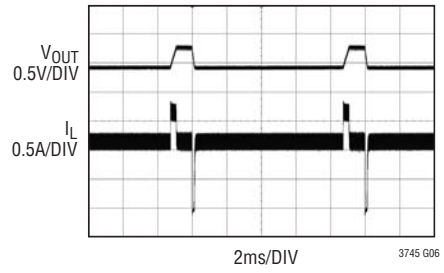
CIRCUIT OF FIGURE 7:
(a) EN = 1, GS_{15} = 0×FFF (c) EN = 1, DC_{15} = 0×00
(b) EN = 1, DC_{15} = 0×3F

200Hz Four-Level DC Dimming



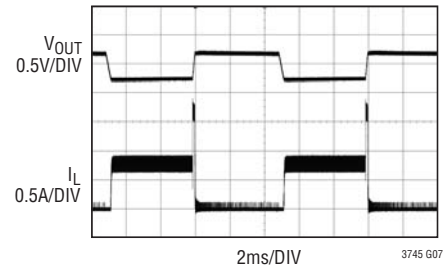
CIRCUIT OF FIGURE 7:
(a) EN = 0, GS_{15} = 0×FFF (c) EN = 1, DC_{15} = 0×00
(b) EN = 1, DC_{15} = 0×3F (d) EN = 1, DC_{15} = 0×20

Adaptive LED Bus Voltage I



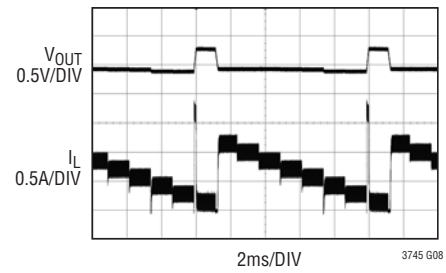
CIRCUIT OF FIGURE 7:
DC_{00-15} = 0×3F, GS_{00-15} = 0×FFF

Adaptive LED Bus Voltage II



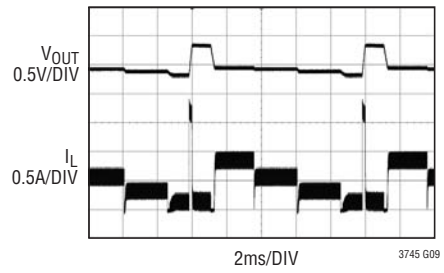
CIRCUIT OF FIGURE 7:
DC_{00-15} = 0×20, GS_{00-15} = 0×800

Adaptive LED Bus Voltage III



CIRCUIT OF FIGURE 7:
DC_{00-15} = 0×3F, GS_{00-01} = 0×1FF, GS_{02-03} = 0×3FF, GS_{04-05} = 0×5FF, GS_{06-07} = 0×7FF, GS_{08-09} = 0×9FF, GS_{10-11} = 0×BFF, GS_{12-13} = 0×DFF, GS_{14-15} = 0×FFF

Adaptive LED Bus Voltage IV

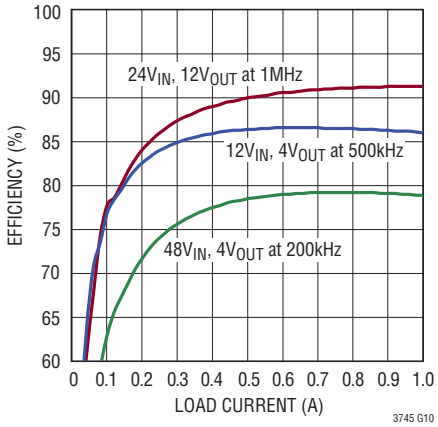


CIRCUIT OF FIGURE 7:
DC_{00-03} = 0×3F, GS_{00-03} = 0×3FF, DC_{04-07} = 0×2F, GS_{04-07} = 0×7FF, DC_{08-11} = 0×1F, GS_{08-11} = 0×BFF, DC_{12-15} = 0×0F, GS_{12-15} = 0×FFF

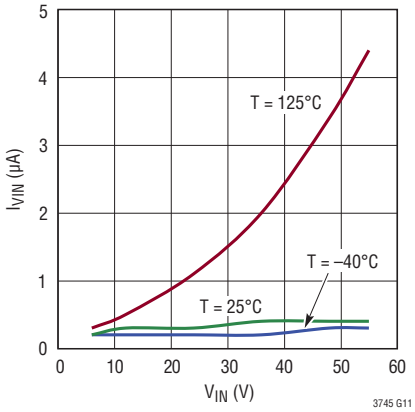
TYPICAL PERFORMANCE CHARACTERISTICS

T_A = 25°C, unless otherwise noted.

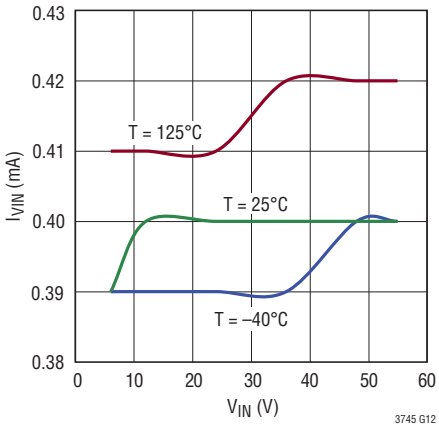
Buck Efficiency



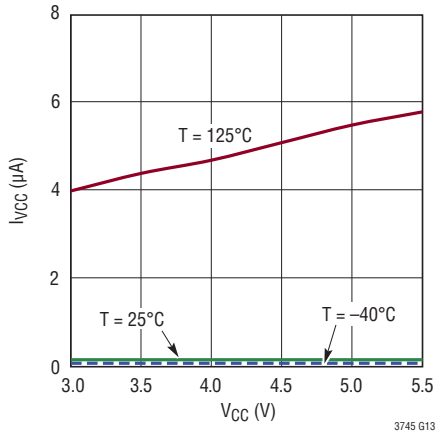
Shutdown I_{VIN} vs V_{IN}



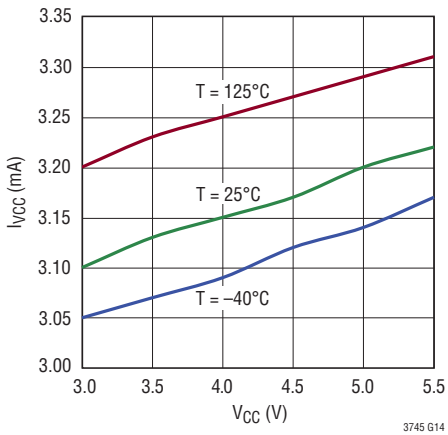
Quiescent I_{VIN} vs V_{IN}



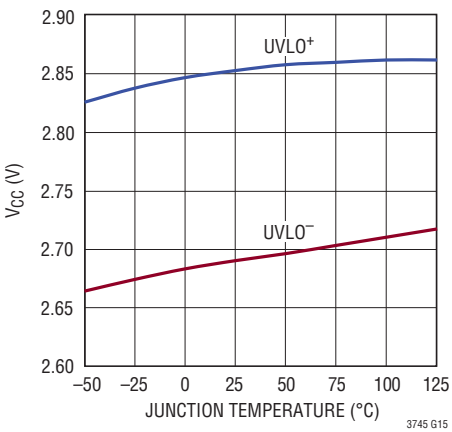
I_{VCC} vs V_{CC} – Shutdown Mode



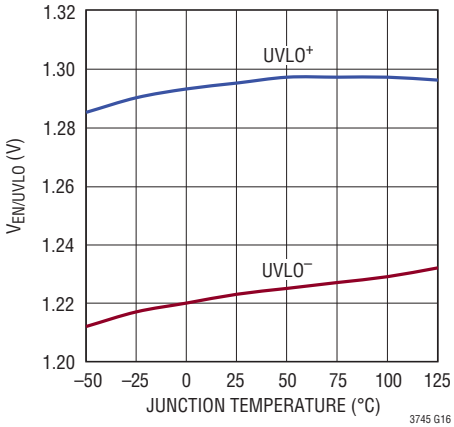
I_{VCC} vs V_{CC} – Channel Off, Data Off



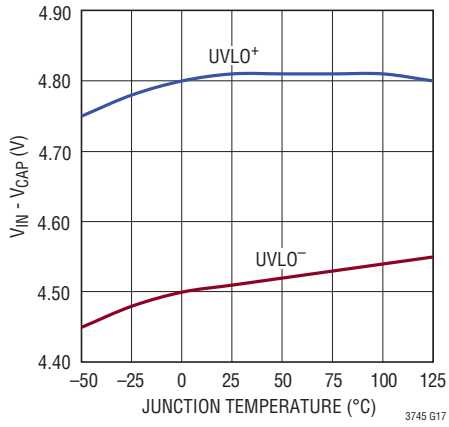
V_{CC} UVLO Threshold vs Temperature



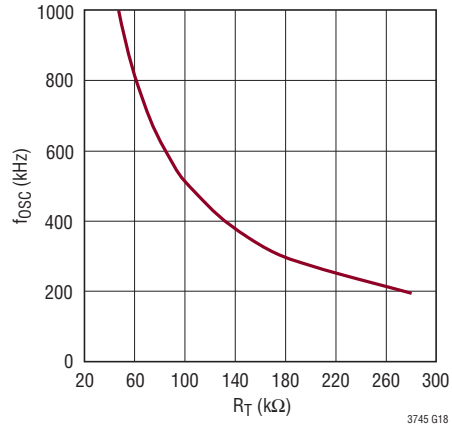
EN/UVLO UVLO Threshold vs Temperature



(V_{IN} - V_{CAP}) UVLO Threshold vs Temperature



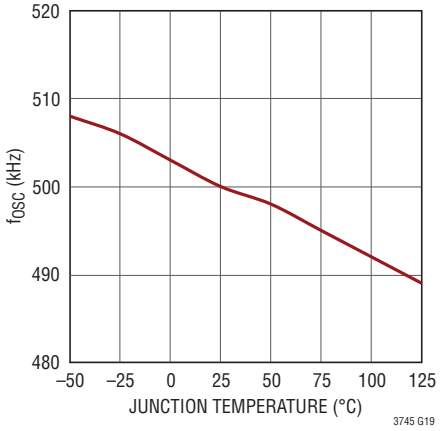
Oscillator Frequency f_{OSC} vs R_T



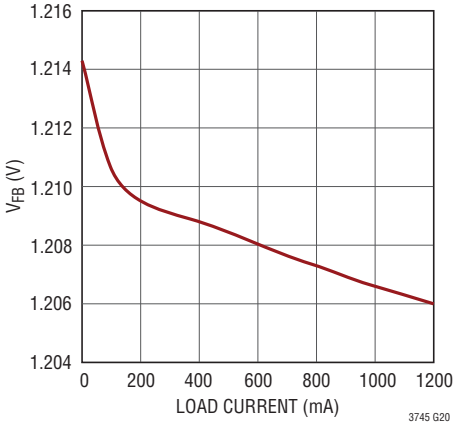
TYPICAL PERFORMANCE CHARACTERISTICS

T_A = 25°C, unless otherwise noted.

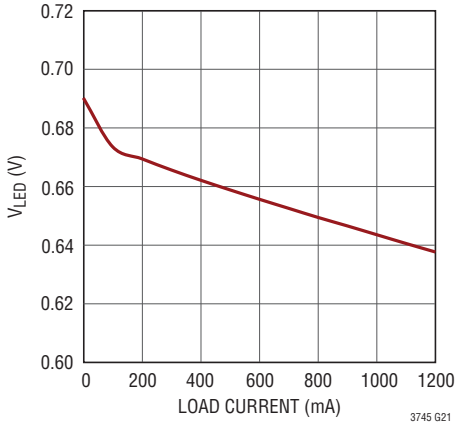
Oscillator Frequency f_{OSC} vs Temperature



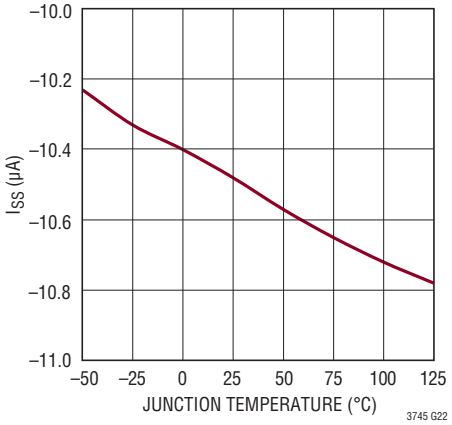
FB Regulation Voltage vs Load Current



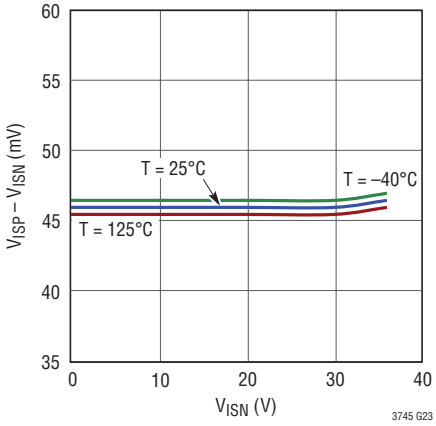
LED Regulation Voltage vs Load Current



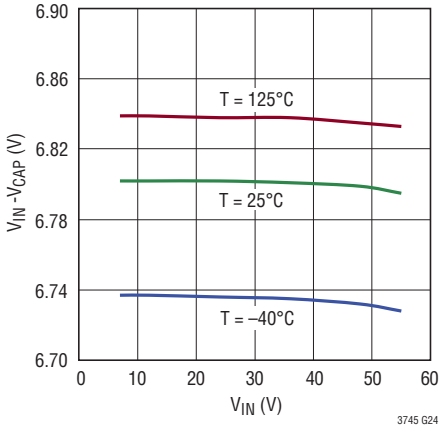
Soft-Start Charge Current I_{SS} vs Temperature



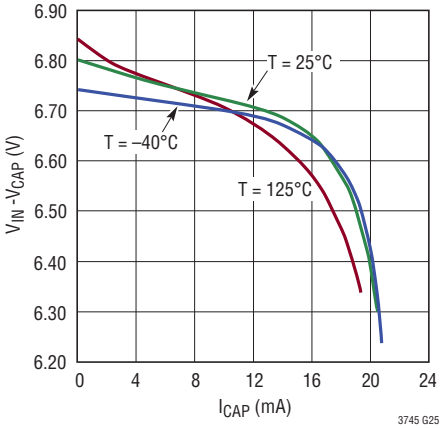
Current Sense Threshold vs V_{ISN}



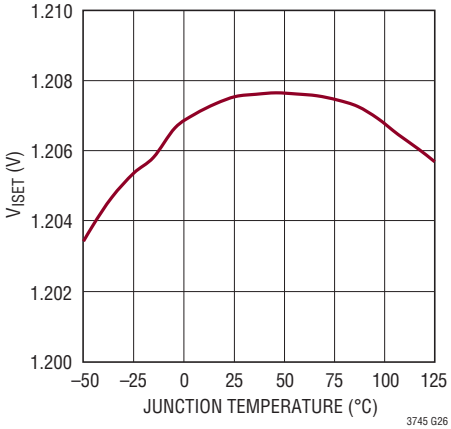
CAP Bias Voltage (V_{IN} - V_{CAP}) vs V_{IN}



CAP Bias Voltage (V_{IN} - V_{CAP}) vs I_{CAP}



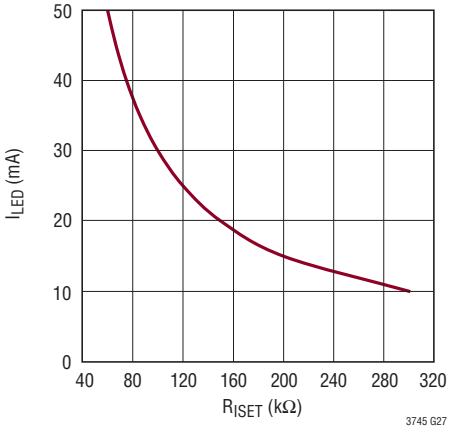
V_{ISET} Pin Voltage vs Temperature



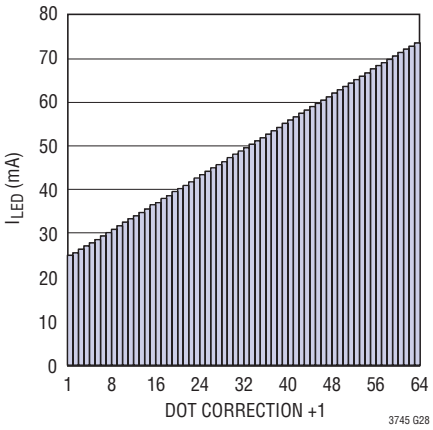
TYPICAL PERFORMANCE CHARACTERISTICS

T_A = 25°C, unless otherwise noted.

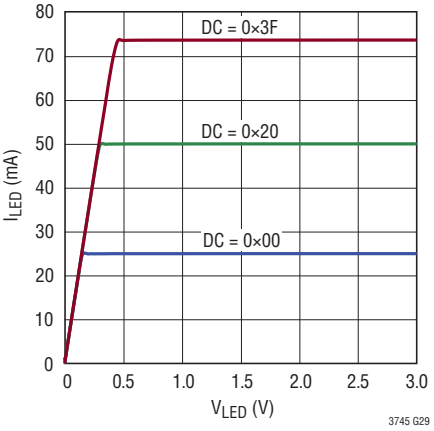
Nominal LED Current vs R_{ISET}



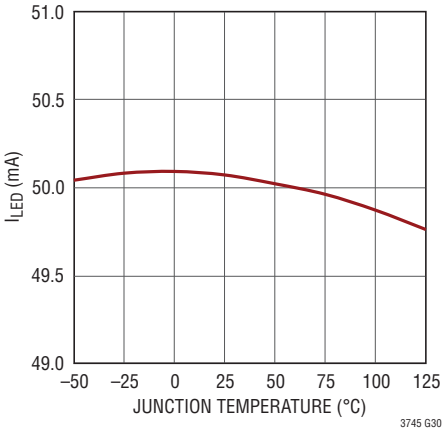
LED Current vs Dot Correction



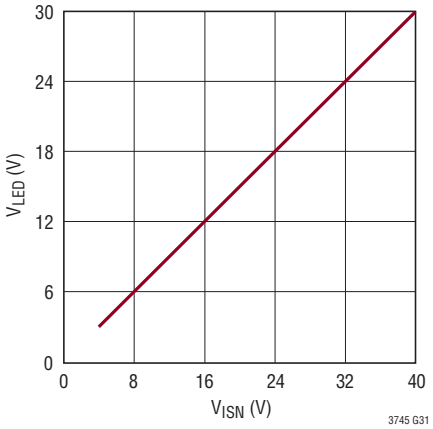
LED Current I_{LED} vs LED Voltage V_{LED}



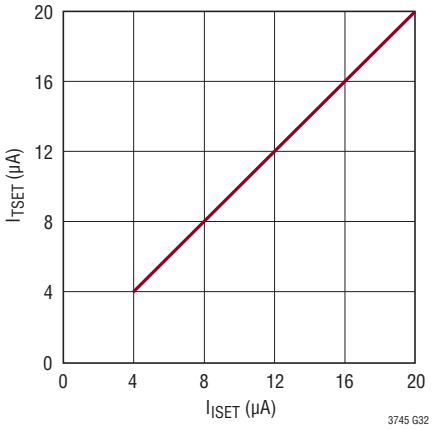
LED Current Variation I_{LED} vs Temperature



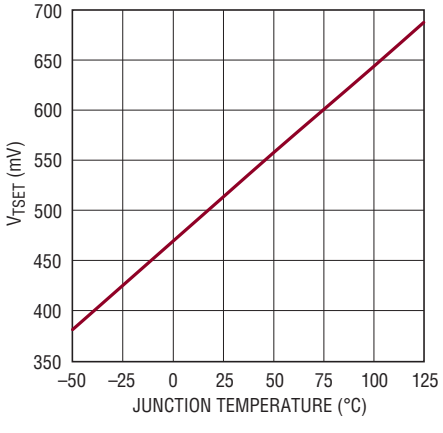
Short LED Threshold vs V_{ISN}



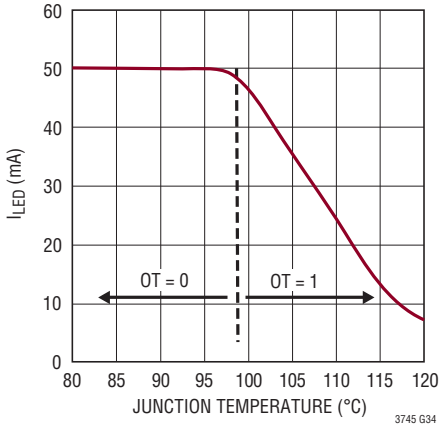
T_{SET} Current vs I_{SET} Current



T_{SET} Threshold vs Temperature



LED Current Derating vs Temperature



PIN FUNCTIONS

EN/UVLO (Pin 1): Enable and Undervoltage Lockout (UVLO) Pin. The pin can accept a digital input signal to enable or disable the chip. Tie to 0.35V or lower to shut down the chip or tie to 1.34V or higher for normal operation. This pin can also be connected to V_{IN} through a resistor divider to program a power input UVLO threshold. If both the enable and UVLO functions are not used, tie this pin to V_{CC} pin.

LED00 to LED15 (Pins 2 to 9, 22 to 29): LED Driver Output Pins. Connect the cathodes of LED strings to these pins.

GND (Pins 10, 12, 19, 21): Ground Pin.

SCKI (Pin 11): Serial Interface TTL/CMOS Logic Clock Input Pin.

SDI (Pin 13): Serial Interface TTL/CMOS Logic Data Input Pin.

LDI (Pin 14): Serial Interface TTL/CMOS Logic Latch Input Pin. An asynchronous input signal at this pin latches the serial data in the shift registers into the proper registers and the status information is ready to shift out with the coming clock pulses. See more details in the Operation section.

V_{CC} (Pin 15): Logic and Control Supply Pin. The pin powers serial data interface and internal control circuitry. Must be locally bypassed with a capacitor to ground.

PWMCK (Pin 16): Grayscale PWM Dimming TTL/CMOS Logic Clock Pin. Individual PWM dimming signal is generated by counting this clock pulse from zero to the bits in its 12-bit grayscale PWM register.

LDO (Pin 17): Serial Interface TTL/CMOS Logic Latch Output Pin.

SDO (Pin 18): Serial Interface TTL/CMOS Logic Data Output Pin.

SCKO (Pin 20): Serial Interface TTL/CMOS Logic Clock Output Pin.

SYNC (Pin 30): Switching Frequency Synchronization Pin. Synchronizes the internal oscillator frequency to an external clock applied to the SYNC pin. The SYNC pin is TTL/CMOS logic compatible. Tie to ground or V_{CC} if not used.

RT (Pin 31): Timing Resistor Pin. Programs the switching frequency from 200kHz to 1MHz. See Table 2 for the recommended R_T values for common switching frequencies.

SS (Pin 32): Soft-Start Pin. Placing a capacitor here programs soft-start timing to limit inductor inrush current during startup. The soft-start cycle will not begin until all the V_{CC}, EN/UVLO, and (V_{IN} - V_{CAP}) voltages are higher than their respective UVLO thresholds.

FB (Pin 33): Feedback Pin. The pin is regulated to the internal bang-gap reference 1.205V during startup and precharging phases. Connect to a resistor divider from the buck converter output to program the maximum LED bus voltage. See more details in the Applications Information section.

ISN (Pin 34): Negative Inductor Current Sense Pin. The pin is connected to one terminal of the external inductor current sensing resistor and the buck converter output supplying parallel LED channels.

ISP (Pin 35): Positive Inductor Current Sense Pin. The pin is connected to the inductor and the other terminal of the external inductor current sensing resistor.

CAP (Pin 36): V_{IN} Referenced Regulator Supply Capacitor Pin. The pin holds the negative terminal of an internal V_{IN} referenced 6.8V linear regulator used to bias the gate driver circuitry. Must be locally bypassed with a capacitor to V_{IN}.

GATE (Pin 37): Gate Driver Pin. The pin drives an external P-channel power MOSFET with a typical peak current of 1A. Connect this pin to the gate of the power MOSFET with a short and wide PCB trace to minimize trace inductance.

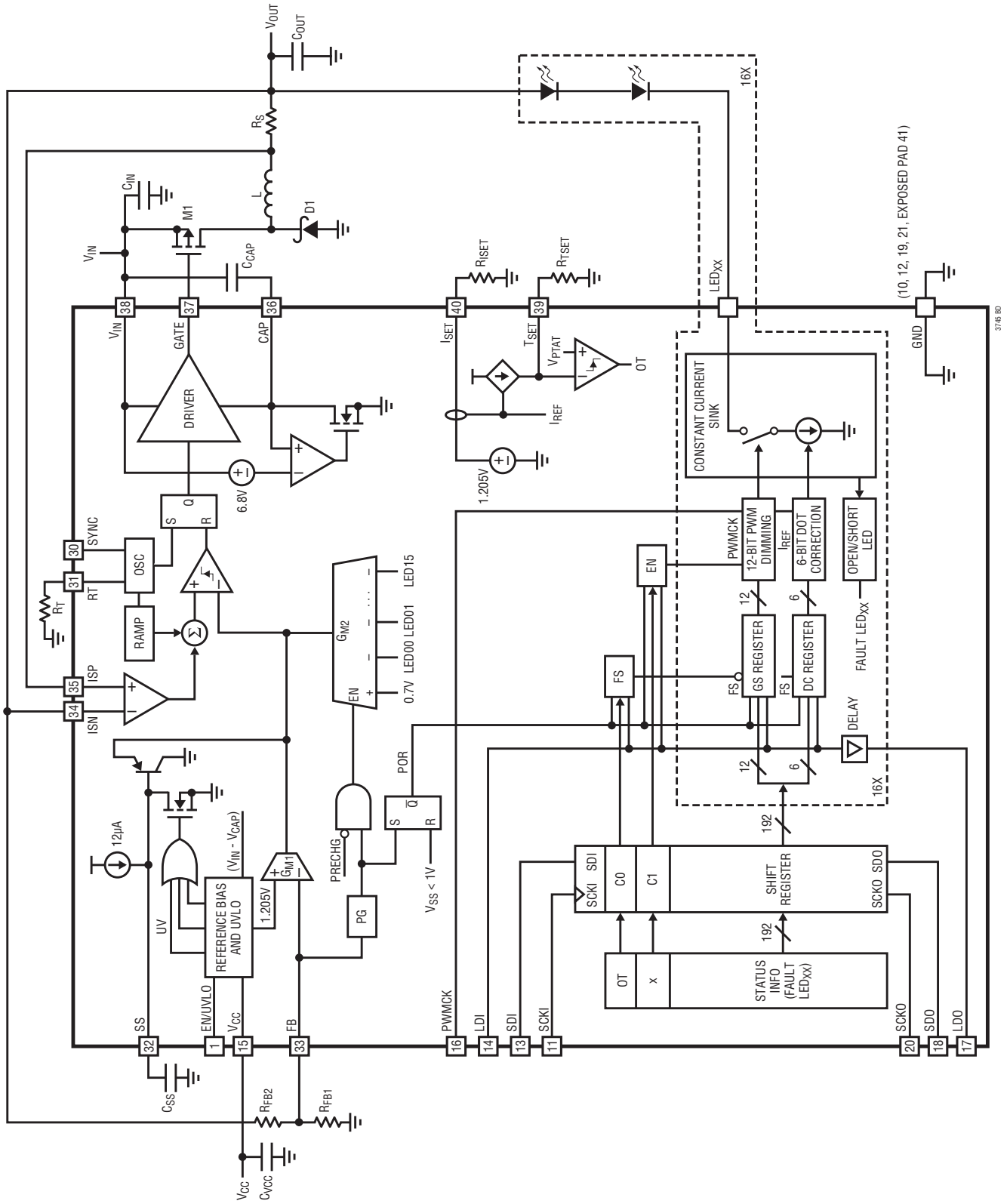
V_{IN} (Pin 38): Power Input Supply Pin. Must be locally bypassed with a capacitor to ground.

T_{SET} (Pin 39): Temperature Threshold Setting Pin. A resistor to ground programs overtemperature threshold. See more details in the Applications Information section.

I_{SET} (Pin 40): Nominal LED Current Setting Pin. A resistor to ground programs the nominal LED current for all the channels. See more details in the Applications Information section.

Exposed Pad (Pin 41): Ground Pin. Must be soldered to a continuous copper ground plane to reduce die temperature and to increase the power capability of the device.

BLOCK DIAGRAM



OPERATION

The LT3745 integrates a single constant-frequency current-mode nonsynchronous buck controller with sixteen linear current sinks. The buck controller generates an adaptive output LED bus voltage to supply parallel LED strings and the sixteen linear current sinks regulate and modulate individual LED strings. Its operation is best understood by referring to the Block Diagram.

Start-Up

The LT3745 enters shutdown mode and drains almost zero current when the EN/UVLO pin is lower than 0.35V. Once the EN/UVLO pin is above 0.35V, the part starts to wake up internal bias currents, generate various references, and charge the capacitor C_{CAP} towards 6.8V regulation voltage. This V_{IN} referenced voltage regulator (V_{IN} - V_{CAP}) will supply the internal gate driver circuitry driving an external P-channel MOSFET in normal operation. The LT3745 remains in undervoltage lockout (UVLO) mode as long as any one of the EN/UVLO, V_{CC}, and (V_{IN} - V_{CAP}) UVLO flags is high. Their UVLO thresholds are typically 1.31V, 2.89V, and 4.9V, respectively. After all the UVLO flags are cleared, the buck controller starts to switch, and the soft-start SS pin is released and charged by a 12µA current source, thereby smoothly ramping up the inductor current and the output LED bus voltage.

Power-on-Reset (POR)

During start-up, an internal power-on-reset (POR) high signal blocks the input signals to the serial data interface and resets all the internal registers except the 194-bit shift register. The 1-bit frame select (FS) register, 1-bit enable LED channel (EN) register, individual 12-bit grayscale (GS) registers, and individual 6-bit dot correction (DC) registers are all reset to zero. Thus all the LED channels are turned off initially with the default grayscale (0x000) and dot correction (0x00) setting. Once the part completes its soft-start (i.e., the SS pin voltage is higher than 1V) and the output LED bus voltage is power good (i.e., within 5% of its FB programmed regulation level), the POR signal goes low to allow the input signals to the serial data interface. Any fault triggering the soft-start will generate another POR high signal and reset internal registers again.

Serial Data Interface

The LT3745 has a 30MHz, fully-buffered, skew-balanced, cascadable serial data interface. The interface uses a novel 6-wire (LDI, SCKI, SDI, LDO, SCKO, and SDO) topology and can be connected to microcontrollers, digital signal processors (DSPs), or field programmable gate arrays (FPGAs).

In a conventional 4-wire topology shown in Figure 1, the LDI and SCKI signals need global routing while the SDI signal only needs local routing between chips. Depending on the number of chips in cascade and the size of system PCB board, external clock-tree type buffers with corresponding driving capability are needed for both the LDI and SCKI signals to minimize signal skews. The propagation delay caused by the buffer insertion on the SCKI signal yields

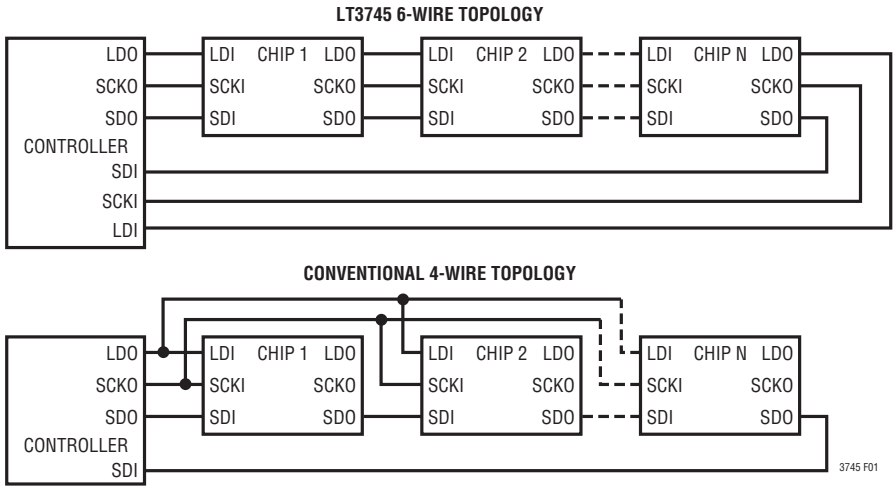


Figure 1. LT3745 6-Wire Topology vs Conventional 4-Wire Topology

OPERATION

the clock skew between the SCKI and SDI signals, which usually requires the customer end to balance it. Since both the SDI and SDO signals require the same SCKI signal to send and receive, the propagation delay between the SDI and SDO signals limits the number of chips in cascade and the series data interface clock frequency.

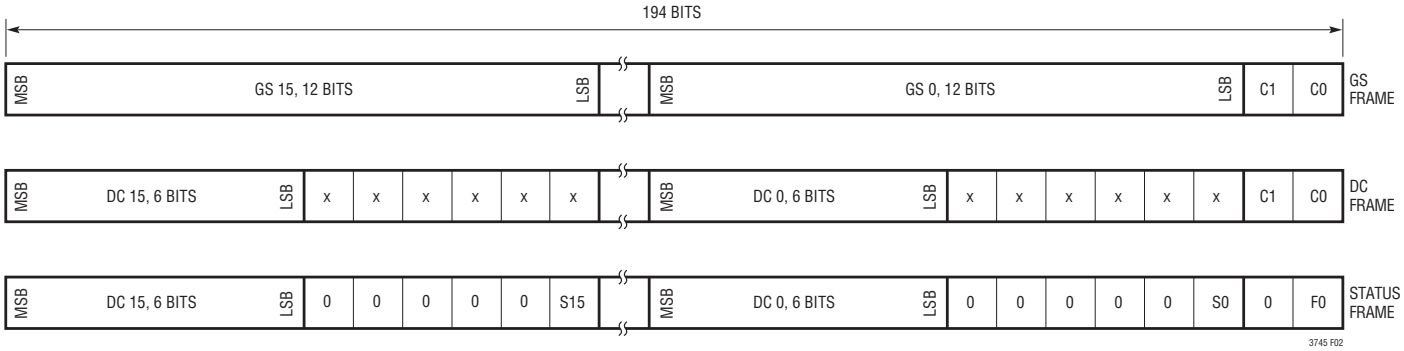
The novel 6-wire topology eliminates the need for global routing and buffer insertion for the LDI and SCKI signals. Instead, it provides the LDO and SCKO signals along with the SDO signal to drive the next chip. The skew inside the chip among the LDI, SCKI, and SDI signals is balanced internally. The skew outside the chip among the LDO, SCKO, and SDO signals can be easily balanced by parallel routing these three signals between chips. The SDI signal is sent with the SCKI signal, and the SDO signal is received with the SCKO signal. A slight duty cycle change between the SCKI and SCKO signals may occur due to the process variation, supply voltage and operating temperature. This duty cycle change results from the difference in propagation delays of the positive and negative edges of the SCKI/SCKO signals and will affect the maximum number of cascadable chips, depending on the SCKI speed. In summary, the 6-wire topology extends the maximum number of cascadable chips, boosts the series data interface clock frequency, eliminates the need for buffer insertion for global signals, and offers an easy PCB layout. In a low-speed application with a small number of cascaded chips, the 6-wire topology can be simplified to the 4-wire topology by ignoring the LDO and SCKO outputs.

Figure 2 shows two serial data input SDI frames (GS frame and DC frame) and one serial data output SDO frame (status frame). All the frames have the same 194-bit in length and are transmitted with the MSB first and the LSB last. The SDI frames are sent with the SCKI signal and the SDO frame is received with the SCKO signal. The C0 bit (frame select) determines any SDI frame to be either a GS frame (C0 = 0) or a DC frame (C0 = 1), and the C1 bit (EN) enables (C1 = 1) or disables (C1 = 0) all the LED channels. The status frame reads back the T_{SET} pin resistor-programmable over-temperature flag and individual open/short LED fault flags, as well as the individual 6-bit DC setting.

Inside the part, there are one 194-bit shift register SR[0:193], one 1-bit frame select (FS) register, one 1-bit enable LED channel (EN) register, sixteen 12-bit grayscale (GS) registers, sixteen 6-bit dot correction (DC) registers, one 1-bit over temperature (OT) flag register, and sixteen 1-bit LED fault flag registers. The input of the 194-bit shift register, i.e., the input of the first bit SR[0], is connected to the SDI signal. The output of the 194-bit shift register, i.e., the output of the last bit SR[193] is connected to the SDO signal. The SCKI signal shifts the SDI frame (GS or DC frame) in and the SCKO signal shift the SDO frame (status frame) out of the 194-bit shift register with their rising edges. The LDI high signal latches the SDI frame (GS or DC frame) from the 194-bit shift register into corresponding FS, EN, GS or DC registers, and loads the SDO frame (status frame) from the OT and LED fault flag registers to the 194-bit shift register at the same time. The LDO signal is a buffered version of the LDI signal with certain delay added to match the delay between the SCKI and SCKO signals. Therefore, a daisy-chain type loop communication with simultaneous writing and reading capability is implemented.

Figure 3 illustrates the timing relation among serial input and serial output signals in more detail. One DC frame followed by another GS frame is sent through the LDI, SCKI, and SDI signals. At the same time, two status frames are received through the LDO, SCKO, and SDO signals. The rising edges of the SCKI signal shift a frame of 194-bit data at the SDI pin into the 194-bit shift register SR[0:193]. After 194 clock cycles, all the 194-bit data sit in the right place waiting for the LDI signal. An asynchronous LDI high signal latches the 1-bit FS register, 1-bit EN register, and individual 12-bit GS registers (when FS = 0) or 6-bit DC registers (when FS = 1) for each channel. At the same time, a frame of status information, including over temperature flag and individual open/short LED fault flags, is parallel loaded into the 194-bit shift register and will be shifted out with the coming clock cycles.

OPERATION



COMMAND REGISTER:

C1: ENABLE LED CHANNELS - ENABLE = 1, DISABLE = 0
C0: FRAME SELECT - GS FRAME = 0, DC FRAME = 1

STATUS REGISTER:

S0-S15: LED 0-15 FAULT - FAULT = 1, OK = 0
F0: OT - OVER TEMPERATURE = 1, OK = 0

Figure 2. Serial Data Frame Format

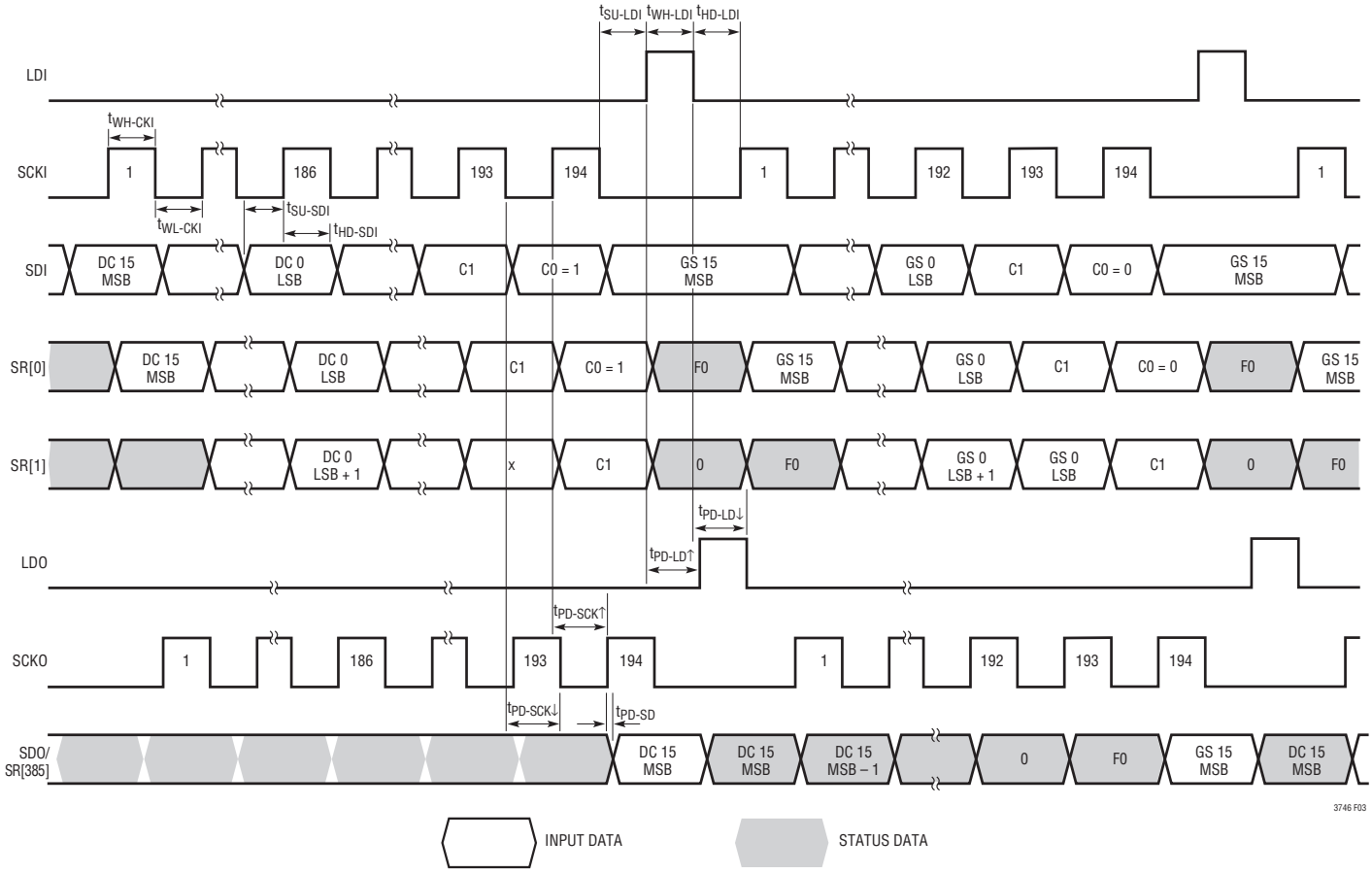


Figure 3. Serial Data Input and Output Timing Chart

OPERATION

Constant Current Sink

Each LED channel has a local constant current sink regulating its own LED current independent of the LED bus voltage V_{OUT}. The recommended LED pin voltage ranges from 0.8V to 3V. As shown in the Typical Performance Characteristics I_{LED} vs V_{LED} curves, the LED current I_{LED} has the best load regulation when the LED pin voltage V_{LED} sits above 0.5V. A lower LED bus voltage V_{OUT} may not regulate all the LED channels across temperature, current, and manufacturing variation, while a higher LED bus voltage V_{OUT} will force a higher LED pin voltage across the current sink, thereby dissipating more power inside the part. See more details about the choice of the LED bus voltage and the power dissipation calculation in the Application Information section.

Dot Correction and Grayscale Digital-to-Analog Conversion

The resistor on the I_{SET} pin programs the nominal LED current (10mA to 50mA) for all the channels. Individual LED channel can be adjusted to a different current setting by its own 6-bit dot correction register. The adjustable LED current ranges from 0.5X to 1.5X of the nominal LED current in 63 linear steps. See more details about setting nominal LED current and dot correction in the Applications Information section.

In addition to the dot correction current adjustment, individual LED channels can also be modulated by their own grayscale PWM dimming signal. To achieve a better performance, all the grayscale PWM dimming signals are synchronized to the same frequency with no phase shift between rising edges. Each constant current sink is enabled or disabled when its grayscale PWM dimming signal goes high or low. This periodic grayscale PWM dimming signal is generated by its own 12-bit grayscale register with a duty cycle from 0/4096 to 4095/4096 and a period equal to 4096 PWMCK clock cycles.

The generation of the grayscale PWM dimming signal is best understood by referring to Figure 4. After EN = 1 is set, the first rising edge of the PWMCK signal will increase the internal 12-bit grayscale counter from zero to one and turn on all the LED channels with grayscale value not zero. Each following rising edge of the PWMCK signal increases the grayscale counter by one. Any LED channel will be turned off when its 12-bit grayscale register value is equal to the value in the grayscale counter. To generate a 100% duty cycle for all the grayscale PWM dimming signals, the PWMCK signal can be paused before counting to the value in any individual 12-bit grayscale registers. Setting EN = 0 will reset the grayscale counter to zero and turn off all the LED channels immediately.

Dual-Loop Analog *OR* Control

The switching frequency can be programmed from 200kHz to 1MHz with the resistor connected to the RT pin and it can be synchronized to an external clock using the SYNC pin. Each switching cycle starts with the gate driver turning on the external P-channel MOSFET M1 and the inductor current is sampled through the sense resistor R_S between the ISP and ISN pins. This current is amplified and added to a slope compensation ramp signal, and the resulting sum is fed into the positive terminal of the PWM comparator. When this voltage exceeds the level at the negative terminal of the PWM comparator, the gate driver turns off M1. The level at the negative terminal of the PWM comparator is set by either of two error amplifiers G_{M1} and G_{M2}. In this dual-loop analog *OR* control, the FB loop G_{M1} regulates the FB pin voltage to 1.205V and the LED loop G_{M2} regulates the minimum *active* LED pin voltage (LED00 to LED15) to 0.7V. In the startup phase, the G_{M2} is disabled and the output LED bus voltage is regulated towards the feedback resistor programmed LED bus voltage. This FB programmed voltage defines the maximum LED bus voltage and should be programmed high enough to supply the worst-case LED string across temperature, current, and manufacturing variation.

OPERATION

Adaptive-Tracking-Plus-Precharging

Higher system efficiency and faster transient response are two highly anticipated specifications in an individually-modulated multi-channel LED driver chip. The LT3745 uses a patent pending adaptive-tracking-plus-precharging technique to achieve both of them simultaneously.

Besides 16 internal grayscale PWM dimming signals, the part also generates another internal precharging signal PRECHG. As shown in Figure 4, the PRECHG signal divides any grayscale PWM dimming cycle into two phases: tracking phase when PRECHG = 0 and precharging phase when PRECHG = 1. During each grayscale PWM dimming cycle – 4096 PWMCK clock cycles, the PRECHG signal stays low for the first 3584 clock cycles (7/8 of the grayscale PWM dimming period) and goes high for the rest 512 clock cycles (1/8 of the grayscale PWM dimming period). In the event of all the LED channels being not *active* (i.e., either fault or off) before the 3585th PWMCK clock, the PRECHG signal will go high immediately.

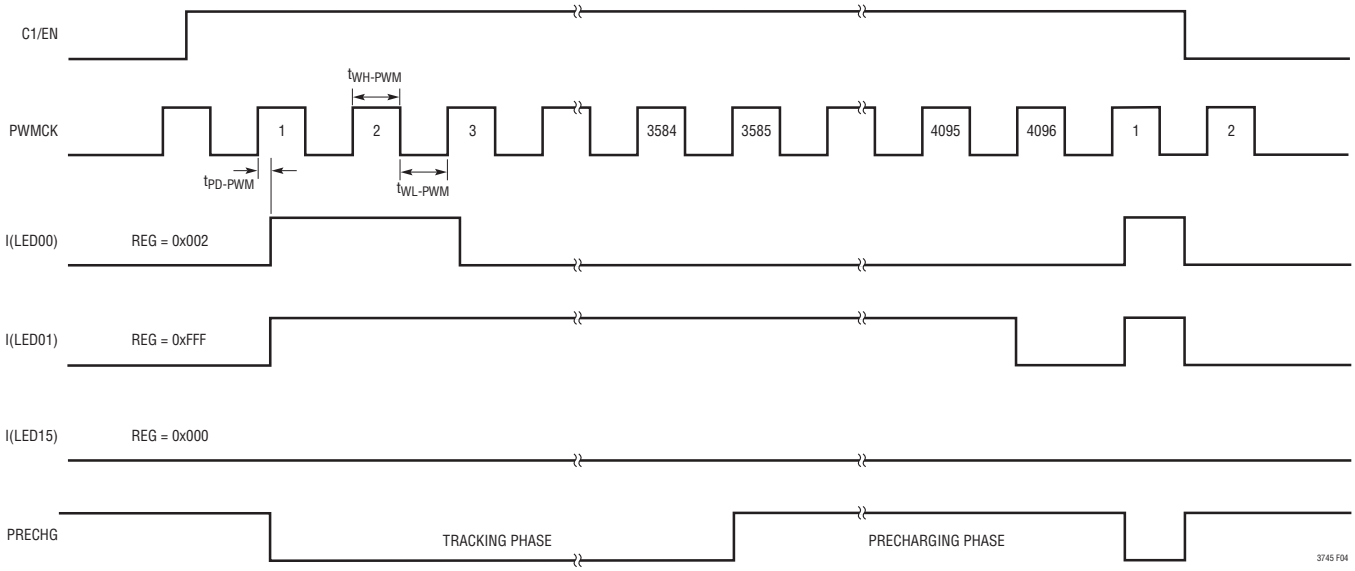


Figure 4. Grayscale PWM Dimming and Precharging Signal Timing Chart

OPERATION

To better explain the operation of the adaptive-tracking-plus-precharging technique, a simplified application system with 3-channel LED array is presented in Figure 5. Each channel consists of a single LED with the forward voltage drop equal to 3.1V, 3.5V, and 3.9V, respectively. Three internal grayscale PWM dimming signals PWM1, PWM2, and PWM3 are used to modulate each LED channel.

At the beginning of each grayscale PWM dimming cycle, all three LED channels are turned on and the tracking phase starts with PRECHG = 0. The amplifier G_{M2} is enabled and takes the control from the amplifier G_{M1}, regulating the minimum *active* LED pin voltage to 0.7V. With the V_{LED3} equal to 0.7V, the output LED bus voltage is tracked to 4.6V. Subsequently, at a certain time instant t_1 when the third channel is turned off, the minimum *active* LED pin voltage goes to V_{LED2}, 1.1V. Then the amplifier G_{M2} tracks the output LED bus voltage down to 4.2V to maintain the minimum *active* LED pin voltage equal to 0.7V again. Similarly, at the next time instant t_2, the output LED bus voltage is tracked down to 3.8V. In this manner, the adaptive-tracking technique eliminates unnecessary power dissipation across the current sinks and yields superior system efficiency when compared to a constant 4.6V output voltage.

At a later time instant t_3 when the PRECHG signal goes high, the amplifier G_{M2} is disabled and gives the control back to the amplifier G_{M1}. The amplifier GM1 regulates the output LED bus voltage towards the FB programmed maximum value 4.6V to guarantee shorter minimum LED on-time for the next grayscale PWM dimming cycle. Without the precharging phase, the output LED bus voltage will stay at 3.8V before the next grayscale PWM dimming cycle, when all the 3 LED channels will be turned on again. At that time the 3.8V LED bus voltage is too low to keep all the LED channels in regulation, and the minimum LED on-time is greatly increased to accommodate the slow transient response of the switching buck converter charging the output capacitor from 3.8V to 4.6V. This adaptive-tracking-plus-precharging LED bus voltage technique simultaneously lowers the power dissipation in the LT3745 and maintains a shorter minimum LED on-time.

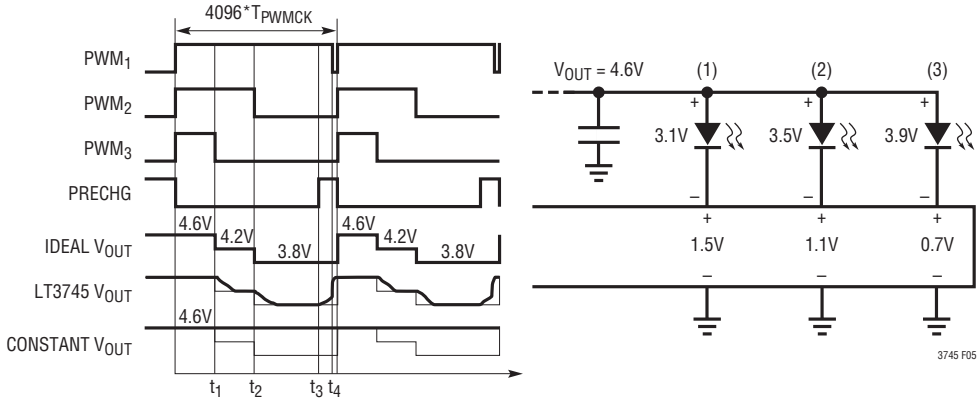


Figure 5. Adaptive-Tracking-Plus-Precharging LED Bus Voltage Technique

APPLICATIONS INFORMATION

Globally, the LT3745 converts a higher input voltage to a single lower LED bus voltage (V_{OUT}) supplying 16 parallel LED strings with the adaptive-tracking-plus-precharging technique. Locally, the part regulates and modulates the current of each string to an independent dot correction and grayscale PWM dimming setting sent by TTL/CMOS logic serial data interface. This Application Information section serves as a guideline of selecting external components (refer to the Block Diagram) and avoiding common pitfalls for the typical application.

Programming Maximum V_{OUT}

The adaptive-tracking-plus-precharging technique regulates V_{OUT} to its maximum value during the startup and precharging phases, and adaptively lowers the voltage to keep the minimum *active* LED pin voltage around 0.7V during the tracking phase. Therefore, the maximum V_{OUT} should be programmed high enough to keep all the LED pin voltages higher than 0.8V to maintain LED current regulation across temperature, current, and manufacturing variation. As a starting point, the maximum LED bus voltage, $V_{OUT(MAX)}$, can be calculated as:

$$V_{OUT(MAX)} = 0.8V + n \bullet V_{F(MAX)}$$

where n is the number of LED per string and $V_{F(MAX)}$ is the maximum LED forward voltage rated at the highest operating current and the lowest operating temperature.

The $V_{OUT(MAX)}$ is programmed with a resistor divider between the output and the FB pin. The resistor values are calculated as:

$$R_{FB2} = R_{FB1}\left(\frac{V_{OUT(MAX)}}{1.205V} - 1\right)$$

Tolerance of the feedback resistors will add additional errors to the output voltage, so 1% resistor values should be used. The FB pin output bias current is typically 120nA, so use of extremely high value feedback resistors could also cause bias current errors. A typical value for R_{FB1} is 10k.

V_{IN} Power Input Supply Range

The power input supply for the LT3745 can range from 6V to 55V, covering a wide variety of industrial power supplies. Another restriction on the minimum input voltage $V_{IN(MIN)}$ is the 2.1V minimum dropout voltage between the V_{IN} and ISN pins, and thus the $V_{IN(MIN)}$ is calculated as:

$$V_{IN(MIN)} = V_{OUT(MAX)} + 2.1V$$

Choosing Switching Frequency

Selection of the switching frequency is a trade-off between efficiency and component size. Low frequency operation improves efficiency by reducing MOSFET switching losses and gate charge losses. However, lower frequency operation requires larger inductor and capacitor values.

Another restriction on the switching frequency comes from the input and output voltage range caused by the minimum switch on and switch off-time. The highest switching frequency $f_{SW(MAX)}$ for a given application can be calculated as:

$$f_{SW(MAX)} = MIN\left(\frac{D_{MIN}}{t_{ON(MIN)}}, \frac{1-D_{MAX}}{t_{OFF(MIN)}}\right)$$

where the minimum duty cycle D_{MIN} and the maximum duty cycle D_{MAX} are determined by:

$$D_{MIN} = \frac{V_{OUT(MIN)} + V_D}{V_{IN(MAX)} + V_D} \text{ and } D_{MAX} = \frac{V_{OUT(MAX)} + V_D}{V_{IN(MIN)} + V_D}$$

$t_{ON(MIN)}$ is the minimum switch on-time (~200ns), $t_{OFF(MIN)}$ is the minimum switch off-time (~120ns), $V_{OUT(MIN)}$ is the minimum adaptive output voltage, $V_{IN(MAX)}$ is the maximum input voltage, and V_D is the catch diode forward voltage (~0.5V). The calculation of $f_{SW(MAX)}$ simplifies to:

$$f_{SW(MAX)} = MIN\left(5 \bullet \frac{V_{OUT(MIN)} + V_D}{V_{IN(MAX)} + V_D}, 8.33 \bullet \frac{V_{IN(MIN)} - V_{OUT(MAX)}}{V_{IN(MIN)} + V_D}\right) MHz$$

Obviously, lower frequency operation accommodates both extremely high and low V_{OUT} to V_{IN} ratios.

APPLICATIONS INFORMATION

Besides these common considerations, the specific application also plays an important role in switching frequency choice. In a noise-sensitive system, the switching frequency is usually chosen to keep the switching noise out of a sensitive frequency band.

Switching Frequency Setting and Synchronization

The LT3745 uses a constant switching frequency that can be programmed from 200kHz to 1MHz with a resistor from the RT pin to ground. Table 2 shows R_T values for common switching frequencies.

Table 2. Switching Frequency f_{SW} vs R_T Value

f_{SW} (kHz)	R_T * (kΩ)
200	280
300	182
400	133
500	105
600	84.5
700	71.5
800	60.4
900	53.6
1000	46.4

* Recommend 1% Standard Values

Synchronizing the LT3745 oscillator to an external frequency can be achieved using the SYNC pin. The square wave amplitude, compatible to TTL/CMOS logic, should have valleys that are below 0.6V and peaks that are above 2.4V. The synchronization frequency also ranges from 200kHz to 1MHz, in which the R_T resistor should be chosen to set the internal switching frequency around 20% below the synchronization frequency. In the case of 200kHz synchronization frequency, R_T = 348k is recommended. It is also important to note that when the synchronization frequency is much higher than the R_T programmed internal frequency, the internal slope compensation will be significantly reduced, which may trigger sub-harmonic oscillation at duty cycles greater than 50%.

Inductor Current Sense Resistor R_S and Current Limit

The current sense resistor, R_S, monitors the inductor current between the ISP and ISN pins, which are the inputs to the internal current sense amplifier. The common mode input voltage of the current sense amplifier ranges from 0V to (V_{IN} – 2.1V) or 36V absolute maximum value, whichever is lower. The current sense amplifier not only provides current information to form the current-mode control, but also a 46.5mV threshold. The 46.5mV threshold across the R_S resistor imposes an accurate current limit to protect both P-channel MOSFET M1 and catch diode D1, and also to prevent inductor current saturation. Good Kelvin sensing is required for accurate current limit. The R_S resistor value can be determined by:

$$I_{OUT(MAX)} = I_{L(MAX)} - \frac{\Delta I_L}{2}$$

where the maximum inductor current $I_{L(MAX)}$ is set by:

$$I_{L(MAX)} = \frac{46.5mV}{R_S}$$

$I_{OUT(MAX)}$ is the maximum output load current, and ΔI_L is the inductor peak-to-peak ripple current. Allowing adequate margin for ripple current and external component tolerances, R_S can be estimated as:

$$R_S = \frac{35mV}{I_{OUT(MAX)}}$$

APPLICATIONS INFORMATION

Inductor Selection

The critical parameters for selection of an inductor are inductance value, DC or RMS current, saturation current, and DCR resistance. For a given input and output voltage, the inductor value and switching frequency will determine the peak-to-peak ripple current, ΔI_L. The ΔI_L value usually ranges from 20% to 50% of the maximum output load current, $I_{OUT(MAX)}$. Lower values of ΔI_L require larger and more costly inductors; higher values of ΔI_L increase the peak currents and the inductor core loss. An inductor current ripple of 30% to 40% offers a good compromise between inductor performance and inductor size and cost. However, for high duty cycle applications, a ΔI_L value of ~20% should be used to prevent sub-harmonic oscillation due to insufficient slope compensation.

The largest inductor ripple current occurs at the highest V_{IN}. To guarantee that the ripple current stays below the specified maximum, the inductor value should be chosen according to the following equation:

$$L \geq \frac{V_{OUT} + V_D}{V_{IN(MAX)} + V_D} \bullet \frac{V_{IN(MAX)} - V_{OUT}}{f_{SW} \bullet \Delta I_L}$$

The inductor DC or RMS current rating must be greater than the maximum output load current $I_{OUT(MAX)}$ and its saturation current should be higher than the maximum inductor current $I_{L(MAX)}$. To achieve high efficiency, the DCR resistance should be less than 0.1Ω, and the core material should be intended for high frequency applications.

Power MOSFET Selection

Important parameters for the external P-channel MOSFET M1 include drain-to-source breakdown voltage ($V_{(BR)DSS}$), maximum continuous drain current ($I_{D(MAX)}$), maximum gate-to-source voltage ($V_{GS(MAX)}$), total gate charge (Q_G), drain-to-source on resistance ($R_{DS(ON)}$), reverse transfer capacitance (C_{RSS}). The MOSFET $V_{(BR)DSS}$ specification should exceed the maximum voltage across the source to the drain of the MOSFET, which is $V_{IN(MAX)}$ plus V_D. The $I_{D(MAX)}$ should exceed the peak inductor current, $I_{L(MAX)}$. Since the gate driver circuit is supplied by the internal 6.8V V_{IN} referenced regulator, the $V_{GS(MAX)}$ rating should be at least 10V.

Each switching cycle the MOSFET is switched off and on, a packet of gate charge Q_G is transferred from the V_{IN} pin to the GATE pin, and then from the GATE pin to the CAP pin. The resulting dQ_G/dt is a current that must be supplied to the C_{CAP} capacitor by the internal regulator. The maximum 22mA current capability of the internal regulator limits the maximum $Q_{G(MAX)}$ it can deliver to:

$$Q_{G(MAX)} = \frac{22mA}{f_{SW}}$$

Therefore, the Q_G at V_{GS} = 6.8V from the MOSFET data sheet should be less than $Q_{G(MAX)}$.

For maximum efficiency, both $R_{DS(ON)}$ and C_{RSS} should be minimized. Lower $R_{DS(ON)}$ means less conduction loss while lower C_{RSS} reduces transition loss. Unfortunately, $R_{DS(ON)}$ is inversely related to C_{RSS}. Thus balancing the conduction loss with the transition loss is a good criterion in selecting a MOSFET. For applications with higher V_{IN} voltages (≥24V) a lower C_{RSS} is more important than a low $R_{DS(ON)}$.

Catch Diode Selection

The catch diode D1 carries load current during the switch off-time. Important parameters for the catch diode includes peak repetitive reverse voltage (V_{RRM}), forward voltage (V_F), and maximum average forward current ($I_{F(AV)}$). The diode V_{RRM} specification should exceed the maximum reverse voltage across it, i.e., $V_{IN(MAX)}$. A fast switching Schottky diode with lower V_F should be used to yield lower power loss and higher efficiency.

In continuous conduction mode, the average current conducted by the catch diode is calculated as:

$$I_{D(AVG)} = I_{OUT} \bullet (1 - D)$$

The worst-case condition for the diode is when V_{OUT} is shorted to ground with maximum V_{IN} and maximum I_{OUT} at present. In this case, the diode must safely conduct the maximum load current almost 100% of the time. To improve efficiency and to provide adequate margin for short circuit operation, a Schottky diode rated to at least the maximum output current is recommended.

APPLICATIONS INFORMATION

C_{IN}, C_{VCC}, and C_{CAP} Capacitor Selection

A local input bypass capacitor C_{IN} is required for buck converters because the input current is pulsed with fast rise and fall times. The input capacitor selection criteria are based on the voltage rating, bulk capacitance, and RMS current capability. The capacitor voltage rating must be greater than $V_{IN(MAX)}$. The bulk capacitance determines the input supply ripple voltage and the RMS current capability is used to keep from overheating the capacitor.

The bulk capacitance is calculated based on maximum input ripple, ΔV_{IN}:

$$C_{IN} = \frac{D_{MAX} \bullet I_{OUT(MAX)}}{\Delta V_{IN} \bullet f_{SW}}$$

ΔV_{IN} is typically chosen at a level acceptable to the user. 100mV is a good starting point. For ceramic capacitors, only X5R or X7R type should be used because they retain their capacitance over wider voltage and temperature ranges than other types such as Y5V or Z5U. Aluminum electrolytic capacitors are a good choice for high voltage, bulk capacitance due to their high capacitance per unit area.

The capacitor RMS current is:

$$I_{CIN(RMS)} = I_{OUT} \bullet \sqrt{\frac{V_{OUT} \bullet (V_{IN} - V_{OUT})}{V_{IN}^2}}$$

If applicable, calculate at the worst-case condition, $V_{IN} = 2 \bullet V_{OUT}$. The capacitor RMS current rating specified by the manufacturer should exceed the calculated $I_{CIN(RMS)}$. Due to their low ESR, ceramic capacitors are a good choice for high voltage, high RMS current handling. Note that the ripple current ratings from aluminum electrolytic capacitor manufacturers are based on 2000 hours of life. This makes it advisable to further derate the capacitor or to choose a capacitor rated at a higher temperature than required.

For a larger high voltage capacitor value, the combination of aluminum electrolytic capacitors and ceramic capacitors is an economical approach. Multiple capacitors may also be paralleled to meet size or height requirements in the design. Locate the capacitor very close to the MOSFET switch and the catch diode, and use short, wide PCB traces to minimize parasitic inductance.

The general discussion above also applies to the capacitor C_{VCC} at the V_{CC} pin and the capacitor C_{CAP} between the V_{IN} and CAP pins. Typically, a 10µF 10V-rated ceramic capacitor for C_{VCC} and a 0.47µF 16V-rated ceramic capacitor for C_{CAP} should be sufficient.

C_{OUT} Capacitor Selection

The output capacitor has two essential functions. Along with the inductor, it filters the square wave generated by the LT3745 to produce the DC output containing a controlled voltage ripple. It also stores energy to satisfy load transients and to stabilize the dual-loop operation. Thus the selection criteria for C_{OUT} are based on the voltage rating, the equivalent series resistance ESR, and the bulk capacitance. As always, choose the C_{OUT} with a voltage rating greater than $V_{OUT(MAX)}$.

The LT3745 utilizes the output as the dominant pole to stabilize the dual loop operation, so the C_{OUT} value determines the unity gain frequency f_{UGF}, which is set around 1/10 of the switching frequency. To stabilize the FB loop during the startup and precharging phases and the LED loop during the tracking phase, a low ESR capacitor (tens of mΩ) should be used and its minimum C_{OUT} is calculated as:

$$C_{OUT} = MAX\left(\frac{0.25}{R_S \bullet f_{UGF}}, \frac{1.5}{V_{OUT(MAX)} \bullet R_S \bullet f_{UGF}}\right)$$

The adaptive-tracking-plus-precharging technique moves the V_{OUT} with the grayscale PWM dimming frequency to improve system efficiency, choosing a ceramic capacitor as the C_{OUT} inevitably generates acoustic noise due to the piezo effect of the ceramic material. In an acoustic noise sensitive application, low ESR tantalum or aluminum capacitors are preferred. When choosing a capacitor, look carefully through the data sheet to find out what the actual capacitance is under operating conditions (applied voltage and temperature). A physically larger capacitor, or one with a higher voltage rating, may be required.

APPLICATIONS INFORMATION

Undervoltage Lockout (UVLO) and Shutdown

LT3745 has three UVLO thresholds with hysteresis for the EN/UVLO, V_{CC}, and CAP pins. The part will remain in UVLO mode not switching until all the EN/UVLO, V_{CC}, and (V_{IN} - V_{CAP}) voltages pass their respective typical thresholds (1.31V, 2.89V, and 4.9V). As shown in Figure 6, the EN/UVLO pin can be controlled in two different ways. The EN/UVLO pin can accept a digital input signal to enable or disable the chip. Tie to 0.35V or lower to shut down the chip or tie to 1.34V or higher for normal operation. This pin can also be connected to a resistor divider between V_{IN} and ground to program a power input V_{IN} UVLO threshold. After R_{UV1} is selected, R_{UV2} can be calculated by:

$$R_{UV2} = R_{UV1} \bullet \left(\frac{V_{IN(ON)}}{1.31V} - 1 \right)$$

where $V_{IN(ON)}$ is the power input voltage above which the part goes into normal operation. It is important to check the EN/UVLO pin voltage not to exceed its 6V absolute maximum rating:

$$V_{IN(MAX)} \bullet \frac{R_{UV1}}{R_{UV1} + R_{UV2}} < 6V$$

Soft-Start

During soft-start, the SS pin voltage smoothly ramps up inductor current and output voltage. The effective voltage range of SS pin is from 0V to 1V. Therefore, the typical soft-start period is:

$$t_{SS} = \frac{C_{SS} \bullet 1V}{12\mu A}$$

where C_{SS} is the capacitor connected at SS pin and 12µA is the soft-start charge current. Whenever a UVLO or thermal shutdown occurs, the SS pin will be discharged and the part will stop switching until the UVLO event has disappeared and the SS pin has reached it reset threshold, 0.35V. The part then initiates a new soft-start cycle.

Setting Nominal LED Current

The nominal LED current is defined as the average LED current across 16-channel when all the individual dot correction registers are set to 0x20. The nominal LED current is programmed by a single resistor, R_{ISET}, between the I_{SET} pin and ground. The voltage at the I_{SET} pin, V_{ISET}, is trimmed to an accurate 1.205V, generating a current

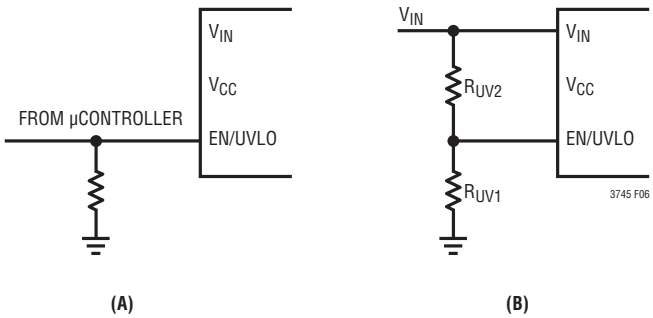


Figure 6. Methods of Controlling the EN/UVLO Pin

APPLICATIONS INFORMATION

inversely proportional to R_{ISET}. The nominal LED current, $I_{LED(NOM)}$, can be calculated as:

$$I_{LED(NOM)} = \frac{V_{ISET}}{R_{ISET}} \bullet 2500$$

$I_{LED(NOM)}$ must be set between 10mA and 50mA. Typical R_{ISET} resistor values for various nominal LED currents are listed in Table 3.

Table 3. Nominal LED Current $I_{LED(NOM)}$ vs. R_{ISET} Value

$I_{LED(NOM)}$ (mA)	R_{ISET} * (kΩ)
10	301
20	150
30	100
40	75
50	60.4

* Recommend 1% Standard Values

Setting Dot Correction

The LT3745 can adjust the LED current for each channel independently. This fine current adjustment, also called dot correction, is mainly used to calibrate the brightness deviation between LED channels. The 6-bit (64 steps) dot correction setting adjusts each LED current from 0.5X to 1.5X of the nominal LED current according to:

$$I_{LEDn} = I_{LED(NOM)} \bullet \left(\frac{DC_n + 32}{64} \right)$$

where I_{LEDn} is the nth LED current and DC_n is the nth programmed dot correction setting (DC_n = 0 to 63). The fine current step over the nominal LED current gives an excellent resolution:

$$\frac{\Delta I_{LED}}{I_{LED(NON)}} = \frac{1}{64} \approx 1.56\%$$

which enhances the relative LED current match accuracy if used as calibration.

Setting Grayscale

Although adjusting the LED current changes its luminous intensity, or brightness, it will also affect the color matching between LED channels by shifting the chromaticity coordinate. The best way to adjust the brightness is to control the amount of LED on-/off-time by pulse width modulation (PWM).

The LT3745 can adjust the brightness for each channel independently. The 12-bit grayscale PWM dimming results in 4096 linear brightness steps from 0% to 99.98%. The brightness level GS_n% for channel n can be calculated as:

$$GS_n\% = \frac{GS_n}{4096} \bullet 100\%$$

where GS_n is the nth programmed grayscale setting (GS_n = 0 to 4095).

Open/Short LED Fault

The LT3745 has individual LED fault diagnostic circuitry that detects both open and short LED faults for each channel. The open LED fault is defined as any LED string is open or disconnected from the circuit; and the short LED fault is defined as any LED string is shorted across itself. The open LED flag is set if the LED pin voltage is lower than 0.35V (typical) during on status with initial 500ns blanking. The short LED flag is set if the LED pin voltage is higher than 75% of the LED bus voltage V_{OUT} any time. If one LED channel is shorted across itself, the channel will be turned off to eliminate unnecessary power dissipation. The function can also be used to disable LED channels by connecting their LED pins to the output directly. Both the open and short LED flags are combined to set the LED fault bits (S0 to S15) in the status frame to 1.

APPLICATIONS INFORMATION

Thermal Protection

The LT3745 has two over temperature thresholds: one is the fixed internal thermal shutdown and the other one is programmed by a resistor, R_{TSET}, between the T_{SET} pin and ground. When the junction temperature exceeds 165°C, the part will enter thermal shutdown mode, shut down serial data interface, turn off LED channels, and stop switching. After the junction temperature drops below 155°C, the part will initiate a new soft-start.

When the R_{TSET} is placed at the T_{SET} pin, a current equal to the current flowing through the R_{ISET} passes the R_{TSET}, generating a voltage V_{TSET} at the T_{SET} pin, which is calculated as:

$$V_{TSET} = 1.205V \bullet \frac{R_{TSET}}{R_{ISET}}$$

Then the V_{TSET} is compared to an internal proportional-to-absolute-temperature voltage V_{PTAT},

$$V_{PTAT} = 1.72mV \bullet (T_J + 273.15)$$

where T_J is the LT3745 junction temperature in °C. When V_{PTAT} is higher than V_{TSET}, an overtemperature flag OT = 1 is set. Once the R_{TSET} programmed temperature is exceeded, the part will also gradually derate the nominal LED current $I_{LED(NOM)}$ to limit the total power dissipation without interrupting its normal operation.

Cascading Devices and Determining Serial Data Interface Clock

In a large LCD backlighting or LED display system, multiple LT3745 chips can be easily cascaded to drive all the LED strings. The LT3745 adopts a 6-wire topology, which balances the internal clock skew and matches the external trace capacitance with an easy PCB layout.

The minimum serial data interface clock frequency f_{SCKI} for a large display system can be calculated as:

$$f_{SCKI} = N_{LT3745} \bullet 194 \bullet f_{REFRESH}$$

where N_{LT3745} is the number of LT3745 chips and $f_{REFRESH}$ is the refresh rate of the whole system.

Calculating Power Dissipation

The total power dissipation inside the chip can be calculated as:

$$P_{TOTAL} = V_{IN} \bullet (I_{VIN} + f_{SW} \bullet Q_G) + V_{CC} \bullet I_{VCC} + \sum_{n=0}^{15} GS_n\% \bullet I_{LEDn} \bullet V_{LEDn}$$

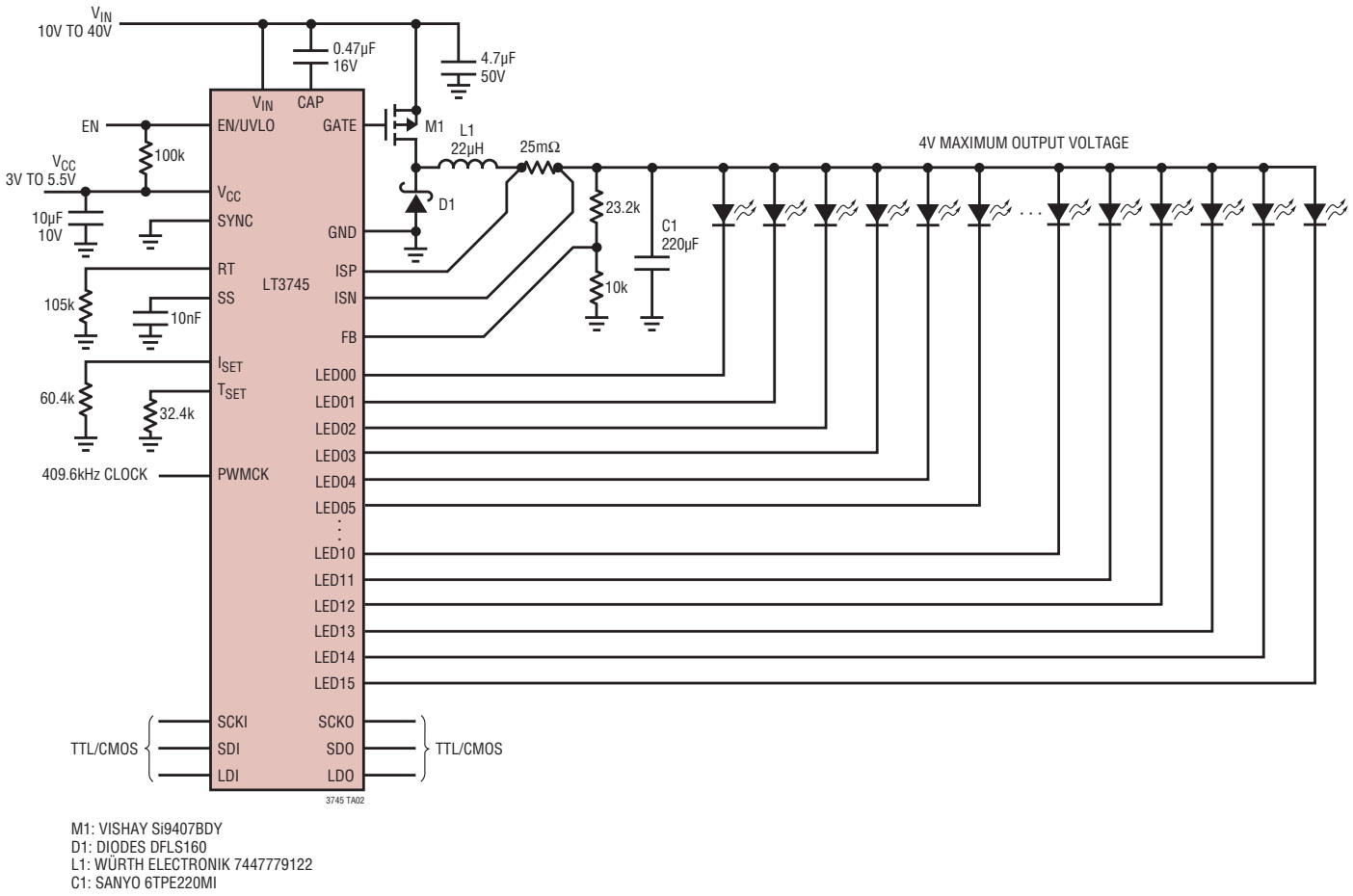
where I_{VIN} is the power input V_{IN} quiescent current, I_{VCC} is the V_{CC} supply current, and V_{LEDn} is the LED pin voltage for channel n.

From the total power dissipation P_{TOTAL}, the junction temperature T_J can be calculated as:

$$T_J = T_A + P_{TOTAL} \bullet \theta_{JA}$$

Keep T_J below the maximum operating junction temperature 125°C.

TYPICAL APPLICATION

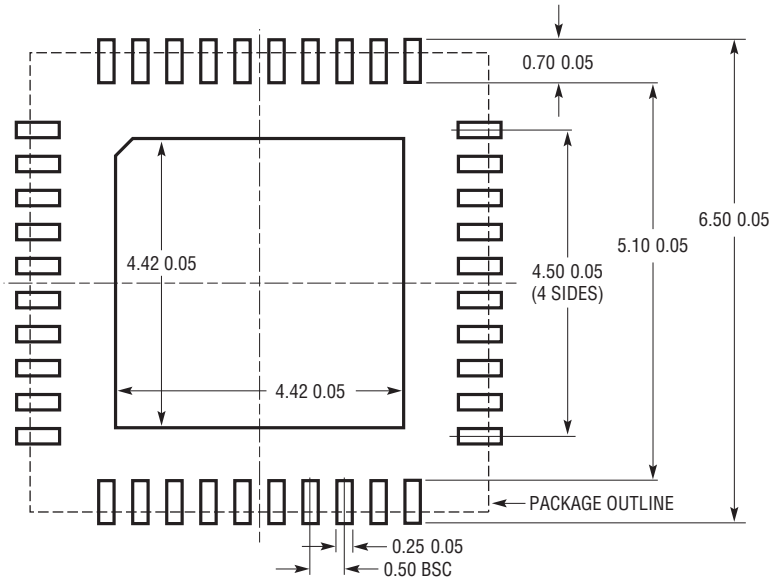


M1: VISHAY Si9407BDY
D1: DIODES DFLS160
L1: WÜRTH ELECTRONIK 7447779122
C1: SANYO 6TPE220MI

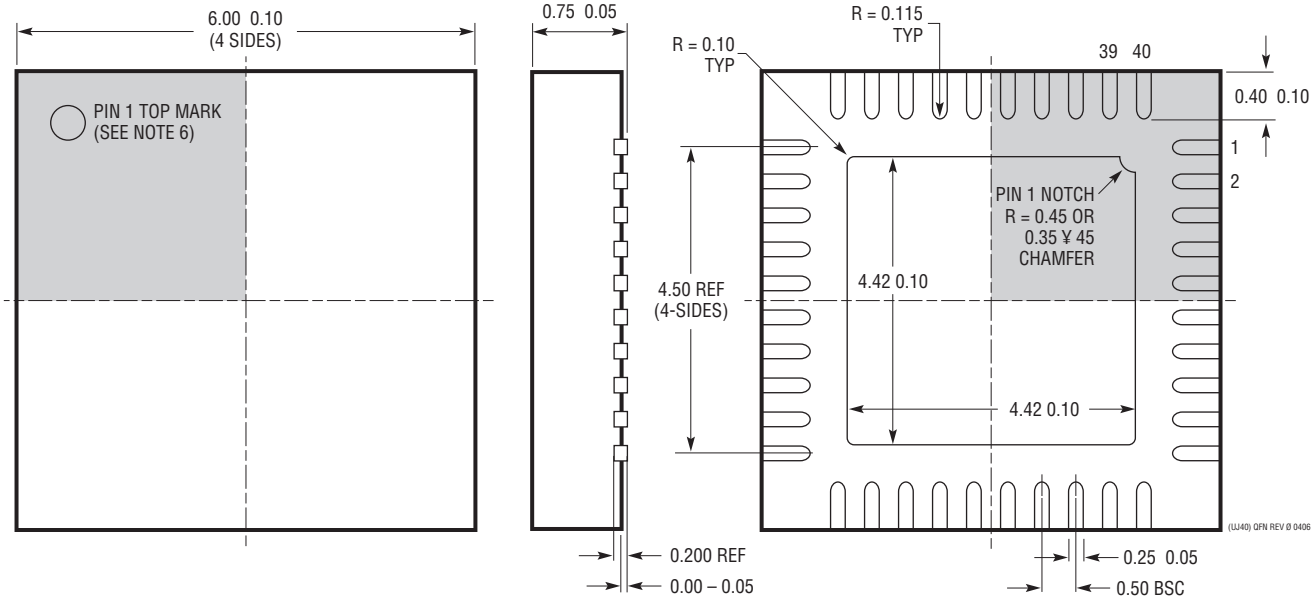
Figure 7. 16-Channel LED Driver, 500kHz Buck, 1 LED 25mA to 75mA per Channel, 100Hz 12-Bit Dimming

PACKAGE DESCRIPTION

UJ Package
40-Lead Plastic QFN (6mm × 6mm)
(Reference LTC DWG # 05-08-1728 Rev Ø)



RECOMMENDED SOLDER PAD PITCH AND DIMENSIONS
APPLY SOLDER MASK TO AREAS THAT ARE NOT SOLDERED



BOTTOM VIEW—EXPOSED PAD

NOTE:
1. DRAWING IS A JEDEC PACKAGE OUTLINE VARIATION OF (WJJD-2)
2. DRAWING NOT TO SCALE
3. ALL DIMENSIONS ARE IN MILLIMETERS
4. DIMENSIONS OF EXPOSED PAD ON BOTTOM OF PACKAGE DO NOT INCLUDE MOLD FLASH. MOLD FLASH, IF PRESENT, SHALL NOT EXCEED 0.20mm ON ANY SIDE, IF PRESENT
5. EXPOSED PAD SHALL BE SOLDER PLATED
6. SHADED AREA IS ONLY A REFERENCE FOR PIN 1 LOCATION ON THE TOP AND BOTTOM OF PACKAGE

Information furnished by Linear Technology Corporation is believed to be accurate and reliable. However, no responsibility is assumed for its use. Linear Technology Corporation makes no representation that the interconnection of its circuits as described herein will not infringe on existing patent rights.

TYPICAL APPLICATION

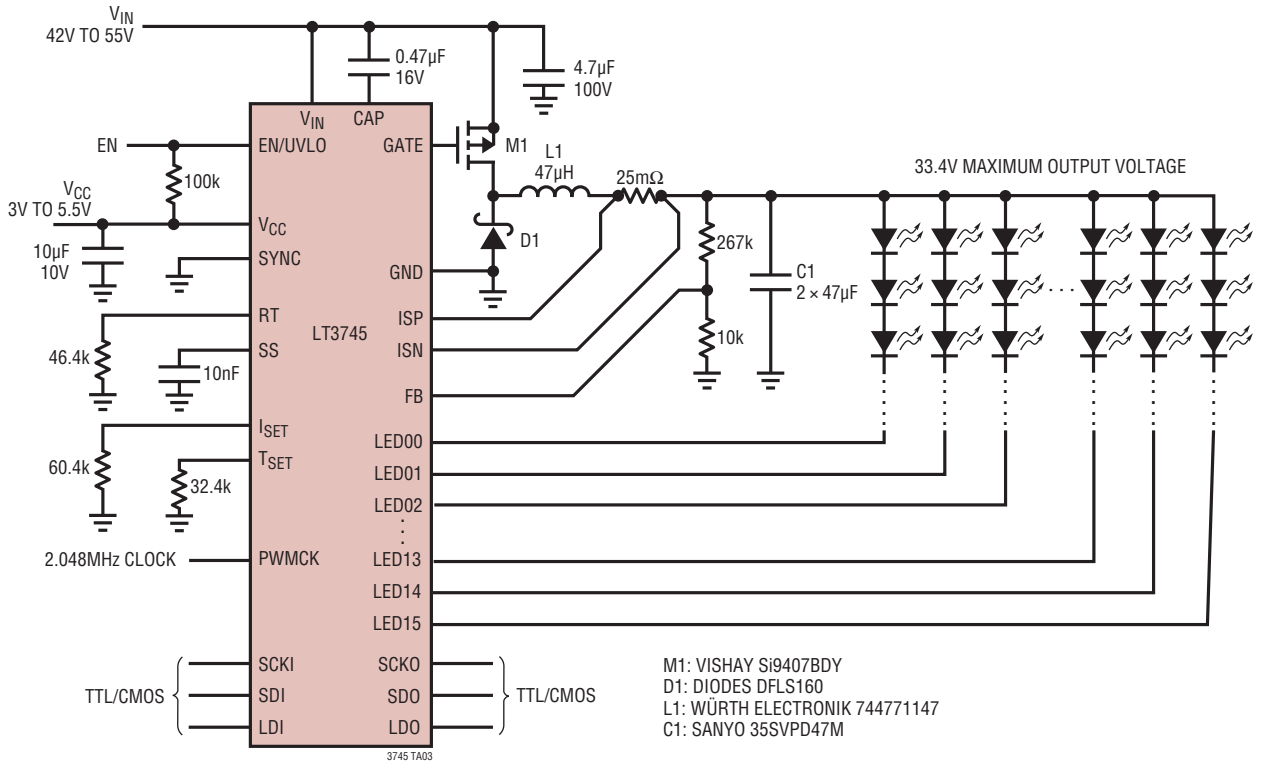


Figure 8. 16-Channel LED Driver, 1MHz Buck, 10 LEDs, 25mA to 75mA per Channel, 500Hz 12-Bit Dimming

RELATED PARTS

PART NUMBER	DESCRIPTION	COMMENTS
LT3746	32-Channel 20mA LED Driver with Buck Controller	V_{IN}: 6V to 55V, $V_{OUT(MAX)}$ = 13V, 6-Bit Dot Correction Current Adjustment, 12-Bit Grayscale Dimming, 5mm × 9mm QFN Package
LT3476	Quad Output 1.5A, 2MHz High Current LED Driver with 1,000:1 Dimming	V_{IN}: 2.8V to 16V, $V_{OUT(MAX)}$ = 36V, True Color PWM™ Dimming = 1000:1, I_{SD} < 10µA, 5mm × 7mm QFN-10 Package
LT3486	Dual 1.3A , 2MHz High Current LED Driver	V_{IN}: 2.5V to 24V, $V_{OUT(MAX)}$ = 36V, True Color PWM Dimming = 1000:1, I_{SD} < 1µA, 5mm × 3mm DFN-16 TSSOP-16E Package
LT3496	Triple Output 750mA, 2.1 MHz High Current LED Driver with 3,000:1 Dimming	V_{IN}: 3V to 30V, $V_{OUT(MAX)}$ = 60V, True Color PWM Dimming = 3000:1, I_{SD} < 1µA, 4mm × 5mm QFN-28 Package
LT3595	45V, 2.5MHz 16-Channel Full Featured LED Driver	V_{IN}: 4.5V to 45V, $V_{OUT(MAX)}$ = 45V, True Color PWM Dimming = 5000:1, I_{SD} < 1µA, 5mm × 9mm QFN-56 Package
LT3598	44V, 1.5A, 2.5MHz Boost 6-Channel 30mA LED Driver	V_{IN}: 3V to 40V, $V_{OUT(MAX)}$ = 44V, True Color PWM Dimming = 1000:1, I_{SD} < 1µA, 4mm × 4mm QFN-24 Package
LT3599	44V, 2A, 2.5MHz Boost 4-Channel 120mA LED Driver	V_{IN}: 3V to 40V, $V_{OUT(MAX)}$ = 44V, True Color PWM Dimming = 1000:1, I_{SD} < 1µA, 4mm × 4mm QFN-24 Package
LT3754	60V, 1MHz Boost 16-Channel 50mA LED Driver with True Color 3,000:1 PWM Dimming and 2.8% Current Matching	V_{IN}: 4.5V to 40V, $V_{OUT(MAX)}$ = 60V, True Color PWM Dimming = 3000:1, I_{SD} < 1µA, 5mm × 5mm QFN-32 Package
LT3756/-1	High Side 100V, 1MHz LED Controller with True Color 3,000:1 PWM Dimming	V_{IN}: 6V to 100V, $V_{OUT(MAX)}$ = 100V, True Color PWM Dimming = 3000:1, I_{SD} < 1µA, 3mm × 3mm QFN-16 MSOP-16E Package
LT3760	60V, 1MHz Boost 8-Channel 100mA LED Driver with True Color 3,000:1 PWM Dimming and 2.8% Current Matching	V_{IN}: 4.5V to 40V, $V_{OUT(MAX)}$ = 60V, True Color PWM Dimming = 3000:1, I_{SD} < 1µA, TSSOP-28E Package

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