Dual Full-Bridge Piezo Driver with 900mA Boost Converter

FEATURES

- 2.7V to 10V Input Voltage Range
- 900mA Boost Converter
- Dual Full-Bridge Piezo Drivers
- Programmable Switching Frequency from 500kHz to 2.25MHz
- Synchronizable Up to 2.5MHz
- Soft-Start
- Separate Enable for Each Piezo Driver and Boost Converter
- Available in a 4mm × 4mm 20-Pin QFN Package

APPLICATIONS

- Piezo Motor Drive

DESCRIPTION

The LT®3572 is a highly integrated dual Piezo motor driver capable of driving two Piezo motors at up to 40V from a 5V supply. Each Piezo driver can be independently turned on or off along with the boost converter.

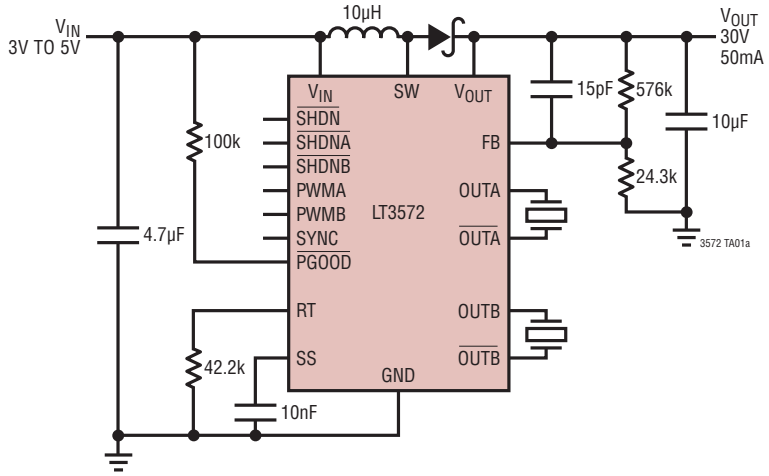
The boost regulator has a soft-start capability that limits the inrush current at start-up. The boost regulator switching frequency is set by an external resistor or the frequency can be synchronized by an external clock. A $\overline{\text{PGOOD}}$ pin indicates when the output of the boost converter is in regulation and the Piezo drivers are allowed to start switching.

The LT3572 is available in a (4mm × 4mm) 20-pin QFN package.

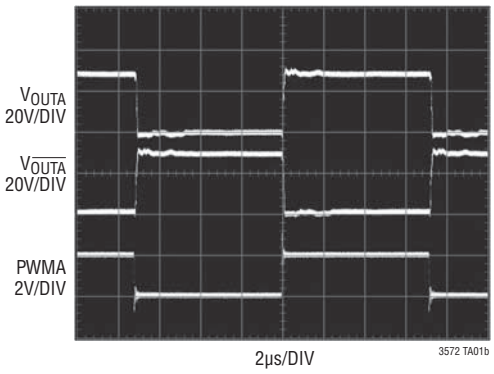
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TYPICAL APPLICATION

Dual Piezo Driver



Response Driving Piezo Motor at 70kHz

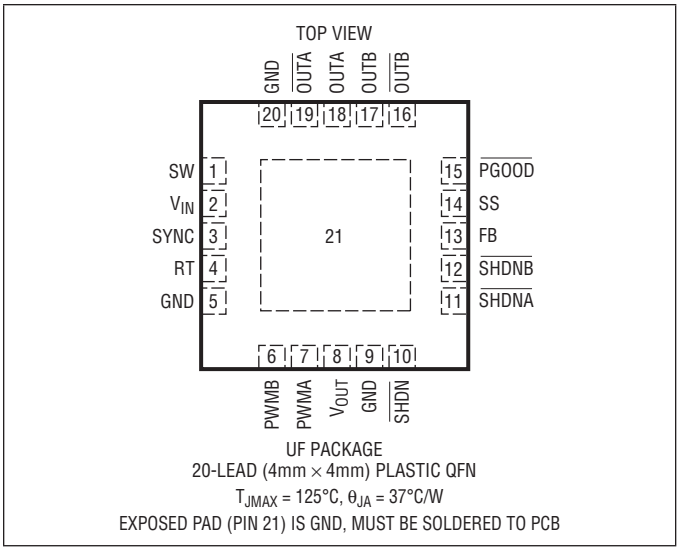


ABSOLUTE MAXIMUM RATINGS

(Note 1)

V_{OUT} Voltage 40V
OUTA, $\overline{OUTA}$, OUTB, $\overline{OUTB}$ Voltage 40V
SW Voltage 42V
RT, SS, SYNC 2V
FB 3V
All Other Pins 10V
Maximum Junction Temperature ..... 125°C
Operating Temperature Range (Note 2) ..... –40°C to 85°C
Storage Temperature Range ..... –65°C to 125°C

PIN CONFIGURATION



UF PACKAGE
20-LEAD (4mm × 4mm) PLASTIC QFN
T_{JMAX} = 125°C, θ_{JA} = 37°C/W
EXPOSED PAD (PIN 21) IS GND, MUST BE SOLDERED TO PCB

ORDER INFORMATION

LEAD FREE FINISH	TAPE AND REEL	PART MARKING	PACKAGE DESCRIPTION	TEMPERATURE RANGE
LT3572EUF#PBF	LT3572EUF#TRPBF	3572	20-Lead (4mm × 4mm) Plastic DFN	–40°C to 85°C

Consult LTC Marketing for parts specified with wider operating temperature ranges.
Consult LTC Marketing for information on non-standard lead based finish parts.

For more information on lead free part marking, go to: http://www.linear.com/leadfree/
For more information on tape and reel specifications, go to: http://www.linear.com/tapeandreel/

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. V_{IN} = 5V, $V_{\overline{SHDNA}}$= $V_{\overline{SHDNB}}$ = $V_{\overline{SHDN}}$ = 5V, unless otherwise noted.

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Minimum Operating Voltage		●		2.5	2.7	V
V_{IN} Quiescent Current	V_{FB} = 1.3V			3.4	4	mA
V_{IN} Shutdown Current	$V_{\overline{SHDN}}$ = $V_{\overline{SHDNA}}$ = $V_{\overline{SHDNB}}$ = 0V			0	1	µA
$\overline{SHDN}$ Pin Threshold			0.3		1.5	V
$\overline{SHDNA}$ Pin Threshold			0.3		1.5	V
$\overline{SHDNB}$ Pin Threshold			0.3		1.5	V
$\overline{SHDN}$ Pin Bias Current	$V_{\overline{SHDN}}$ = 5V, $V_{\overline{SHDNA}}$ = 0V, $V_{\overline{SHDNB}}$ = 0V $V_{\overline{SHDN}}$ = 0V, $V_{\overline{SHDNA}}$ = 0V, $V_{\overline{SHDNB}}$ = 0V			8 0.1	15 1	µA µA
$\overline{SHDNA}$ Pin Bias Current	$V_{\overline{SHDN}}$ = 0V, $V_{\overline{SHDNA}}$ = 5V, $V_{\overline{SHDNB}}$ = 0V $V_{\overline{SHDN}}$ = 0V, $V_{\overline{SHDNA}}$ = 0V, $V_{\overline{SHDNB}}$ = 0V			8 0.1	15 1	µA µA
$\overline{SHDNB}$ Pin Bias Current	$V_{\overline{SHDN}}$ = 0V, $V_{\overline{SHDNA}}$ = 0V, $V_{\overline{SHDNB}}$ = 5V $V_{\overline{SHDN}}$= 0V, $V_{\overline{SHDNA}}$ = 0V, $V_{\overline{SHDNB}}$ = 0V			8 0.1	15 1	µA µA

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. V_{IN} = 5V, $V_{\overline{SHDNA}}$= $V_{\overline{SHDNB}}$ = $V_{\overline{SHDN}}$ = 5V, unless otherwise noted.

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
PWMA Pin Threshold			0.3		1.5	V
PWMB Pin Threshold			0.3		1.5	V
$\overline{PGOOD}$ Rising Threshold	(Note 3)	●	1.12	1.16	1.19	V
$\overline{PGOOD}$ Falling Threshold	(Note 4)	●	1.01	1.04	1.065	V
$\overline{PGOOD}$ Resistance		●		1	3	kΩ
Switching Frequency	RT = 75.0kΩ RT = 13.0kΩ	● ●	425 1.9	500 2.25	575 2.6	kHz MHz
Maximum Duty Cycle	RT = 75.0kΩ RT = 13.0kΩ	● ●	95 85			% %
Synchronization Frequency			575		2500	kHz
SYNC Pin Thresholds	(Note 5)		0.3		1.5	V
SS Current				4.5		µA
FB Pin Voltage		●	1.195	1.225	1.255	V
FB Pin Voltage Line Regulation	V_{IN} = 2.5V to 10V			0.01	0.05	%/V
FB Pin Bias Current	V_{FB} = 1.225V (Note 6)			50	200	nA
SW Current Limit	(Note 7)		0.9	1.3	1.7	A
SW V_{CESAT}	I_{SW} = 800mA			310	450	mV
SW Leakage Current	SW = 40V			0.2	5	µA
OUTx Rise Time	C = 2.2nF, V_{OUT} = 30V (Note 8)				120	ns
OUTx Fall Time	C = 2.2nF, V_{OUT} = 30V (Note 8)				120	ns

Note 1: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to any Absolute Maximum Rating condition for extended periods may affect device reliability and lifetime.

Note 2: The LT3572 is guaranteed to meet specified performance from 0°C to 70°C operating junction temperature. Specifications over the –40°C to 85°C operating junction temperature range are assured by design, characterization and correlation with statistical process controls.

Note 3: Rising threshold voltage on FB pin that pulls $\overline{PGOOD}$ low.

Note 4: Falling threshold voltage on FB pin that causes a high impedance on $\overline{PGOOD}$.

Note 5: Minimum pulse width is 100ns. Maximum off pulse width is 100ns.

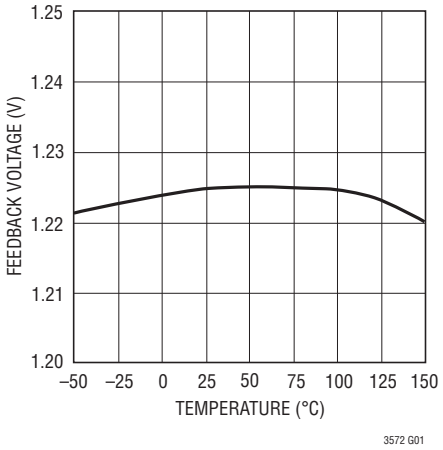
Note 6: Current flows into the pin.

Note 7: Current limit guaranteed by design and/or correlation to static test.

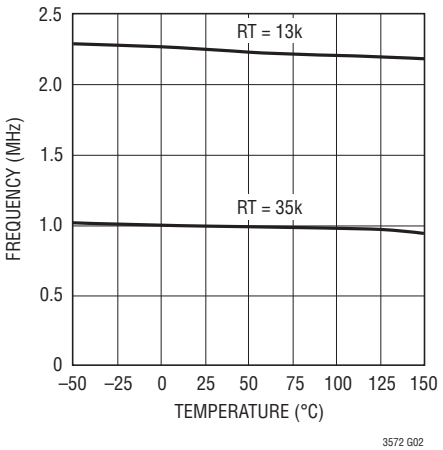
Note 8: OUTx refers to OUTA, $\overline{OUTA}$, OUTB, $\overline{OUTB}$.

TYPICAL PERFORMANCE CHARACTERISTICS

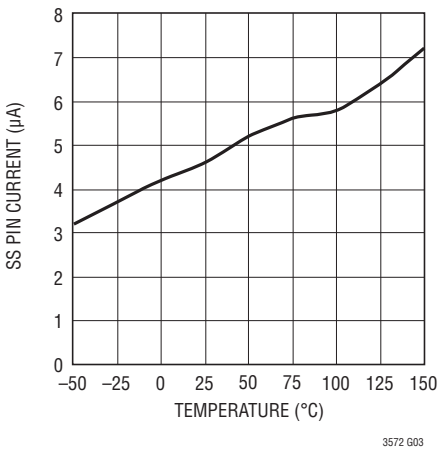
Feedback Pin Voltage vs Temperature



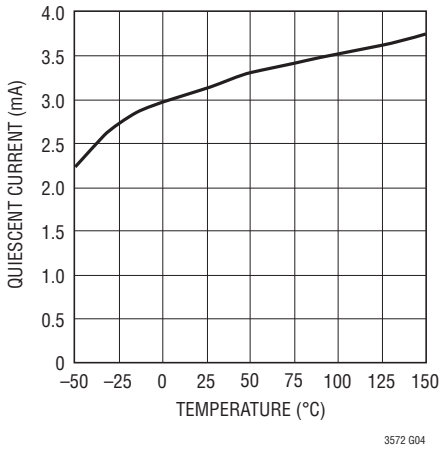
Oscillator Frequency vs Temperature



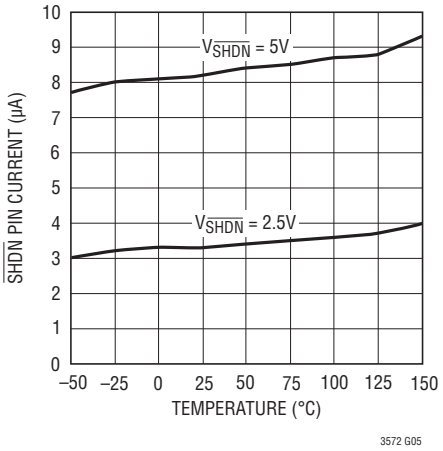
SS Pin Current vs Temperature



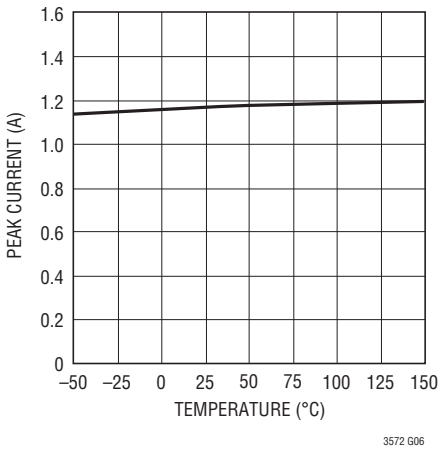
Quiescent Current vs Temperature



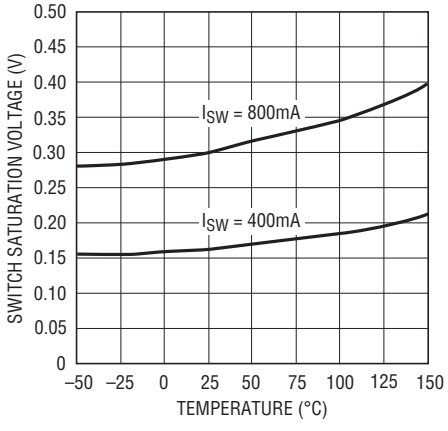
$\overline{SHDN}$ Pin Current vs Temperature



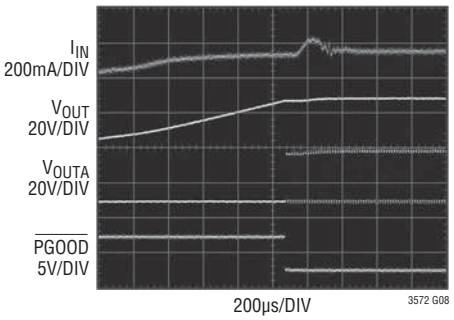
SW Current Limit vs Temperature



SW Saturation Voltage vs Temperature



Start-Up



PIN FUNCTIONS

SW (Pin 1): Switch Node. This pin connects to the collector of an internal NPN power switch.

V_{IN} (Pin 2): Input Supply Pin. This pin must be locally bypassed with a capacitor.

SYNC (Pin 3): Synchronization Pin. This pin is used to synchronize the internal oscillator to an external signal. The synchronizing range is 15% above the free running frequency set by the RT pin up to 2.5MHz. If not used, this pin must be tied to GND.

RT (Pin 4): Frequency Set Pin. Place a resistor to GND to set the internal frequency. The range of oscillation is 500kHz to 2.25MHz.

GND (Pins 5, 9, 20): Ground.

PWMB (Pin 6): Logic Input for the Driver. A high signal on this input sets OUTB high and $\overline{OUTB}$ low.

PWMA (Pin 7): Logic Input for the Driver. A high signal on this input sets OUTA high and $\overline{OUTA}$ low.

V_{OUT} (Pin 8): Output for the Switching Regulator and the Input Supply for the Drivers.

$\overline{SHDN}$ (Pin 10): Shutdown Pin. Tie to 1.5V or more to enable the switcher. Pull low to disable the switcher.

$\overline{SHDNA}$ (Pin 11): Shutdown Pin. Tie to 1.5V or more to enable OUTA and $\overline{OUTA}$. Pull low to place OUTA and $\overline{OUTA}$ in a high impedance state.

$\overline{SHDNB}$ (Pin 12): Shutdown Pin. Tie to 1.5V or more to enable OUTB and $\overline{OUTB}$. Pull low to place OUTB and $\overline{OUTB}$ in a high impedance state.

FB (Pin 13): Feedback Pin. The LT3572 regulates this pin to 1.225V. Connect the feedback resistors to this pin to set the output voltage for the switching regulator.

SS (Pin 14): Soft-Start Pin. Place a soft-start capacitor here. A capacitor on the soft-start pin slowly ramps the current limit of the part from 0A to 1.3A.

$\overline{PGOOD}$ (Pin 15): This pin is an open-drain output that pulls low when the FB pin is within 95% of its regulation value.

$\overline{OUTB}$ (Pin 16): The Output Driver. This node switches between V_{OUT} and GND and is inverted from OUTB.

OUTB (Pin 17): The Output Driver. This node switches between V_{OUT} and GND.

OUTA (Pin 18): The Output Driver. This node switches between V_{OUT} and GND .

$\overline{OUTA}$ (Pin 19): The Output Driver. This node switches between V_{OUT} and GND and is inverted from OUTA.

Exposed Pad (Pin 21): Ground. The Exposed Pad of the package provides both electrical contact to ground and good thermal contact to the printed circuit board. The Exposed Pad must be soldered to the circuit board for proper operation.

BLOCK DIAGRAM

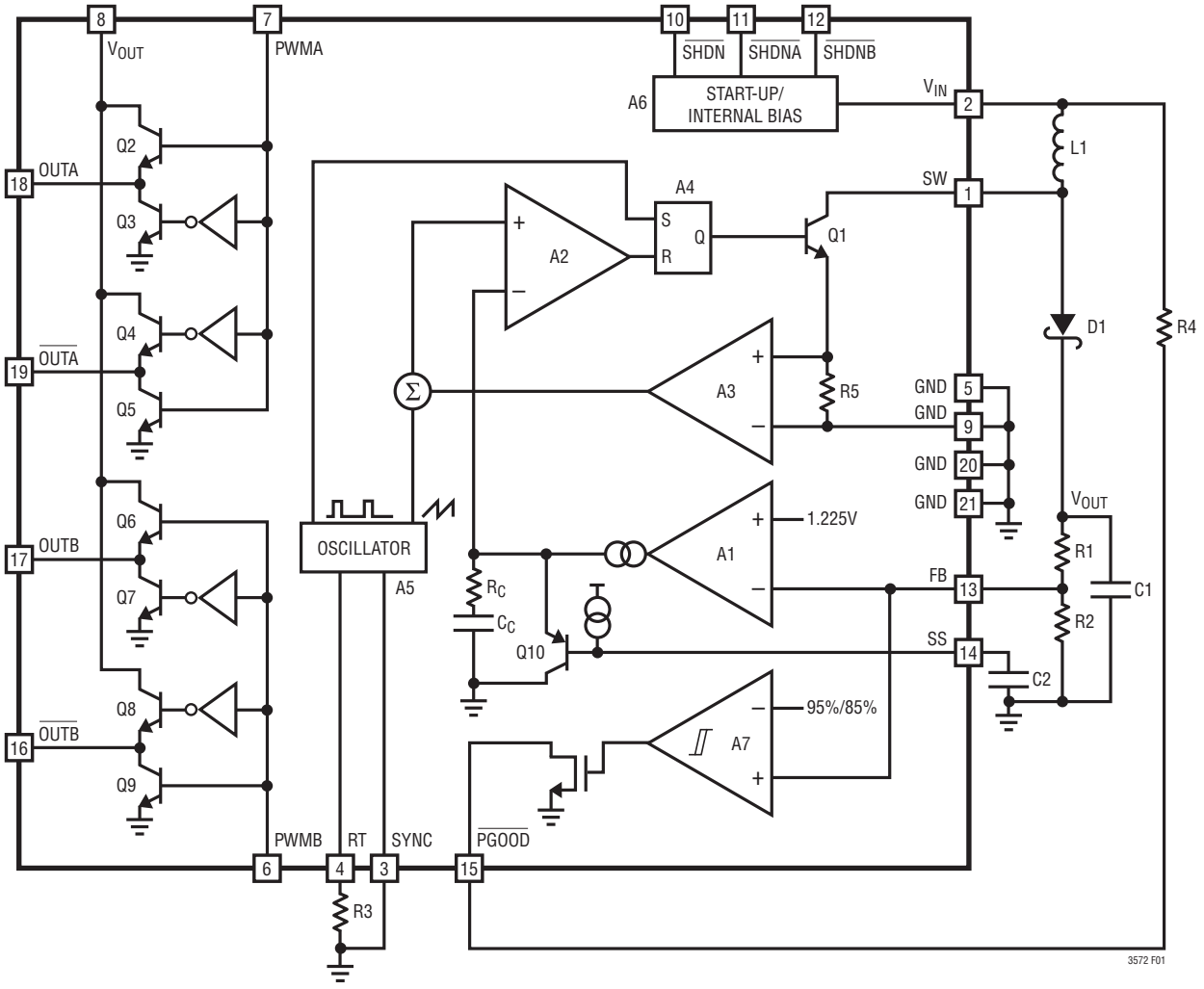


Figure 1. Block Diagram

OPERATION

Switching Regulator

The LT3572 uses a constant frequency, current mode, control scheme to provide excellent line and load regulation for the output drivers. Operation can be best understood by referring to the Block Diagram in Figure 1. A pulse from the oscillator sets the RS flip-flop, A4, and turns on the internal NPN bipolar power switch, Q1. Current in Q1 and the external inductor, L1, begins to increase. When this current exceeds a level determined by the voltage at the output of the error amplifier A1, comparator A2 resets A4, turning Q1 off. The current in L1 flows through the external Schottky diode D1 and begins to decrease. The cycle begins again at the next pulse from the oscillator. In this way, the voltage at the output of the error amplifier controls the current through the indictor to the output. The soft-start capacitor, C2, clamps the output of the error amplifier causing the current limit to slowly increase. This helps reduce overshoot on the output and helps minimize inrush current on the input.

Output Drivers

The function of the driver section is to level shift the input of the PWM pins to the voltage of the V_{OUT} pin. The drivers operate in an H-bridge fashion, where the OUTA and OUTB pins are the same polarity as the PWMA and PWMB pins respectively and the $\overline{OUTA}$ and $\overline{OUTB}$ are inverted from PWMA and PWMB respectively. The OUT pins will be high impedance until the FB pin is within 95% of its regulated voltage. The OUT pins will follow PWMA and PWMB as long as FB stays within 85% of the regulated voltage. If FB drops below 85%, the OUT pins will go high impedance.

APPLICATIONS INFORMATION

Duty Cycle

The typical maximum duty cycle of the LT3572 is 95% at 1MHz. This maximum duty cycle reduces as the switching frequency is increased. The duty cycle for a given application is given by:

$$DC = \frac{V_{OUT} + V_D - V_{IN}}{V_{OUT} + V_D - V_{CESAT}}$$

where V_D is the diode forward drop, typically 0.5V and V_{CESAT} is, in the worst case, 310mV at 0.8A. The LT3572 can be used at higher duty cycles, but must be operated in the discontinuous mode so that the actual duty cycle is reduced.

FB Resistor Network

The output voltage is programmed with a resistor divider between the output and the FB pin. Choose the resistors according to:

$$R1 = R2\left(\frac{V_{OUT}}{1.225V} - 1\right)$$

Shutdown Pins

When held below 0.3V, $\overline{SHDNA}$ and $\overline{SHDNB}$ prevent the drivers from switching and keep the outputs in a high impedance state. If $\overline{SHDN}$ is held below 0.3V then the switching regulator is prevented from turning on. When any one of these pins are pulled above 1.5V the internal circuitry is turned on and the respective output is allowed to operate. When the LT3572 is not in use all three pins should be pulled low.

Oscillator

The LT3572 can operate at switching frequencies from 500kHz up to 2.25MHz by changing the value of the resistor R3 on the RT pin. Figure 2 shows a graph of RT vs Switching Frequency.

The oscillator can be synchronized with an external clock applied to the SYNC pin. When synchronizing the oscillator, the free running frequency must be set approximately

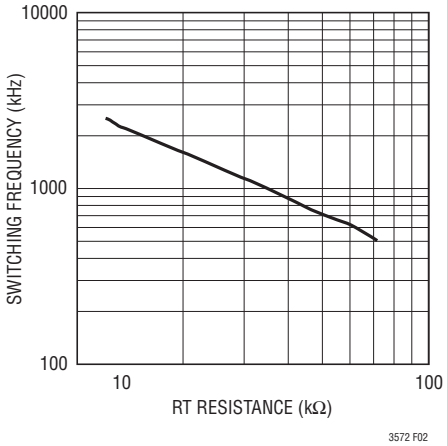


Figure 2. RT Resistance vs Switching Frequency

15% lower than the desired synchronized frequency. If the sync function is not used the SYNC pin must be tied to ground.

$\overline{PGOOD}$

The part has a power good feature that detects when the output boost converter is up and in regulation. When the part is turned off or not in regulation the $\overline{PGOOD}$ pin is in a high impedance state. When the part is within 95% of regulation the $\overline{PGOOD}$ pin is pulled low signaling that the output is valid. If the output then falls below 85% of regulation the $\overline{PGOOD}$ pin is put back in a high impedance state. Whenever the output is not in regulation the output pins in the driver aren't allowed to switch and are placed in a high impedance state. The $\overline{PGOOD}$ pin is an open drain of an NMOS devices with an impedance of 1kΩ and should be tied to V_{IN} through a resistor.

Soft-Start

The soft-start feature limits the inrush current drawn from the supply upon start-up. An internal current source with a nominal 4.5µA current source charges an external capacitor C2. The voltage on the soft-start pin is used to control the output of the error amplifier, which limits the maximum peak current through the inductor and the inrush current drawn from the supply during start-up.

APPLICATIONS INFORMATION

PWM

The LT3572 can PWM the output drivers at a very high frequency. The limitation on the frequency is determined by the internal rise in die temperature that occurs when driving the motor. The power delivered to the piezo motor is propotional to V_{OUT}^2, the capacitance of the motor, and the PWM frequency. When any of these are increased the power dissipated in the part increases causing the internal die temperature to increase. Driving two 2.2nF capacitors with V_{OUT} at 30V, the maximum PWM frequency should be less than 80 kHz. The LT3572 can run at a higher frequency but either V_{OUT} needs to be reduced or the capacitance needs to be lowered. A piezo motor has an associated capacitance that cannot be reduced so the output voltage must be lowered. Since the power is proportional to V_{OUT}^2 a reduction of V_{OUT} to 25V from 30V will allow the LT3572 to run at a maxim frequency of 115 kHz. If a different motor is used the maximum PWM frequency will need to be adjusted inversely to the equivolent capacitance of the motor.

Inductor Selection

A 10µH inductor is recommended for most LT3572 applications. Choose an inductor that will handle at least 1A without saturating, and ensure that the inductor has a low DCR (copper-wire resistance) to minimize I^2R power losses. Table 1 lists several inductor manufacturers.

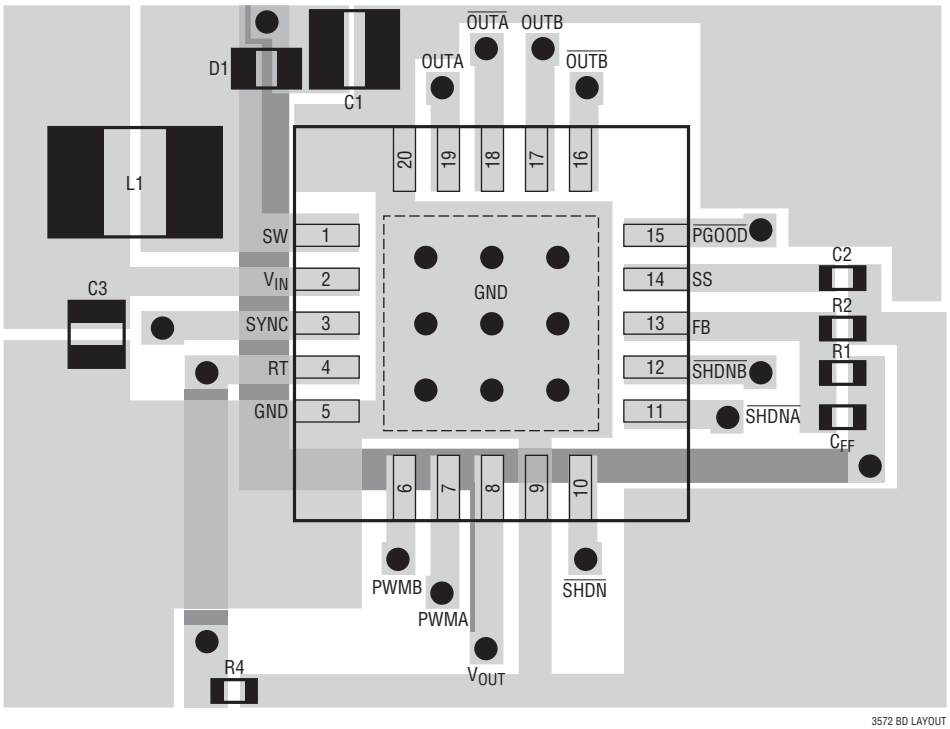
Table 1. Inductor Manufacturers

Sumida	(847) 956-0666	www.sumida.com
TDK	(847) 803-6100	www.tdk.com
Murata	(714) 852-2001	www.murata.com
FDK	(408) 432-8331	www.tdk.co.jp

Capacitor Selection

The small size of ceramic capacitors makes them ideal for LT3572 applications. Only X5R or X7R types should be used because they retain their capacitance over wider voltage and temperature ranges than other types such as Y5V or Z5U. A 4.7µF to 15µF output capacitor is sufficient for stable transient response, however, more output capacitance can help limit the voltage droop on V_{OUT} during transients.

Ceramic capacitors also make a good choice for the input decoupling capacitor, which should be placed as close as possible to the LT3572. A 1µF to 4.7µF input capacitor is sufficient for most applications. Table 2 shows a list



APPLICATIONS INFORMATION

of several ceramic capacitor manufacturers. Consult the manufacturers for detailed information on their entire selection of ceramic parts.

Table 2. Ceramic Capacitor Manufacturers

Taiyo Yuden	(408) 573-4150	www.t-yuden.com
AVX	(803) 448-9411	www.avxcorp.com
Murata	(714) 852-2001	www.murata.com

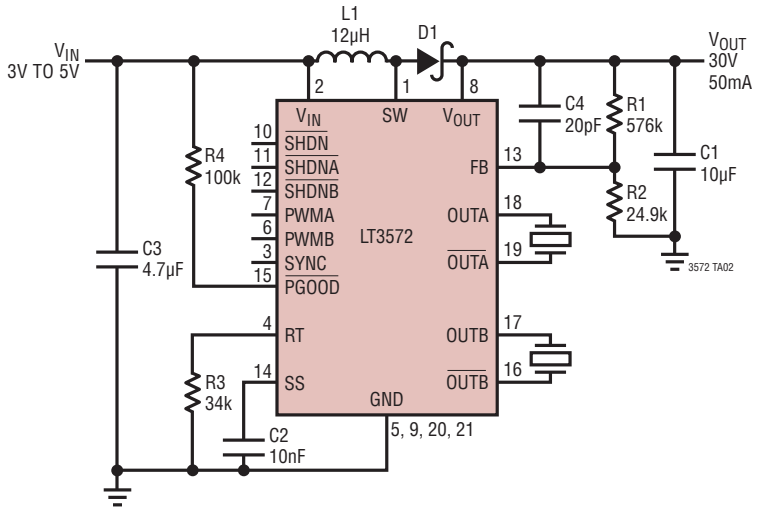
Diode Selection

A Schottky diode is recommended for use with the LT3572. The Philips PMEG 3005 is a good choice. If the switch voltage exceeds 30V, a PMEG 4005 (a 40V diode) can be used. These diodes are rated to handle an average forward current of 0.5A. For higher efficiency, use a diode with better thermal characteristics such as the On Semiconductor MBRM140 (a 40V diode).

Layout Hints

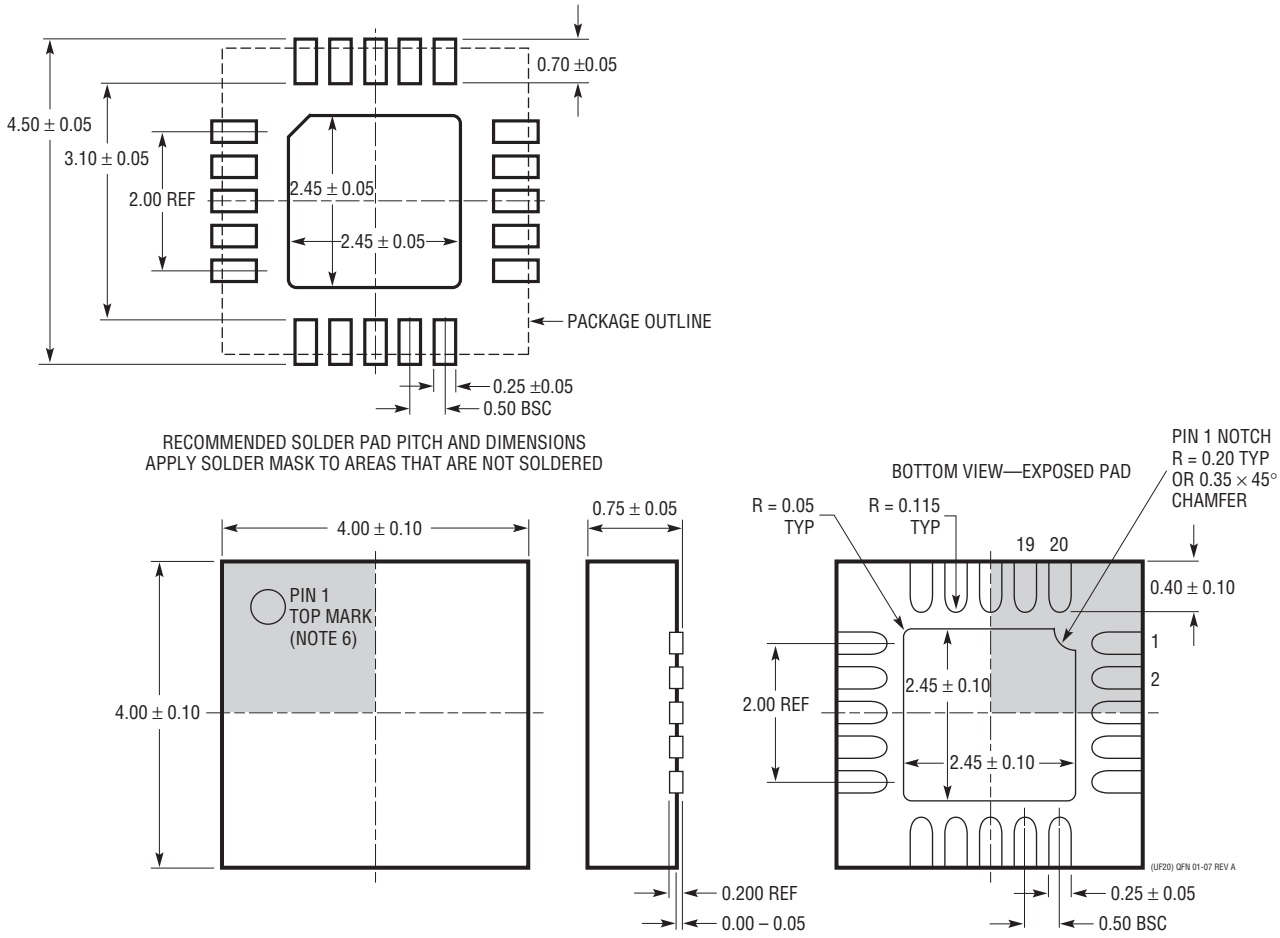
As with all switching regulators, careful attention must be paid to the PCB board layout and component placement. To maximize efficiency, switch rise and fall times are made as short as possible. Note the vias under the Exposed Pad. These should connect to a local ground plane for better thermal performance.

TYPICAL APPLICATION



PACKAGE DESCRIPTION

UF Package
20-Lead Plastic QFN (4mm × 4mm)
(Reference LTC DWG # 05-08-1710 Rev A)



NOTE:
1. DRAWING IS PROPOSED TO BE MADE A JEDEC PACKAGE OUTLINE MO-220 VARIATION (WGGD-1)—TO BE APPROVED
2. DRAWING NOT TO SCALE
3. ALL DIMENSIONS ARE IN MILLIMETERS
4. DIMENSIONS OF EXPOSED PAD ON BOTTOM OF PACKAGE DO NOT INCLUDE MOLD FLASH. MOLD FLASH, IF PRESENT, SHALL NOT EXCEED 0.15mm ON ANY SIDE
5. EXPOSED PAD SHALL BE SOLDER PLATED
6. SHADED AREA IS ONLY A REFERENCE FOR PIN 1 LOCATION ON THE TOP AND BOTTOM OF PACKAGE

Information furnished by Linear Technology Corporation is believed to be accurate and reliable. However, no responsibility is assumed for its use. Linear Technology Corporation makes no representation that the interconnection of its circuits as described herein will not infringe on existing patent rights.

RELATED PARTS

PART NUMBER	DESCRIPTION	COMMENTS
LT1160	Half-/Full-Bridge N-Channel MOSFET Driver	V_{IN}: 10V to 15V, $V_{OUT(MAX)}$ = 60V, 24-Lead SO Package
LT3469	Piezo Microactuator Driver with Boost Regulator	V_{IN}: 2.5V to 16V, V_{OUT} = 35V Maximum, 40mA Current Limit for Piezo Microactuator
LT3479	3A, Full Featured DC/DC Converter with Soft-Start and Inrush Current Protection	V_{IN}: 2.5V to 24V, $V_{OUT(MAX)}$ = 40V, I_Q = Analog/PWM, I_{SD} < 1µA, DFN, TSSOP Packages
LT3580	42V, 2A, 2.5MHz High Efficiency Step-Up DC/DC Converter	V_{IN}: 2.5V to 32V, $V_{OUT(MAX)}$ = 40V, I_Q = 1mA, I_{SD} < 1µA, 3mm × 3mm DFN8 and MS8E Packages

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