Micropower 1A Boost Converter with Schottky and Output Disconnect

FEATURES

- **Tiny Solution Size**
- **Low Quiescent Current:**
  150μA in Active Mode (V_{IN} = 3.6V, V_{OUT} = 15V, No Load)
  1μA in Shutdown Mode
- **Internal 1A, 36V Switch**
- **Integrated Schottky Diode**
- **Integrated PNP Output Disconnect**
- **Internal Reference Override Pin**
- PGOOD Pin
- 25V at 80mA from 3.6V Input
- Auxiliary NPNs for Intermediate Bias Voltages (LT3473A)
- Automatic Burst Mode® Operation at Light Load
- Constant Switching Frequency: 1.2MHz
- Thermal Shutdown
- Input Range: 2.2V to 16V
- Low Profile (3mm × 3mm) DFN Package (LT3473)
- Low Profile (4mm × 3mm) DFN Package (LT3473A)

APPLICATIONS

- OLED Bias
- CCD Bias

DESCRIPTION

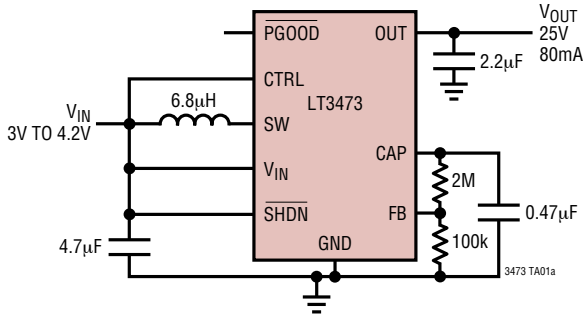
The LT®3473/LT3473A are micropower step-up DC/DC converters with integrated Schottky diode and output disconnect circuitry in low profile DFN packages. The small package size, high level of integration and the use of tiny SMT components yield a solution size of less than 50mm^2. The internal 1A switch allows the device to deliver 25V at up to 80mA from a Li-Ion cell, while automatic Burst Mode operation maintains efficiency at light load. An auxiliary reference input (CTRL) allows the user to override the internal 1.25V feedback reference with any lower value, allowing full control of the output voltage during operation. A PGOOD pin sinks current when the output voltage reaches 90% of final value.

The LT3473A includes two NPN transistors for generating intermediate bias voltages from the output and is offered in a 12-lead (4mm × 3mm) DFN package. The LT3473 does not include these NPNs and is offered in an 8-lead (3mm × 3mm) package.

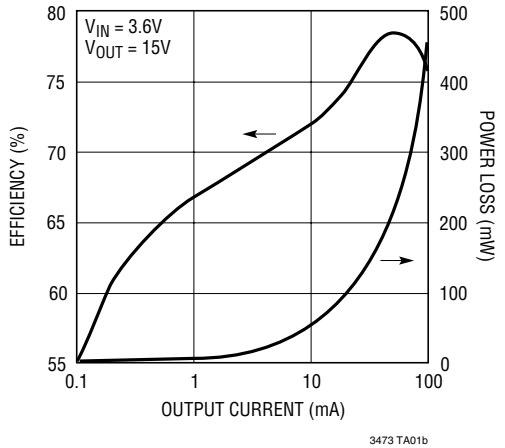
The rugged 36V switch and output disconnect circuitry allow outputs up to 34V to be easily generated in a simple boost topology.

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Burst Mode is a registered trademark of Linear Technology Corporation.
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TYPICAL APPLICATION



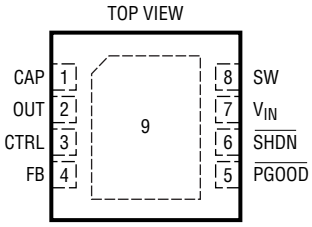
Conversion Efficiency and Power Loss vs Output Current



ABSOLUTE MAXIMUM RATINGS (Note 1)

V_{IN} Voltage 16V
$\overline{SHDN}$ Voltage 16V
SW Voltage 36V
$\overline{PGOOD}$ Voltage 36V
CAP Voltage 36V
OUT Voltage 36V
FB Voltage 10V
CTRL Voltage 10V
NB1, NB2 Voltage 36V
NE1, NE2 Voltage 36V
Maximum Junction Temperature ..... 125°C
Operating Temperature Range (Note 2) .. –40°C to 85°C
Storage Temperature Range ..... –65°C to 125°C

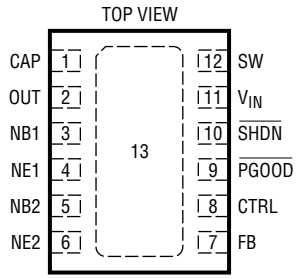
PACKAGE/ORDER INFORMATION



DD PACKAGE
8-LEAD (3mm × 3mm) PLASTIC DFN

T_{JMAX} = 125°C, θ_{JA} = 43°C/W
EXPOSED PAD (PIN 9) IS GND
MUST BE SOLDERED TO PCB (NOTE 3)

ORDER PART NUMBER
LT3473EDD
DD PART MARKING
LBJJ



DE PACKAGE
12-LEAD (4mm × 3mm) PLASTIC DFN

T_{JMAX} = 125°C, θ_{JA} = 43°C/W
EXPOSED PAD (PIN 13) IS GND
MUST BE SOLDERED TO PCB (NOTE 3)

ORDER PART NUMBER
LT3473AEDE
DE PART MARKING
3473A

Consult LTC Marketing for parts specified with wider operating temperature ranges.

ELECTRICAL CHARACTERISTICS

The ● denotes specifications which apply over the full operating temperature range, otherwise specifications are T_A = 25°C. V_{IN} = 3V, $\overline{SHDN}$ = 3V, CTRL = 2V, unless otherwise specified.

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Minimum Operation Voltage			2.2			V
Maximum Operation Voltage					16	V
Supply Current	$\overline{SHDN}$ = 3V, Not Switching $\overline{SHDN}$ = 0V			100 0.1	 1	µA µA
$\overline{SHDN}$ Voltage to Enable Chip		●	1.4			V
$\overline{SHDN}$ Voltage to Disable Chip		●			0.2	V
$\overline{SHDN}$ Pin Bias Current				2		µA
FB Voltage		●	1.235	1.25	1.26	V
FB Voltage Line Regulation	3V < V_{IN} < 16V			0.01		%/V
FB Pin Bias Current	FB = 1.27V			20		nA
CTRL to FB Offset	CTRL = 0.5V			5	20	mV
CTRL Pin Bias Current	CTRL = 1V			50		nA
FB Threshold for $\overline{PGOOD}$	CTRL = 2V CTRL = 0.5V			1.15 0.40		V V
$\overline{PGOOD}$ Current Capacity		●	100			µA

ELECTRICAL CHARACTERISTICS

The ● denotes specifications which apply over the full operating temperature range, otherwise specifications are T_A = 25°C. V_{IN} = 3V, $\overline{SHDN}$ = 3V, CTRL = 2V, unless otherwise specified.

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Switching Frequency			0.9	1.2	1.4	MHz
Maximum Duty Cycle		●	88	92		%
Switch Current Limit		●	1.2			A
Switch V_{CESAT}	I_{SW} = 100mA			45		mV
Switch Leakage Current	V_{SW} = 5V			0.1	5	µA
Schottky Forward Drop	I_D = 100mA			0.45		V
Schottky Leakage Current	CAP = 36V, SW = 0V				4	µA
Disconnect PNP Voltage Drop	I_{OUT} = 100µA, CAP = 20V I_{OUT} = 50mA, CAP = 20V			80 250		mV mV
Disconnect PNP Quiescent Current	CAP = 20V			1.2		µA
Disconnect PNP Leakage Current	$\overline{SHDN}$ = OUT = 0V, CAP = 20V			0.01	0.1	µA
LTC3473A Only						
NPN1 Voltage Drop	INE1 = 1mA			0.8		V
NPN1 Beta	INE1 = 1mA		60			
NPN2 Voltage Drop	INE2 = 1mA			0.8		V
NPN2 Beta	INE2 = 1mA		60			

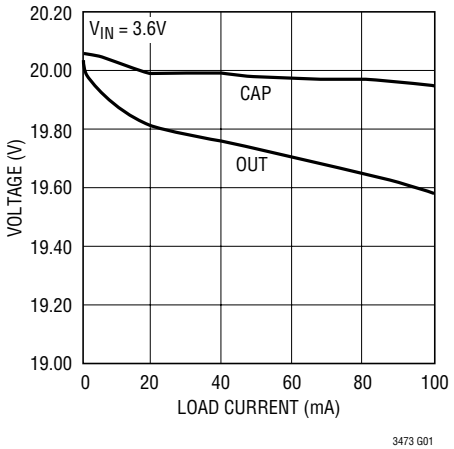
Note 1: Absolute Maximum Ratings are those values beyond which the life of a device may be impaired.

Note 2: The LT3473EDD and LT3473AEDE are guaranteed to meet performance specifications from 0°C to 70°C. Specifications over the –40°C to 85°C operating temperature range are assured by design, characterization and correlation with statistical process controls.

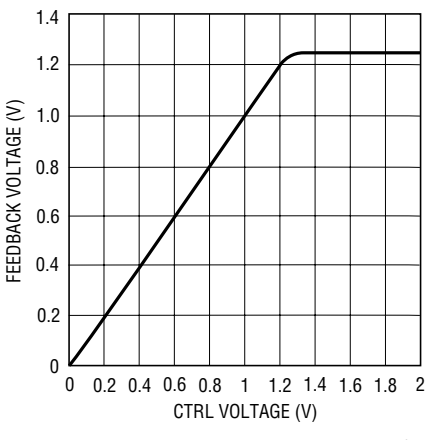
Note 3: Failure to correctly solder the Exposed Pad of the package to the PC board will result in a thermal resistance much higher than 40°C.

TYPICAL PERFORMANCE CHARACTERISTICS T_A = 25°C unless otherwise noted.

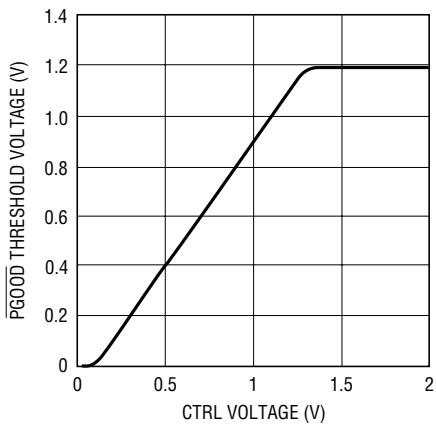
Load Regulation (Feedback Taken from CAP)



Feedback Voltage

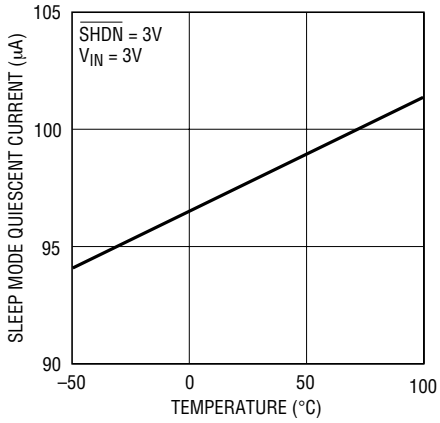


$\overline{PGOOD}$ Threshold Voltage

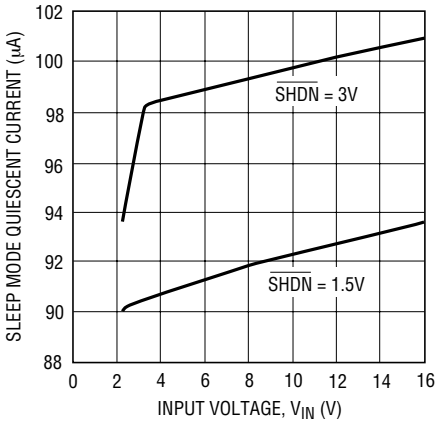


TYPICAL PERFORMANCE CHARACTERISTICS T_A = 25°C unless otherwise noted.

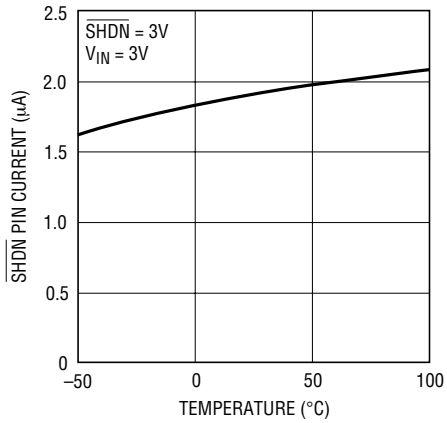
Sleep Mode Quiescent Current



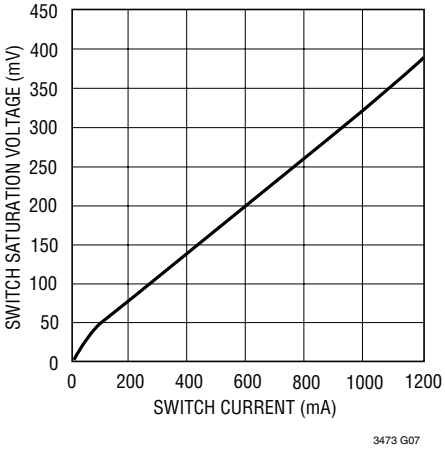
Sleep Mode Quiescent Current (Not Switching)



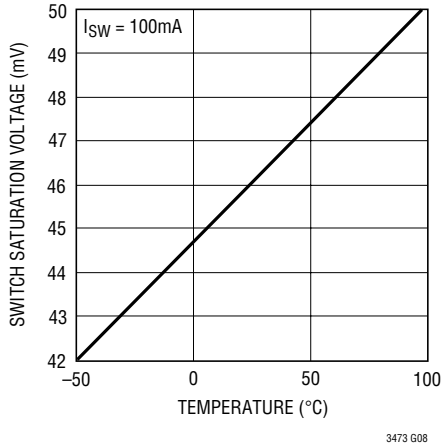
SHDN Pin Current



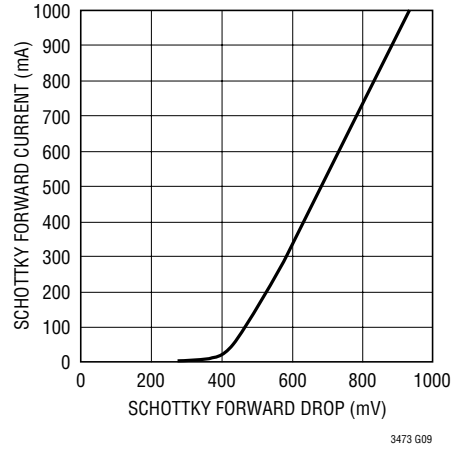
Switch $V_{CE(SAT)}$



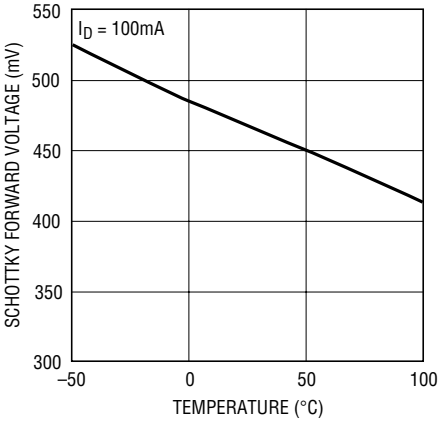
Switch Saturation Voltage



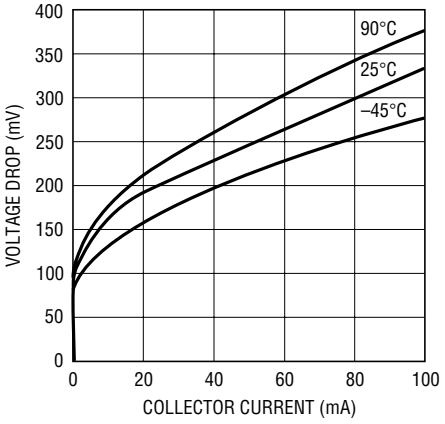
Schottky I-V Characteristic



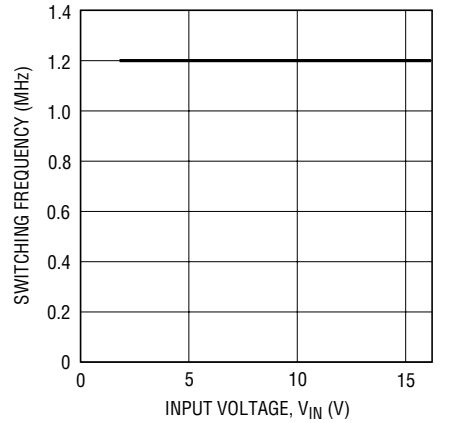
Schottky Forward Voltage



Output Disconnect Voltage Drop

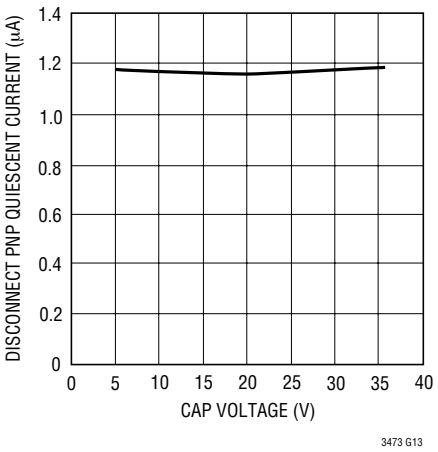


Switching Frequency

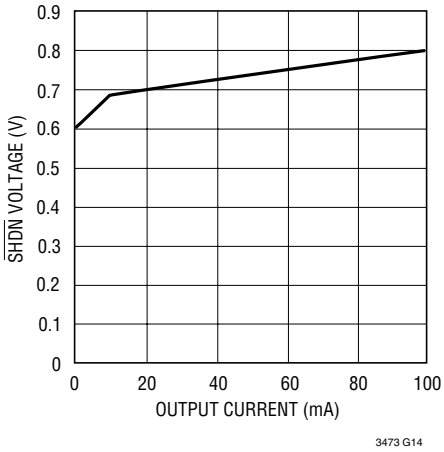


TYPICAL PERFORMANCE CHARACTERISTICS T_A = 25°C unless otherwise noted.

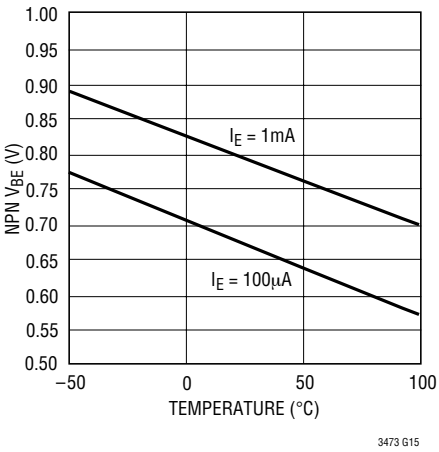
Disconnect PNP Quiescent Current



$\overline{SHDN}$ Voltage to Turn-On Disconnect PNP



Auxiliary NPN V_{BE}



PIN FUNCTIONS (LT3473/LT3473A)

CAP (Pin 1/Pin 1): Internal Output Voltage. This pin is the Schottky cathode and disconnect PNP emitter. Connect output capacitor here.

OUT (Pin 2/Pin 2): Output of Disconnect Circuit. Bypass this pin with capacitor to ground.

CTRL (Pin 3/Pin 8): External Reference Pin. This pin sets the FB voltage externally between 0V and 1.25V. Tie this pin 1.5V or higher to use the internal 1.25V reference.

FB (Pin 4/Pin 7): Feedback Pin. Pin voltage is regulated to 1.25V if internal reference is used or to the CTRL pin voltage if the CTRL pin voltage is between 0V and 1.25V. Connect the feedback resistor divider to this pin. The output voltage is regulated to:

$$V_{OUT} = V_{REF} \bullet \left(\frac{R2}{R1} + 1\right)$$

$\overline{PGOOD}$ (Pin 5/Pin 9): Power Good Output. Open collector logic output that starts to sink current when FB reaches within 100mV of the reference voltage.

$\overline{SHDN}$ (Pin 6/Pin 10): Shutdown Pin. Connect to 1.4V or higher to enable device; 0.2V or less to disable device. Also functions as soft-start. Use RC filter as shown in Figure 4.

V_{IN} (Pin 7/Pin 11): Input Supply Pin. Must be locally bypassed with a X5R or X7R type ceramic capacitor.

SW (Pin 8/Pin 12): Switch Pin. Connect inductor here. Minimize the metal trace area connected to the pin to minimize EMI.

Exposed Pad (Pin 9/Pin 13): Ground. Solder directly to PCB ground plane through multiple vias under the package for optimum thermal performance.

LT3473A Only

NB1 (Pin 3): NPN1 Base.

NE1 (Pin 4): NPN1 Emitter.

NB2 (Pin 5): NPN2 Base.

NE2 (Pin 6): NPN2 Emitter.

BLOCK DIAGRAM

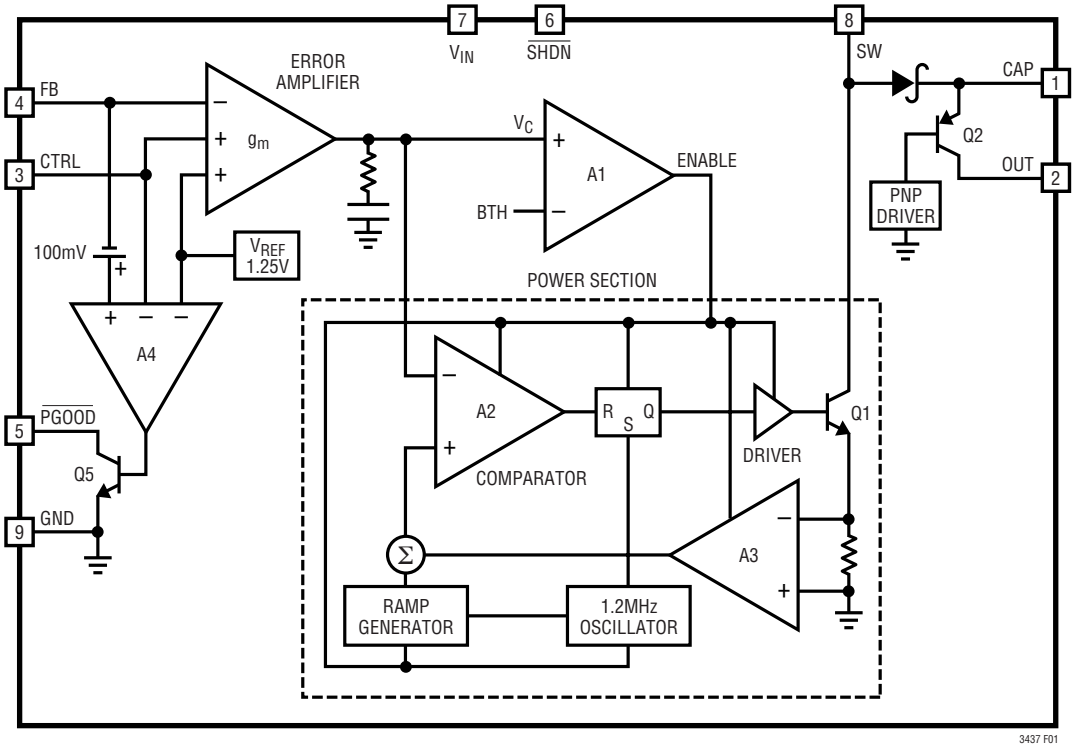


Figure 1. LT3473 Block Diagram

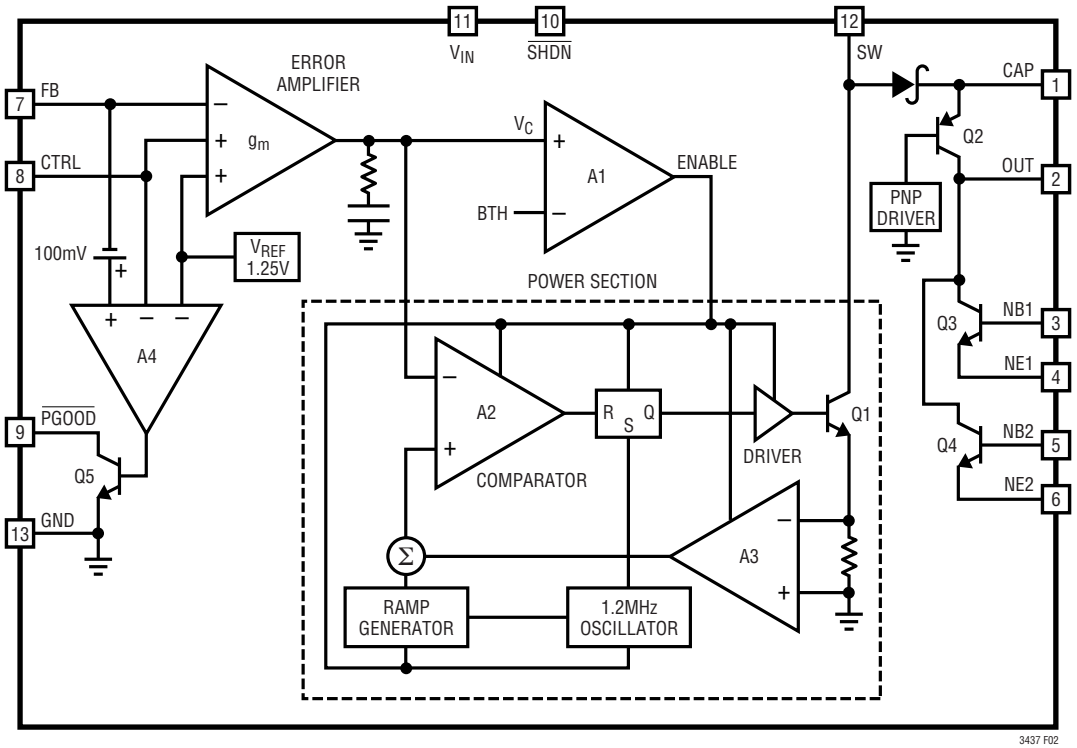


Figure 2. LT3473A Block Diagram

APPLICATIONS INFORMATION

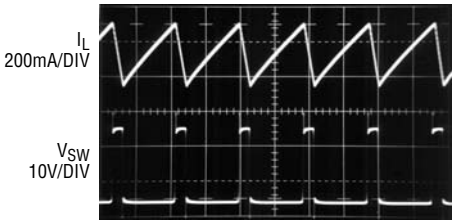
Operation

The LT3473 combines a current mode, fixed frequency PWM architecture with Burst Mode micropower operation to maintain high efficiency at light loads. Operation can best be understood by referring to the Block Diagram.

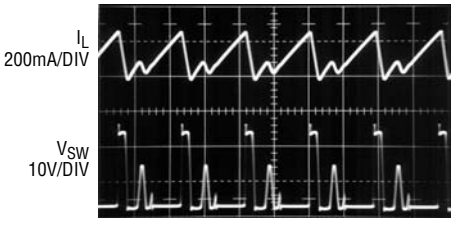
The reference of the part is determined by the lower of the internal 1.25V bandgap reference and the voltage at the CTRL pin. The error amplifier compares voltage at the FB pin with the reference and generates an error signal V_C. When V_C is below the Burst Mode threshold voltage, B_{TH}, the hysteretic comparator, A1, shuts off the power section leaving only the low power circuitry running. Total current consumption in this state is minimized. As output loading causes the FB voltage to decrease, V_C increases causing A1 to enable the power section circuitry. The chip starts switching. If the load is light, the output voltage (and FB voltage) will increase until A1 turns off the power section. The output voltage starts to fall again. This cycle repeats and generates low frequency ripple at the output. This Burst Mode operation keeps the output regulated and reduces average current into the IC, resulting in high efficiency at light load. If the output load increases sufficiently, A1's output remains high, resulting in continuous operation.

At the start of each oscillator cycle, the SR latch is set, turning on the power switch Q1. A voltage proportional to the switch current is added to a stabilizing ramp and the

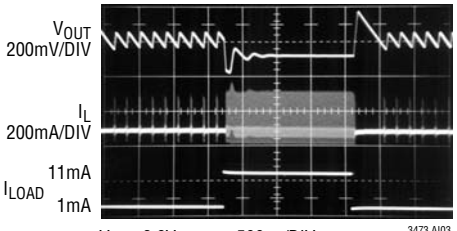
Switching Waveforms



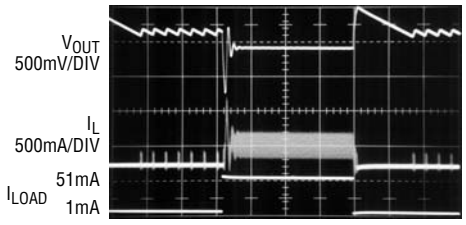
Switching Waveforms



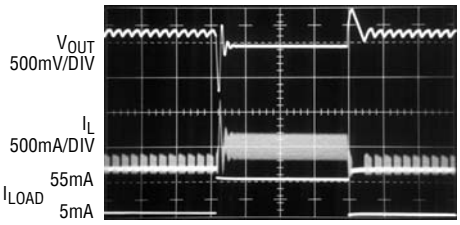
Transient Response



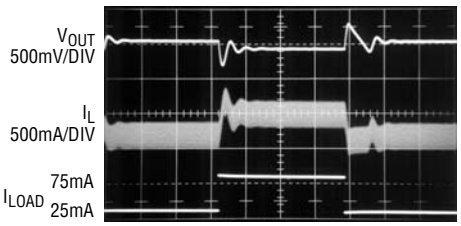
Transient Response



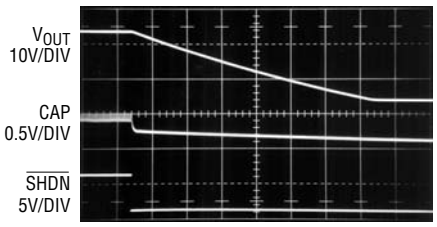
Transient Response



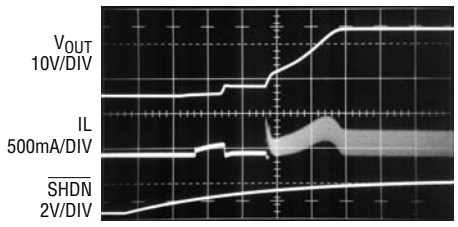
Transient Response



Shutdown Waveforms



Start-Up Waveforms



APPLICATIONS INFORMATION

resulting sum is fed into the positive terminal of the PWM comparator A2. When this voltage exceeds the level of the error signal V_C, the SR latch is reset, turning off the power switch Q1. The error amplifier sets the peak current level to keep the output in regulation. If the error amplifier's output increases, more current is delivered to the output; if it decreases, less current is delivered.

The LT3473 includes an internal power Schottky diode and a PNP transistor, Q2, for output disconnect. Q2 disconnects the load from the input during shutdown. The part also has a power good indication pin, $\overline{PGOOD}$. When the FB voltage reaches within 100mV of the reference voltage, the comparator A4 turns on Q5, sinking current from $\overline{PGOOD}$ pin.

The LT3473 has thermal shutdown feature with threshold at about 145°C.

Inductor Selection

A 6.8µH inductor is recommended for the LT3473. The minimum inductor size that may be used in a given application depends on required efficiency and output current.

Inductors with low core losses and small DCR (copper wire resistance) at 1.2MHz are good choices for LT3473 applications. Some inductors in this category with small size are listed in Table 1. The efficiency comparison of different inductors is shown in Figure 3.

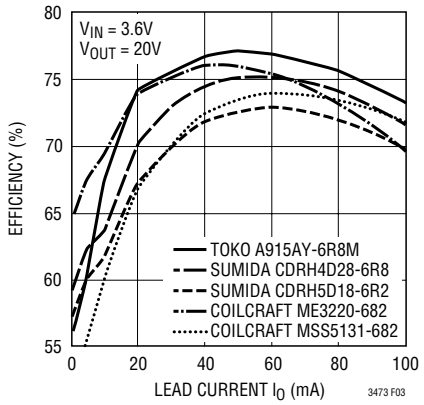


Figure 3. Efficiency Comparison of Different Inductors

Capacitor Selection

The small package of ceramic capacitors makes them suitable for LT3473 applications. X5R and X7R types of ceramic capacitors are recommended because they retain their capacitance over wider voltage and temperature ranges than other types such as Y5V or Z5U. A 4.7µF input capacitor, a 0.47µF output capacitor and a 2.2µF capacitor bypassing output disconnect PNP are sufficient for most LT3473 applications.

Table 2. Recommended Ceramic Capacitor Manufacturers

MANUFACTURER	TELEPHONE	URL
Taiyo Yuden	408-573-4150	www.t-yuden.com
AVX	843-448-9411	www.avxcorp.com
Murata	814-237-1431	www.murata.com
Kemet	408-986-0424	www.kemet.com

Table 1. Recommended Inductors

PART	DCR (mΩ)	CURRENT RATING (A)	DIMENSION (mm)	MANUFACTURER
DO1605T-682 ME3220-682 MSS6122-682 MSS5131-682	200 270 100 60	1.1 1.0 1.45 1.05	5.4 × 4.2 × 1.8 3.2 × 2.5 × 2.0 6.1 × 6.1 × 2.2 5.1 × 5.1 × 3.1	Coilcraft 800-322-2645 www.coilcraft.com
LQH55DN6R8	74	2.0	5.7 × 5.0 × 4.7	Murata 814-237-1431 www.murata.com
CDRH5D18-6R2 CDRH4D28-6R8 CDRH5D28-6R2 CRD53-4R7	71 81 33 74	1.4 1.12 1.8 1.68	5.7 × 5.7 × 2.0 4.7 × 4.7 × 3.0 5.7 × 5.7 × 3.0 6.0 × 5.2 × 3.2	Sumida 847-956-0666 www.sumida.com
A918CY-6R2M (TYPE D62LCB) A915AY-6R8M (TYPE D53LC)	62 68	1.49 1.51	6.0 × 6.0 × 2.0 5.0 × 5.0 × 3.0	Toko 408-432-8281 www.tokoam.com

APPLICATIONS INFORMATION

Inrush Current

The LT3473 has an integrated Schottky power diode. When supply voltage is abruptly applied to the V_{IN} pin while the output capacitor is discharged, the voltage difference between V_{IN} and CAP generates inrush current flowing from the input through the inductor and the internal Schottky diode to charge the output capacitor at the CAP pin. The maximum current the LT3473's Schottky can sustain is 2A. The selection of inductor and capacitor values should ensure that the peak inrush current is less than 2A. Peak inrush current can be calculated as follows:

$$I_P = \frac{V_{IN} - 0.6}{L \bullet \omega} \bullet \exp\left(-\frac{\alpha}{\omega} \bullet \arctan\left(\frac{\omega}{\alpha}\right)\right) \bullet \sin\left(\arctan\left(\frac{\omega}{\alpha}\right)\right)$$

$$\alpha = \frac{r + 1.5}{2 \bullet L}$$

$$\omega = \sqrt{\frac{1}{L \bullet C} - \frac{r}{4 \bullet L^2}}$$

where L is the inductance, r is the resistance of the inductor and C is the output capacitance. For a low DCR inductor, which is usually the case for this application, the peak inrush current can be simplified as follows:

$$I_P = \frac{V_{IN} - 0.6}{L \bullet \omega} \bullet \exp\left(-\frac{\alpha}{\omega} \bullet \frac{\pi}{2}\right)$$

A large abrupt voltage step at V_{IN} and/or a large capacitor at the CAP pin generate larger inrush current. Table 3 gives inrush peak currents for some component selections. An inductor with low saturation current could generate very large inrush current. For this case, inrush current should be measured to ensure safe operation. Note that inrush current is not a concern if the input voltage rises slowly.

Table 3. Inrush Peak Current

V_{IN} (V)	R (Ω)	L (μH)	C (μF)	I_P (A)
5	0.05	6.8	0.47	0.86
10	0.05	6.8	0.47	1.83
3.6	0.05	6.8	0.47	0.58
3.6	0.05	4.7	0.47	0.67

Setting the Output Voltages

The LT3473 has both an internal 1.25V reference and an external reference input. This allows the user to select between using the built-in reference and supplying an external reference voltage. The voltage at the CTRL pin can be adjusted while the device is operating to alter the output voltage for purposes such as display dimming or contrast adjustment. To use the internal 1.25V reference, the CTRL pin must be held higher than 1.5V. When the CTRL pin is held between 0V and 1.2V, the LT3473 will regulate the output such that the FB pin voltage is equal to the CTRL pin voltage.

The CAP pin should be used as the feedback node. To set the output voltage, select the values of R1 and R2 according to the following equation.

$$V_{INT} = V_{REF} \bullet \left(1 + \frac{R2}{R1}\right)$$

where V_{REF} = 1.25V if the internal reference is used, or $V_{REF} = V_{CTRL}$ if V_{CTRL} is between 0V and 1.2V.

To maintain output voltage accuracy, 1% resistors are recommended.

Soft-Start

The $\overline{SHDN}$ pin also functions as soft-start. Use an RC filter at the $\overline{SHDN}$ pin to limit the start-up current. The small bias current of the $\overline{SHDN}$ pin allows using a small capacitor for a large RC time constant.

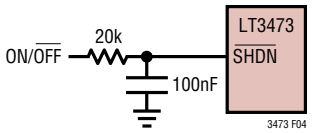


Figure 4. Soft-Start Circuitry

Output Disconnect Considerations

The LT3473 has an output disconnect PNP that isolates the load from the input during shutdown. The drive circuit maintains the PNP at the edge of saturation, adaptively according to the load, thus yielding the best compromise between V_{CESAT} and quiescent current to minimize power loss. To remain stable, it requires a bypass capacitor connected between the OUT pin and the CAP pin or

APPLICATIONS INFORMATION

between the OUT pin and ground. A ceramic capacitor with a value of 1μF is a good choice. The voltage drop (PNP V_{CESAT}) can be accounted for by setting the output voltage according to the following formula:

$$V_{OUT} = V_{INT} - V_{CESAT} = V_{REF} \bullet \left(1 + \frac{R2}{R1}\right) - V_{CESAT}$$

Auxiliary NPN Devices (LT3473A Only)

The LT3473A has two auxiliary NPNs as shown in the Block Diagram that can provide intermediate outputs less than OUT. The collectors of the NPNs are connected to the OUT pin internally. Each NPN can dissipate 100mW safely and has a minimum beta of 60. A resistor string can be connected to the two bases as shown in Figure 5 to generate buffered voltage at the emitters. When sourcing high current at low voltage, keep in mind that the NPNs will be dissipating a fair amount of power, which must be supplied by the DC/DC converter.

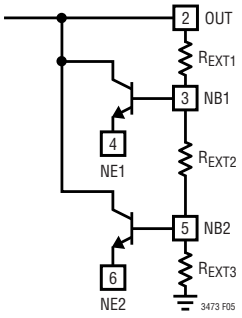


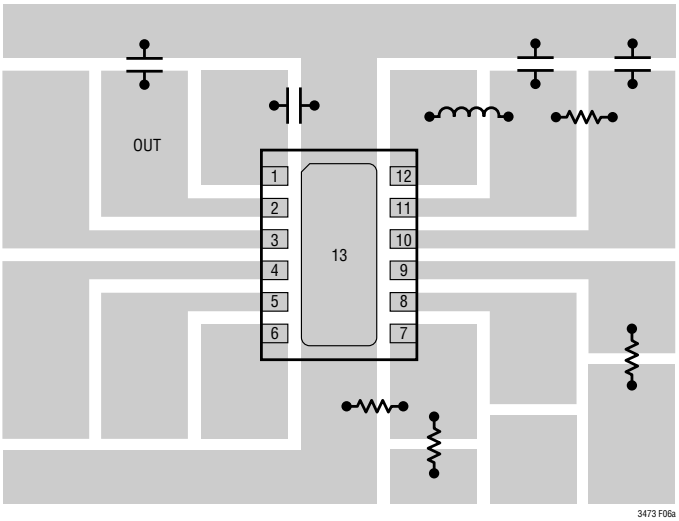
Figure 5. Auxiliary NPN Transistors in LT3473A. R_{EXT1}, R_{EXT2} and R_{EXT3} Set Intermediate Voltage at NE1 and NE2

Thermal Shutdown

The LT3473 has thermal shutdown circuitry that shuts down the part when the junction temperature reaches approximately 145°C to protect the part from abnormal operation with high power dissipation, such as an output short circuit or excessive power dissipation in the auxiliary NPNs. The part will turn back on when the junction cools down to approximately 125°C. If the abnormal condition remains, the part will turn on and off while maintaining the junction temperature within the window between 125°C and 145°C.

Board Layout Consideration

As with all switching regulators, careful attention must be paid to the PCB board layout and component placement. To maximize efficiency, switch rise and fall times are made as short as possible. To prevent electromagnetic interference (EMI) problems, proper layout of the high frequency switching path is essential. The voltage signal of the SW pin has sharp rise and fall edges. Minimize the length and area of all traces connected to the SW pin and always use a ground plane under the switching regulator to minimize interplane coupling. Recommended component placement is shown in Figure 6.



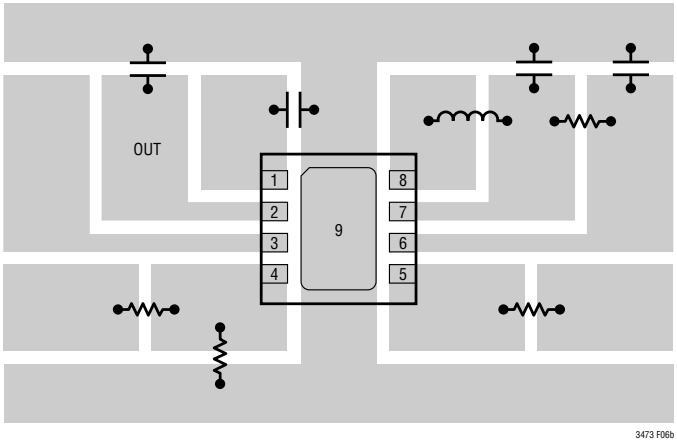
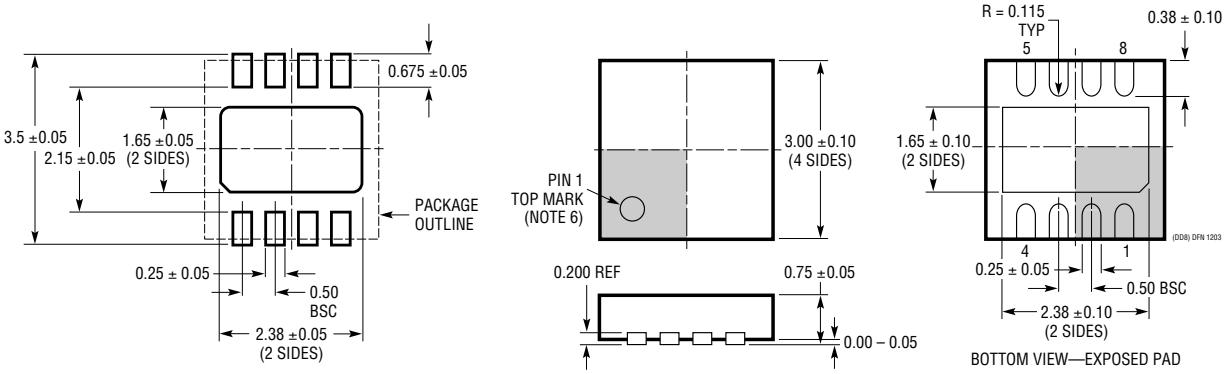


Figure 6. Recommended Component Placement

PACKAGE DESCRIPTION

DD Package
8-Lead Plastic DFN (3mm × 3mm)
(Reference LTC DWG # 05-08-1698)

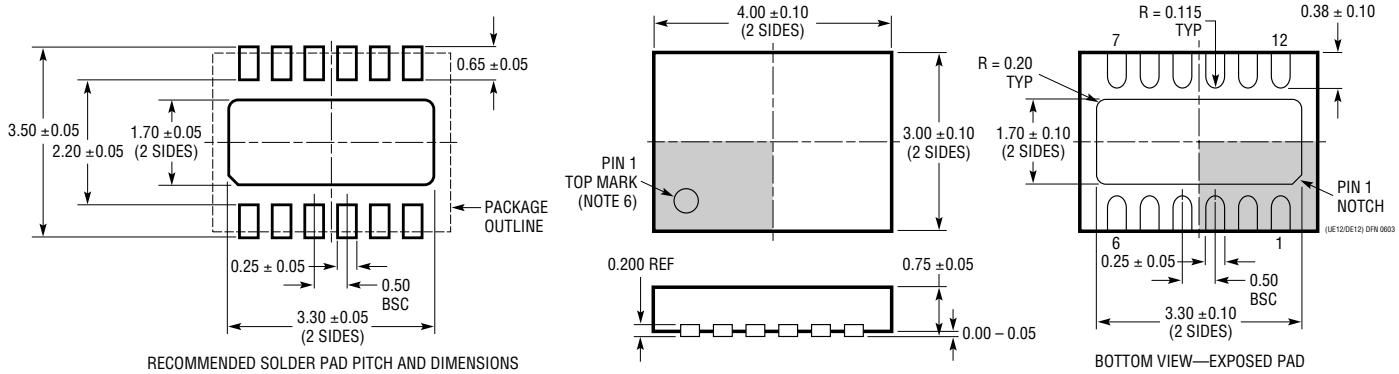


RECOMMENDED SOLDER PAD PITCH AND DIMENSIONS

BOTTOM VIEW—EXPOSED PAD

NOTE:
1. DRAWING TO BE MADE A JEDEC PACKAGE OUTLINE M0-229 VARIATION OF (WEED-1)
2. DRAWING NOT TO SCALE
3. ALL DIMENSIONS ARE IN MILLIMETERS
4. DIMENSIONS OF EXPOSED PAD ON BOTTOM OF PACKAGE DO NOT INCLUDE MOLD FLASH. MOLD FLASH, IF PRESENT, SHALL NOT EXCEED 0.15mm ON ANY SIDE
5. EXPOSED PAD SHALL BE SOLDER PLATED
6. SHADED AREA IS ONLY A REFERENCE FOR PIN 1 LOCATION ON TOP AND BOTTOM OF PACKAGE

DE Package
12-Lead Plastic DFN (4mm × 3mm)
(Reference LTC DWG # 05-08-1708)



RECOMMENDED SOLDER PAD PITCH AND DIMENSIONS

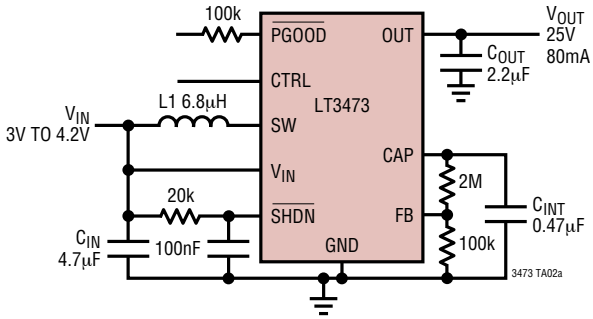
BOTTOM VIEW—EXPOSED PAD

NOTE:
1. DRAWING PROPOSED TO BE A VARIATION OF VERSION (WGED) IN JEDEC PACKAGE OUTLINE M0-229
2. DRAWING NOT TO SCALE
3. ALL DIMENSIONS ARE IN MILLIMETERS
4. DIMENSIONS OF EXPOSED PAD ON BOTTOM OF PACKAGE DO NOT INCLUDE MOLD FLASH. MOLD FLASH, IF PRESENT, SHALL NOT EXCEED 0.15mm ON ANY SIDE
5. EXPOSED PAD SHALL BE SOLDER PLATED
6. SHADED AREA IS ONLY A REFERENCE FOR PIN 1 LOCATION ON THE TOP AND BOTTOM OF PACKAGE

Information furnished by Linear Technology Corporation is believed to be accurate and reliable. However, no responsibility is assumed for its use. Linear Technology Corporation makes no representation that the interconnection of its circuits as described herein will not infringe on existing patent rights.

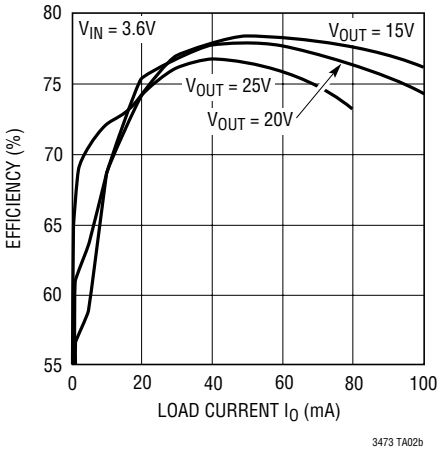
TYPICAL APPLICATION

OLED Bias



C_{IN}: TAIYO YUDEN JMK107BJ475
C_{INT}: TAIYO YUDEN GMK212BJ474
C_{OUT}: TAIYO YUDEN GMK325BJ225
L1: TOKO A915AY-6R8M (TYPE D53LC)

Efficiency



RELATED PARTS

PART NUMBER	DESCRIPTION	COMMENTS
LT1613	550mA (I_{SW}), 1.4MHz, High Efficiency Step-Up DC/DC Converter	V_{IN}: 0.9V to 10V, $V_{OUT(MAX)}$ = 34V, I_Q = 3mA, I_{SD} < 1µA, ThinSOT™ Package
LT1615/LT1615-1	300mA/80mA (I_{SW}), High Efficiency Step-Up DC/DC Converter	V_{IN}: 1V to 15V, $V_{OUT(MAX)}$ = 34V, I_Q = 20µA, I_{SD} < 1µA, ThinSOT Package
LT1930/LT1930A	1A (I_{SW}), 1.2MHz/2.2MHz, High Efficiency Step-Up DC/DC Converter	V_{IN}: 2.6V to 16V, $V_{OUT(MAX)}$ = 34V, I_Q = 4.2mA/5.5mA, I_{SD} < 1µA, ThinSOT Package
LT1935	2A (I_{SW}), 1.2MHz, High Efficiency Step-Up DC/DC Converter with Integrated Soft-Start	V_{IN}: 2.3V to 16V, $V_{OUT(MAX)}$ = 38V, I_Q = 3mA, I_{SD} < 1µA, ThinSOT Package
LT1945	Dual Output, Boost/Inverter, 350mA (I_{SW}), Constant Off-Time, High Efficiency Step-Up DC/DC Converter	V_{IN}: 1.2V to 15V, $V_{OUT(MAX)}$ = ±34V, I_Q = 40µA, I_{SD} < 1µA, 10-Lead MS Package
LT1946/LT1946A	1.5A (I_{SW}), 1.2MHz/2.7MHz, High Efficiency Step-Up DC/DC Converter	V_{IN}: 2.45V to 16V, $V_{OUT(MAX)}$ = 34V, I_Q = 3.2mA, I_{SD} < 1µA, MS8 Package
LTC®3436	3A (I_{SW}), 1MHz, 34V Step-Up DC/DC Converter	V_{IN}: 3V to 25V, $V_{OUT(MAX)}$ = 34V, I_Q = 0.9mA, I_{SD} < 6µA, TSSOP-16E Package
LT3461/LT3461A	300mA (I_{SW}), 1.3MHz/3MHz High Efficiency Step-Up DC/DC Converter with Integrated Schottky Diode	V_{IN}: 2.5V to 16V, $V_{OUT(MAX)}$ = 38V, I_Q = 2.8mA, I_{SD} < 1µA, ThinSOT Package
LT3463/LT3463A	Dual Output, Boost/Inverter, 250mA (I_{SW}), Constant Off-Time, High Efficiency Step-Up DC/DC Converters with Integrated Schottkys	V_{IN}: 2.3V to 15V, $V_{OUT(MAX)}$ = ±40V, I_Q = 40µA, I_{SD} < 1µA, DFN Package
LT3464	85mA (I_{SW}), High Efficiency Step-Up DC/DC Converter with Integrated Schottky and PNP Disconnect	V_{IN}: 2.3V to 10V, $V_{OUT(MAX)}$ = 34V, I_Q = 25µA, I_{SD} < 1µA, ThinSOT Package
LT3467/LT3467A	1.1A (I_{SW}), 1.3MHz/2.1MHz, High Efficiency Step-Up DC/DC Converter with Soft-Start	V_{IN}: 2.4V to 16V, $V_{OUT(MAX)}$ = 40V, I_Q = 1.2mA, I_{SD} < 1µA, ThinSOT Package
LT3471	Dual Output, Boost/Inverter, 1.3A (I_{SW}), 1.2MHz, High Efficiency Boost-Inverting DC/DC Converter	V_{IN}: 2.4V to 16V, $V_{OUT(MAX)}$ = ±40V, I_Q = 2.5mA, I_{SD} < 1µA, DFN Package
LT3479	3A (I_{SW}), 3.5MHz, 42V Step-Up DC/DC Converter	V_{IN}: 2.5V to 24V, $V_{OUT(MAX)}$ = 40V, I_Q = 5mA, I_{SD} < 1µA, DFN, TSSOP-16E Packages

ThinSOT is a trademark of Linear Technology Corporation.

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