LT3042EDD
20V, 200mA, Ultralow Noise Ultrahigh PSRR RF LDO Regulator

DESCRIPTION

DC2246B is a linear regulator featuring the LT®3042EDD, which is a 200mA, ultralow noise, and ultrahigh power supply rejection ratio (PSRR) RF low dropout (LDO) regulator with programmable current limit.

DC2246B operates over an input voltage range of 3.8V to 20V. The LT3042 has a maximum output current of 200mA. It features ultralow noise (0.8μV_{RMS} from 10Hz to 100kHz) and very high PSRR (79dB at 1MHz). The power good feedback (PGFB) pin voltage is programmable for power good threshold. A current limit function is provided. Current monitoring is also achievable by sensing the voltage on the ILIM pin.

Built-in protection includes reverse battery protection, reverse current protection, internal current limit with foldback and thermal limit with hysteresis.

The LT3042 data sheet gives a complete description of the device, operation and applications information. The data sheet must be read in conjunction with this Demo Manual for demonstration circuit DC2246B. The LT3042EDD is assembled in a 10-lead (3mm × 3mm) plastic DFN package with an exposed pad on the bottom-side of the IC. **Proper board layout is essential for maximum thermal performance.**

Design files for this circuit board are available at http://www.linear.com/demo/DC2246B

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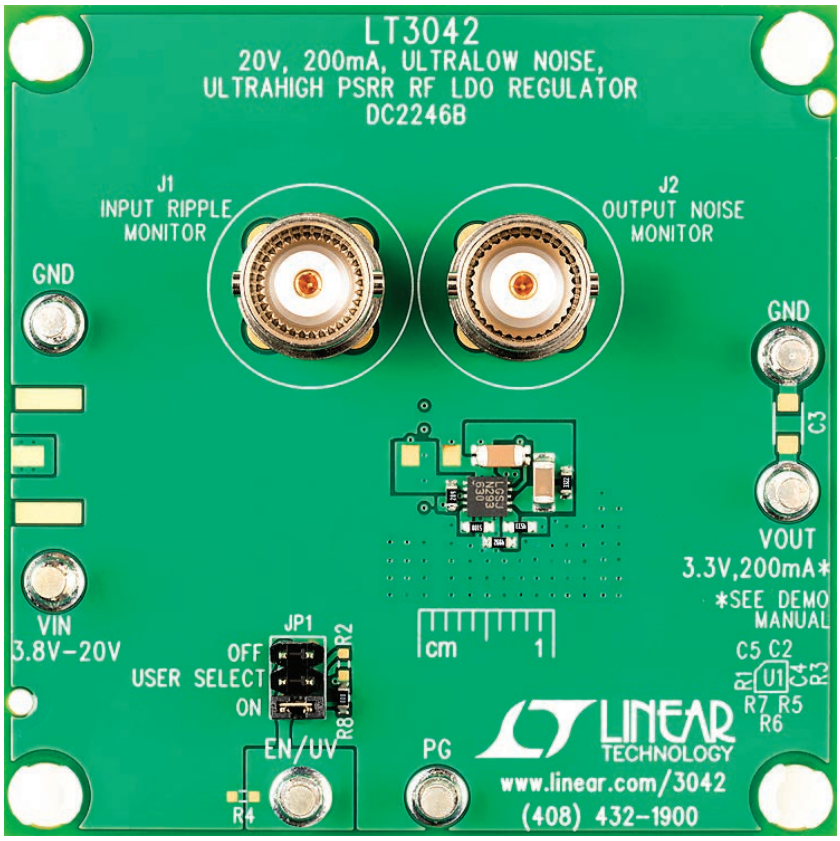
PERFORMANCE SUMMARY

Specifications are at T_A = 25°C

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Input Voltage Range (V_{IN})	V_{OUT} = 3.3V	3.8		20	VDC
Shutdown Input Current (I_{IN})	JP1 = OFF, V_{IN} = 6V		0.1		µA
Output Voltage (V_{OUT})	V_{IN} = 5V, I_{OUT} = 200mA	3.2	3.3	3.4	VDC
Output Current Range (I_{OUT})	V_{IN} = 3.8V~19.7V, V_{OUT} = 3.3V	0		200	mA
Output Current Range (I_{OUT})	V_{IN} = 3.8V~20V, V_{OUT} = 3.3V	0		195*	mA

* Please refer to the Current Limit vs Input-to-Output Differential in the LT3042 data sheet.

BOARD PHOTO


LT3042
20V, 200mA, ULTRALOW NOISE,
ULTRAHIGH PSRR RF LDO REGULATOR
DC2246B
J1
INPUT RIPPLE
MONITOR
J2
OUTPUT NOISE
MONITOR
GND
GND
C3
VOUT
3.3V,200mA*
*SEE DEMO
MANUAL
VIN
3.8V–20V
JP1
OFF
USER SELECT
ON
R2
R8
EN/UV
R4
PG
cm
1
C5 C2
R1
U1
C4
R3
R7 R5
R6
LINEAR
TECHNOLOGY
www.linear.com/3042
(408) 432-1900

QUICK START PROCEDURE

The DC2246B is easy to set up to evaluate the performance of the LT3042EDD. Refer to Figure 1 for proper measurement equipment setup and follow the procedure below:

1. Connect Load between the VOUT and GND terminals.
2. With power off, connect the input power supply to the VIN and GND terminals.
3. Make sure the shunt of JP1 is at ON option.
4. Turn the input power supply on and make sure the voltage is between 3.8V and 20V.
5. Refer to Application Notes AN70 and AN159 for measuring the output noise and PSRR.
6. R2 and R4 can define an accurate undervoltage lockout (UVLO) threshold when the shunt of JP1 is at USER SELECT option.

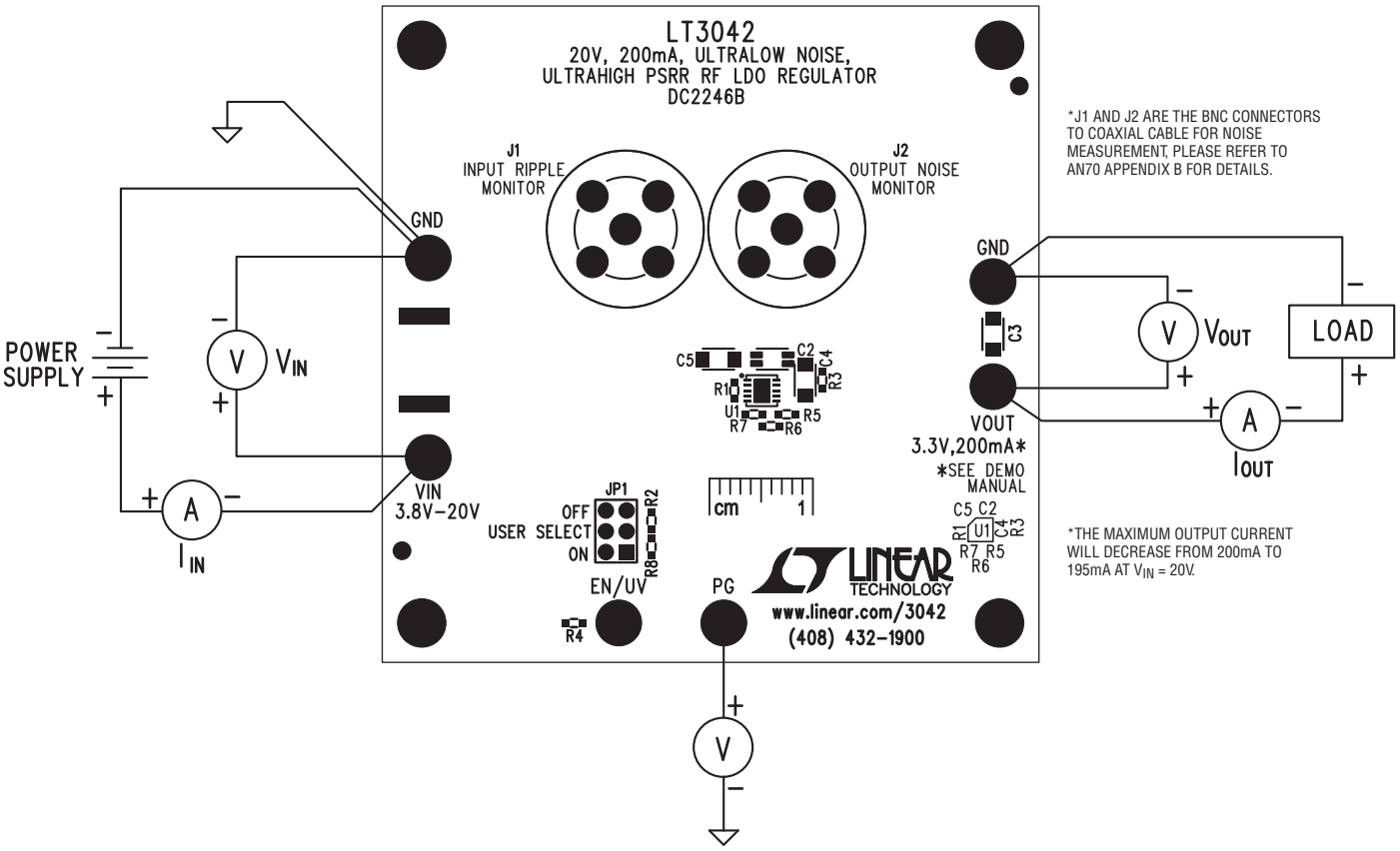


Figure 1. Test Procedure Setup Drawing for DC2246B

PCB LAYOUT

Best PSRR Performance: PCB Layout for Input Trace

For applications utilizing the LT3042 for post-regulating switching converters, placing a capacitor directly at the LT3042 input results in AC current (at the switching frequency) to flow near the LT3042. Without careful attention to PCB layout, this relatively high frequency switching current generates an Electromagnetic Field (EMF) that couples to the LT3042 output, thereby degrading its effective PSRR. While highly dependent on the PCB, the switching preregulator, the input capacitor size, among other factors, the PSRR degradation can easily be 30dB at 1MHz. This degradation is present even if the LT3042 is de-soldered from the board, because it effectively degrades the PSRR of the PC board itself. While negligible for conventional low PSRR LDOs, LT3042's ultrahigh PSRR requires careful attention to higher order parasitics in order to realize the full performance offered by the regulator.

The LT3042 demo board alleviates this degradation in PSRR by using a specialized layout technique. On layer 3, the input trace (VIN) is highlighted in red, with the return path (GND) highlighted on the bottom layer together with input capacitor C1. When an AC voltage is applied to the input of the board, AC current flows on this path, thus generating EMF. This EMF couples to output capacitor C2 and related traces, making the PSRR appear worse than it actually is. **With the input trace directly above the return path, the EMFs are in opposite directions, and consequently cancels each other out. Making sure these traces exactly overlap each other maximizes the cancellation effect and thus provides the maximum PSRR offered by the regulator.**

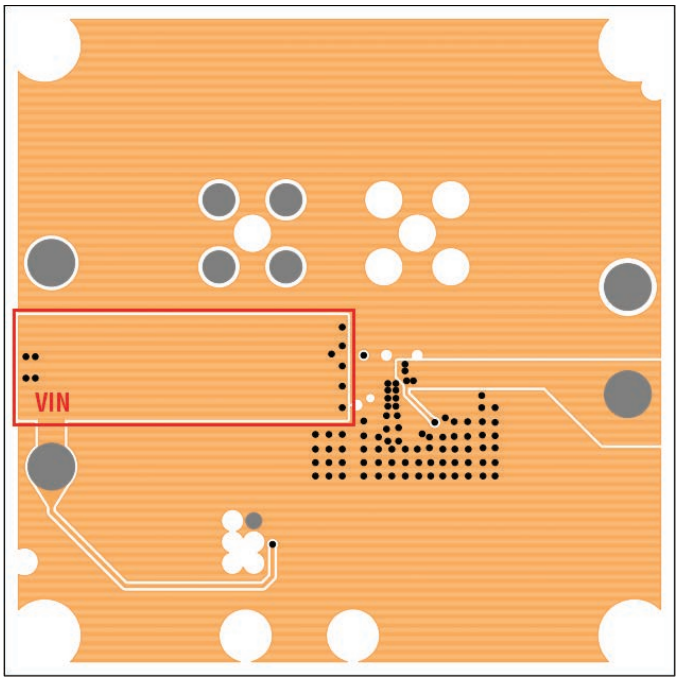


Figure 2. Layer 3 of the DC2246B

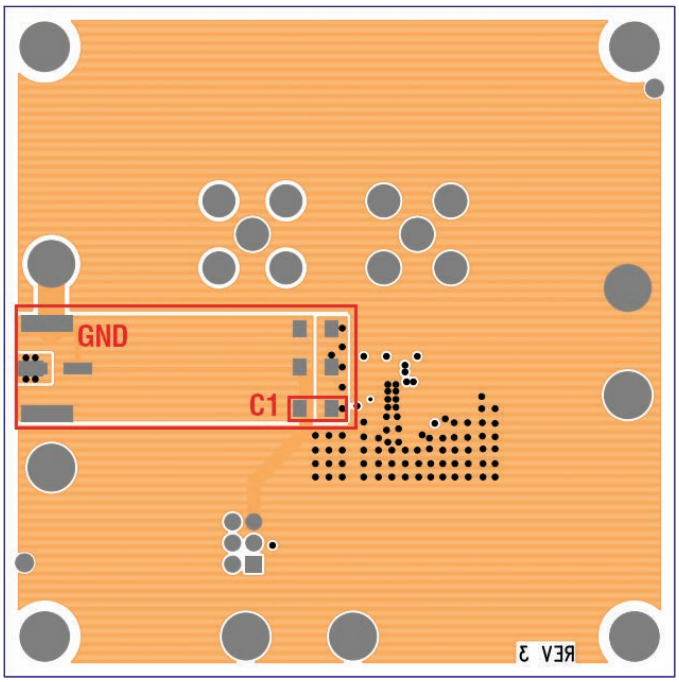


Figure 3. Bottom Layer of the DC2246B

PCB LAYOUT

Best AC Performance: PCB Layout for Output Capacitor C2

For ultrahigh PSRR performance, the LT3042 bandwidth is made quite high (~1MHz), making it close to the output capacitor's self-resonance frequency (~2MHz). Therefore, it is very important to avoid adding extra impedance (ESL and ESR) outside the feedback loop. To that end, minimize the effects of PCB trace and solder inductance by Kelvin connecting OUTS and SET pin capacitor (C4) GND directly to output capacitor (C2) terminals using split capacitor techniques. Pad 4 connects to the OUTS pin and Pad 1 connects to the GND side of the SET pin capacitor. With only small AC current flowing through these connections, the impact of solder joint/PCB trace inductance on stability is eliminated. While the LT3042 is robust enough not to oscillate if the recommended layout is not followed, phase/gain margin and stability will degrade.

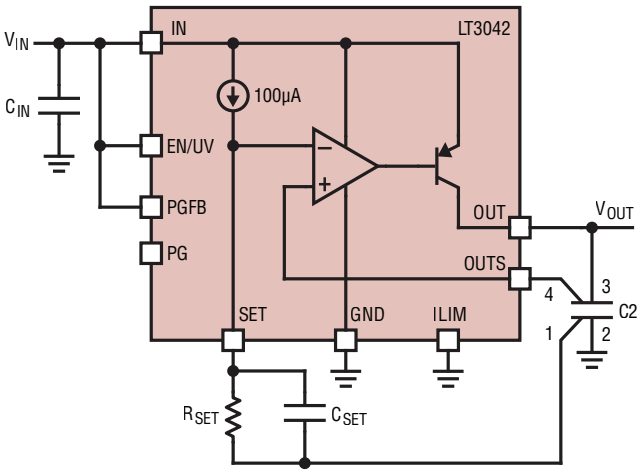


Figure 4. C2 and C_{SET} Connections for Best Performance

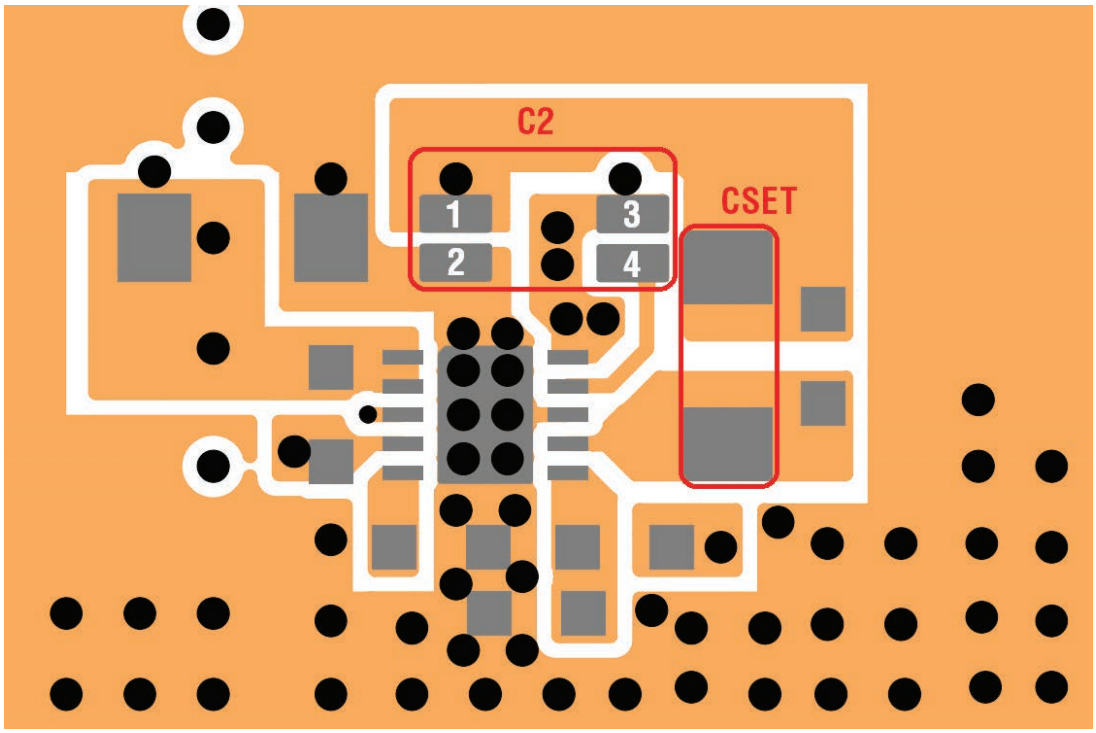
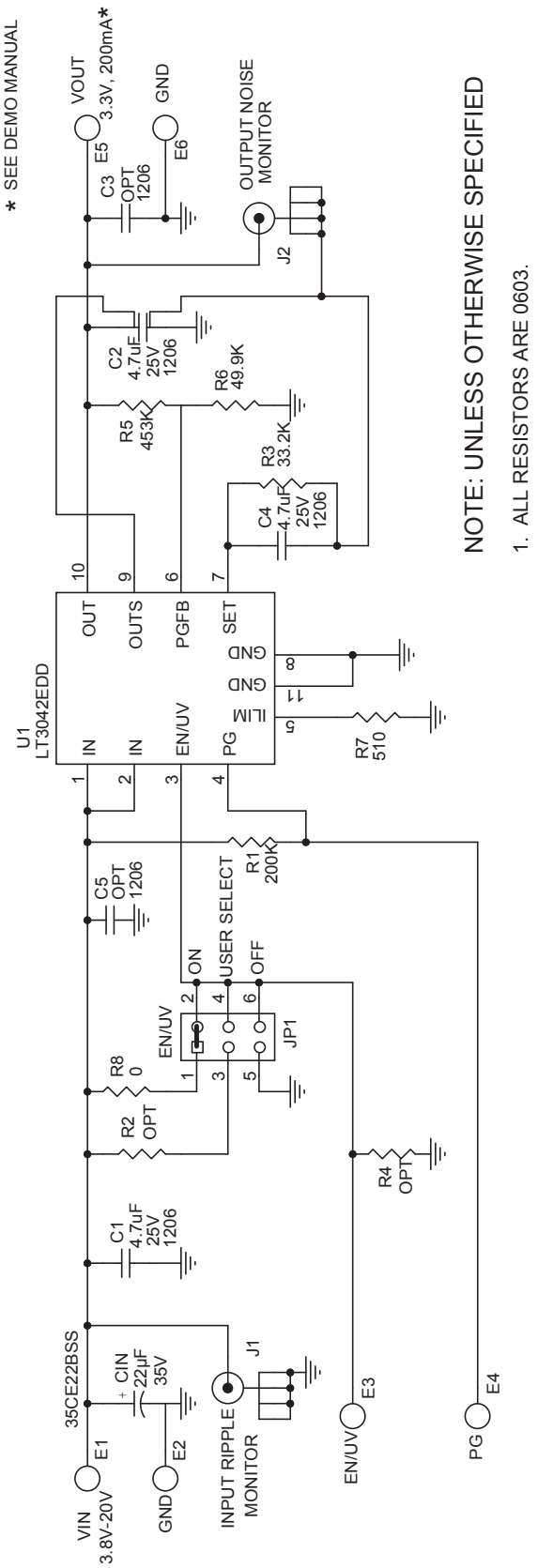


Figure 5. Split Pads for C2 on Top Layer of DC2246B

PARTS LIST

ITEM	QTY	REFERENCE	PART DESCRIPTION	MANUFACTURER/PART NUMBER
Required Circuit Components				
1	1	CIN	CAP., ALUM, 22µF, 35V, 5X5.4MM	SUN ELEC., 32CE22BSS
2	3	C1, C2, C4	CAP., X7R, 4.7µF, 25V, 10%, 1206	MURATA, GRM31CR71E475KA88L
3	1	R1	RES., CHIP, 200k, 1/16W, 5% 0603	VISHAY, CRCW0603200KJNEA
4	1	R3	RES., CHIP, 33.2k, 1/8W, 1% 0603	VISHAY, CRCW060333K2FKEA
5	1	R5	RES., CHIP, 453k, 1/8W, 1% 0603	VISHAY, CRCW0603453KFKEA
6	1	R6	RES., CHIP, 49.9k, 1/8W, 1% 0603	VISHAY, CRCW060349K9FKEA
7	1	R7	RES., CHIP, 510Ω, 1/10W, 1% 0603	VISHAY, CRCW0603510RFKEA
8	1	U1	IC, LT3042EDD DFN 3X3MM	LINEAR TECH., LT3042EDD#PBF
Optional Electronic Components				
1	1	R8	RES., CHIP, 0Ω, 1/16W, 5% 0603	VISHAY, CRCW06030000Z0EA
2	0	R2, R4 (OPT)	RES., OPT, 0603	
3	0	C3, C5(OPT)	CAP., OPT, 1206	
Hardware: For Demo Board Only				
1	6	E1-E6	TESTPOINT, TURRET, 0.094" PBF	MILL-MAX, 2501-2-00-80-00-00-07-0
2	1	JP1	HEADER 3 PIN 0.079" DOUBLE ROW	WURTH ELEKTRONIK, 62000621121
3	1	XJP1	SHUNT, 0.079" CENTER	WURTH ELEKTRONIK, 60800213421
4	2	J1, J2	CONN, BNC, 5 PINS	CONNEX, 112404
5	4	MH1-MH4	STAND-OFF, NYLON 6.4MM	WURTH ELEKTRONIK, 702931000

SCHEMATIC DIAGRAM



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This notice contains important safety information about temperatures and voltages. For further safety concerns, please contact a LTC application engineer.

Mailing Address:

Linear Technology
1630 McCarthy Blvd.
Milpitas, CA 95035

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