Dual 100mA/500mA Low Dropout, Low Noise, Micropower Regulators with Independent Inputs

FEATURES

- **Low Noise: 20μV_{RMS} (10Hz to 100kHz)**
- **Low Quiescent Current: 30μA/Output**
- **Independent Inputs**
- **Wide Input Voltage Range: 1.8V to 20V**
- **Output Current: 100mA/500mA**
- **Very Low Shutdown Current: <0.1μA**
- **Low Dropout Voltage: 300mV/320mV at 100mA/500mA**
- Adjustable Outputs from 1.22V to 20V
- Stable with as Low as 1μF/3.3μF Output Capacitor
- Stable with Aluminum, Tantalum or Ceramic Capacitors
- Reverse-Battery Protected
- No Protection Diodes Needed
- Overcurrent and Overtemperature Protected
- Tracking/Sequencing Capability
- Thermally Enhanced 16-Lead TSSOP and 16-Lead (5mm × 3mm) DFN Packages

APPLICATIONS

- Cellular Phones
- Pagers
- Battery-Powered Systems
- Frequency Synthesizers
- Wireless Modems
- Tracking/Sequencing Power Supplies

DESCRIPTION

The LT®3028 is a dual, micropower, low noise, low dropout regulator with independent inputs. With an external 0.01μF bypass capacitor, output noise is a low 20μV_{RMS} over a 10Hz to 100kHz bandwidth. Designed for use in battery-powered systems, the low 30μA quiescent current per output makes it an ideal choice. In shutdown, quiescent current drops to less than 0.1μA. Shutdown control is independent for each output, allowing for flexibility in power management. The device is capable of operating over an input voltage range of 1.8V to 20V. Output 1 can supply 500mA of output current with a dropout voltage of 320mV. The device can supply 100mA of output current from Output 2 with a dropout voltage of 300mV. Quiescent current is well controlled in dropout.

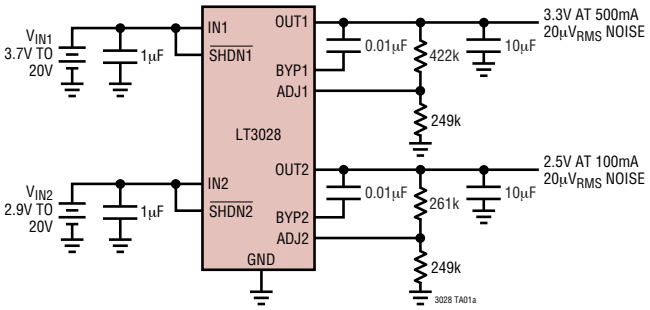
The LT3028 regulator is stable with output capacitors as low as 1μF for the 100mA output and 3.3μF for the 500mA output. Small ceramic capacitors can be used without the series resistance required by other regulators.

Internal protection circuitry includes reverse-battery protection, current limiting and thermal limiting protection. The device is available as an adjustable device with a 1.22V reference voltage. The LT3028 regulator is available in the thermally enhanced 16-lead TSSOP and 16-lead, low profile (5mm × 3mm × 0.75mm) DFN packages.

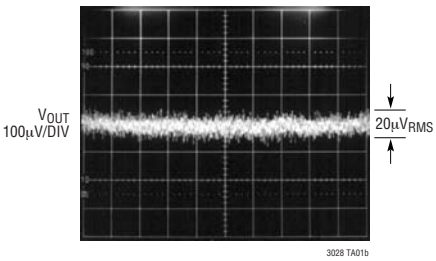
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TYPICAL APPLICATION

3.3V/2.5V Low Noise Regulators



10Hz to 100kHz Output Noise

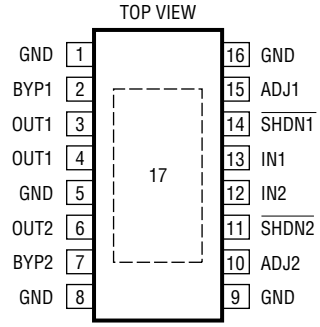


ABSOLUTE MAXIMUM RATINGS (Note 1)

IN1, IN2 Pin Voltage ..... ±20V
OUT1, OUT2 Pin Voltage ..... ±20V
Input-to-Output Differential Voltage ..... ±20V
ADJ1, ADJ2 Pin Voltage ..... ±7V
BYP1, BYP2 Pin Voltage ..... ±0.6V
$\overline{SHDN1}$, $\overline{SHDN2}$ Pin Voltage ..... ±20V
Output Short-Circut Duration ..... Indefinite

Operating Junction Temperature Range
(Note 2) ..... –40°C to 125°C
Storage Temperature Range
FE Package ..... –65°C to 150°C
DHC Package ..... –65°C to 125°C
Lead Temperature (Soldering, 10 sec) ..... 300°C

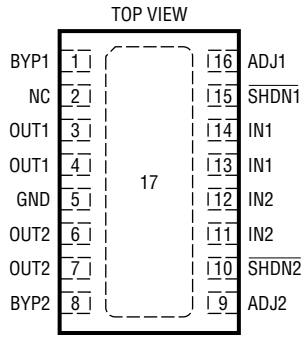
PACKAGE/ORDER INFORMATION



FE PACKAGE
16-LEAD PLASTIC TSSOP

T_{JMAX} = 150°C, θ_{JA} = 38°C/W, θ_{JC} = 8°C/W
EXPOSED PAD (PIN 17) IS GND
MUST BE SOLDERED TO PCB

ORDER PART NUMBER
LT3028EFE LT3028IFE
FE PART MARKING
3028EFE 3028IFE



DHC PACKAGE
16-LEAD (5mm × 3mm) PLASTIC DFN

T_{JMAX} = 125°C, θ_{JA} = 40°C/W, θ_{JC} = 10°C/W
EXPOSED PAD (PIN 17) IS GND
MUST BE SOLDERED TO PCB

ORDER PART NUMBER
LT3028EDHC LT3028IDHC
DHC PART MARKING
3028 3028I

Consult factory for parts specified with wider operating temperature ranges.

ELECTRICAL CHARACTERISTICS

The ● denotes specifications which apply over the full operating temperature range, otherwise specifications are T_A = 25°C. (Note 2)

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Minimum Input Voltage (Notes 3, 10)	Output 2, I_{LOAD} = 100mA Output 1, I_{LOAD} = 500mA	● ●		1.8 1.8	2.3 2.3	V V
ADJ1, ADJ2 Pin Voltage (Notes 3, 4)	V_{IN} = 2V, I_{LOAD} = 1mA Output 2, 2.3V < V_{IN2} < 20V, 1mA < I_{LOAD} < 100mA Output 1, 2.3V < V_{IN1} < 20V, 1mA < I_{LOAD} < 500mA	 ● ●	1.205 1.190 1.190	1.220 1.220 1.220	1.235 1.250 1.250	V V V
Line Regulation (Note 3)	ΔV_{IN} = 2V to 20V, I_{LOAD} = 1mA	●		1	10	mV
Load Regulation (Note 3)	Output 2, V_{IN2} = 2.3V, ΔI_{LOAD} = 1mA to 100mA V_{IN2} = 2.3V, ΔI_{LOAD} = 1mA to 100mA	 ●		1	12 25	mV mV
	Output 1, V_{IN1} = 2.3V, ΔI_{LOAD} = 1mA to 500mA V_{IN1} = 2.3V, ΔI_{LOAD} = 1mA to 500mA	 ●		1	12 25	mV mV

ELECTRICAL CHARACTERISTICS

The ● denotes specifications which apply over the full operating temperature range, otherwise specifications are T_A = 25°C. (Note 2)

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Dropout Voltage (Output 2) $V_{IN2} = V_{OUT2(NOMINAL)}$ (Notes 5, 6, 10)	I_{LOAD} = 1mA I_{LOAD} = 1mA	 ●		0.10	0.15 0.19	V V
	I_{LOAD} = 10mA I_{LOAD} = 10mA	 ●		0.17	0.22 0.29	V V
	I_{LOAD} = 50mA I_{LOAD} = 50mA	 ●		0.24	0.31 0.40	V V
	I_{LOAD} = 100mA I_{LOAD} = 100mA	 ●		0.30	0.35 0.45	V V
Dropout Voltage (Output 1) $V_{IN1} = V_{OUT1(NOMINAL)}$ (Notes 5, 6, 10)	I_{LOAD} = 10mA I_{LOAD} = 10mA	 ●		0.12	0.19 0.25	V V
	I_{LOAD} = 50mA I_{LOAD} = 50mA	 ●		0.17	0.22 0.32	V V
	I_{LOAD} = 100mA I_{LOAD} = 100mA	 ●		0.21	0.28 0.34	V V
	I_{LOAD} = 500mA I_{LOAD} = 500mA	 ●		0.32	0.37 0.47	V V
GND Pin Current (Output 2) $V_{IN2} = V_{OUT2(NOMINAL)}$ (Notes 5, 7)	I_{LOAD} = 0mA I_{LOAD} = 1mA I_{LOAD} = 10mA I_{LOAD} = 50mA I_{LOAD} = 100mA	● ● ● ● ●		25 60 230 1 2.2	50 95 400 2 4	µA µA µA mA mA
GND Pin Current (Output 1) $V_{IN1} = V_{OUT1(NOMINAL)}$ (Notes 5, 7)	I_{LOAD} = 0mA I_{LOAD} = 1mA I_{LOAD} = 50mA I_{LOAD} = 100mA I_{LOAD} = 250mA I_{LOAD} = 500mA	● ● ● ● ● ●		30 65 1 2 5 10	75 120 1.6 3 8 16	µA µA mA mA mA mA
Output Voltage Noise	C_{OUT} = 10µF, C_{BYP} = 0.01µF, I_{LOAD} = Full Current, BW = 10Hz to 100kHz			20		μV_{RMS}
ADJ1/ADJ2 Pin Bias Current	ADJ1, ADJ2 (Notes 3, 8)			30	100	nA
Shutdown Threshold	V_{OUT} = Off to On V_{OUT} = On to Off	● ●	 0.25	0.80 0.65	1.4	V V
$\overline{SHDN1}$/$\overline{SHDN2}$ Pin Current (Note 9)	$V_{\overline{SHDN1}}$, $V_{\overline{SHDN2}}$ = 0V $V_{\overline{SHDN1}}$, $V_{\overline{SHDN2}}$ = 20V	● ●		0 1	0.5 3.0	µA µA
Quiescent Current in Shutdown	V_{IN} = 6V, $V_{\overline{SHDN1}}$ = 0V, $V_{\overline{SHDN2}}$ = 0V			0.01	0.1	µA
Ripple Rejection	V_{IN} = 2.72V (Avg), V_{RIPPLE} = 0.5V_{P-P}, f_{RIPPLE} = 120Hz, I_{LOAD} = Full Current		55	65		dB
Current Limit	Output 2, V_{IN2} = 7V, V_{OUT2} = 0V V_{IN2} = 2.3V, ΔV_{OUT2} = –0.1V	 ●	 110	500		mA mA
	Output 1, V_{IN1} = 7V, V_{OUT1} = 0V V_{IN1} = 2.3V, ΔV_{OUT1} = –0.1V	 ●	 520	1.3		A mA
Input Reverse Leakage Current	V_{IN} = –20V, V_{OUT} = 0V	●			1	mA

Note 1: Absolute Maximum Ratings are those values beyond which the life of a device may be impaired.

Note 2: The LT3028 regulator is tested and specified under pulse load conditions such that $T_J \approx T_A$. The LT3028E is guaranteed to meet performance specifications from 0°C to 125°C junction temperature. Specifications over the –40°C to 125°C operating junction temperature range are assured by design, characterization and correlation with statistical process controls. The LT3028I is guaranteed and tested over the full –40°C to 125°C operating junction temperature range.

Note 3: The LT3028 is tested and specified for these conditions with the ADJ1/ADJ2 pin connected to the corresponding OUT1/OUT2 pin.

ELECTRICAL CHARACTERISTICS

Note 4: Operating conditions are limited by maximum junction temperature. The regulated output voltage specification will not apply for all possible combinations of input voltage and output current. When operating at maximum input voltage, the output current range must be limited. When operating at maximum output current, the input voltage range must be limited.

Note 5: To satisfy requirements for minimum input voltage, the LT3028 is tested and specified for these conditions with an external resistor divider (two 250k resistors) for an output voltage of 2.44V. The external resistor divider will add a 5μA DC load on the output.

Note 6: Dropout voltage is the minimum input to output voltage differential needed to maintain regulation at a specified output current. In dropout, the output voltage will be equal to: $V_{IN} - V_{DROPOUT}$.

Note 7: GND pin current is tested with V_{IN} = 2.44V and a current source load. This means the device is tested while operating in its dropout region or at the minimum input voltage specification. This is the worst-case GND pin current. The GND pin current will decrease slightly at higher input voltages. Total GND pin current is equal to the sum of GND pin currents from Output 1 and Output 2.

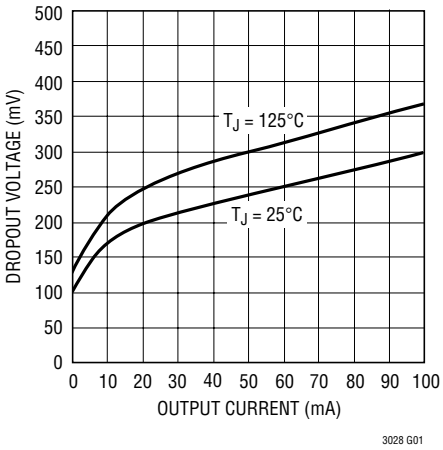
Note 8: ADJ1 and ADJ2 pin bias current flows into the pin.

Note 9: $\overline{SHDN1}$ and $\overline{SHDN2}$ pin current flows into the pin.

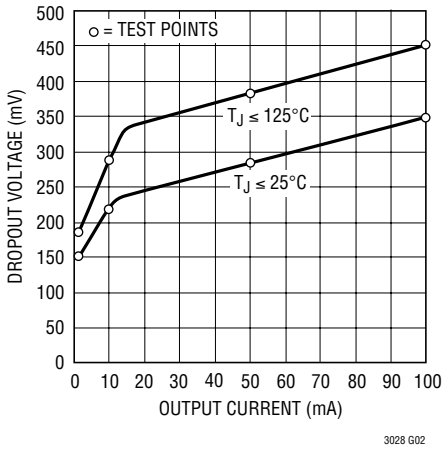
Note 10: For the LT3028 dropout voltage will be limited by the minimum input voltage specification under some output voltage/load conditions. See the curve of Minimum Input Voltage in the Typical Performance Characteristics.

TYPICAL PERFORMANCE CHARACTERISTICS

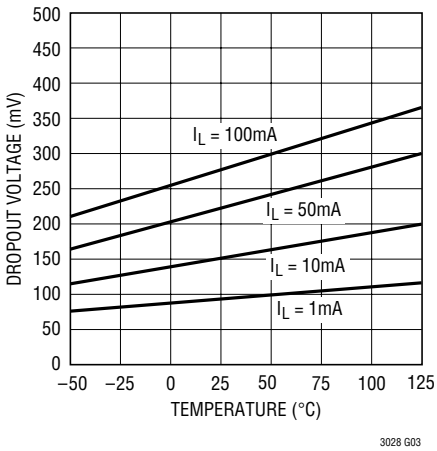
Output 2
Typical Dropout Voltage



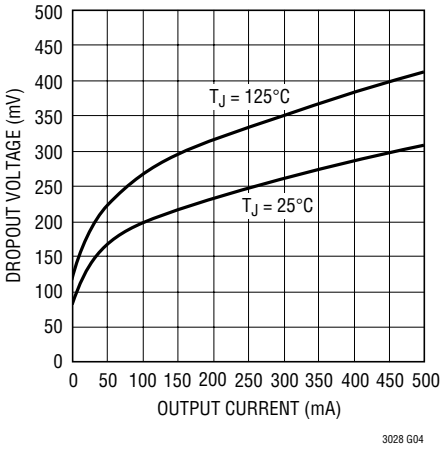
Output 2
Guaranteed Dropout Voltage



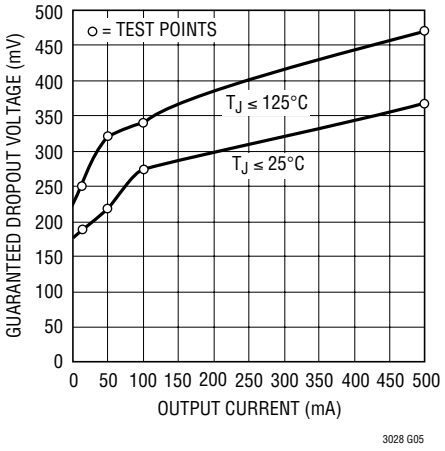
Output 2 Dropout Voltage



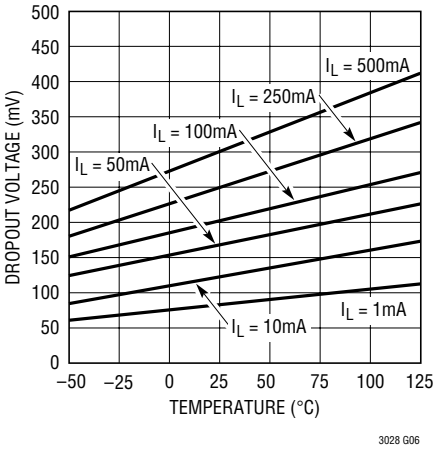
Output 1
Typical Dropout Voltage



Output 1
Guaranteed Dropout Voltage

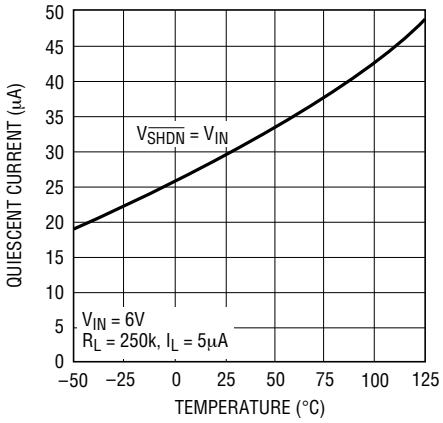


Output 1 Dropout Voltage

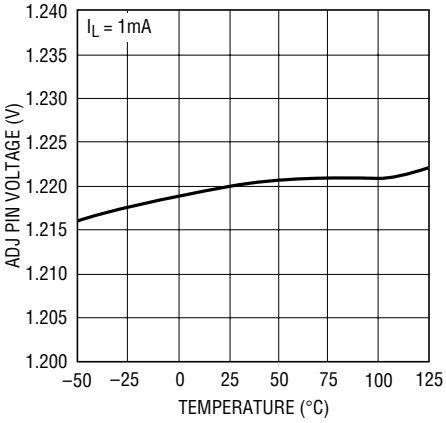


TYPICAL PERFORMANCE CHARACTERISTICS

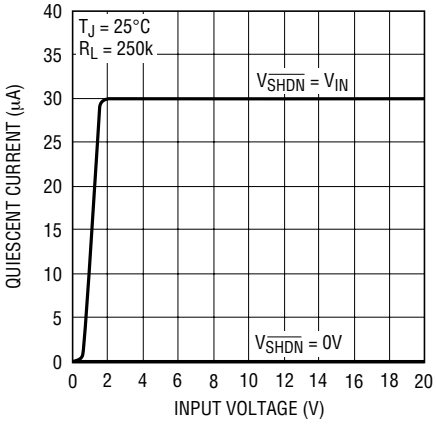
Quiescent Current (Per Output)



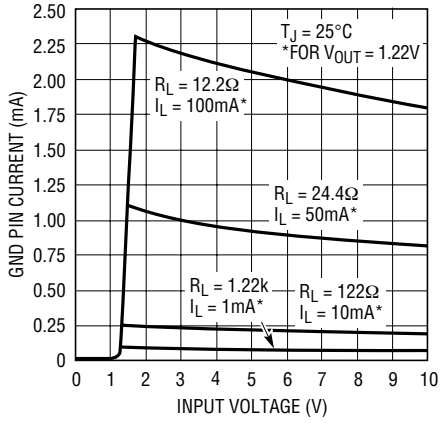
ADJ1 or ADJ2 Pin Voltage



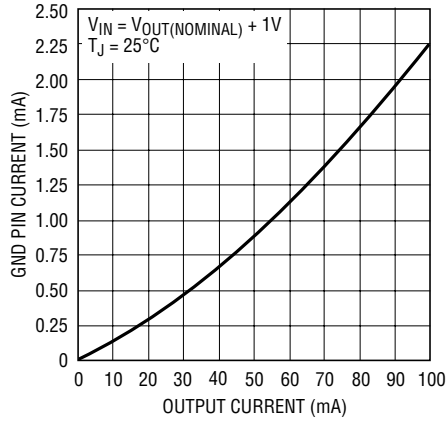
Quiescent Current (Per Output)



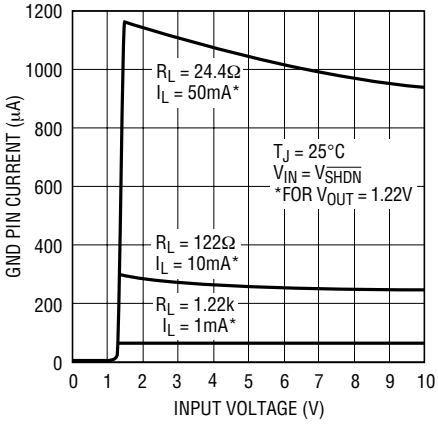
Output 2 GND Pin Current



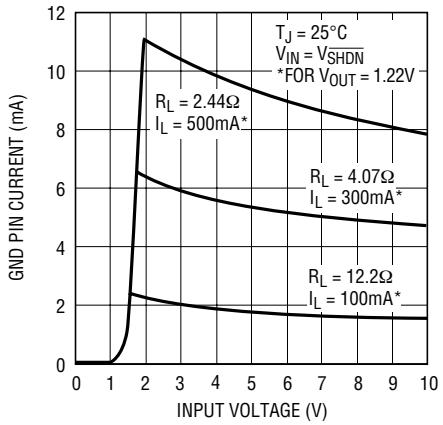
Output 2 GND Pin Current vs I_{LOAD}



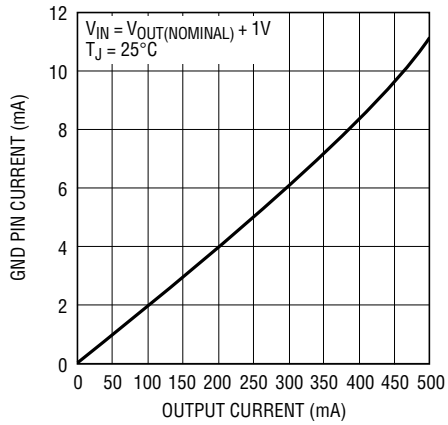
Output 1 GND Pin Current



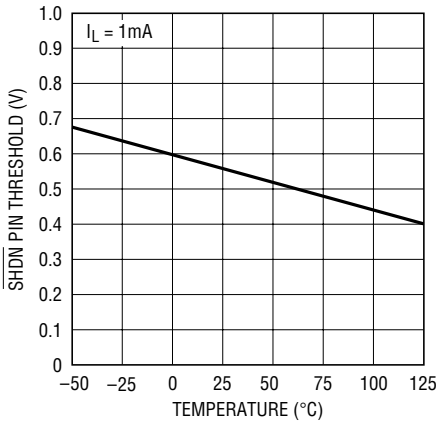
Output 1 GND Pin Current



Output 1 GND Pin Current vs I_{LOAD}

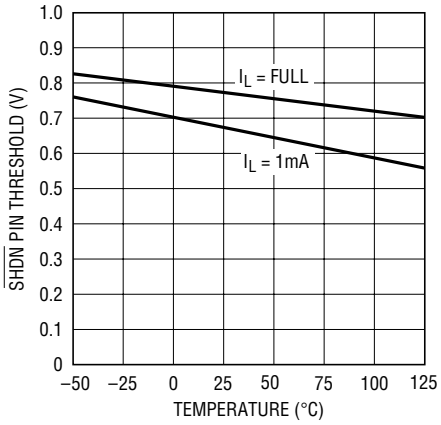


$\overline{SHDN1}$ or $\overline{SHDN2}$ Pin Threshold (On-to-Off)

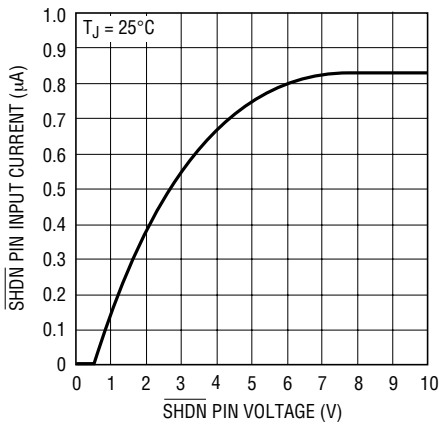


TYPICAL PERFORMANCE CHARACTERISTICS

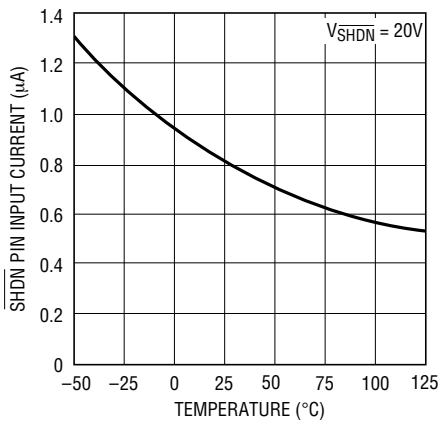
$\overline{SHDN1}$ or $\overline{SHDN2}$ Pin Threshold (Off-to-On)



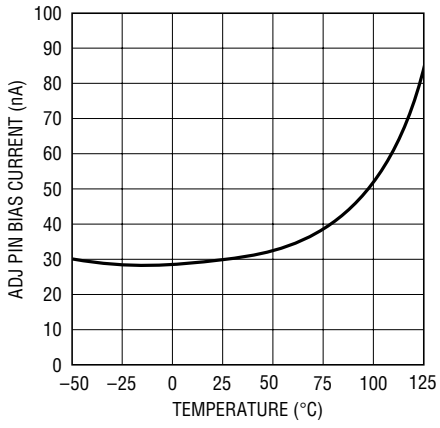
$\overline{SHDN1}$ or $\overline{SHDN2}$ Pin Input Current



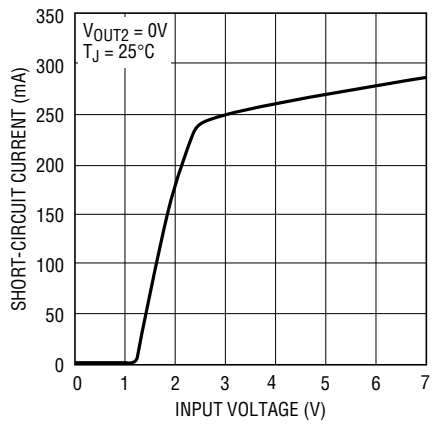
$\overline{SHDN1}$ or $\overline{SHDN2}$ Pin Input Current



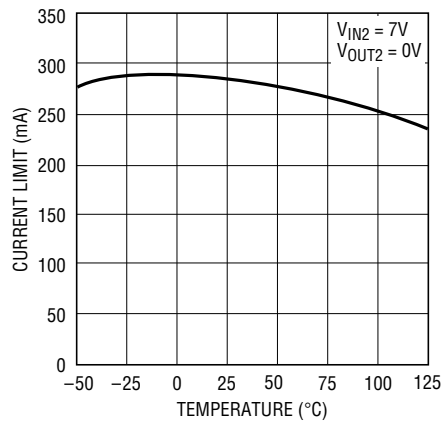
ADJ1 or ADJ2 Pin Bias Current



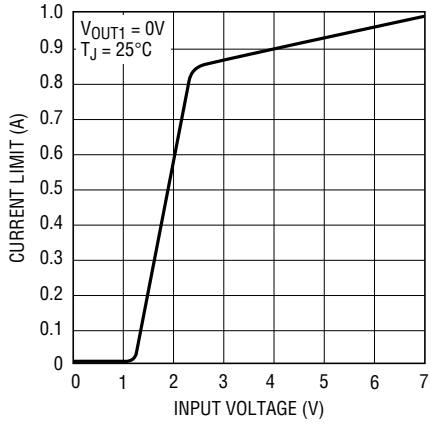
Output 2 Current Limit



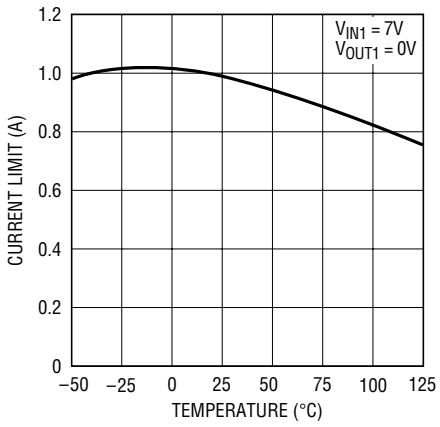
Output 2 Current Limit



Output 1 Current Limit

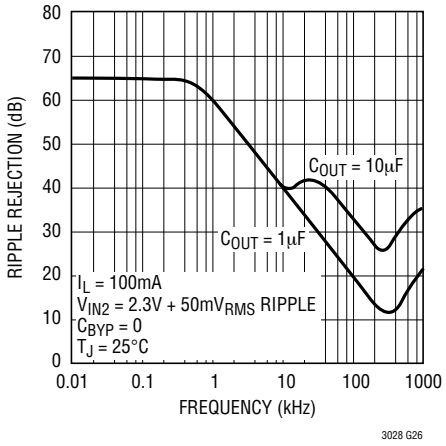


Output 1 Current Limit

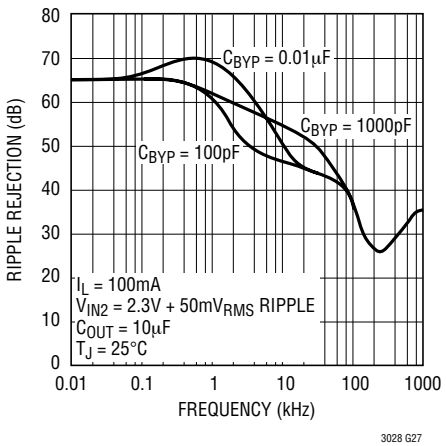


TYPICAL PERFORMANCE CHARACTERISTICS

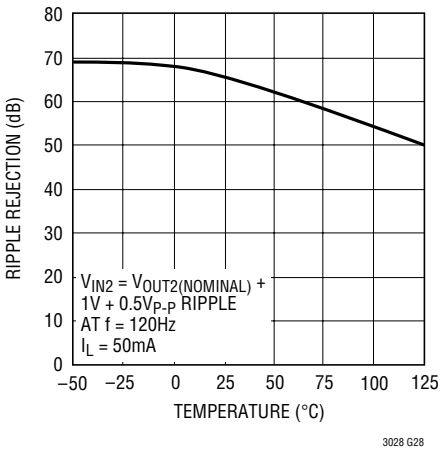
Output 2
Input Ripple Rejection



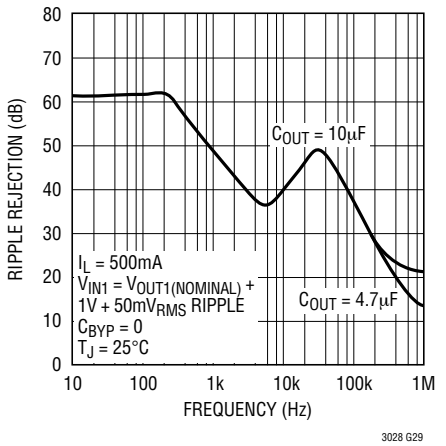
Output 2
Input Ripple Rejection



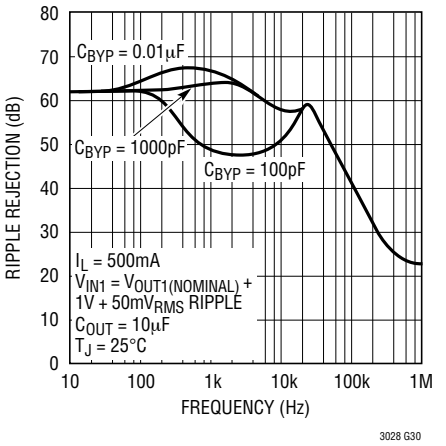
Output 2
Input Ripple Rejection



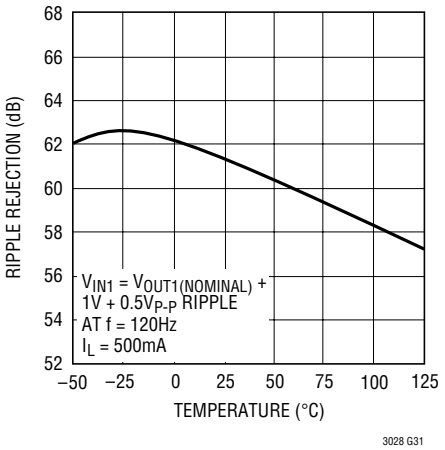
Output 1
Input Ripple Rejection



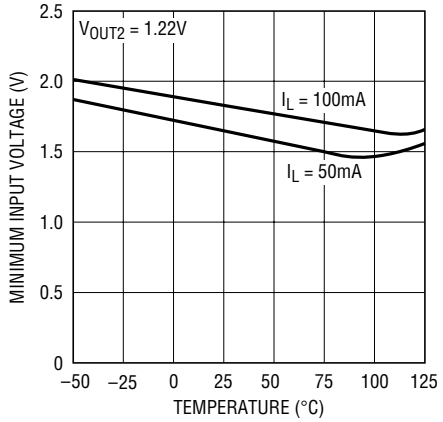
Output 1
Input Ripple Rejection



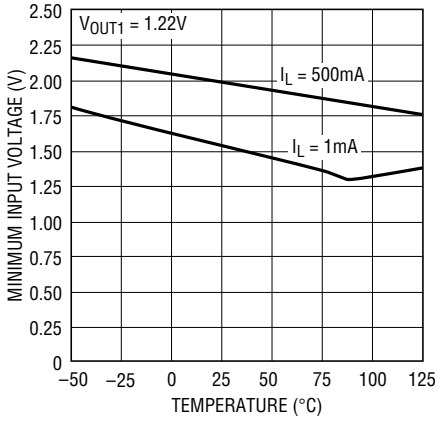
Output 1 Ripple Rejection



Output 2 Minimum Input Voltage

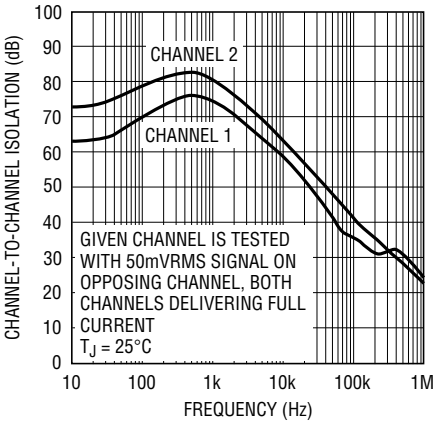


Output 1 Minimum Input Voltage

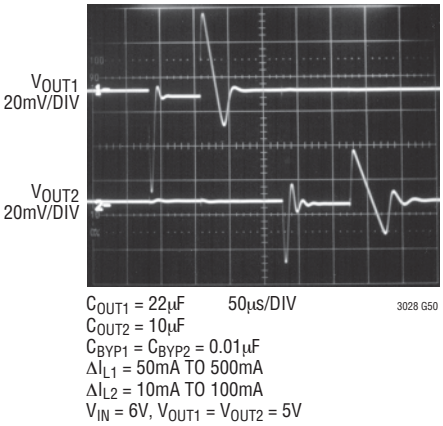


TYPICAL PERFORMANCE CHARACTERISTICS

Channel-to-Channel Isolation

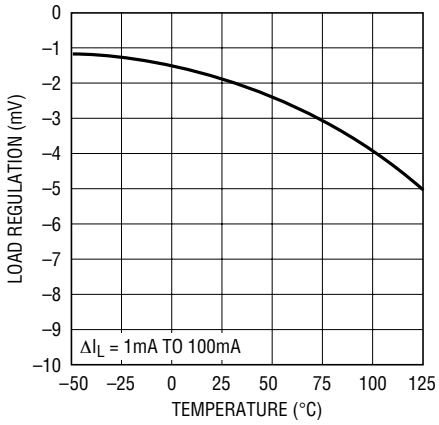


Channel-to-Channel Isolation

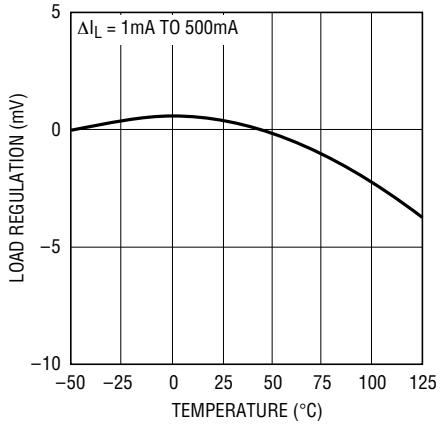


C_{OUT1} = 22µF
C_{OUT2} = 10µF
C_{BYP1} = C_{BYP2} = 0.01µF
ΔI_{L1} = 50mA TO 500mA
ΔI_{L2} = 10mA TO 100mA
V_{IN} = 6V, V_{OUT1} = V_{OUT2} = 5V

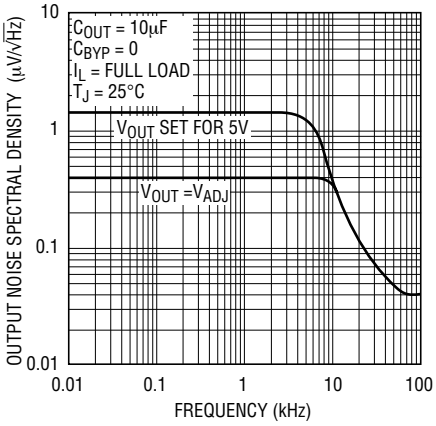
Output 2 Load Regulation



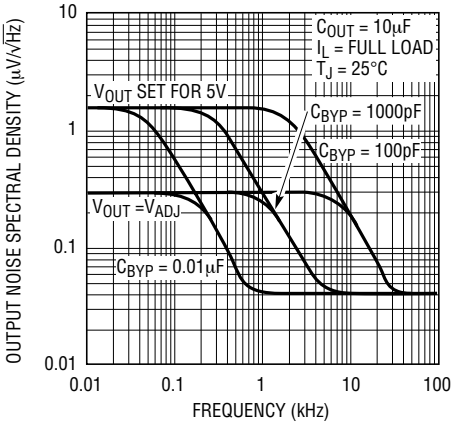
Output 1 Load Regulation



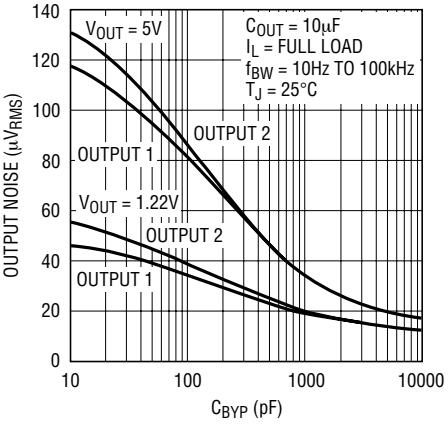
Output Noise Spectral Density



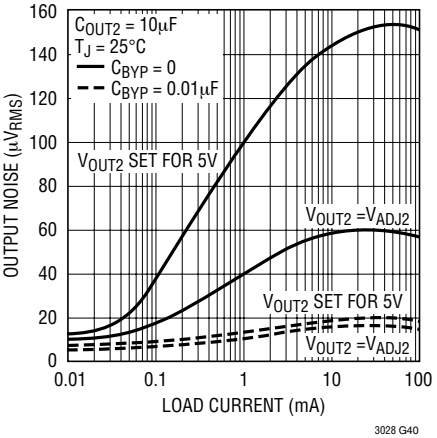
Output Noise Spectral Density



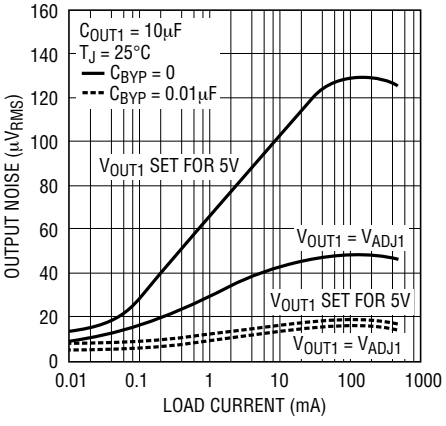
RMS Output Noise vs Bypass Capacitor



Output 2 RMS Output Noise vs Load Current (10Hz to 100kHz)

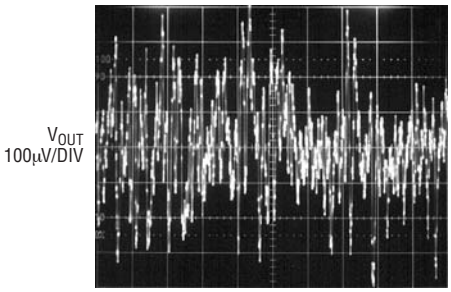


Output 1 RMS Output Noise vs Load Current (10Hz to 100kHz)



TYPICAL PERFORMANCE CHARACTERISTICS

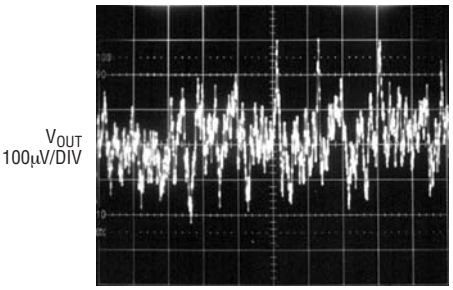
10Hz to 100kHz Output Noise
C_{BYP} = 0pF



C_{OUT} = 10µF 1ms/DIV
I_L = FULL LOAD
V_{OUT} SET FOR 5V

3028 G42

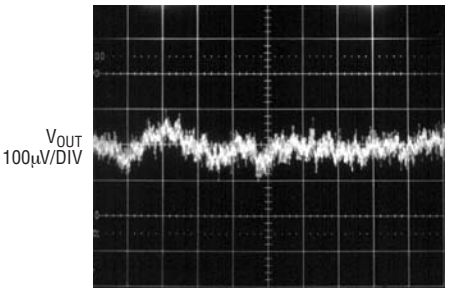
10Hz to 100kHz Output Noise
C_{BYP} = 100pF



C_{OUT} = 10µF 1ms/DIV
I_L = FULL LOAD
V_{OUT} SET FOR 5V

3028 G43

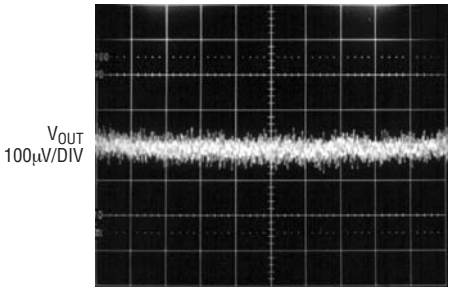
10Hz to 100kHz Output Noise
C_{BYP} = 1000pF



C_{OUT} = 10µF 1ms/DIV
I_L = FULL LOAD
V_{OUT} SET FOR 5V

3028 G44

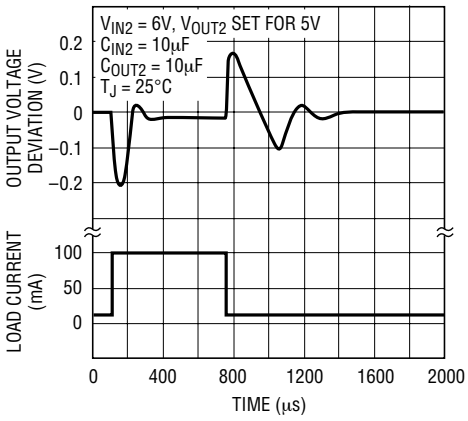
10Hz to 100kHz Output Noise
C_{BYP} = 0.01µF



C_{OUT} = 10µF 1ms/DIV
I_L = FULL LOAD
V_{OUT} SET FOR 5V

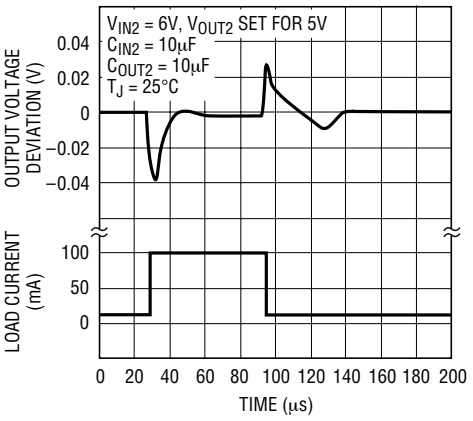
3028 G45

Output 2 Transient Response
C_{BYP} = 0pF



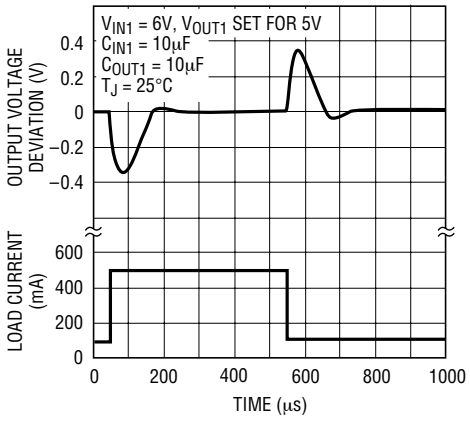
3028 G46

Output 2 Transient Response
C_{BYP} = 0.01µF



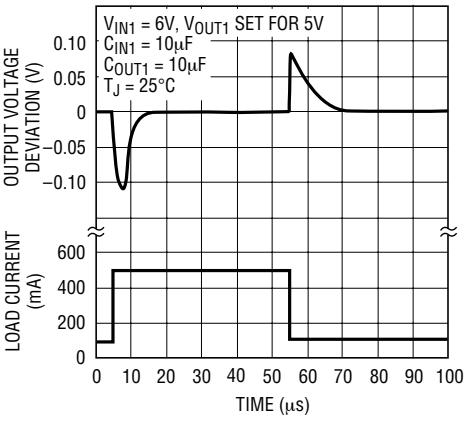
3028 G47

Output 1 Transient Response
C_{BYP} = 0pF



3028 G48

Output 1 Transient Response
C_{BYP} = 0.01µF



3028 G49

PIN FUNCTIONS (DFN Package)/(TSSOP Package)

GND (Pins 5, 17)/(Pins 1, 5, 8, 9, 16, 17): Ground. The Exposed Pad must be soldered to PCB ground for optimum thermal performance.

ADJ1/ADJ2 (Pins 16/9)/(Pins 15/10): Adjust Pin. These are the inputs to the error amplifiers. These pins are internally clamped to ±7V. They have a bias current of 30nA which flows into the pin (see curve of ADJ1/ADJ2 Pin Bias Current vs Temperature in the Typical Performance Characteristics section). The ADJ1 and ADJ2 pin voltage is 1.22V referenced to ground and the output voltage range is 1.22V to 20V.

BYP1/BYP2 (Pins 1/8)/(Pins 2/7): Bypass. The BYP1/BYP2 pins are used to bypass the reference of the LT3028 regulator to achieve low noise performance from the regulator. The BYP1/BYP2 pins are clamped internally to ±0.6V (one V_{BE}) from ground. A small capacitor from the corresponding output to this pin will bypass the reference to lower the output voltage noise. A maximum value of 0.01μF can be used for reducing output voltage noise to a typical 20μV_{RMS} over a 10Hz to 100kHz bandwidth. If not used, this pin must be left unconnected.

OUT1/OUT2 (Pins 3, 4/6, 7)/(Pins 3, 4/6): Output. The outputs supply power to the loads. A minimum output capacitor of 1μF is required to prevent oscillations on Output 2; Output 1 requires a minimum of 3.3μF. Larger output capacitors will be required for applications with large transient loads to limit peak voltage transients. See the Applications Information section for more information on output capacitance and reverse output characteristics.

$\overline{SHDN1}$/$\overline{SHDN2}$ (Pins 15/10)/(Pins 14/11): Shutdown. The $\overline{SHDN1}$/$\overline{SHDN2}$ pins are used to put the corresponding output of the LT3028 regulator into a low power shutdown state. The output will be off when the pin is pulled low. The $\overline{SHDN1}$/$\overline{SHDN2}$ pins can be driven either by 5V logic or open-collector logic with pull-up resistors. The pull-up resistors are required to supply the pull-up current of the open-collector gates, normally several microamperes, and the $\overline{SHDN1}$/$\overline{SHDN2}$ pin current, typically 1μA. If unused, the pin must be connected to V_{IN}. The device will not function if the $\overline{SHDN1}$/$\overline{SHDN2}$ pins are not connected.

IN1/IN2 (Pins 13, 14/11, 12)/(Pins 13/12): Inputs. Power is supplied to the device through the IN pins. A bypass capacitor is required on these pins if the device is more than six inches away from the main input filter capacitor. In general, the output impedance of a battery rises with frequency, so it is advisable to include a bypass capacitor in battery-powered circuits. A bypass capacitor in the range of 1μF to 10μF is sufficient. The LT3028 regulator is designed to withstand reverse voltages on the IN pins with respect to ground and the OUT pins. In the case of a reverse input, which can happen if a battery is plugged in backwards, the device will act as if there is a diode in series with its input. There will be no reverse current flow into the regulator and no reverse voltage will appear at the load. The device will protect both itself and the load.

APPLICATIONS INFORMATION

The LT3028 is a dual 100mA/500mA low dropout regulator with independent inputs, micropower quiescent current, and shutdown. The device is capable of supplying 100mA from Output 2 at a dropout voltage of 300mV. Output 1 delivers 500mA at a dropout voltage of 320mV. The two regulators have common GND pins and are thermally coupled, however, the two inputs and outputs of the LT3028 operate independently. They can be shut down independently and a fault condition on one output will not affect the other output electrically. Output voltage noise can be lowered to 20μV_{RMS} over a 10Hz to 100kHz bandwidth with the addition of a 0.01μF reference bypass capacitor. Additionally, the reference bypass capacitor will improve transient response of the regulator, lowering the settling time for transient load conditions. The low operating quiescent current (30μA per output) drops to less

APPLICATIONS INFORMATION

than 1μA in shutdown. In addition to the low quiescent current, the LT3028 regulator incorporates several protection features which make it ideal for use in battery-powered systems. The device is protected against reverse input voltages. Additionally, in dual supply applications where the regulator load is returned to a negative supply, the output can be pulled below ground by as much as 20V and still allow the device to start and operate.

Adjustable Operation

The LT3028 has an output voltage range of 1.22V to 20V. The output voltage is set by the ratio of two external resistors as shown in Figure 1. The device servos the output to maintain the corresponding ADJ pin voltage at 1.22V referenced to ground. The current in R1 is then equal to 1.22V/R1 and the current in R2 is the current in R1 plus the ADJ pin bias current. The ADJ pin bias current, 30nA at 25°C, flows through R2 into the ADJ pin. The output voltage can be calculated using the formula in Figure 1. The value of R1 should be no greater than 250k to minimize errors in the output voltage caused by the ADJ pin bias current. Note that in shutdown the output is turned off and the divider current will be zero. Curves of ADJ Pin Voltage vs Temperature and ADJ Pin Bias Current vs Temperature appear in the Typical Performance Characteristics.

The device is tested and specified with the ADJ pin tied to the corresponding OUT pin for an output voltage of 1.22V. Specifications for output voltages greater than 1.22V will be proportional to the ratio of the desired output voltage to 1.22V: V_{OUT}/1.22V. For example, load regulation on Output 2 for an output current change of 1mA to 100mA

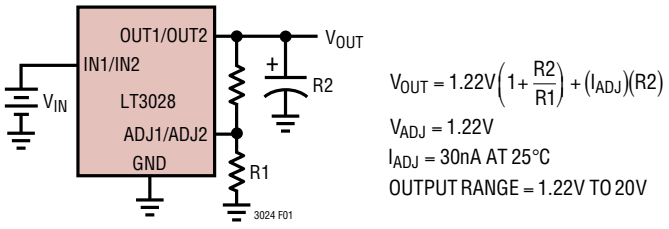


Figure 1. Adjustable Operation

is –1mV typical at V_{OUT} = 1.22V. At V_{OUT} = 12V, load regulation is:

(12V/1.22V)(–1mV) = –9.8mV

Bypass Capacitance and Low Noise Performance

The LT3028 regulator may be used with the addition of a bypass capacitor from V_{OUT} to the corresponding BYP pin to lower output voltage noise. A good quality low leakage capacitor is recommended. This capacitor will bypass the reference of the regulator, providing a low frequency noise pole. The noise pole provided by this bypass capacitor will lower the output voltage noise to as low as 20μV_{RMS} with the addition of a 0.01μF bypass capacitor. Using a bypass capacitor has the added benefit of improving transient response. With no bypass capacitor and a 10μF output capacitor, a 10mA to 100mA load step on Output 2 will settle to within 1% of its final value in less than 100μs. With the addition of a 0.01μF bypass capacitor, the output will stay within 1% for the same load step. Both outputs exhibit this improvement in transient response (see Transient Reponse in Typical Performance Characteristics section). However, regulator start-up time is inversely proportional to the size of the bypass capacitor, slowing to 15ms with a 0.01μF bypass capacitor and 10μF output capacitor.

Output Capacitance and Transient Response

The LT3028 regulator is designed to be stable with a wide range of output capacitors. The ESR of the output capacitor affects stability, most notably with small capacitors. A minimum output capacitor of 1μF with an ESR of 3Ω or less is recommended for Output 2 to prevent oscillations. A minimum output capacitor of 3.3μF with an ESR of 3Ω or less is recommended for Output 1. The LT3028 is a micropower device and output transient response will be a function of output capacitance. Larger values of output capacitance decrease the peak deviations and provide improved transient response for larger load current changes. Bypass capacitors, used to decouple individual components powered by the LT3028, will increase the effective output capacitor value. With larger capacitors

APPLICATIONS INFORMATION

used to bypass the reference (for low noise operation), larger values of output capacitors are needed. For 100pF of bypass capacitance on Output 2, 2.2μF of output capacitor is recommended. With a 330pF bypass capacitor or larger on this output, a 3.3μF output capacitor is recommended. For Output 1, 4.7μF of output capacitor is recommended for 100pF of bypass capacitance. With 1000pF or larger bypass capacitor on this output, a 6.8μF output capacitor is recommended. The shaded region of Figures 2 and 3 define the regions over which the LT3028 regulator is stable. The minimum ESR needed is defined by the amount of bypass capacitance used, while the maximum ESR is 3Ω.

Extra consideration must be given to the use of ceramic capacitors. Ceramic capacitors are manufactured with a variety of dielectrics, each with different behavior across temperature and applied voltage. The most common dielectrics used are Z5U, Y5V, X5R and X7R. The Z5U and Y5V dielectrics are good for providing high capacitances in a small package, but exhibit strong voltage and temperature coefficients as shown in Figures 4 and 5. When used with a 5V regulator, a 10μF Y5V capacitor can exhibit an effective value as low as 1μF to 2μF over the operating temperature range. The X5R and X7R dielectrics result in more stable characteristics and are more suitable for use as the output capacitor. The X7R type has better stability across temperature, while the X5R is less expensive and is available in higher values.

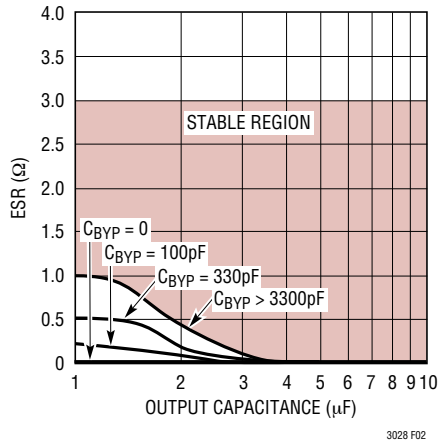


Figure 2. Output 2 Stability

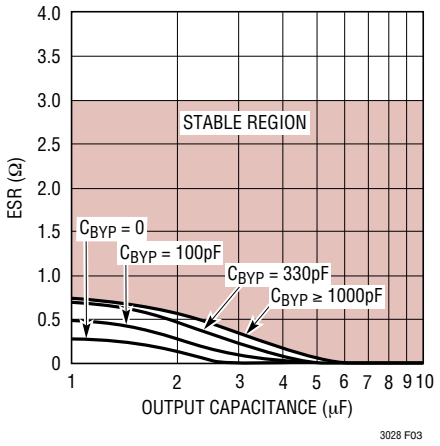


Figure 3. Output 1 Stability

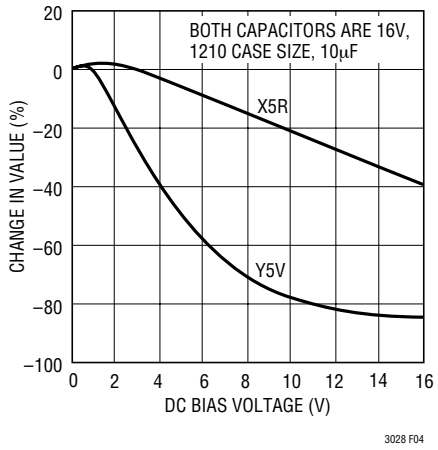


Figure 4. Ceramic Capacitor DC Bias Characteristics

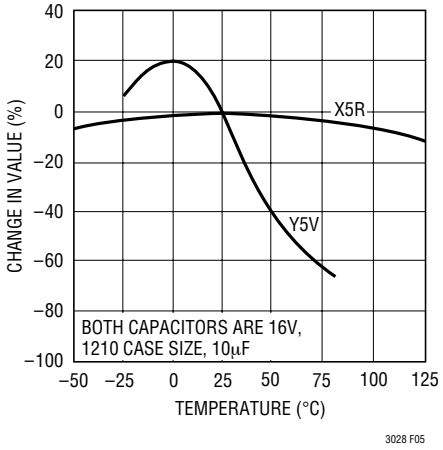


Figure 5. Ceramic Capacitor Temperature Characteristics

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Voltage and temperature coefficients are not the only sources of problems. Some ceramic capacitors have a piezoelectric response. A piezoelectric device generates voltage across its terminals due to mechanical stress, similar to the way a piezoelectric accelerometer or microphone works. For a ceramic capacitor the stress can be induced by vibrations in the system or thermal transients. The resulting voltages produced can cause appreciable amounts of noise, especially when a ceramic capacitor is used for noise bypassing. A ceramic capacitor produced Figure 6's trace in response to light tapping from a pencil. Similar vibration induced behavior can masquerade as increased output voltage noise.

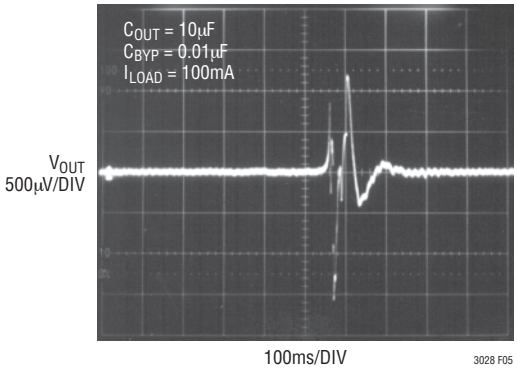


Figure 6. Noise Resulting from Tapping on a Ceramic Capacitor

Thermal Considerations

The power handling capability of the device will be limited by the maximum rated junction temperature (125°C). The power dissipated by the device will be made up of two components for each output:

1. Output current multiplied by the input/output voltage differential: $(I_{OUT})(V_{IN} – V_{OUT})$, and
2. GND pin current multiplied by the input voltage: $(I_{GND})(V_{IN})$.

The ground pin current can be found by examining the GND Pin Current curves in the Typical Performance Characteristics section. Power dissipation will be equal to the sum of the two components listed above.

The LT3028 regulator has internal thermal limiting designed to protect the device during overload conditions. For continuous normal conditions, the maximum junction temperature rating of 125°C must not be exceeded. It is important to give careful consideration to all sources of thermal resistance from junction to ambient. Additional heat sources mounted nearby must also be considered.

For surface mount devices, heat sinking is accomplished by using the heat spreading capabilities of the PC board and its copper traces. Copper board stiffeners and plated through-holes can also be used to spread the heat generated by power devices.

The following tables list thermal resistance for several different board sizes and copper areas. All measurements were taken in still air on 3/32" FR-4 board with one ounce copper.

Table 1. FE Package, 16-Lead TSSOP

COPPER AREA			THERMAL RESISTANCE
TOPSIDE*	BACKSIDE	BOARD AREA	(JUNCTION-TO-AMBIENT)
2500mm^2	2500mm^2	2500mm^2	38°C/W
1000mm^2	2500mm^2	2500mm^2	43°C/W
225mm^2	2500mm^2	2500mm^2	48°C/W
100mm^2	2500mm^2	2500mm^2	60°C/W

*Device is mounted on topside.

Table 2. DHC Package, 16-Lead DFN

COPPER AREA			THERMAL RESISTANCE
TOPSIDE*	BACKSIDE	BOARD AREA	(JUNCTION-TO-AMBIENT)
2500mm^2	2500mm^2	2500mm^2	40°C/W
1000mm^2	2500mm^2	2500mm^2	45°C/W
225mm^2	2500mm^2	2500mm^2	50°C/W
100mm^2	2500mm^2	2500mm^2	62°C/W

*Device is mounted on topside.

The thermal resistance junction-to-case (θ_{JC}), measured at the Exposed Pad on the back of the die is 10°C/W for the DFN package and 8°C/W for the TSSOP package.

Calculating Junction Temperature

Example: Given Output 1 set for an output voltage of 3.3V, Output 2 set for an output voltage of 2.5V, an input voltage range of 3.8V to 5V, an output current range of 0mA to 500mA for Output 1, an output current range of 0mA to 100mA for Output 2 and a maximum ambient temperature of 50°C, what will the maximum junction temperature be?

APPLICATIONS INFORMATION

The power dissipated by each output will be equal to:

$$I_{OUT(MAX)}(V_{IN(MAX)} - V_{OUT}) + I_{GND}(V_{IN(MAX)})$$

Where for Output 1:

$I_{OUT(MAX)}$ = 500mA
$V_{IN(MAX)}$ = 5V
I_{GND} at (I_{OUT} = 500mA, V_{IN} = 5V) = 9mA

For Output 2:

$I_{OUT(MAX)}$ = 100mA
$V_{IN(MAX)}$ = 5V
I_{GND} at (I_{OUT} = 100mA, V_{IN} = 5V) = 2mA

So for Output 1:

P = 500mA (5V – 3.3V) + 9mA (5V) = 0.90W

For Output 2:

P = 100mA (5V – 2.5V) + 2mA (5V) = 0.26W

The thermal resistance will be in the range of 35°C/W to 55°C/W depending on the copper area. So the junction temperature rise above ambient will be approximately equal to:

(0.90W + 0.26W) 50°C/W = 57.8°C

The maximum junction temperature will then be equal to the maximum junction temperature rise above ambient plus the maximum ambient temperature or:

T_{JMAX} = 50°C + 57.8°C = 107.8°C

Protection Features

The LT3028 regulator incorporates several protection features which make it ideal for use in battery-powered circuits. In addition to the normal protection features associated with monolithic regulators, such as current limiting and thermal limiting, the device is protected against reverse input voltages and reverse voltages from output to input. The two regulators have common inputs and GND pins and are thermally coupled, however, the two outputs of the LT3028 operate independently. They can be shut down independently and a fault condition on one output will not affect the other output electrically.

Current limit protection and thermal overload protection are intended to protect the device against current overload conditions at the output of the device. For normal operation, the junction temperature should not exceed 125°C.

The input of the device will withstand reverse voltages of 20V. Current flow into the device will be limited to less than 1mA (typically less than 100μA) and no negative voltage will appear at the output. The device will protect both itself and the load. This provides protection against batteries which can be plugged in backward.

The output of the LT3028 can be pulled below ground without damaging the device. If the input is left open circuit or grounded, the output can be pulled below ground by 20V. The output will act like an open circuit; no current will flow out of the pin. If the input is powered by a voltage source, the output will source the short-circuit current of the device and will protect itself by thermal limiting. In this case, grounding the $\overline{SHDN1}$/$\overline{SHDN2}$ pins will turn off the device and stop the output from sourcing the short-circuit current.

The ADJ pins can be pulled above or below ground by as much as 7V without damaging the device. If the input is left open circuit or grounded, the ADJ pins will act like an open circuit when pulled below ground and like a large resistor (typically 100k) in series with a diode when pulled above ground.

In situations where the ADJ pins are connected to a resistor divider that would pull the pins above their 7V clamp voltage if the output is pulled high, the ADJ pin input current must be limited to less than 5mA. For example, a resistor divider is used to provide a regulated 1.5V output from the 1.22V reference when the output is forced to 20V. The top resistor of the resistor divider must be chosen to limit the current into the ADJ pin to less than 5mA when the ADJ pin is at 7V. The 13V difference between output and ADJ pin divided by the 5mA maximum current into the ADJ pin yields a minimum top resistor value of 2.6k.

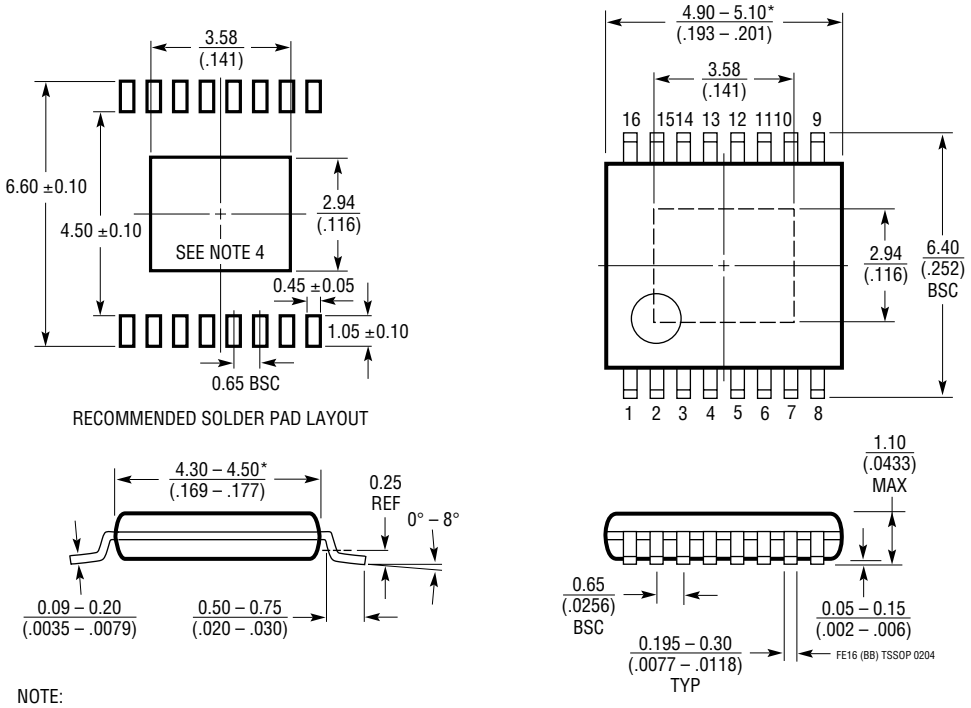
APPLICATIONS INFORMATION

In circuits where a backup battery is required, several different input/output conditions can occur. The output voltage may be held up while the input is either pulled to ground, pulled to some intermediate voltage or is left open circuit.

When the IN pin of the LT3028 is forced below either OUT pin or either OUT pin is pulled above the IN pin, input current for the corresponding regulator will typically drop to less than 2μA. This can happen if the input of the device is connected to a discharged (low voltage) battery and the output is held up by either a backup battery or a second regulator circuit. The state of the $\overline{SHDN1}/SHDN2$ pin will have no effect on the reverse output current when the output is pulled above the input.

PACKAGE DESCRIPTION

FE Package
16-Lead Plastic TSSOP (4.4mm)
(Reference LTC DWG # 05-08-1663)
Exposed Pad Variation BB

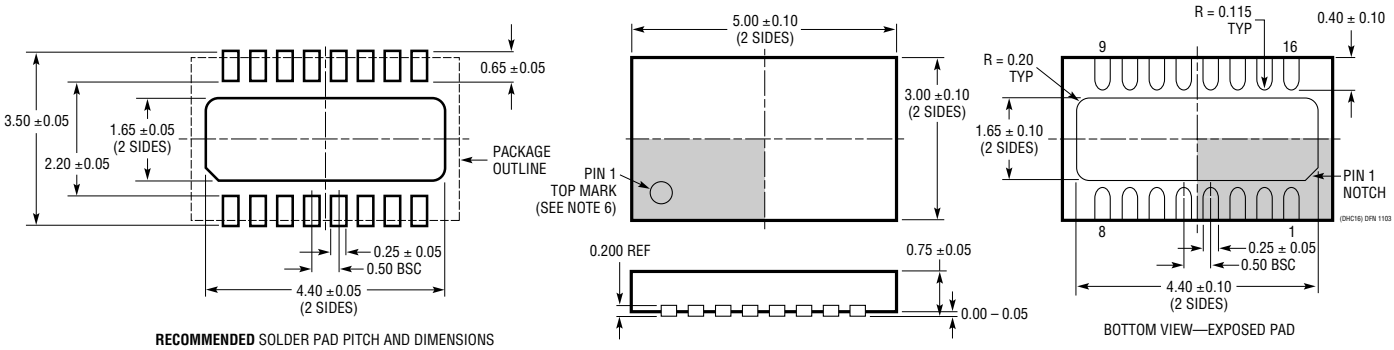


NOTE:
1. CONTROLLING DIMENSION: MILLIMETERS
2. DIMENSIONS ARE IN $\frac{\text{MILLIMETERS}}{\text{(INCHES)}}$
3. DRAWING NOT TO SCALE
4. RECOMMENDED MINIMUM PCB METAL SIZE FOR EXPOSED PAD ATTACHMENT
*DIMENSIONS DO NOT INCLUDE MOLD FLASH. MOLD FLASH SHALL NOT EXCEED 0.150mm (.006") PER SIDE

Information furnished by Linear Technology Corporation is believed to be accurate and reliable. However, no responsibility is assumed for its use. Linear Technology Corporation makes no representation that the interconnection of its circuits as described herein will not infringe on existing patent rights.

PACKAGE DESCRIPTION

DHC Package
16-Lead Plastic DFN (5mm × 3mm)
(Reference LTC DWG # 05-08-1706)



NOTE:
1. DRAWING PROPOSED TO BE MADE VARIATION OF VERSION (WJED-1) IN JEDEC PACKAGE OUTLINE MO-229
2. DRAWING NOT TO SCALE
3. ALL DIMENSIONS ARE IN MILLIMETERS
4. DIMENSIONS OF EXPOSED PAD ON BOTTOM OF PACKAGE DO NOT INCLUDE MOLD FLASH. MOLD FLASH, IF PRESENT, SHALL NOT EXCEED 0.15mm ON ANY SIDE
5. EXPOSED PAD SHALL BE SOLDER PLATED
6. SHADED AREA IS ONLY A REFERENCE FOR PIN 1 LOCATION ON THE TOP AND BOTTOM OF PACKAGE

RELATED PARTS

PART NUMBER	DESCRIPTION	COMMENTS
LT1129	700mA, Micropower, LDO	V_{IN}: 4.2V to 30V, $V_{OUT(MIN)}$ = 3.75V, I_Q = 50μA, I_{SD} < 16μA, DD, SOT-223, S8,TO220, TSSOP20 Packages
LT1175	500mA, Micropower Negative LDO	Guaranteed Voltage Tolerance and Line/Load Regulation V_{IN}: –20V to –4.3V, $V_{OUT(MIN)}$ = –3.8V, I_Q = 45μA, I_{SD} < 10μA, DD,SOT-223, S8 Packages
LT1185	3A, Negative LDO	Accurate Programmable Current Limit, Remote Sense V_{IN}: –35V to –4.2V, $V_{OUT(MIN)}$ = –2.40V, I_Q = 2.5mA, I_{SD} < 1μA, TO220-5 Package
LT1761	100mA, Low Noise Micropower, LDO	Low Noise < 20μV_{RMS}, Stable with 1μF Ceramic Capacitors, V_{IN}: 1.8V to 20V, $V_{OUT(MIN)}$ = 1.22V, I_Q = 20μA, I_{SD} < 1μA, ThinSOT Package
LT1762	150mA, Low Noise Micropower, LDO	Low Noise < 20μV_{RMS}, V_{IN}: 1.8V to 20V, $V_{OUT(MIN)}$ = 1.22V, I_Q = 25μA, I_{SD} < 1μA, MS8 Package
LT1763	500mA, Low Noise Micropower, LDO	Low Noise < 20μV_{RMS}, V_{IN}: 1.8V to 20V, $V_{OUT(MIN)}$ = 1.22V, I_Q = 30μA, I_{SD} < 1μA, S8 Package
LT1764/LT1764A	3A, Low Noise, Fast Transient Response, LDO	Low Noise < 40μV_{RMS}, "A" Version Stable with Ceramic Capacitors, V_{IN}: 2.7V to 20V, $V_{OUT(MIN)}$ = 1.21V, I_Q = 1mA, I_{SD} < 1μA, DD, TO220 Packages
LTC1844	150mA, Very Low Drop-Out LDO	Low Noise < 30μV_{RMS}, Stable with 1μF Ceramic Capacitors, V_{IN}: 1.6V to 6.5V, $V_{OUT(MIN)}$ = 1.25V, I_Q = 40μA, I_{SD} < 1μA, ThinSOT Package
LT1962	300mA, Low Noise Micropower, LDO	Low Noise < 20μV_{RMS}, V_{IN}: 1.8V to 20V, $V_{OUT(MIN)}$ = 1.22V, I_Q = 30μA, I_{SD} < 1μA, MS8 Package
LT1963/LT1963A	1.5A, Low Noise, Fast Transient Response, LDO	Low Noise < 40μV_{RMS}, "A" Version Stable with Ceramic Capacitors, V_{IN}: 2.1V to 20V, $V_{OUT(MIN)}$ = 1.21V, I_Q = 1mA, I_{SD} < 1μA, DD, TO220, SOT-223, S8 Packages
LT1964	200mA, Low Noise Micropower, Negative LDO	Low Noise < 30μV_{RMS}, Stable with Ceramic Capacitors, V_{IN}: –0.9V to –20V, $V_{OUT(MIN)}$ = –1.21V, I_Q = 30μA, I_{SD} < 3μA, ThinSOT Package
LT3023	Dual 100mA, Low Noise, Micropower LDO	Low Noise < 20μV_{RMS}, Stable with 1μF Ceramic Capacitors, V_{IN}: 1.8V to 20V, $V_{OUT(MIN)}$ = 1.22V, I_Q = 40μA, I_{SD} < 1μA, MS10E, DFN Packages
LT3024	Dual 100mA/500mA, Low Noise, Micropower LDO	Low Noise < 20μV_{RMS}, Stable with 1μF Ceramic Capacitors, V_{IN}: 1.8V to 20V, $V_{OUT(MIN)}$ = 1.22V, I_Q = 30μA, I_{SD} < 1μA, DFN, TSSOP Packages

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