140V CMOS Rail-to-Rail Output, Picoamp Input Current Op Amp

FEATURES

- **Supply Range: ±4.75V to ±70V (140V)**
- **0.1Hz to 10Hz Noise: 3.5μV_{P-P}**
- **Input Bias Current: 50pA**
- **Low Offset Voltage: 1.6mV Maximum**
- Rail-to-Rail Output Stage
- Output Sink and Source 10mA
- 10MHz Gain Bandwidth Product
- 19V/μs Slew Rate
- 11nV/√Hz Noise Density
- Thermal Shutdown
- Available in Thermally Enhanced SOIC-8E or TSSOP-16E Packages

APPLICATIONS

- ATE
- Piezo Drivers
- Photodiode Amplifier
- High Voltage Regulators
- Optical Networking

DESCRIPTION

The LTC®6090 is a high voltage precision operational amplifier. The low noise, low bias current input stage is ideal for high gain configurations. The LTC6090 has low input offset voltage, a rail-to-rail output stage, and can be run from a single 140V or split ±70V supplies.

The LTC6090 is internally protected against overtemperature conditions. A thermal warning output, $\overline{TFLAG}$, goes active when the die temperature approaches 150°C. The output stage can be turned off with the output disable pin $\overline{OD}$. By tying the $\overline{OD}$ pin to the thermal warning output, the part will disable the output stage when it is out of the safe operating area. These pins easily interface to any logic family.

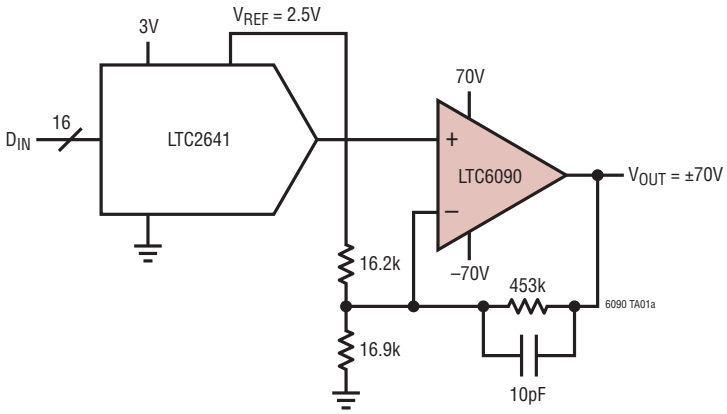
The LTC6090 is unity gain stable with up to a 200pF output capacitor. A wide input and output common mode range along with many features makes the LTC6090 useful for many high voltage applications.

The LTC6090 is available in an 8-lead SO and 16-lead TSSOP with exposed pad for low thermal resistance.

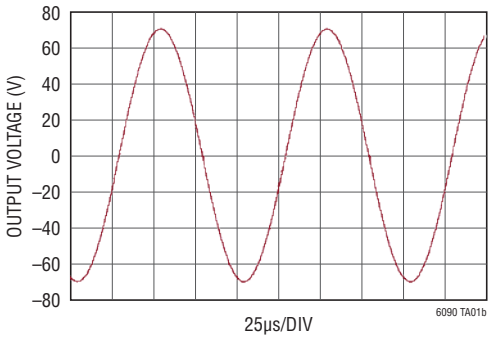
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TYPICAL APPLICATION

High Voltage DAC Buffer Application



140V_{P-P} Sine Wave Output

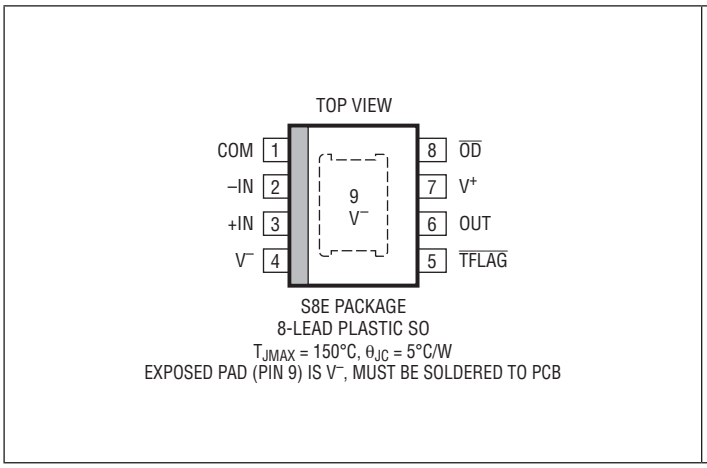


ABSOLUTE MAXIMUM RATINGS (Note 1)

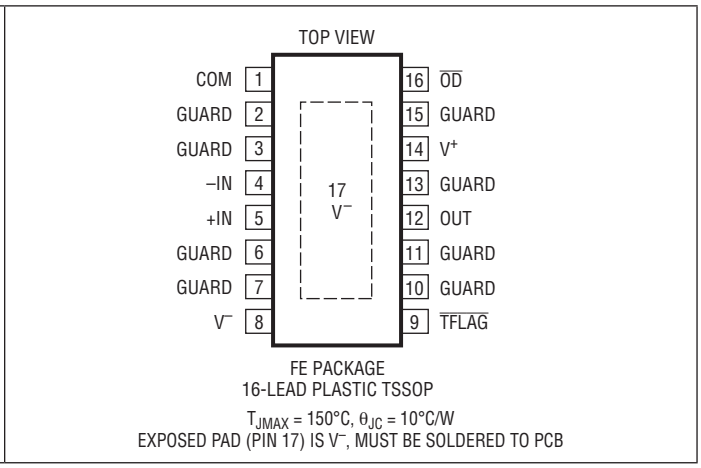
Total Supply Voltage (V^+ to V^-) 150V
COM ..... V^- to V^+
Input Voltage
  $\overline{OD}$ ..... V^- to V^+ + 0.3V
  +IN, –IN, ... V^- – 0.3V to V^+ + 0.3V
  $\overline{OD}$ to COM ..... 0V to 6V
Input Current
  +IN, –IN ..... ±10mA
$\overline{TFLAG}$ Output
  $\overline{TFLAG}$ ..... V^- – 0.3V to V^+ + 0.3V
  $\overline{TFLAG}$ to COM ..... –0.3V to 6V
Output Current
  OUT Short-Circuit Duration (Note 2) ..... Indefinite
Operating Junction Temperature Range
(Note 3) ..... –40°C to 125°C
Specified Junction Temperature Range (Note 4)
  LTC6090C ..... 0°C to 70°C
  LTC6090I ..... –40°C to 85°C
  LTC6090H ..... –40°C to 125°C
Junction Temperature (Note 5) ..... 150°C
Storage Temperature Range ..... –65°C to 150°C
Lead Temperature (Soldering, 10 sec) ..... 300°C

ESD Sensitive: The input pins (+IN and –IN) to this device are sensitive to ESD. Any ESD of 250V (HBM) or greater may result in elevated input bias current. Please use proper precautionary measures to avoid electrical damage.

PIN CONFIGURATION



S8E PACKAGE
8-LEAD PLASTIC SO
T_{JMAX} = 150°C, θ_{JC} = 5°C/W
EXPOSED PAD (PIN 9) IS V^-, MUST BE SOLDERED TO PCB



FE PACKAGE
16-LEAD PLASTIC TSSOP
T_{JMAX} = 150°C, θ_{JC} = 10°C/W
EXPOSED PAD (PIN 17) IS V^-, MUST BE SOLDERED TO PCB

ORDER INFORMATION

LEAD FREE FINISH	TAPE AND REEL	PART MARKING*	PACKAGE DESCRIPTION	JUNCTION TEMPERATURE RANGE
LTC6090CS8E#PBF	LTC6090CS8E#TRPBF	6090	8-Lead Plastic SO	0°C to 70°C
LTC6090IS8E#PBF	LTC6090IS8E#TRPBF	6090	8-Lead Plastic SO	–40°C to 85°C
LTC6090HS8E#PBF	LTC6090HS8E#TRPBF	6090	8-Lead Plastic SO	–40°C to 125°C
LTC6090CFE#PBF	LTC6090CFE#TRPBF	6090FE	16-Lead Plastic TSSOP	0°C to 70°C
LTC6090IFE#PBF	LTC6090IFE#TRPBF	6090FE	16-Lead Plastic TSSOP	–40°C to 85°C
LTC6090HFE#PBF	LTC6090HFE#TRPBF	6090FE	16-Lead Plastic TSSOP	–40°C to 125°C

Consult LTC Marketing for parts specified with wider operating temperature ranges. *The temperature grade is identified by a label on the shipping container.
Consult LTC Marketing for information on non-standard lead based finish parts.

For more information on lead free part marking, go to: http://www.linear.com/leadfree/
For more information on tape and reel specifications, go to: http://www.linear.com/tapeandreel/

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_J = 25°C. Test conditions are V^+ = 70V, V^- = –70V, V_{CM} = V_{OUT} = 0V, $V_{\overline{OD}}$ = Open unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS		C-, I-SUFFIXES MIN	C-, I-SUFFIXES TYP	C-, I-SUFFIXES MAX	H-SUFFIX MIN	H-SUFFIX TYP	H-SUFFIX MAX	UNITS
V_{OS}	Input Offset Voltage		 ●		±330 ±330	±1000 ±1600		±330 ±330	±1000 ±1600	µV µV
$\Delta V_{OS}/\Delta T$	Input Offset Voltage Drift		●		4			4		µV/°C
I_B	Input Bias Current (Note 6)	Supply Voltage = ±70V Supply Voltage = ±15V Supply Voltage = ±15V	 ●		3 3	 50		3 3	 800	pA pA pA
I_{OS}	Input Offset Current (Note 6)	Supply Voltage = ±15V	 ●		0.5	 30		0.5	 120	pA pA
e_n	Input Noise Voltage Density	f = 1kHz f = 10kHz			14 11			14 11		nV/√Hz nV/√Hz
	Input Noise Voltage	0.1Hz to 10Hz			3.5			3.5		μV_{P-P}
i_n	Input Noise Current Density				1			1		fA/√Hz
V_{CM}	Input Common Mode Range	Guaranteed by CMRR	 ●		±68	 V^+–3V		±68	 V^+–3V	V V
C_{IN}	Common Mode Input Capacitance				9			9		pF
C_{DIFF}	Differential Input Capacitance				5			5		pF
CMRR	Common Mode Rejection Ratio	V_{CM} = –67V to 67V	 ●	105 100	125		105 100	125		dB dB
PSRR	Power Supply Rejection Ratio	V_S = ±4.75V to ±70V	 ●	105 100	118		105 100	118		dB dB
V_{OUT}	Output Voltage Swing High (Referred to V^+)	No Load I_{SOURCE} = 1mA I_{SOURCE} = 10mA	● ● ●		25 100 750	50 200 1500		25 100 750	50 200 1500	mV mV mV
	Output Voltage Swing Low (Referred to V^-)	No Load I_{SINK} = 1mA I_{SINK} = 10mA	● ● ●		10 40 250	25 80 600		10 40 250	25 80 600	mV mV mV
A_{VOL}	Large-Signal Voltage Gain	R_L = 10k, V_{OUT} from –60V to 60V	 ●	500 400	12000		500 400	12000		V/mV V/mV

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_J = 25°C. Test conditions are V^+ = 70V, V^- = –70V, V_{CM} = V_{OUT} = 0V, $V_{\overline{OD}}$ = Open unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS		C-, I-SUFFIXES MIN	C-, I-SUFFIXES TYP	C-, I-SUFFIXES MAX	H-SUFFIX MIN	H-SUFFIX TYP	H-SUFFIX MAX	UNITS
I_{SC}	Output Short-Circuit Current (Source and Sink) Supply Voltage = ±15V	Supply Voltage = ±70V	 ●	 15	50		 15	50		mA mA
SR	Slew Rate	A_V = –2, R_L = 10k	 ●	 8	19		 8	19		V/µs V/µs
GBW	Gain-Bandwidth Product	f_{TEST} = 20kHz, R_L = 10k	 ●	 5	10		 4	10		MHz MHz
Φ_M	Phase Margin	R_L = 10k, C_L = 50pF			52			52		Deg
FPBW	Full Power Bandwidth	V_O = 125V_{P-P}	 ●	25 20			25 20			kHz kHz
t_S	Settling Time 0.1%	V_{STEP} = 1V, Av = 1, R_L = 10k			2			2		µs
I_S	Supply Current	No Load	 ●		2.7	3.9 4.2		2.7	3.9 4.5	mA mA
V_S	Supply Voltage Range	Guaranteed by the PSRR Test	●	9.5		140	9.5		140	V
$\overline{OD}_H$ $\overline{OD}_L$	$\overline{OD}$ Pin Voltage, Referenced to COM Pin	V_{IH} V_{IL}	● ●	COM+2.5V		 COM+0.65V	COM+2.5V		 COM+0.65V	V V
	Amplifier DC Output Impedance, Disabled	DC, $\overline{OD}$ = COM			450			450		kΩ
COM_{CM}	COM Pin Voltage Range		●	V^-		V^+ – 5	V^-		V^+ – 5	V
COM_V	COM Pin Open Circuit Voltage		●	20	21	22.5	20	21	22.5	V
COM_R	COM Pin Resistance		●	500	665	850	500	665	850	kΩ
$TEMP_F$	Die Temperature Where $\overline{TFLAG}$ Is Active		●		145			145		°C
$TEMP_{HYS}$	$\overline{TFLAG}$ Output Hysteresis		●		5			5		°C
$I_{\overline{TFLAG}}$	$\overline{TFLAG}$ Pull-Down Current	$\overline{TFLAG}$ Output Voltage = 0V	●	70	120	170	70	120	170	µA

Note 1: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to any Absolute Maximum Rating condition for extended periods may affect device reliability and lifetime.

Note 2: A heat sink may be required to keep the junction temperature below the absolute maximum rating when the output is shorted indefinitely.

Note 3: The LTC6090C/LTC6090I are guaranteed functional over the operating junction temperature range –40°C to 85°C. The LTC6090H is guaranteed functional over the operating junction temperature range –40°C to 125°C. Specifying the junction temperature range as an operating condition is applicable for devices with potentially significant quiescent power dissipation.

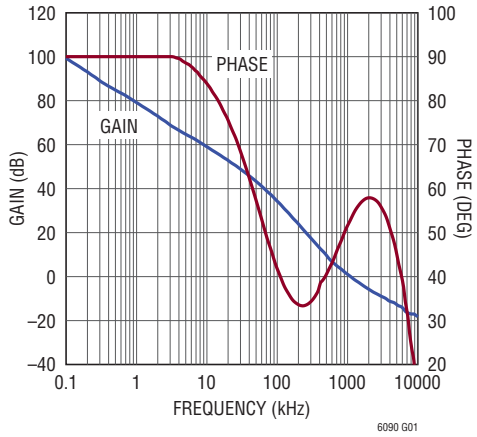
Note 4: The LTC6090C is guaranteed to meet specified performance from 0°C to 70°C. The LTC6090C is designed, characterized, and expected to meet specified performance from –40°C to 85°C but is not tested or QA sampled at these temperatures. The LTC6090I is guaranteed to meet specified performance from –40°C to 85°C. The LTC6090H is guaranteed to meet specified performance from –40°C to 125°C.

Note 5: This device includes over temperature protection that is intended to protect the device during momentary overload conditions. Operation above the specified maximum operating junction temperature is not recommended.

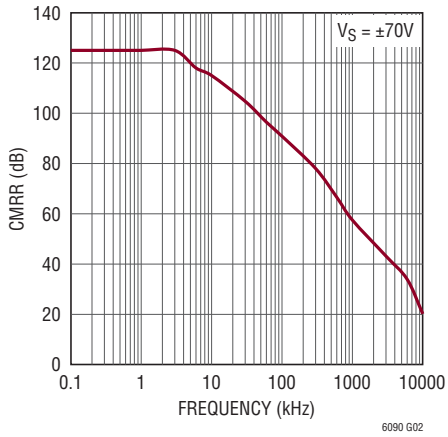
Note 6: Input bias and offset current is production tested with ±15V supplies. See Typical Performance Characteristics curves of actual typical performance over full supply range.

TYPICAL PERFORMANCE CHARACTERISTICS

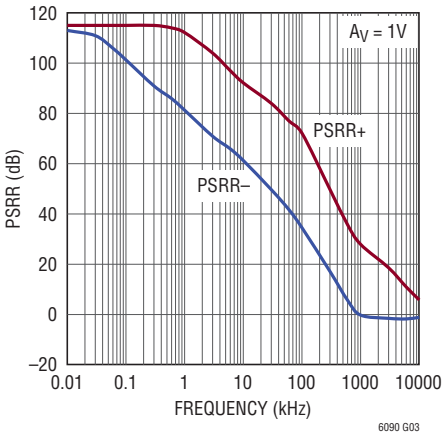
A_{VOL} and Phase vs Frequency



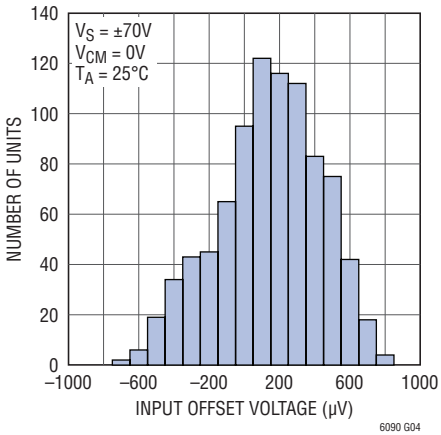
CMRR vs Frequency



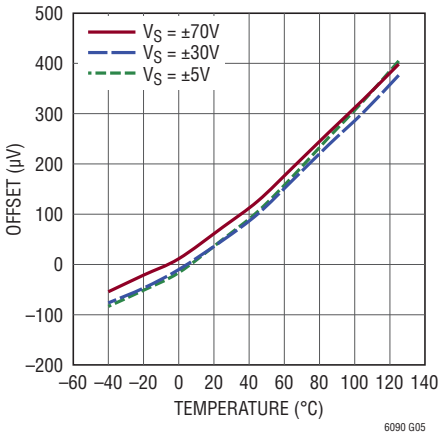
PSRR vs Frequency



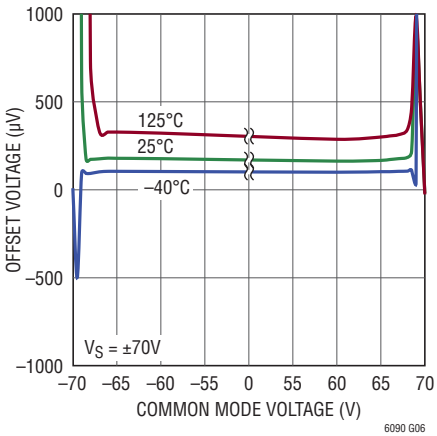
V_{OS} Distribution



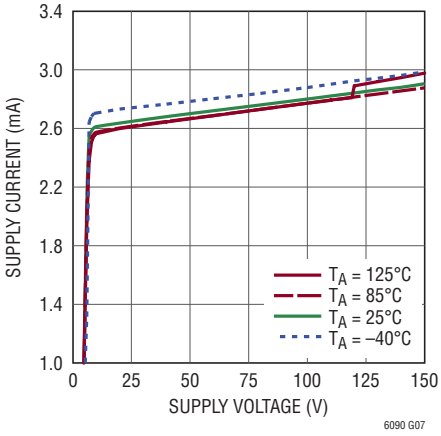
Offset Voltage Drift



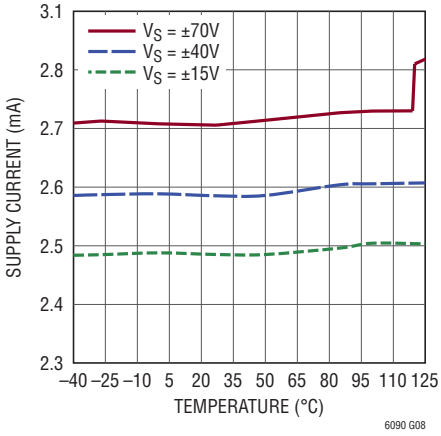
Offset Voltage vs Common Mode Voltage



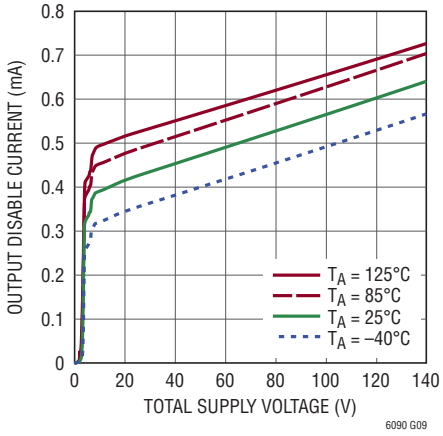
Supply Current vs Supply Voltage



Supply Current vs Temperature

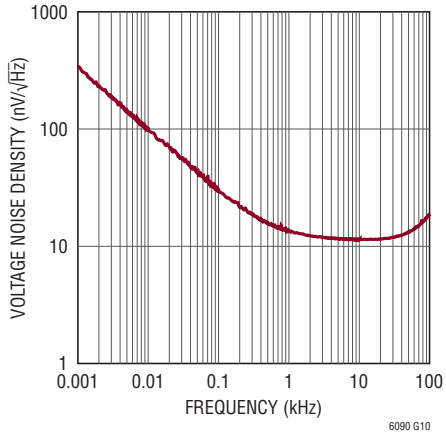


Output Disable Supply Current vs Supply Voltage

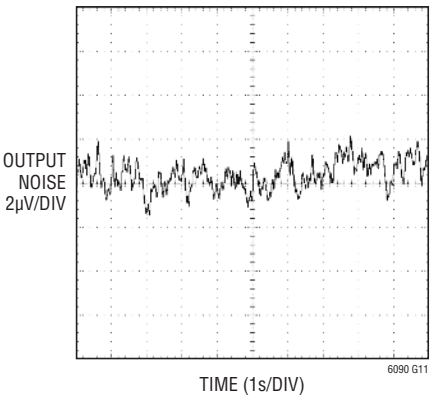


TYPICAL PERFORMANCE CHARACTERISTICS

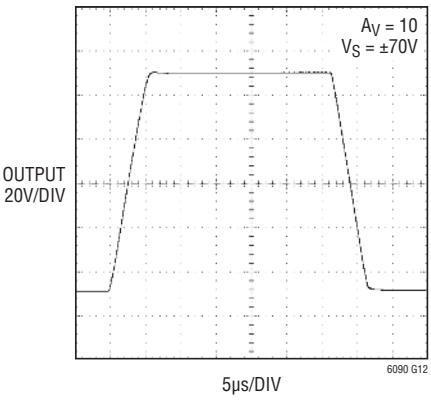
Voltage Noise vs Frequency



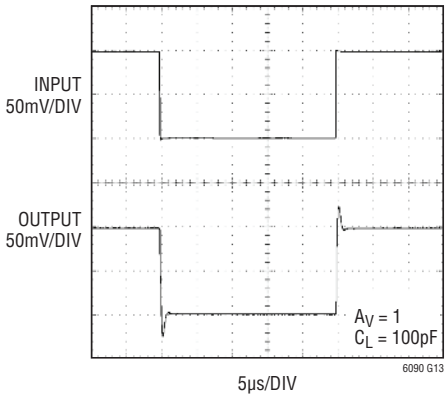
0.1Hz to 10Hz Voltage Noise



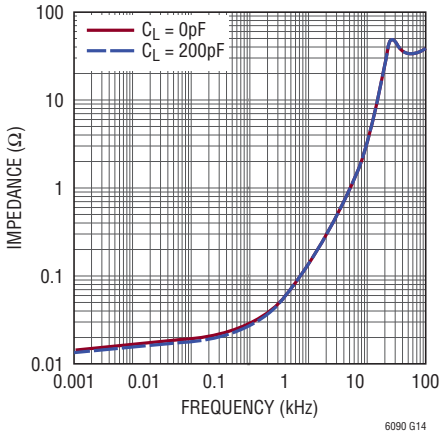
Large Signal Transient Response



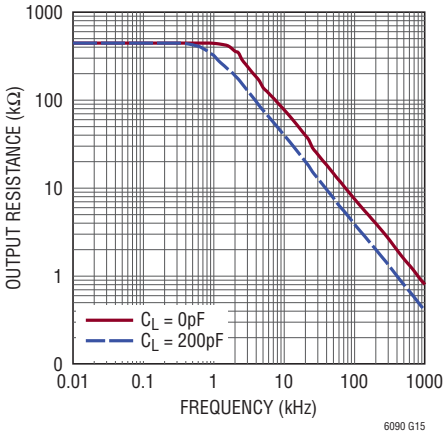
Small Signal Transient Response



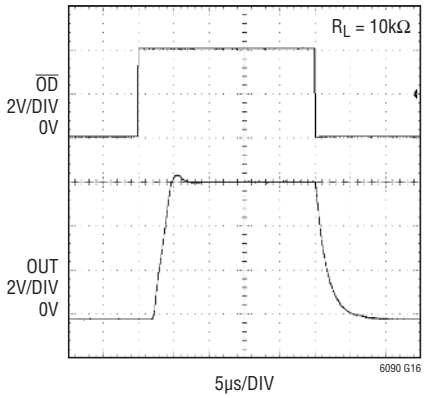
Output Impedance vs Frequency



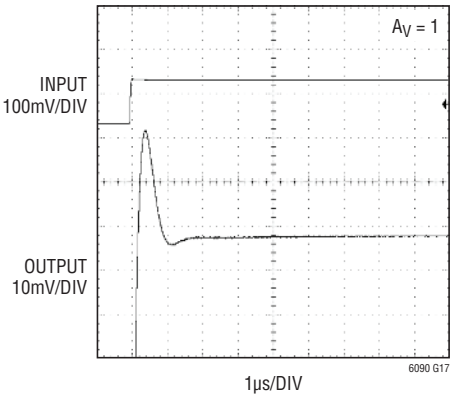
Output Impedance vs Frequency with Output Disabled ($\overline{OD}$ = COM)



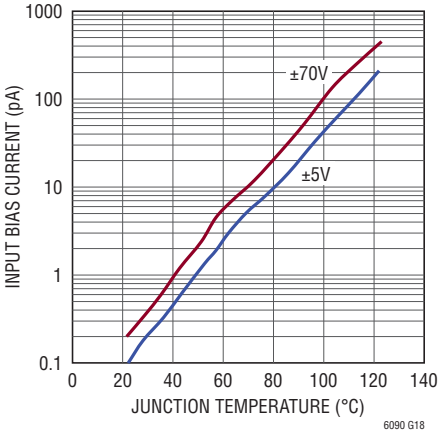
Output Disable Response Time



Settling Time

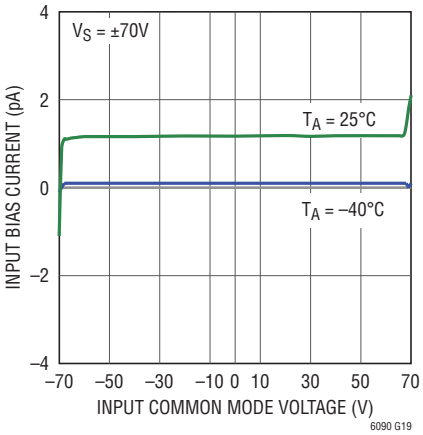


Input Bias Current vs Temperature

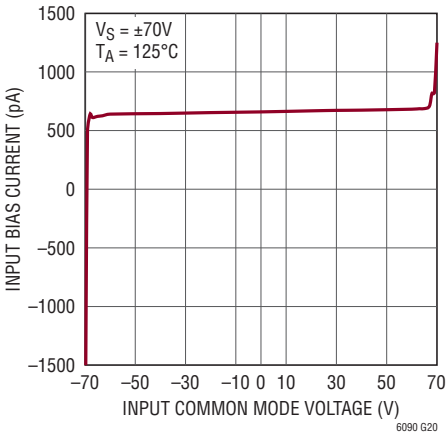


TYPICAL PERFORMANCE CHARACTERISTICS

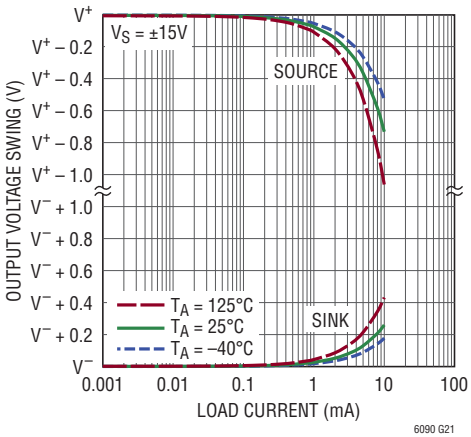
Input Bias Current vs Common Mode Voltage



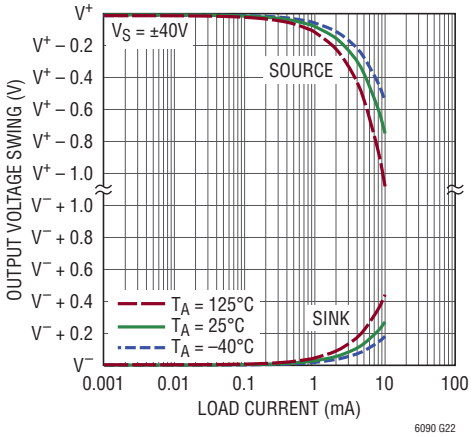
Input Bias Current vs Common Mode Voltage



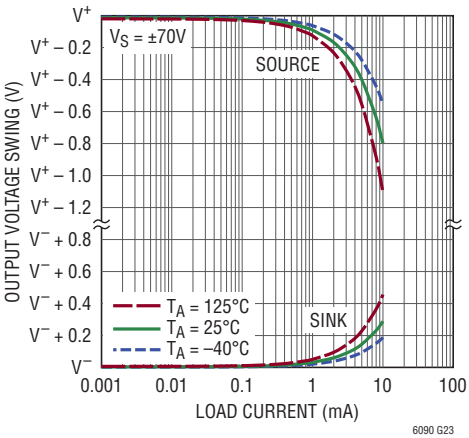
Output Voltage Swing vs Load Current, ±15V



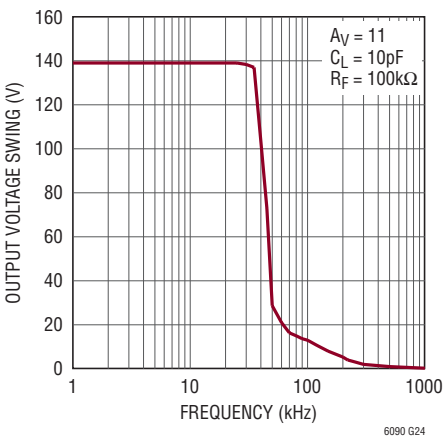
Output Voltage Swing vs Load Current, ±40V



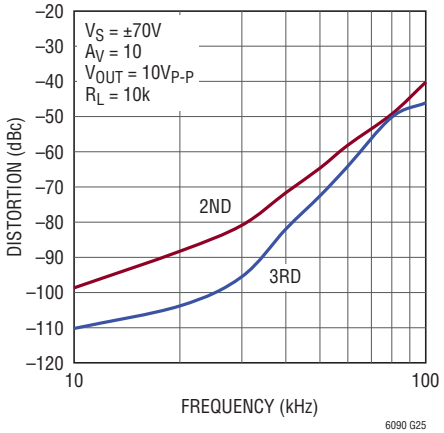
Output Voltage Swing vs Load Current, ±70V



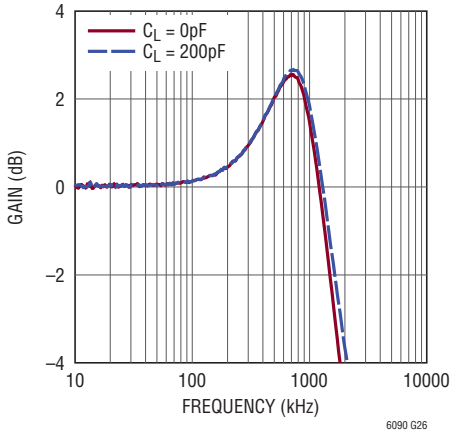
Output Voltage Swing vs Frequency



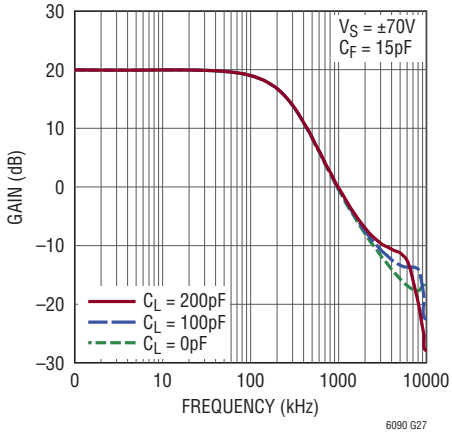
Distortion vs Frequency



Frequency Response, A_V = +1

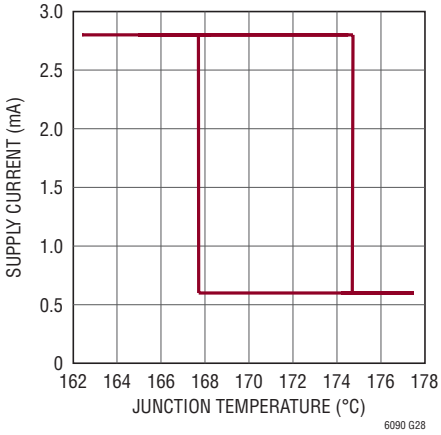


Frequency Response, A_V = +10

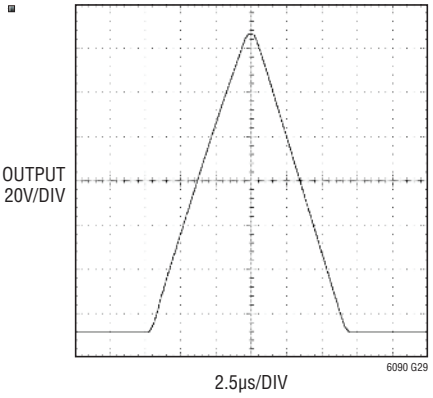


TYPICAL PERFORMANCE CHARACTERISTICS

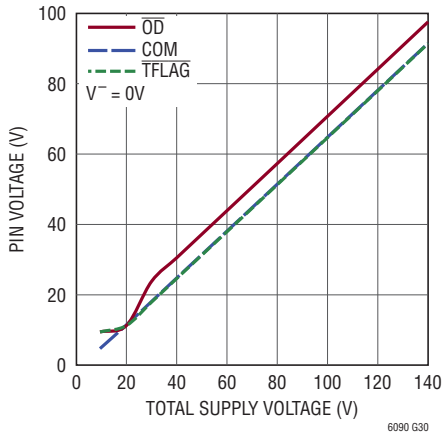
Thermal Shutdown Hysteresis



Output Slewing with A_V = –10



Open Circuit Voltage of COM, $\overline{OD}$, $\overline{TFLAG}$



PIN FUNCTIONS (S8E/FE)

COM (Pin 1/Pin 1): COM Pin is used to interface $\overline{OD}$ and $\overline{TFLAG}$ pins to voltage control circuits. Tie this pin to the low voltage ground, or let it float.

–IN (Pin 2/Pin 4): Inverting Input Pin. Input common mode range is V^- + 3V to V^+ – 3V. Do not exceed absolute maximum voltage range.

+IN (Pin 3/Pin 5): Noninverting Input Pin. Input common mode range is V^- + 3V to V^+ – 3V. Do not exceed absolute maximum voltage range.

V^- (Pin 4, Exposed Pad Pin 9/Pin 8, Exposed Pad Pin 17): Negative Supply Pin. Connect to V^- Only. To achieve low thermal resistance connect this pin to the V^- power plane. The V^- power plane connection removes heat from the device and should be electrically isolated from all other power planes.

$\overline{TFLAG}$ (Pins 5, 9/Pins 9, 17): Temperature Flag Pin. The $\overline{TFLAG}$ pin is an open drain output that sinks current when the die temperature exceeds 145°C.

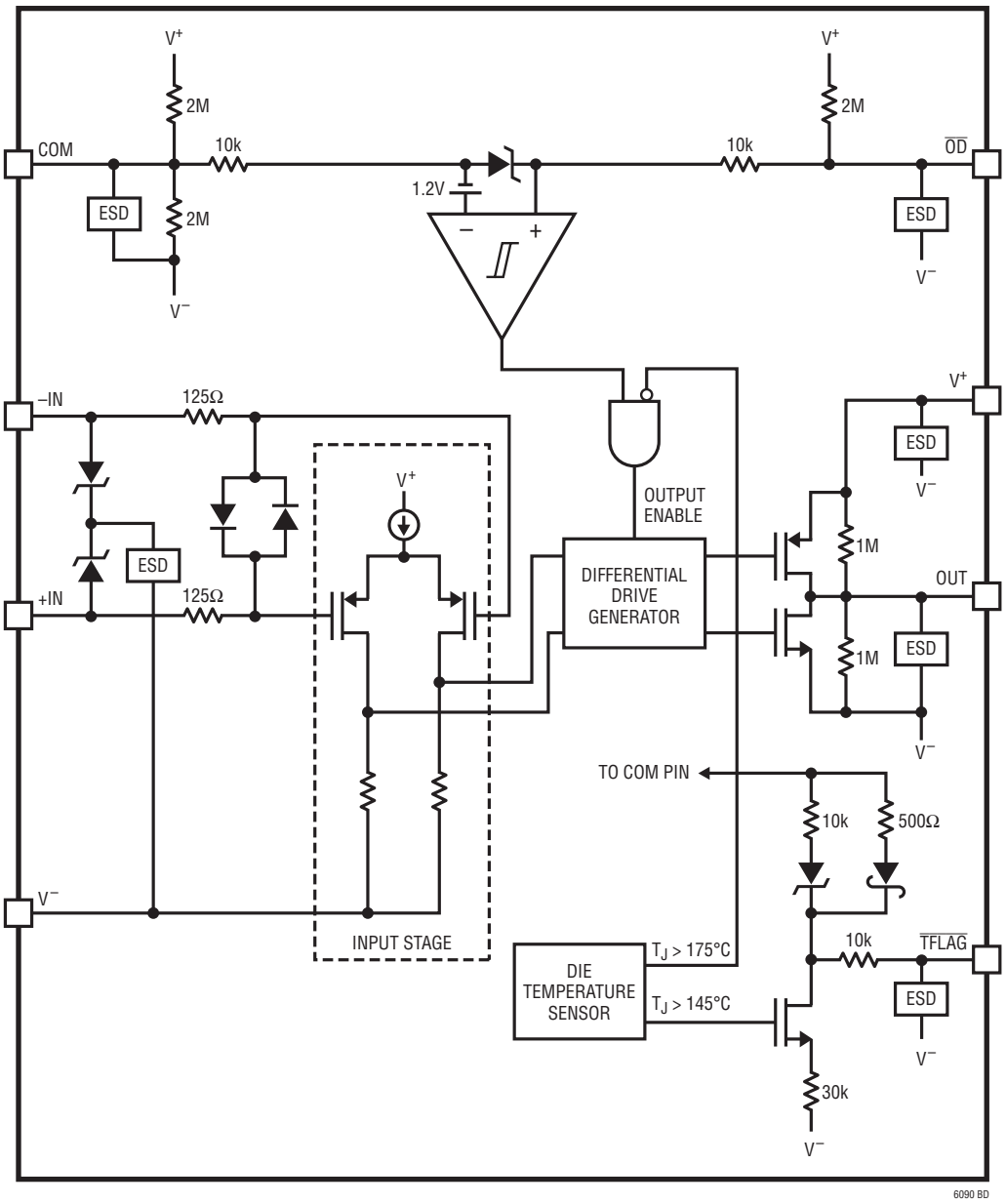
OUT (Pin 6/Pin 12): Output Pin. If this rail-to-rail output goes below V^- , the ESD protection diode will forward bias. If OUT goes above V^+, then output device diodes will forward bias. Avoid forward biasing the diodes on the OUT pin. Excessive current can cause damage.

V^+ (Pin 7/Pin 14): Positive Supply Pin.

$\overline{OD}$ (Pin 8/Pin 16): Output Disable Pin. Active low input disables the output stage. If left open, an internal pull-up resistor enables the amplifier. Input voltage levels are referred to the COM pin.

GUARD (NA/Pins 2, 3, 6, 7, 10, 11, 13, 15): Guard pins increase clearance and creepage between other pins. Pins 3 and 6 can be used to build guard rings around the inputs.

BLOCK DIAGRAM



APPLICATIONS INFORMATION

General

The LTC6090 high voltage operational amplifier is designed in a Linear Technology proprietary process enabling a rail-to-rail output stage with a 140V supply while maintaining precision, low offset, and low noise.

Power Supply

The LTC6090 works off single or split supplies. Split supplies can be balanced or unbalanced. For example, two ±70V supplies can be used, or a 100V and –40V supply can be used. For single supply applications place a high quality surface mount ceramic 0.1µF bypass capacitor between the supply pins close to the part. For dual supply applications use two high quality surface mount ceramic capacitors between V^+ to ground, and $V^–$ to ground located close to the part. When using split supplies, supply sequencing does not cause problems.

Input Protection

As shown in the block diagram, the LTC6090 has a comprehensive protection network to prevent damage to the input devices. The current limiting resistors and back to back diodes are to keep the inputs from being driven apart. The voltage-current relationship combines exponential and resistive until the voltage difference between the pins reach 12V.

At that point the Zeners turn on. Additional current into the pins will snap back the input differential voltage to 9V. In the event of an ESD strike between an input and $V^–$, the voltage clamps and ESD device fire providing a current path to $V^–$ protecting the input devices.

The input pin protection is designed to protect against momentary ESD events. A repetitive large fast input swing (>5.5V and <20ns rise time) will cause repeated stress on the MOSFET input devices. When in such an application, anti-parallel diodes (1N4148) should be connected between the inputs to limit the swing.

Output Range

To get full benefit of the output drive, the feedback resistor should be chosen carefully. Consider an amplifier with $A_V = –50$ and a 5k feedback resistor. A 1V input will cause the output to rise to 50V. Since +IN is at the same potential as –IN, a current of 10mA will flow through the feedback resistor limiting the ability of the amplifier to drive a load. A better choice is a 50k feedback resistor reducing the current in the feedback resistor to 1mA.

Interfacing to Low Voltage Circuits

The COM pin is provided to set a common signal ground for communication to a microprocessor or other low voltage logic circuit. The COM pin should be tied to the low voltage ground as shown in Figure 1. If left floating, the internal resistive voltage divider will cause the COM pin to rise 30% above mid-supply. The COM, $\overline{OD}$, and $\overline{TFLAG}$ pins are protected from overvoltage by internal Zener diodes and current limiting resistors. Care should be taken to observe the absolute maximum voltage between the COM, $\overline{OD}$ and $\overline{TFLAG}$ pins which are limited ≤6V with respect to COM.

Output Disable

The $\overline{OD}$ pin is an active low disable with an internal 2MΩ resistor that will pull up the $\overline{OD}$ pin enabling the output stage. The $\overline{OD}$ pin voltage is limited by an internal Zener diode. When the $\overline{OD}$ pin is brought low to the COM pin, the output stage is disabled, leaving the bias and input circuits enabled. This results in 680µA (typical) standby current through the device. The $\overline{OD}$ pin can be directly connected to the low voltage driving circuitry or an open drain NMOS device can be used as shown in Figure 1.

APPLICATIONS INFORMATION

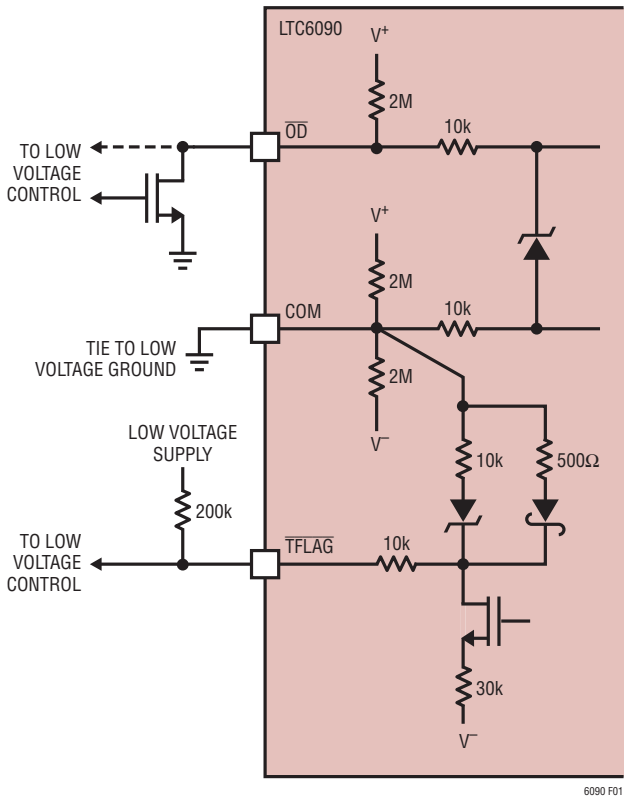


Figure 1. Low Voltage Interface

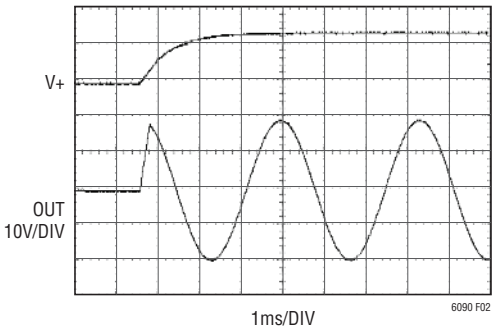


Figure 2. Starting Up

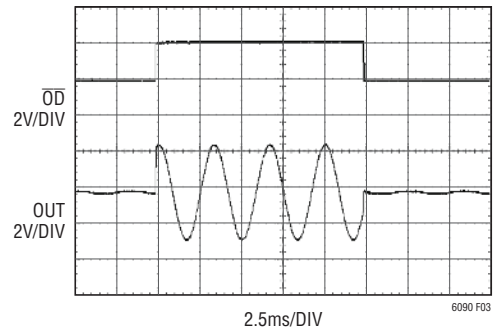


Figure 3. LTC6090 Output Disable Function

For simplest shutdown operation, float the COM pin, and tie the $\overline{OD}$ pin to the $\overline{TFLAG}$ pin. This will float the low voltage control pins, and the overtemperature circuit will safely shutdown the output stage if the die temperature reaches 145°C.

Since the $\overline{OD}$ pin is referenced to the COM pin, precaution should be exercised and the absolute maximum ratings should be observed for the COM and $\overline{OD}$ pins.

When coming out of shutdown the LTC6090 bias circuits and input stage are already powered up leaving only the output stage to turn on and drive to the proper output voltage. Figures 2 and 3 show the part starting up and coming out of shutdown, respectively.

Thermal Shutdown

The $\overline{TFLAG}$ pin is an open drain output pin that sinks 120µA (typical) when the die temperature exceeds 145°C. The temperature sensor has 5°C of hysteresis requiring the part to cool to 140°C before disabling the $\overline{TFLAG}$ pin. Since the $\overline{TFLAG}$ pin is referenced to the COM pin, precaution should be exercised and the absolute maximum ratings should be observed for the COM and $\overline{TFLAG}$ pins.

Tying the $\overline{TFLAG}$ pin to the $\overline{OD}$ pin will automatically shut down the output stage when the die temperature exceeds 145°C as shown in Figure 4. This will ensure that the junction temperature does not exceed 150°C.

For safety, an independent second overtemperature threshold shuts down the output stage if the internal die temperature rises to 175°C. There is hysteresis in the thermal shutdown circuit requiring the die temperature to cool 7°C. Once the device has cooled sufficiently, the output stage will enable. **Degradation can occur or reliability may be affected when the junction temperature of the device exceeds 150°C.**

APPLICATIONS INFORMATION

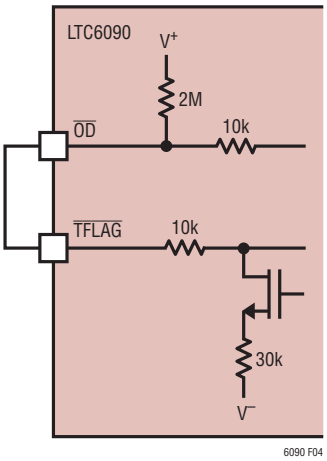


Figure 4. Automatic Thermal Output Disable Using the $\overline{\text{TFLAG}}$ Pin

Board Layout

The LTC6090 is a precision low offset high gain amplifier that requires good analog PCB layout techniques to maintain high performance. Start with a ground plane that is star connected. Pull back the ground plane from any high voltage vias. Critical signals such as the inputs should have short lead lengths to reduce stray capacitance which also improves stability. Use high quality surface mount ceramic capacitors to bypass the supply(s).

In addition to the typical layout issues encountered with a precision operational amplifier, there are the issues of high voltage and high power. Important consideration for high voltage traces are spacing, humidity and dust. High voltage electric fields between adjacent conductors attract dust. Moisture is absorbed by the dust and can contribute to board leakage and electrical breakdown.

It is important to clean the PCB after soldering down the part. Solder flux will accumulate dust and become a leakage hazard. It is recommended to clean the PCB with a solvent, or simply use soap and water to remove residue. Baking the PCB will remove left over moisture. Depending on the application, a special low leakage board material may be considered.

The TSSOP package has guard pins for applications that require a guard ring. An example schematic diagram and PCB layout is shown in Figures 5a and 5b, respectively, of a circuit using a guard ring to protect the –IN pin. The guard ring completely encloses the high impedance node –IN. To simplify the PCB layout avoid using vias on this node. In addition, the solder mask should be pulled back along the guard ring exposing the metal. To help the spacing between nodes, one of the extra pins on the TSSOP package is used to route the guard ring behind the –IN pin. The PCB should be thoroughly cleaned after soldering to ensure there is no solder paste between the exposed pad (Pin 17) and the guard ring.

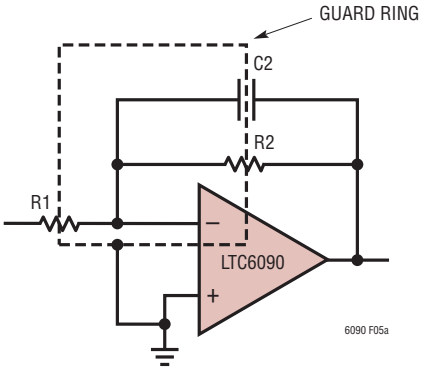


Figure 5a. Circuit Diagram Showing Guard Ring

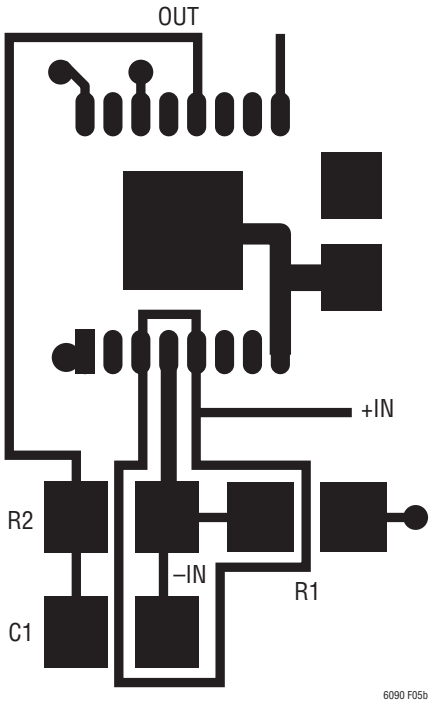


Figure 5b. TSSOP Package PCB Layout with Guard Ring

APPLICATIONS INFORMATION

Power Dissipation

With a supply voltage of 140V it doesn't take much current to consume a lot of power. Consider that 10mA at 140V consumes 1.4W of power and needs to be dissipated in a small plastic SO package. To aid in power dissipation both LTC6090 packages have exposed pads for low thermal resistance. The amount of metal connected to the exposed pad will lower the θ_{JA} of a package. An optimal amount of PCB metal connected to the SO package will lower the junction to ambient thermal resistance down to 33°C/W. If minimal metal is used, the θ_{JA} could more than double (see Table 1). If the exposed pad has no metal beneath it, θ_{JA} could be as high 120°C/W.

It's recommended that the exposed pad have as much PCB metal connected to it as reasonably available. The more PCB metal connected to the exposed pad, the lower the thermal resistance. Use multiple vias from the exposed pad to the V^- supply plane. The exposed pad is electrically connected to the V^- pin. In addition, a heat sink may be necessary if operating near maximum junction temperature. See Table 1 for guidance on how thermal resistance changes as a function of metal area connected to the exposed pad.

The LTC6090 is specified to source and sink 10mA at 140V. If the total supply voltage is dropped across the device, 1.4W of power will need to be dissipated. If the quiescent power is included (140V • 2.8mA = 0.4W), the total power dissipated is 1.8W. The internal die temperature will rise 59° using an optimal layout in a SO package. A sub-optimal layout could more than double the amount of temperature increase due to power dissipation.

Table 1. Thermal Resistance as PCB Area of Exposed Pad Varies

EXAMPLE A	EXAMPLE B	EXAMPLE C	EXAMPLE D
TOP LAYER A	TOP LAYER B	TOP LAYER C	TOP LAYER D
			
BOTTOM LAYER A	BOTTOM LAYER B	BOTTOM LAYER C	BOTTOM LAYER D
			
θ_{JA} = 43°C/W θ_{JC} = 5°C/W θ_{CA} = 38°C/W	θ_{JA} = 50°C/W θ_{JC} = 5°C/W θ_{CA} = 45°C/W	θ_{JA} = 57°C/W θ_{JC} = 5°C/W θ_{CA} = 52°C/W	θ_{JA} = 72°C/W θ_{JC} = 5°C/W θ_{CA} = 67°C/W
MINIMUM BOTTOM LAYER A	MINIMUM BOTTOM LAYER B	MINIMUM BOTTOM LAYER C	
			
θ_{JA} = 54°C/W θ_{JC} = 5°C/W θ_{CA} = 49°C/W	θ_{JA} = 57°C/W θ_{JC} = 5°C/W θ_{CA} = 52°C/W	θ_{JA} = 58°C/W θ_{JC} = 5°C/W θ_{CA} = 53°C/W	

APPLICATIONS INFORMATION

In order to avoid damaging the device, the absolute maximum junction temperature should not be exceeded (T_{JMAX} = 150°C). Junction temperature is determined using the expression:

$$T_J = PD \bullet \theta_{JA} + T_A$$

where P_D is the power dissipated in the package, θ_{JA} is the package thermal resistance from ambient to junction and T_A is the ambient temperature. For example, if the part has a 140V supply voltage with 2.8mA of quiescent current and the output is 20V above the negative rail sourcing 10mA, the total power dissipated in the device is (120V • 10mA) + (140V • 2.8mA) = 1.6W. Under these conditions the ambient temperature should not exceed:

$$T_A = T_{JMAX} - (P_D \bullet \theta_{JA}) = 150°C - (1.6W \bullet 33°C/W) = 97°C.$$

Safe Operating Area

The safe operating area, or SOA, illustrates the voltage, current, and temperature conditions where the device can be reliably operated. Shown below in Figure 6 is the SOA for the LTC6090. The SOA takes into account the power dissipated by the device. This includes the product of the load current and difference between the supply and output voltage, and the quiescent current and supply voltage.

The LTC6090 is safe when operated within the boundaries shown in Figure 6. Thermal resistance junction to case, θ_{JC}, is rated at a constant 5°C/W. Thermal resistance junction to ambient, θ_{JA}, is dependent on board layout and any additional heat sinking. The three SOA curves in Figure 6 show the direct effect of θ_{JA} on SOA.

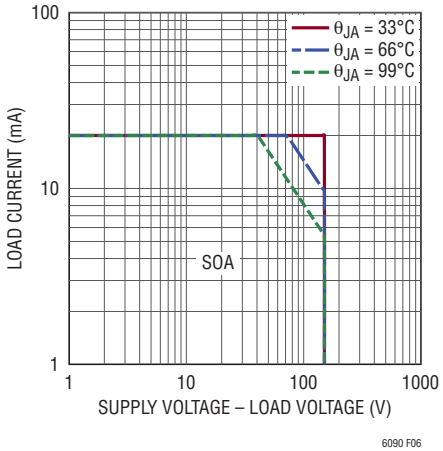


Figure 6. Safe Operating Area

Stability with Large Resistor Values

A large feedback resistor along with the intrinsic input capacitance will create an additional pole that affects stability and causes peaking in the closed loop response as shown in Figure 7. To mitigate the peaking a small feedback capacitor placed around the feedback resistor, as shown in Figure 8, will reduce the peaking and overshoot. Figure 9 shows the closed loop response with a 10pF feedback capacitor.

Additionally stray capacitance on the input pins should be kept to a minimum.

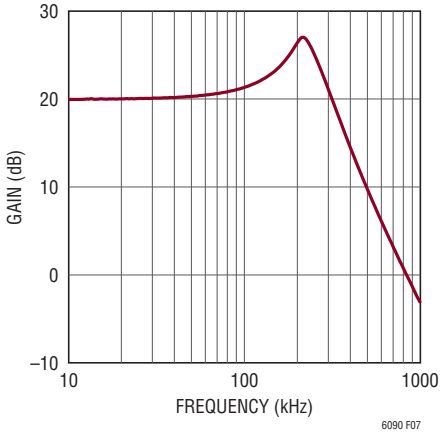


Figure 7. Uncompensated Closed Loop Response

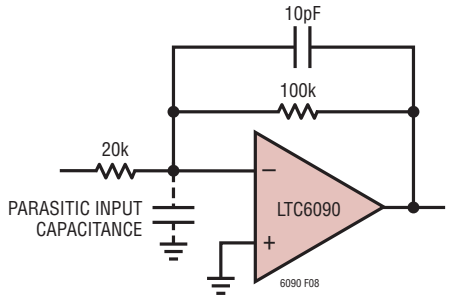


Figure 8. LTC6090 with Feedback Capacitance to Reduce Peaking

APPLICATIONS INFORMATION

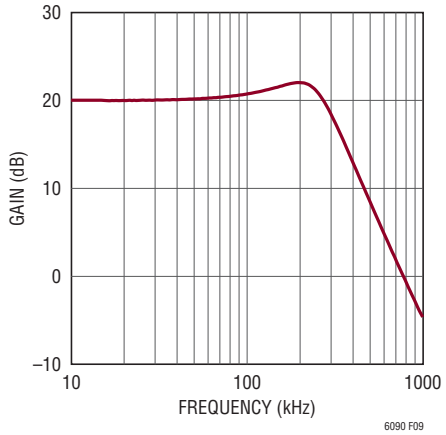


Figure 9. Compensated Closed Loop Response Reduces Peaking

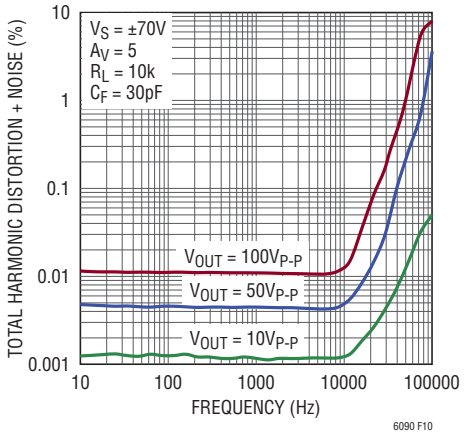


Figure 10. Distortion vs Frequency for Large Output Swings

Slew Enhancement

The LTC6090 includes a slew enhancement circuit which boosts the slew rate to 19V/µs making the part capable of slewing rail-to-rail across the 140V output range in less than 8µs. To optimize the slew rate and minimize settling, stray capacitance should be kept to a minimum. A feedback capacitor reduces overshoot and nonlinearities associated with the slew enhancement circuit. The size of the feedback capacitor should be tailored to the specific board, supply voltage and load conditions.

Slewing is a nonlinear behavior and will affect distortion. The relationship between slew rate and full power bandwidth is given in the relationship below.

$$SR = V_O \bullet \omega$$

Where V_O is the peak output voltage and ω is frequency in radians. The fidelity of a large sine wave output is limited by the slew rate. The graph in Figure 10 shows distortion versus frequency for several output levels.

Multiplexer Application

Several LTC6090s may be arranged to act as a high voltage analog multiplexer as shown in Figure 11. When using this arrangement, it is possible for the output to affect the source on the disabled amplifier's noninverting input. The inverting and noninverting inputs are clamped through resistors and back to back diodes. There is a path for current to flow from the multiplexer output through the disabled amplifier's feedback resistor, and through the inputs to the noninverting input's source. For example, if the enabled amplifier has a –70V output, and the disabled amplifier has a 5V input, there is 75V across the two resistors and the input pins. To keep this current below 1mA the combined resistance of the R_{IN} and feedback resistor needs to be about 75k.

The output impedance of the disabled amplifier is 450kΩ at DC. The AC output impedance is shown in the Typical Performance Characteristics section.

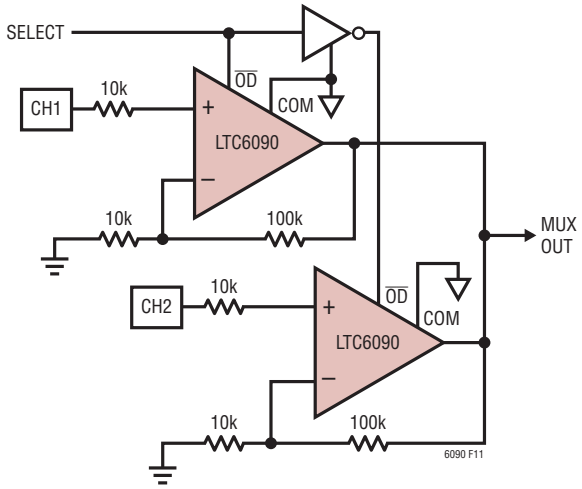
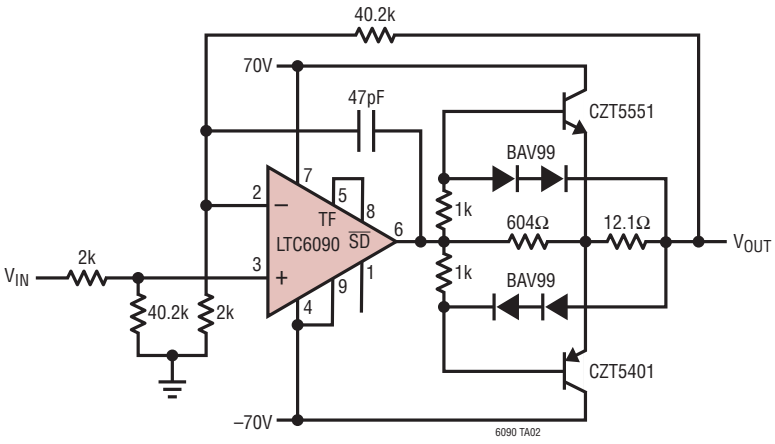


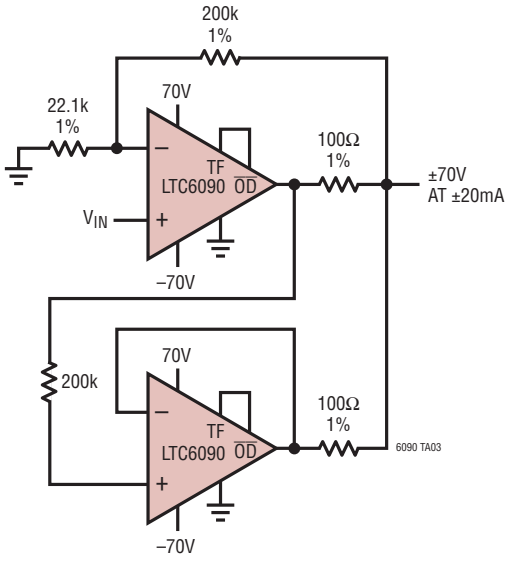
Figure 11. Multiplexer Application

TYPICAL APPLICATIONS

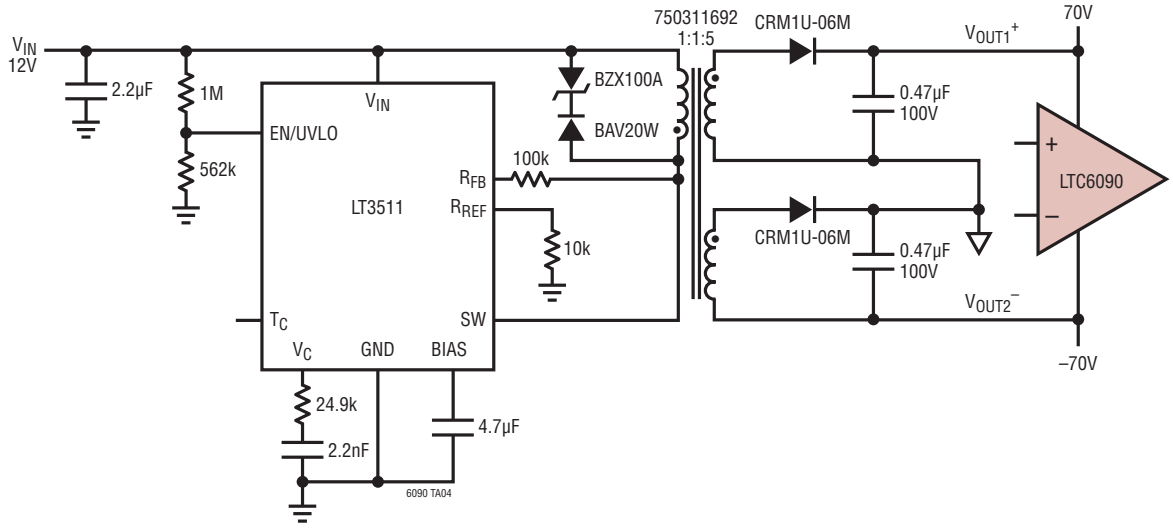
Gain of 20 Amplifier with a 40mA Protected Output Driver



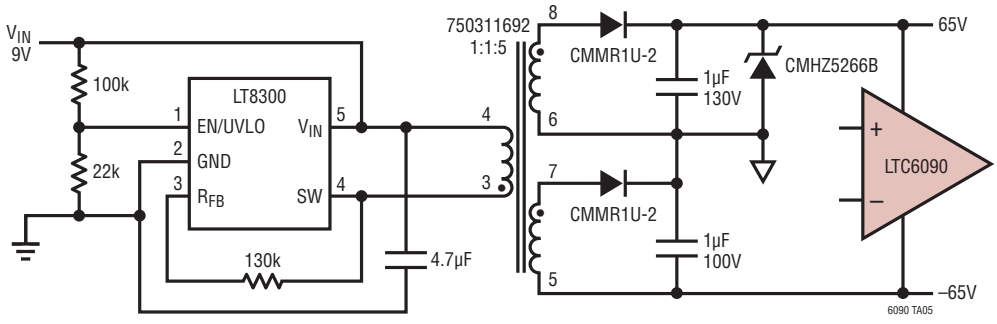
Gain of 10 with Protected Output Current Doubler



12V to ±70V Isolated Flyback Converter for Amplifier Supply

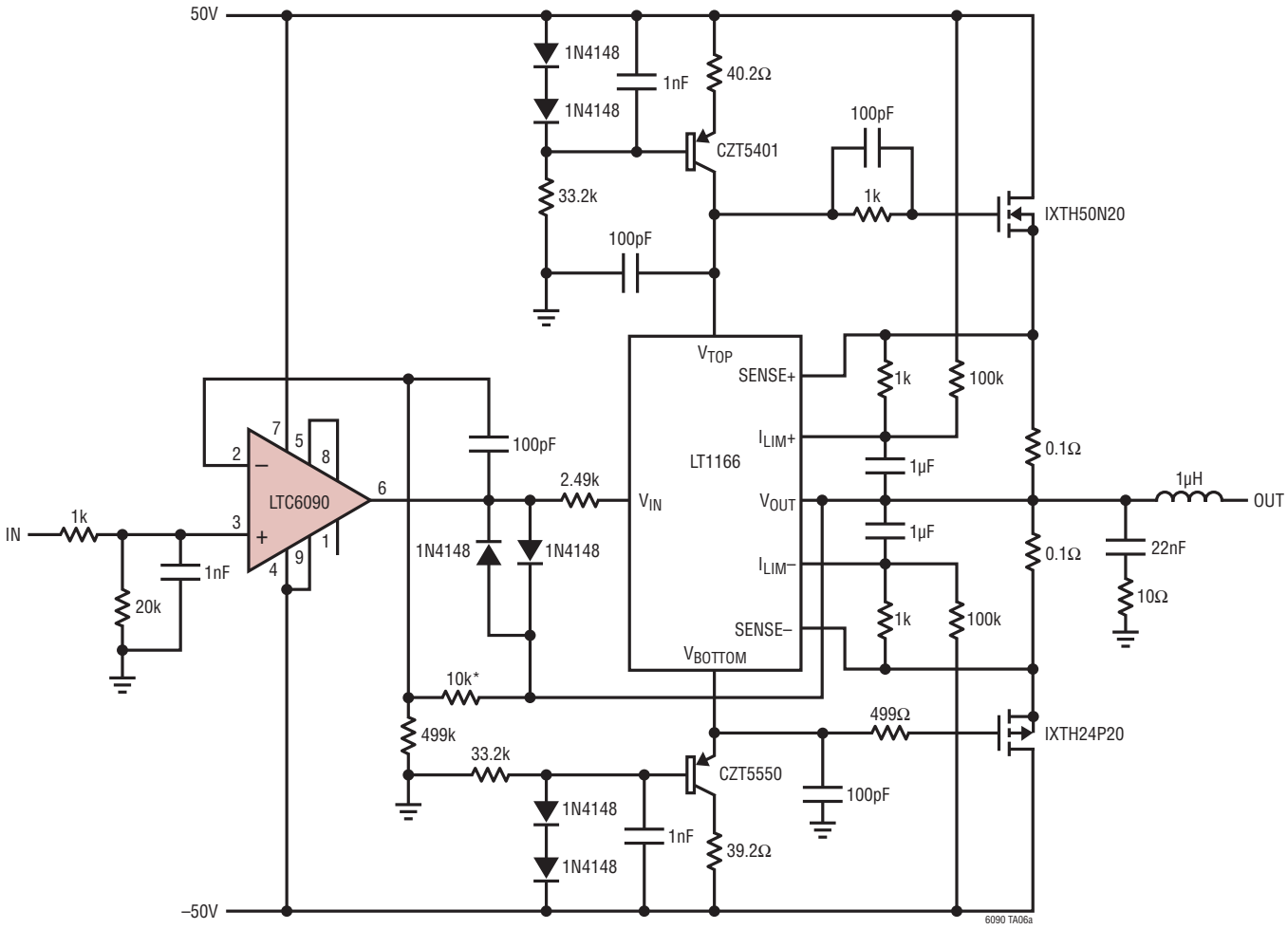


9V to ±65V Isolated Flyback Converter for Amplifier Supply



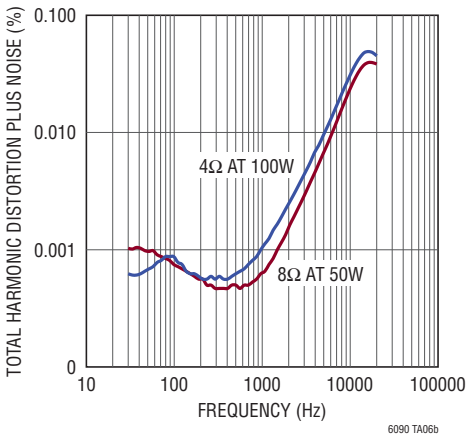
TYPICAL APPLICATIONS

Audio Power Amplifier



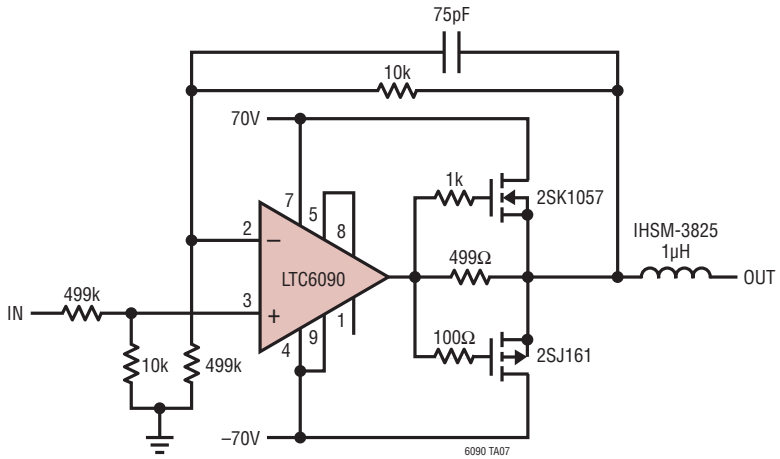
* USE SEVERAL SERIES RESISTORS TO REDUCE DISTORTION (i.e. 5 × 2kΩ).

Total Harmonic Distortion Plus Noise Analyzer Passband 10Hz to 80kHz

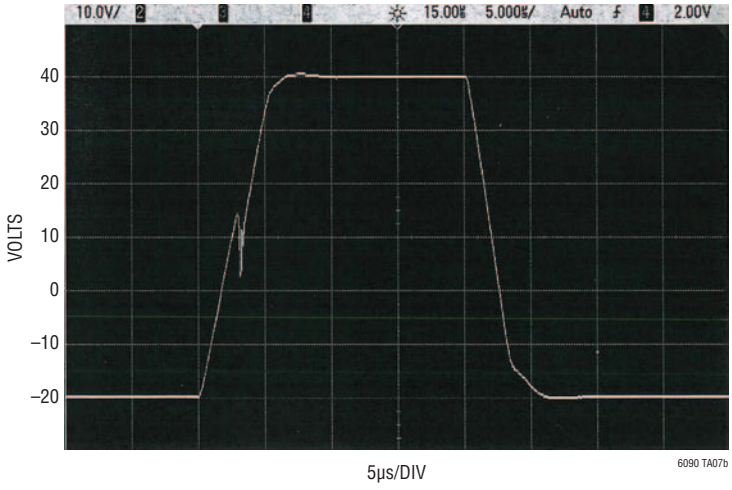


TYPICAL APPLICATIONS

High Current Pulse Amplifier

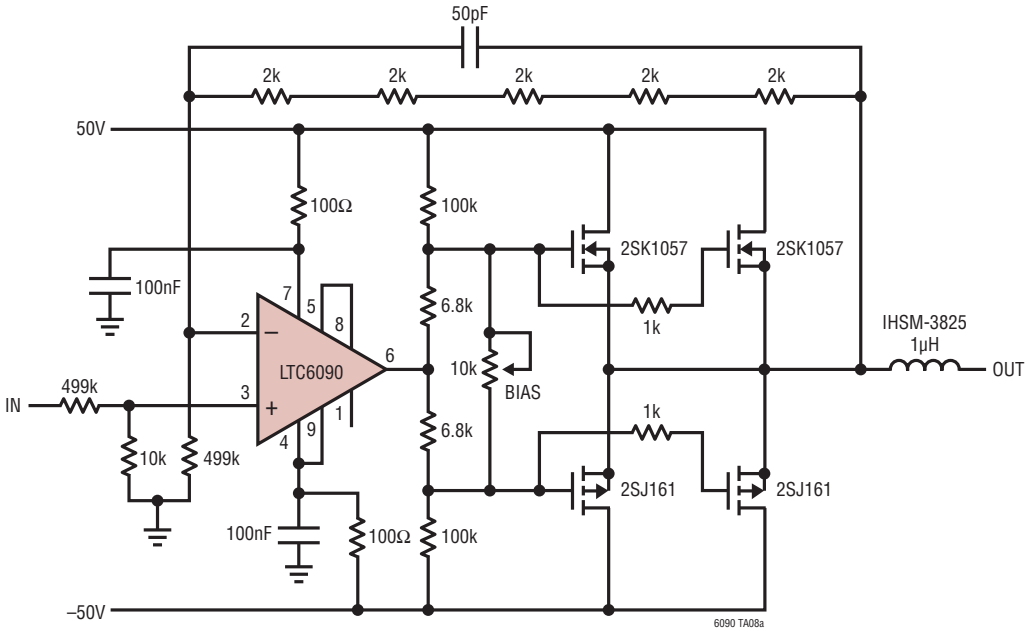


60V Step Response Into 10Ω



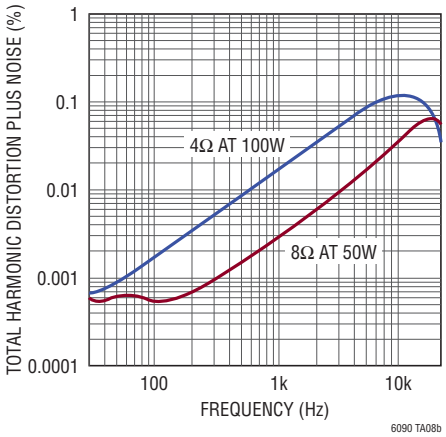
TYPICAL APPLICATIONS

Simple 100W Audio Amplifier



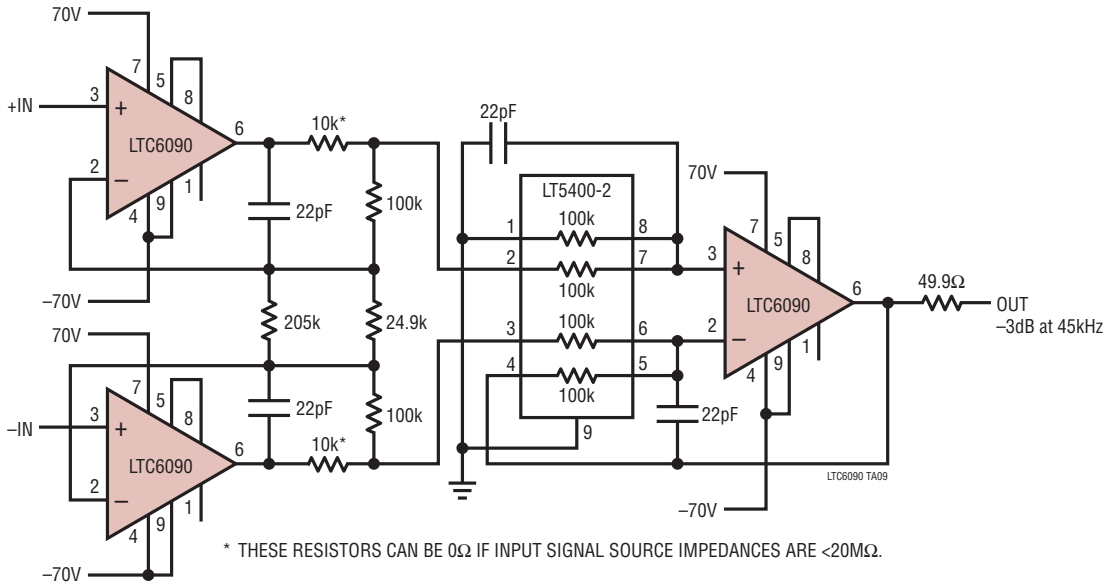
SET QUIESCENT SUPPLY CURRENT AT ABOUT 200mA WITH BIAS ADJUSTMENT.
SET QUIESCENT CURRENT TO 100mA IF PARALLEL MOSFETs ARE NOT USED (FOR 8Ω OR HIGHER).

Total Harmonic Distortion Plus Noise vs Frequency

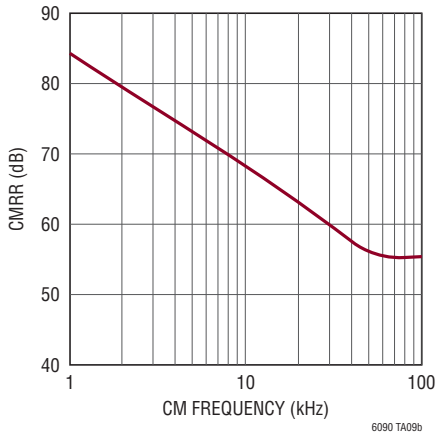


TYPICAL APPLICATIONS

Wide Common Mode Range 10x Gain Instrumentation Amplifier
Typically <1mV Input-Referred Error



* THESE RESISTORS CAN BE 0Ω IF INPUT SIGNAL SOURCE IMPEDANCES ARE <20MΩ.

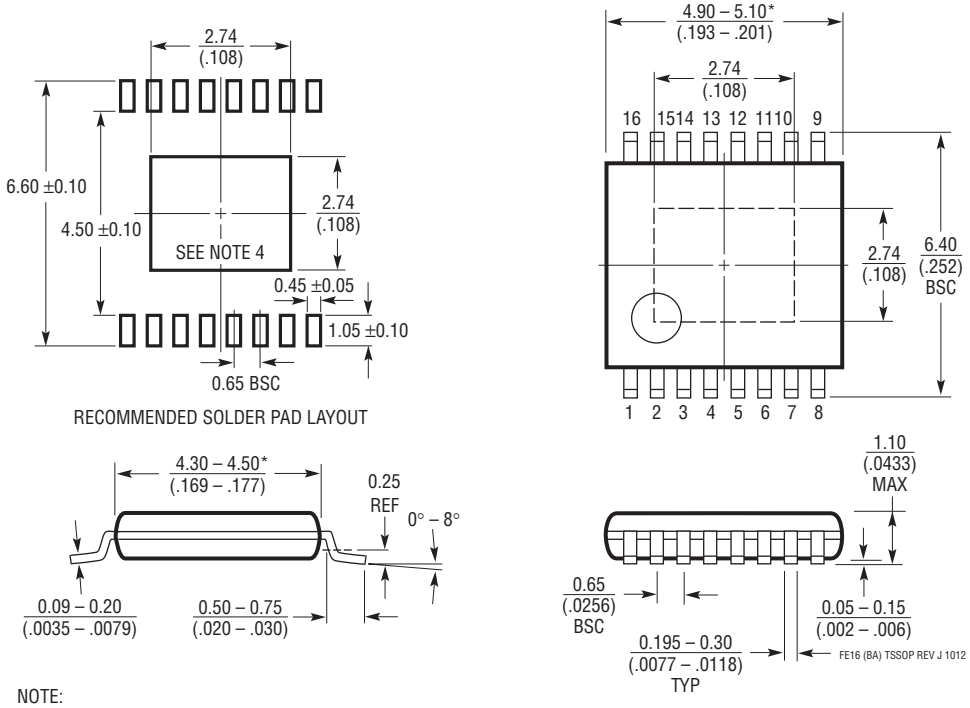


PACKAGE DESCRIPTION

Please refer to http://www.linear.com/designtools/packaging/ for the most recent package drawings.

FE Package
16-Lead Plastic TSSOP (4.4mm)
(Reference LTC DWG # 05-08-1663 Rev J)

Exposed Pad Variation BA



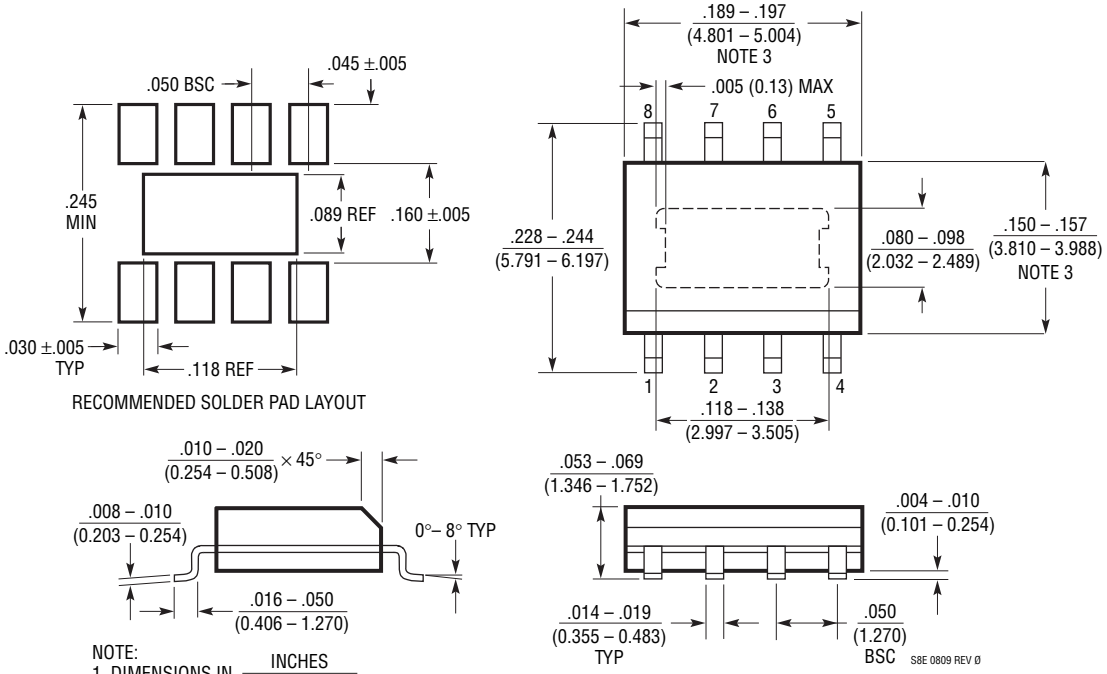
NOTE:
1. CONTROLLING DIMENSION: MILLIMETERS
2. DIMENSIONS ARE IN $\frac{\text{MILLIMETERS}}{(\text{INCHES})}$
3. DRAWING NOT TO SCALE
4. RECOMMENDED MINIMUM PCB METAL SIZE FOR EXPOSED PAD ATTACHMENT

*DIMENSIONS DO NOT INCLUDE MOLD FLASH. MOLD FLASH SHALL NOT EXCEED 0.150mm (.006") PER SIDE

PACKAGE DESCRIPTION

Please refer to http://www.linear.com/designtools/packaging/ for the most recent package drawings.

S8E Package
8-Lead Plastic SOIC (Narrow .150 Inch) Exposed Pad
(Reference LTC DWG # 05-08-1857 Rev Ø)



NOTE:
1. DIMENSIONS IN $\frac{\text{INCHES}}{(\text{MILLIMETERS})}$
2. DRAWING NOT TO SCALE
3. THESE DIMENSIONS DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS.
   MOLD FLASH OR PROTRUSIONS SHALL NOT EXCEED .006" (0.15mm)

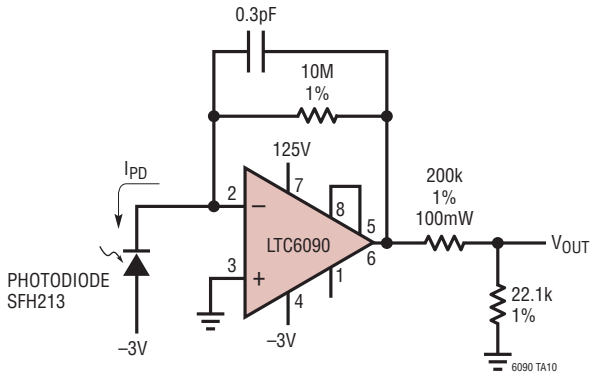
REVISION HISTORY

REV	DATE	DESCRIPTION	PAGE NUMBER
A	11/12	Added ESD Statement.	2

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TYPICAL APPLICATION

Extended Dynamic Range 1MΩ Transimpedance Photodiode Amplifier



$V_{OUT} = I_{PD} \bullet 1M$
OUTPUT NOISE = $21\mu V_{RMS}$ (1kHz – 40kHz)
OUTPUT OFFSET = 150µV MAXIMUM
BANDWIDTH = 40kHz (–3dB)
OUTPUT SWING = 0V TO 12V

RELATED PARTS

PART NUMBER	DESCRIPTION	COMMENTS
Amplifiers		
LT1990	±250V Input Range G = 1, 10, Micropower, Difference Amplifier	Pin Selectable Gain of 1 or 10
LT1991	Precision, 100µA Gain Selectable Amplifier	Pin Configurable as a Difference Amplifier, Inverting and Noninverting Amplifier
Matched Resistors		
LT5400	Quad Matched Resistor Network	Excellent Matching Specifications Over the Entire Temperature Range
Digital to Analog Converters		
LTC2641/LTC2462	16-Bit V_{OUT} DACs in 3mm × 3mm DFN	Guaranteed Monotonic Over Temperature
LTC2756	Serial 18-Bit SoftSpan I_{OUT} DAC	18-Bit Settling Time: 2.1µs Maximum 18-Bit INL Error: ±1 LSB Over Temperature
Flyback Controllers		
LT3511	Monolithic High Voltage Isolated Flyback Converter	4.5V to 100V Input Voltage Range, No Optocoupler Required
LT8300	$100V_{IN}$ Micropower Isolated Flyback Converter with 150V/260mA Switch	6V to 100V Input Voltage Range. V_{OUT} Set with a Single External Resistor

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