1.5A, Low Noise, Fast Transient Response LDO Regulators

FEATURES

- **Optimized for Fast Transient Response**
- **Output Current: 1.5A**
- **Dropout Voltage: 340mV**
- **Low Noise: 40μV_{RMS} (10Hz to 100kHz)**
- **1mA Quiescent Current**
- No Protection Diodes Needed
- Controlled Quiescent Current in Dropout
- Fixed Output Voltages: 1.5V, 1.8V, 2.5V, 3.3V
- Adjustable Output from 1.21V to 20V
- <1μA Quiescent Current in Shutdown
- Stable with 10μF Output Capacitor
- Reverse Battery Protection
- No Reverse Current
- Thermal Limiting
- 5-Lead TO-220, DD, 3-Lead SOT-223, 8-Lead SO and 16-Lead TSSOP Packages

APPLICATIONS

- 3.3V to 2.5V Logic Power Supplies
- Post Regulator for Switching Supplies

DESCRIPTION

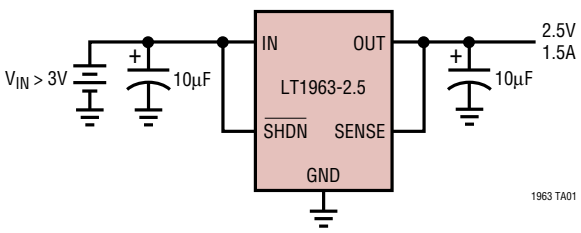
The LT®1963 series are low dropout regulators optimized for fast transient response. The devices are capable of supplying 1.5A of output current with a dropout voltage of 340mV. Operating quiescent current is 1mA, dropping to <1μA in shutdown. Quiescent current is well controlled; it does not rise in dropout as it does with many other regulators. In addition to fast transient response, the LT1963 regulators have very low output noise which makes them ideal for sensitive RF supply applications.

Output voltage range is from 1.21V to 20V. The LT1963 regulators are stable with output capacitors as low as 10μF. Internal protection circuitry includes reverse battery protection, current limiting, thermal limiting and reverse current protection. The devices are available in fixed output voltages of 1.5V, 1.8V, 2.5V, 3.3V and as an adjustable device with a 1.21V reference voltage. The LT1963 regulators are available in 5-lead TO-220, DD, 3-lead SOT-223, 8-lead SO, and Exposed Pad 16-lead TSSOP packages.

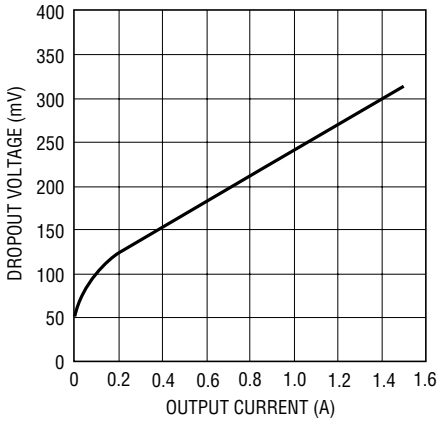
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TYPICAL APPLICATION

3.3V to 2.5V Regulator



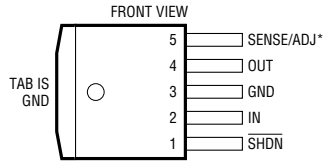
Dropout Voltage



ABSOLUTE MAXIMUM RATINGS (Note 1)

IN Pin Voltage ..... ±20V
OUT Pin Voltage ..... ±20V
Input to Output Differential Voltage (Note 2) ..... ±20V
SENSE Pin Voltage ..... ±20V
ADJ Pin Voltage ..... ±7V
$\overline{SHDN}$ Pin Voltage ..... ±20V
Output Short-Circuit Duration ..... Indefinite
Operating Junction Temperature Range –40°C to 125°C
Storage Temperature Range ..... –65°C to 150°C
Lead Temperature (Soldering, 10 sec) ..... 300°C

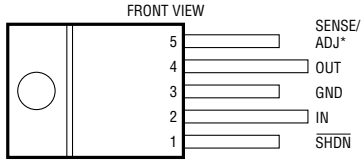
PACKAGE/ORDER INFORMATION



Q PACKAGE
5-LEAD PLASTIC DD

*PIN 5 = SENSE FOR LT1963-1.5/LT1963-1.8/ LT1963-2.5/LT1963-3.3
= ADJ FOR LT1963

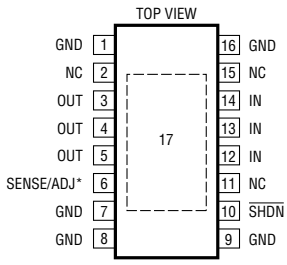
T_{JMAX} = 150°C, θ_{JA} = 30°C/W



T PACKAGE
5-LEAD PLASTIC TO-220

*PIN 5 = SENSE FOR LT1963-1.5/LT1963-1.8/ LT1963-2.5/LT1963-3.3
= ADJ FOR LT1963

T_{JMAX} = 150°C, θ_{JA} = 50°C/W

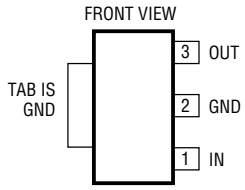


FE PACKAGE
16-LEAD PLASTIC TSSOP
EXPOSED PAD (PIN 17) IS GND. MUST BE SOLDERED TO THE PCB.

T_{JMAX} = 150°C, θ_{JA} = 38°C/W

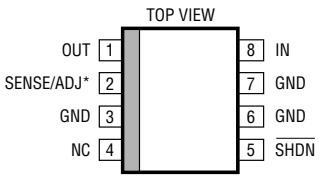
*PIN 6 = SENSE FOR LT1963-1.5/ LT1963-1.8/LT1963-2.5/ LT1963-3.3
= ADJ FOR LT1963

ORDER PART NUMBER	ORDER PART NUMBER	ORDER PART NUMBER	FE PART MARKING
LT1963EQ LT1963EQ-1.5 LT1963EQ-1.8 LT1963EQ-2.5 LT1963EQ-3.3	LT1963ET LT1963ET-1.5 LT1963ET-1.8 LT1963ET-2.5 LT1963ET-3.3	LT1963EFE LT1963EFE-1.5 LT1963EFE-1.8 LT1963EFE-2.5 LT1963EFE-3.3	1963EFE 1963EFE15 1963EFE18 1963EFE25 1963EFE33



ST PACKAGE
3-LEAD PLASTIC SOT-223

T_{JMAX} = 150°C, θ_{JA} = 50°C/W



S8 PACKAGE
8-LEAD PLASTIC SO

*PIN 2 = SENSE FOR LT1963-1.5/LT1963-1.8/ LT1963-2.5/LT1963-3.3
= ADJ FOR LT1963

T_{JMAX} = 150°C, θ_{JA} = 70°C/W

ORDER PART NUMBER	ST PART MARKING	ORDER PART NUMBER	S8 PART MARKING
LT1963EST-1.5 LT1963EST-1.8 LT1963EST-2.5 LT1963EST-3.3	196315 196318 196325 196333	LT1963ES8 LT1963ES8-1.5 LT1963ES8-1.8 LT1963ES8-2.5 LT1963ES8-3.3	1963 196315 196318 196325 196333

Order Options Tape and Reel: Add #TR
Lead Free: Add #PBF Lead Free Tape and Reel: Add #TRPBF
Lead Free Part Marking: http://www.linear.com/leadfree/

Consult LTC Marketing for parts specified with wider operating temperature ranges.

ELECTRICAL CHARACTERISTICS

The ● denotes specifications which apply over the full operating temperature range, otherwise specifications are T_A = 25°C. (Note 3)

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Minimum Input Voltage (Notes 4,12)	I_{LOAD} = 0.5A			1.9		V
	I_{LOAD} = 1.5A 2.5V < V_{IN} < 20V, 1mA < I_{LOAD} < 1.5A	●		2.1	2.5	V
Regulated Output Voltage (Note 5)	LT1963-1.5 V_{IN} = 2.21V, I_{LOAD} = 1mA		1.477	1.500	1.523	V
	2.5V < V_{IN} < 20V, 1mA < I_{LOAD} < 1.5A	●	1.447	1.500	1.545	V
	LT1963-1.8 V_{IN} = 2.3V, I_{LOAD} = 1mA		1.773	1.800	1.827	V
	2.8V < V_{IN} < 20V, 1mA < I_{LOAD} < 1.5A	●	1.737	1.800	1.854	V
	LT1963-2.5 V_{IN} = 3V, I_{LOAD} = 1mA		2.462	2.500	2.538	V
	3.5V < V_{IN} < 20V, 1mA < I_{LOAD} < 1.5A	●	2.412	2.500	2.575	V
	LT1963-3.3 V_{IN} = 3.8V, I_{LOAD} = 1mA		3.250	3.300	3.350	V
	4.3V < V_{IN} < 20V, 1mA < I_{LOAD} < 1.5A	●	3.200	3.300	3.400	V
ADJ Pin Voltage (Notes 4, 5)	LT1963 V_{IN} = 2.21V, I_{LOAD} = 1mA		1.192	1.210	1.228	V
	2.5V < V_{IN} < 20V, 1mA < I_{LOAD} < 1.5A	●	1.174	1.210	1.246	V
Line Regulation	LT1963-1.5 ΔV_{IN} = 2.21V to 20V, I_{LOAD} = 1mA	●		2.0	10	mV
	LT1963-1.8 ΔV_{IN} = 2.3V to 20V, I_{LOAD} = 1mA	●		2.5	10	mV
	LT1963-2.5 ΔV_{IN} = 3V to 20V, I_{LOAD} = 1mA	●		3.0	10	mV
	LT1963-3.3 ΔV_{IN} = 3.8V to 20V, I_{LOAD} = 1mA	●		3.5	10	mV
	LT1963 (Note 4) ΔV_{IN} = 2.21V to 20V, I_{LOAD} = 1mA	●		1.5	10	mV
Load Regulation	LT1963-1.5 V_{IN} = 2.5V, ΔI_{LOAD} = 1mA to 1.5A			2	9	mV
	V_{IN} = 2.5V, ΔI_{LOAD} = 1mA to 1.5A	●			18	mV
	LT1963-1.8 V_{IN} = 2.8V, ΔI_{LOAD} = 1mA to 1.5A			2	10	mV
	V_{IN} = 2.8V, ΔI_{LOAD} = 1mA to 1.5A	●			20	mV
	LT1963-2.5 V_{IN} = 3.5V, ΔI_{LOAD} = 1mA to 1.5A			2.5	15	mV
	V_{IN} = 3.5V, ΔI_{LOAD} = 1mA to 1.5A	●			30	mV
	LT1963-3.3 V_{IN} = 4.3V, ΔI_{LOAD} = 1mA to 1.5A			3	20	mV
	V_{IN} = 4.3V, ΔI_{LOAD} = 1mA to 1.5A	●			35	mV
	LT1963 (Note 4) V_{IN} = 2.5V, ΔI_{LOAD} = 1mA to 1.5A			2	8	mV
	V_{IN} = 2.5V, ΔI_{LOAD} = 1mA to 1.5A	●			15	mV
Dropout Voltage V_{IN} = $V_{OUT(NOMINAL)}$ (Notes 6, 7, 12)	I_{LOAD} = 1mA			0.02	0.06	V
	I_{LOAD} = 1mA	●			0.10	V
	I_{LOAD} = 100mA			0.10	0.17	V
	I_{LOAD} = 100mA	●			0.22	V
	I_{LOAD} = 500mA			0.19	0.27	V
	I_{LOAD} = 500mA	●			0.35	V
	I_{LOAD} = 1.5A			0.34	0.45	V
	I_{LOAD} = 1.5A	●			0.55	V
GND Pin Current V_{IN} = $V_{OUT(NOMINAL)}$ + 1V (Notes 6, 8)	I_{LOAD} = 0mA	●		1.0	1.5	mA
	I_{LOAD} = 1mA	●		1.1	1.6	mA
	I_{LOAD} = 100mA	●		3.8	5.5	mA
	I_{LOAD} = 500mA	●		15	25	mA
	I_{LOAD} = 1.5A	●		80	120	mA
Output Voltage Noise	C_{OUT} = 10µF, I_{LOAD} = 1.5A, BW = 10Hz to 100kHz			40		μV_{RMS}
ADJ Pin Bias Current	(Notes 4, 9)			3	10	µA
Shutdown Threshold	V_{OUT} = Off to On	●		0.90	2	V
	V_{OUT} = On to Off	●	0.25	0.75		V
$\overline{SHDN}$ Pin Current (Note 10)	$V_{\overline{SHDN}}$ = 0V			0.01	1	µA
	$V_{\overline{SHDN}}$ = 20V			3	30	µA
Quiescent Current in Shutdown	V_{IN} = 6V, $V_{\overline{SHDN}}$ = 0V			0.01	1	µA
Ripple Rejection	V_{IN} – V_{OUT} = 1.5V (Avg), V_{RIPPLE} = 0.5V_{P-P}, f_{RIPPLE} = 120Hz, I_{LOAD} = 0.75A		55	63		dB

ELECTRICAL CHARACTERISTICS

The ● denotes specifications which apply over the full operating temperature range, otherwise specifications are T_A = 25°C. (Note 3)

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Current Limit	V_{IN} = 7V, V_{OUT} = 0V			2		A
	V_{IN} = $V_{OUT(NOMINAL)}$ + 1V, ΔV_{OUT} = –0.1V	●	1.6			A
Input Reverse Leakage Current (Note 13)	Q, T, S8 Packages V_{IN} = –20V, V_{OUT} = 0V	●			1	mA
	ST Package V_{IN} = –20V, V_{OUT} = 0V	●			2	mA
Reverse Output Current (Note 11)	LT1963-1.5 V_{OUT} = 1.5V, V_{IN} < 1.5V			600	1200	µA
	LT1963-1.8 V_{OUT} = 1.8V, V_{IN} < 1.8V			600	1200	µA
	LT1963-2.5 V_{OUT} = 2.5V, V_{IN} < 2.5V			600	1200	µA
	LT1963-3.3 V_{OUT} = 3.3V, V_{IN} < 3.3V			600	1200	µA
	LT1963 (Note 4) V_{OUT} = 1.21V, V_{IN} < 1.21V			300	600	µA

Note 1: Absolute Maximum Ratings are those values beyond which the life of a device may be impaired.

Note 2: Absolute maximum input to output differential voltage can not be achieved with all combinations of rated IN pin and OUT pin voltages. With the IN pin at 20V, the OUT pin may not be pulled below 0V. The total measured voltage from IN to OUT can not exceed ±20V.

Note 3: The LT1963 regulators are tested and specified under pulse load conditions such that $T_J \approx T_A$. The LT1963 is 100% tested at T_A = 25°C. Performance at –40°C and 125°C is assured by design, characterization and correlation with statistical process controls.

Note 4: The LT1963 (adjustable version) is tested and specified for these conditions with the ADJ pin connected to the OUT pin.

Note 5: Operating conditions are limited by maximum junction temperature. The regulated output voltage specification will not apply for all possible combinations of input voltage and output current. When operating at maximum input voltage, the output current range must be limited. When operating at maximum output current, the input voltage range must be limited.

Note 6: To satisfy requirements for minimum input voltage, the LT1963 (adjustable version) is tested and specified for these conditions with an external resistor divider (two 4.12k resistors) for an output voltage of 2.4V. The external resistor divider will add a 300µA DC load on the output.

Note 7: Dropout voltage is the minimum input to output voltage differential needed to maintain regulation at a specified output current. In dropout, the output voltage will be equal to: $V_{IN} – V_{DROPOUT}$.

Note 8: GND pin current is tested with V_{IN} = $V_{OUT(NOMINAL)}$ + 1V and a current source load. The GND pin current will decrease at higher input voltages.

Note 9: ADJ pin bias current flows into the ADJ pin.

Note 10: $\overline{SHDN}$ pin current flows into the $\overline{SHDN}$ pin.

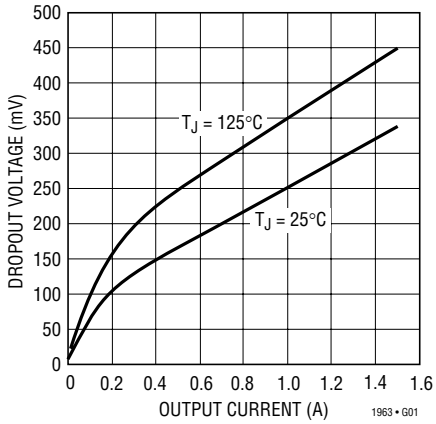
Note 11: Reverse output current is tested with the IN pin grounded and the OUT pin forced to the rated output voltage. This current flows into the OUT pin and out the GND pin.

Note 12. For the LT1963, LT1963-1.5 and LT1963-1.8 dropout voltage will be limited by the minimum input voltage specification under some output voltage/load conditions.

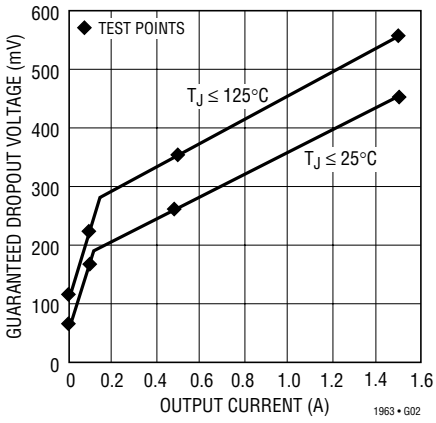
Note 13. For the ST package, the input reverse leakage current increases due to the additional reverse leakage current for the $\overline{SHDN}$ pin, which is tied internally to the IN pin.

TYPICAL PERFORMANCE CHARACTERISTICS

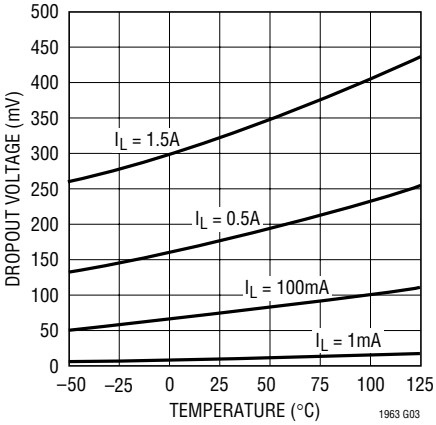
Typical Dropout Voltage



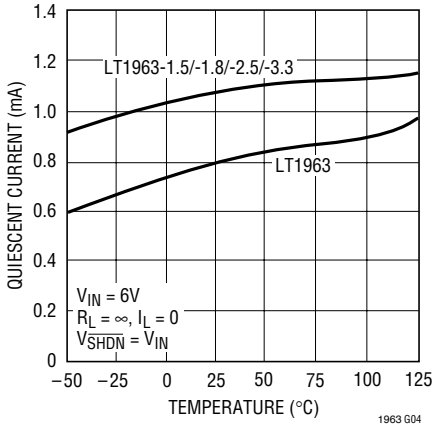
Guaranteed Dropout Voltage



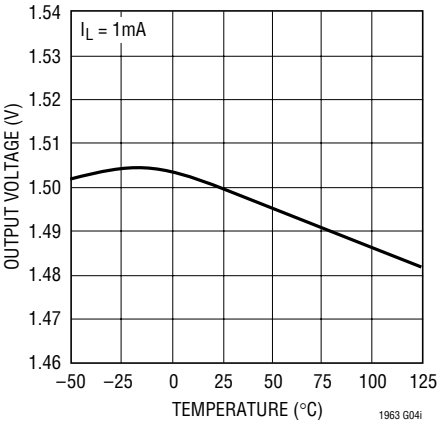
Dropout Voltage



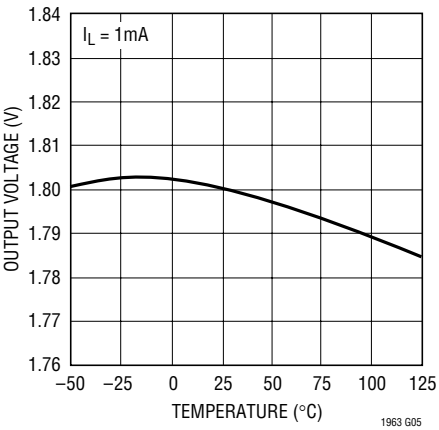
Quiescent Current



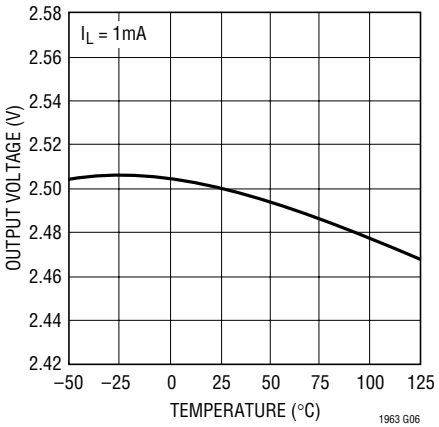
LT1963-1.5 Output Voltage



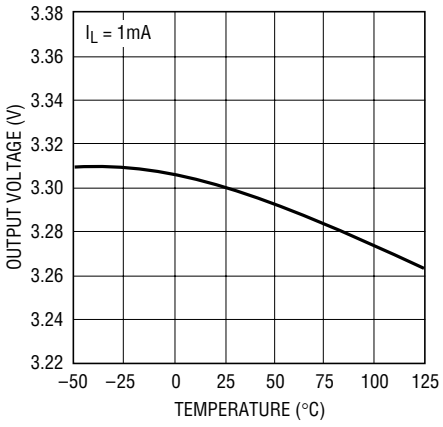
LT1963-1.8 Output Voltage



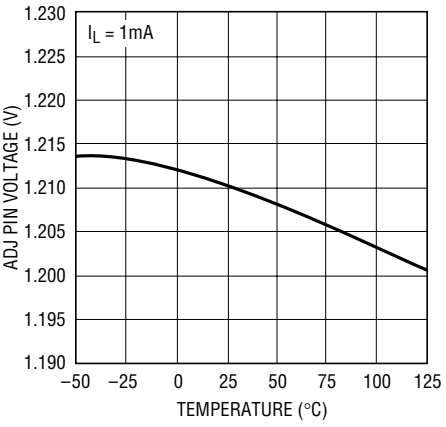
LT1963-2.5 Output Voltage



LT1963-3.3 Output Voltage

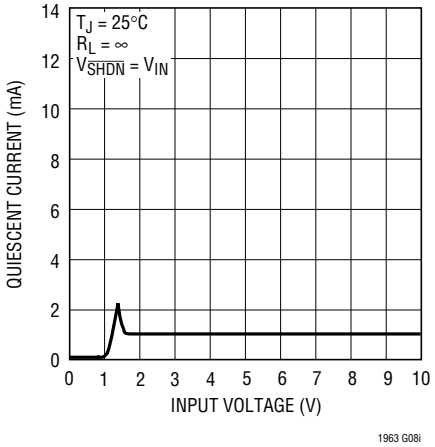


LT1963 ADJ Pin Voltage

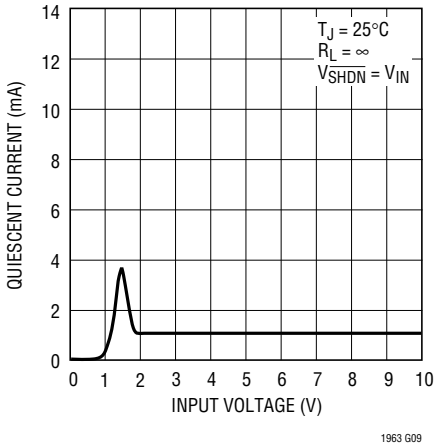


TYPICAL PERFORMANCE CHARACTERISTICS

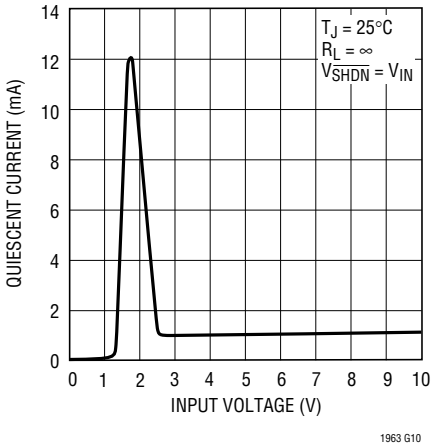
LT1963-1.5 Quiescent Current



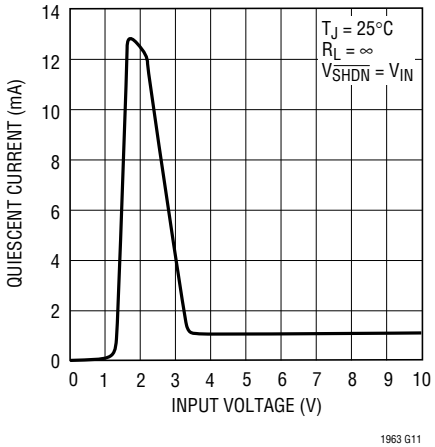
LT1963-1.8 Quiescent Current



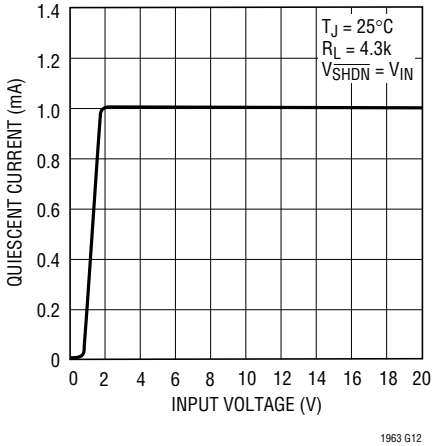
LT1963-2.5 Quiescent Current



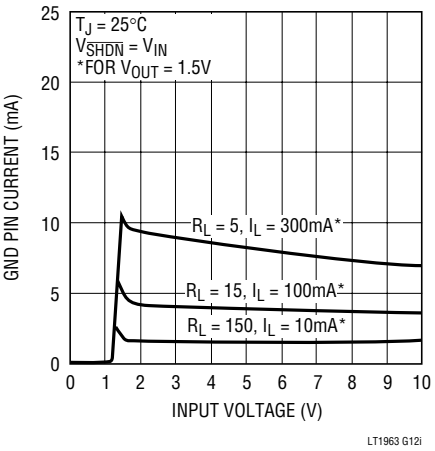
LT1963-3.3 Quiescent Current



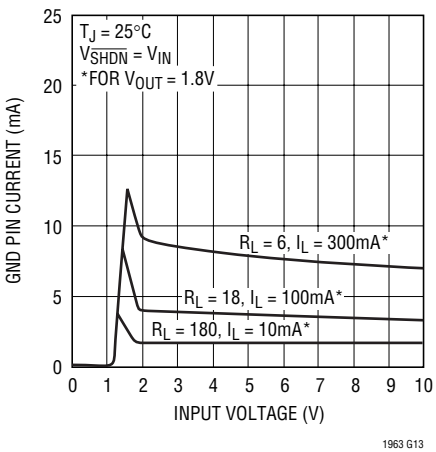
LT1963 Quiescent Current



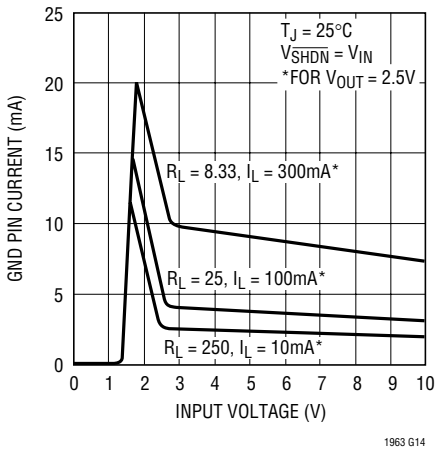
LT1963-1.5 GND Pin Current



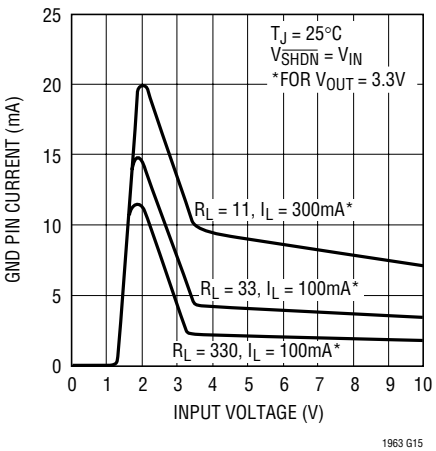
LT1963-1.8 GND Pin Current



LT1963-2.5 GND Pin Current

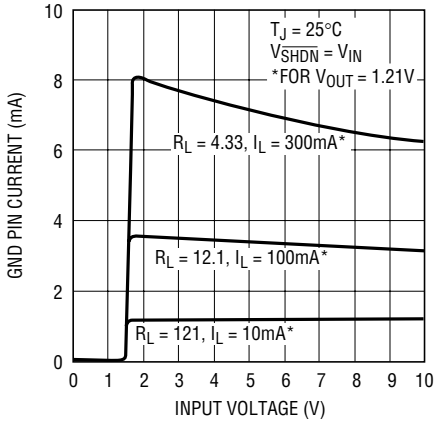


LT1963-3.3 GND Pin Current

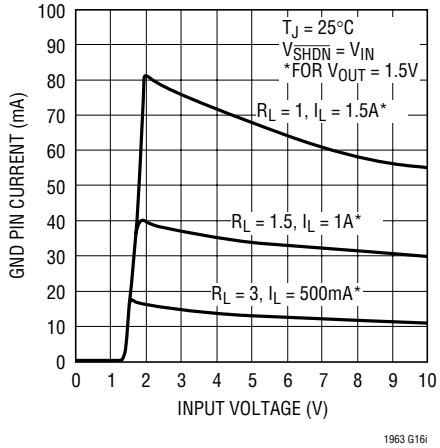


TYPICAL PERFORMANCE CHARACTERISTICS

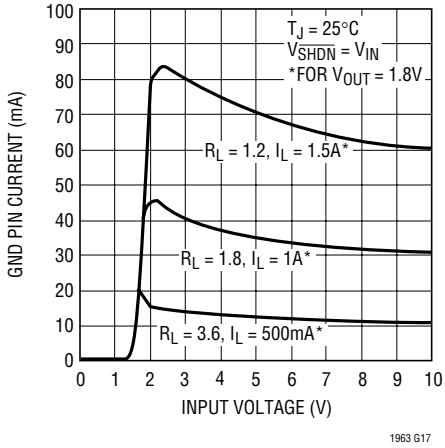
LT1963 GND Pin Current



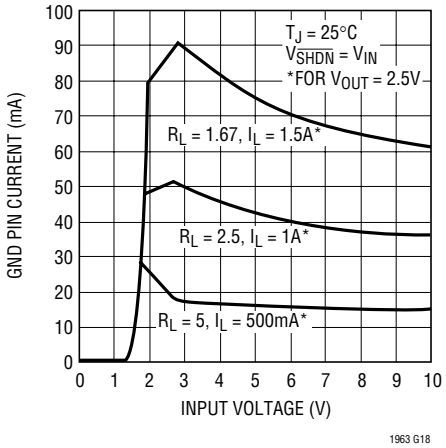
LT1963-1.5 GND Pin Current



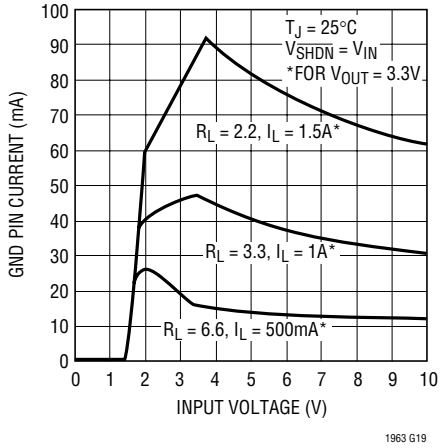
LT1963-1.8 GND Pin Current



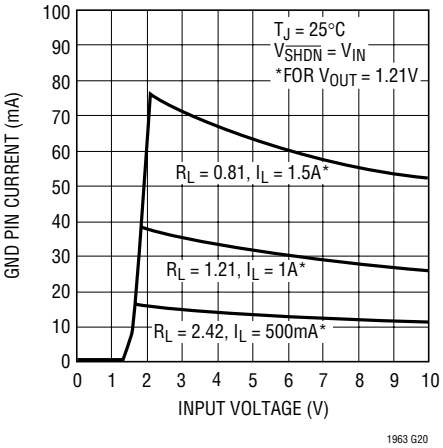
LT1963-2.5 GND Pin Current



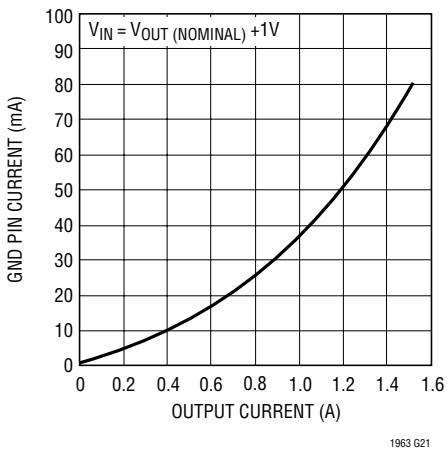
LT1963-3.3 GND Pin Current



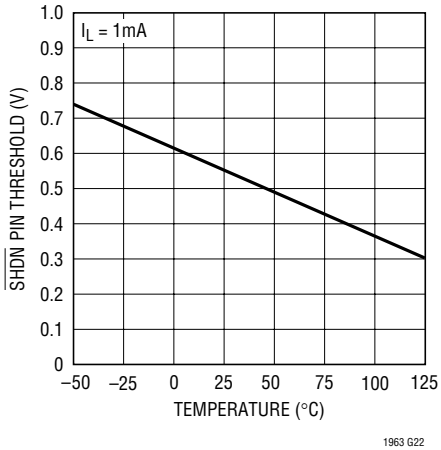
LT1963 GND Pin Current



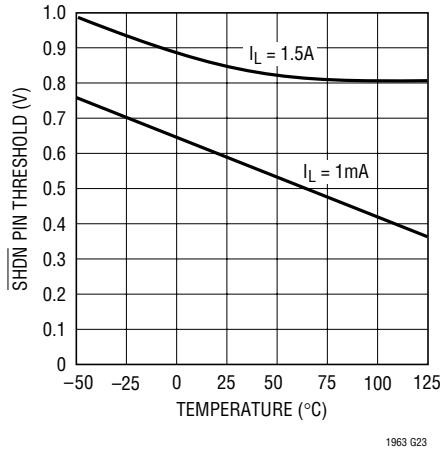
GND Pin Current vs I_{LOAD}



$\overline{SHDN}$ Pin Threshold (On-to-Off)

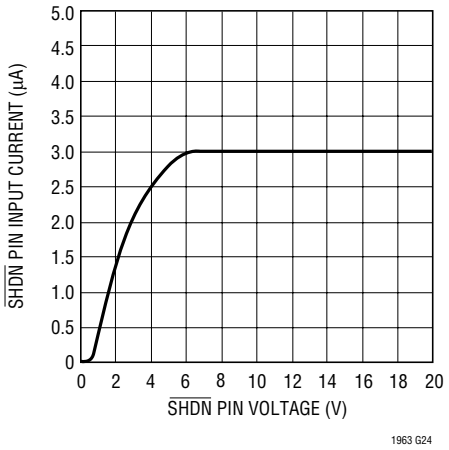


$\overline{SHDN}$ Pin Threshold (Off-to-On)

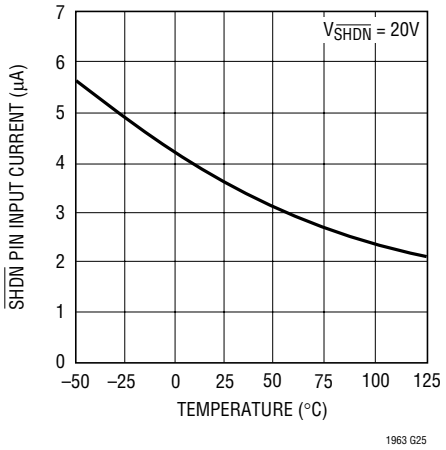


TYPICAL PERFORMANCE CHARACTERISTICS

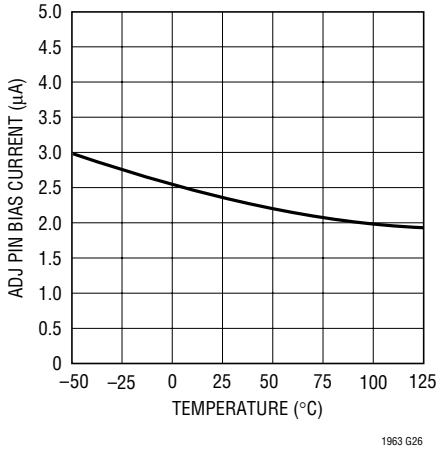
$\overline{SHDN}$ Pin Input Current



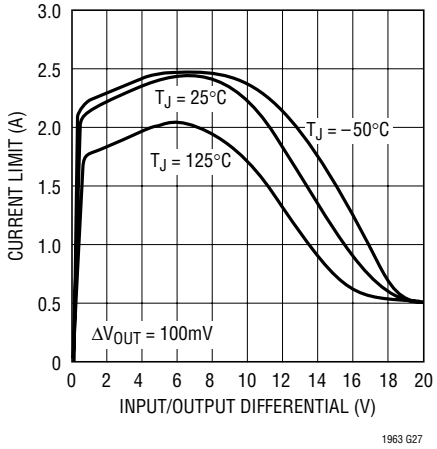
$\overline{SHDN}$ Pin Input Current



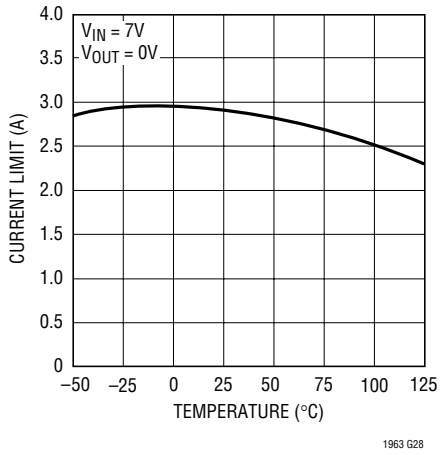
ADJ Pin Bias Current



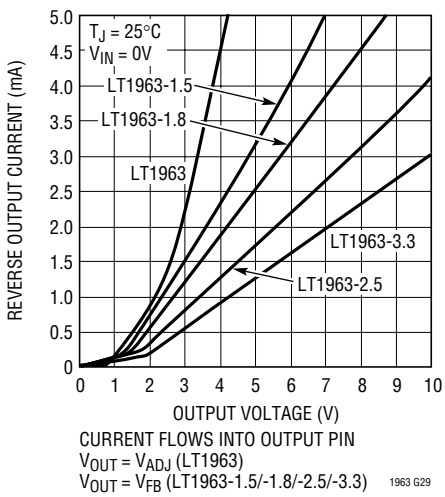
Current Limit



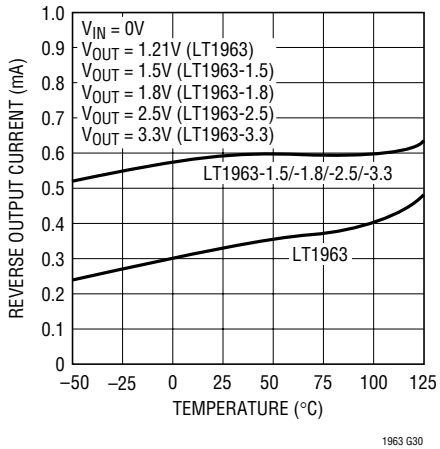
Current Limit



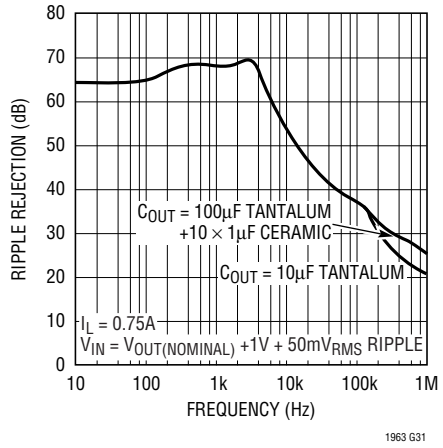
Reverse Output Current



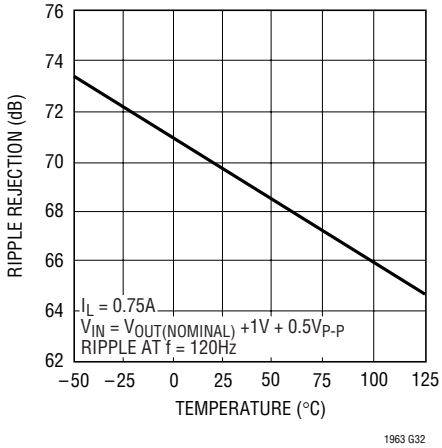
Reverse Output Current



Ripple Rejection

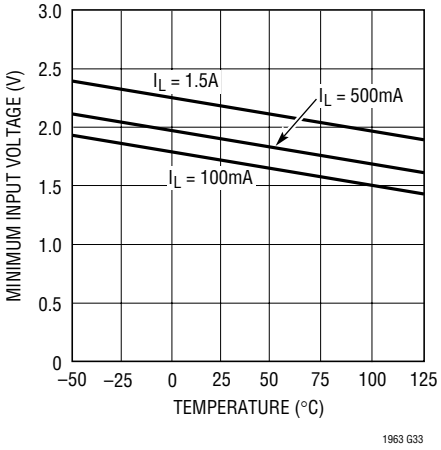


Ripple Rejection

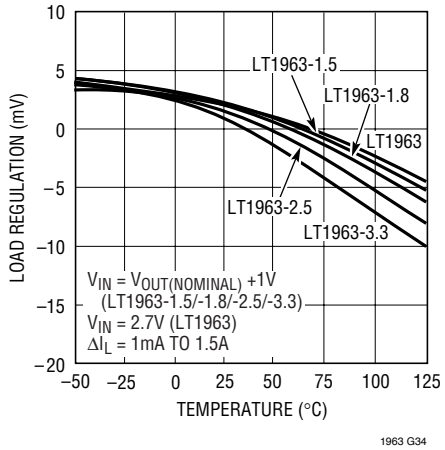


TYPICAL PERFORMANCE CHARACTERISTICS

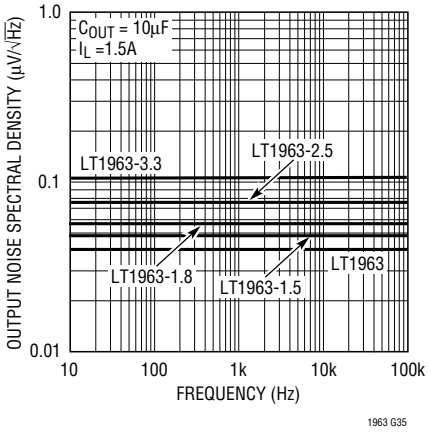
LT1963 Minimum Input Voltage



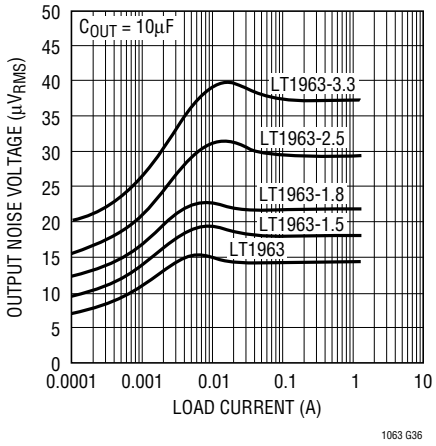
Load Regulation



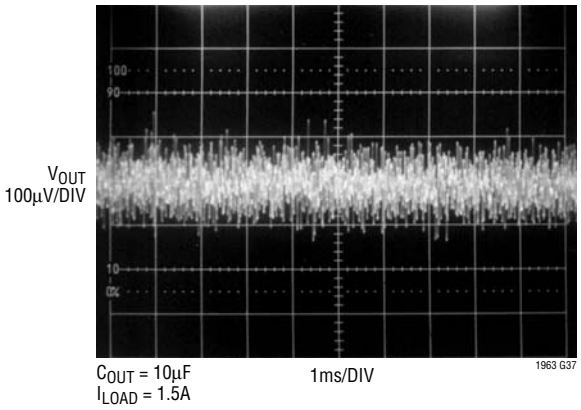
Output Noise Spectral Density



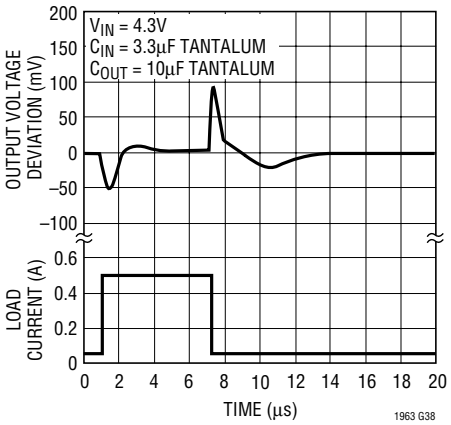
RMS Output Noise vs Load Current (10Hz to 100kHz)



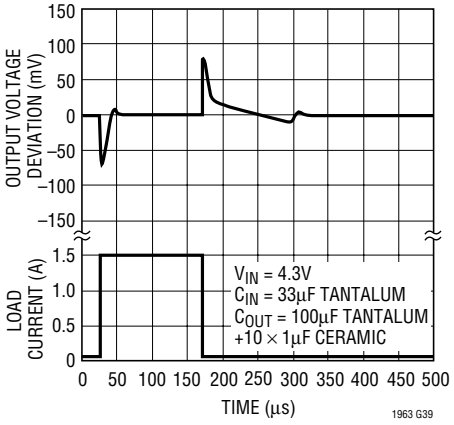
LT1963-3.3 10Hz to 100kHz Output Noise



LT1963-3.3 Transient Response



LT1963-3.3 Transient Response



PIN FUNCTIONS

OUT: Output. The output supplies power to the load. A minimum output capacitor of 10µF is required to prevent oscillations. Larger output capacitors will be required for applications with large transient loads to limit peak voltage transients. See the Applications Information section for more information on output capacitance and reverse output characteristics.

SENSE: Sense. For fixed voltage versions of the LT1963 (LT1963-1.5/LT1963-1.8/LT1963-2.5/LT1963-3.3), the SENSE pin is the input to the error amplifier. Optimum regulation will be obtained at the point where the SENSE pin is connected to the OUT pin of the regulator. In critical applications, small voltage drops are caused by the resistance (R_P) of PC traces between the regulator and the load. These may be eliminated by connecting the SENSE pin to the output at the load as shown in Figure 1 (Kelvin Sense Connection). Note that the voltage drop across the external PC traces will add to the dropout voltage of the regulator. The SENSE pin bias current is 600µA at the nominal rated output voltage. The SENSE pin can be pulled below ground (as in a dual supply system where the regulator load is returned to a negative supply) and still allow the device to start and operate.

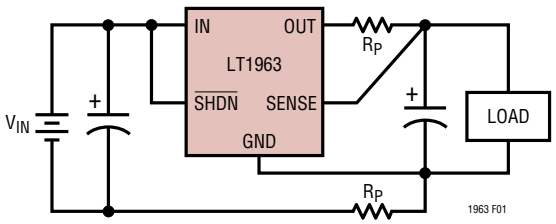


Figure 1. Kelvin Sense Connection

ADJ: Adjust. For the adjustable LT1963, this is the input to the error amplifier. This pin is internally clamped to ±7V. It has a bias current of 3µA which flows into the pin. The ADJ pin voltage is 1.21V referenced to ground and the output voltage range is 1.21V to 20V.

$\overline{\text{SHDN}}$: Shutdown. The $\overline{\text{SHDN}}$ pin is used to put the LT1963 regulators into a low power shutdown state. The output will be off when the $\overline{\text{SHDN}}$ pin is pulled low. The $\overline{\text{SHDN}}$ pin can be driven either by 5V logic or open-collector logic with a pull-up resistor. The pull-up resistor is required to supply the pull-up current of the open-collector gate, normally several microamperes, and the $\overline{\text{SHDN}}$ pin current, typically 3µA. If unused, the $\overline{\text{SHDN}}$ pin must be connected to V_{IN}. The device will be in the low power shutdown state if the $\overline{\text{SHDN}}$ pin is not connected.

IN: Input. Power is supplied to the device through the IN pin. A bypass capacitor is required on this pin if the device is more than six inches away from the main input filter capacitor. In general, the output impedance of a battery rises with frequency, so it is advisable to include a bypass capacitor in battery-powered circuits. A bypass capacitor in the range of 1µF to 10µF is sufficient. The LT1963 regulators are designed to withstand reverse voltages on the IN pin with respect to ground and the OUT pin. In the case of a reverse input, which can happen if a battery is plugged in backwards, the device will act as if there is a diode in series with its input. There will be no reverse current flow into the regulator and no reverse voltage will appear at the load. The device will protect both itself and the load.

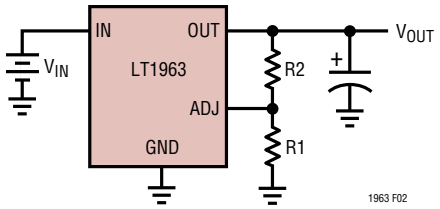
Exposed Pad: GND. The Exposed Pad (FE Package) is ground and must be soldered to the PCB for rated thermal performance.

APPLICATIONS INFORMATION

The LT1963 series are 1.5A low dropout regulators optimized for fast transient response. The devices are capable of supplying 1.5A at a dropout voltage of 350mV. The low operating quiescent current (1mA) drops to less than 1μA in shutdown. In addition to the low quiescent current, the LT1963 regulators incorporate several protection features which make them ideal for use in battery-powered systems. The devices are protected against both reverse input and reverse output voltages. In battery backup applications where the output can be held up by a backup battery when the input is pulled to ground, the LT1963-X acts like it has a diode in series with its output and prevents reverse current flow. Additionally, in dual supply applications where the regulator load is returned to a negative supply, the output can be pulled below ground by as much as 20V and still allow the device to start and operate.

Adjustable Operation

The adjustable version of the LT1963 has an output voltage range of 1.21V to 20V. The output voltage is set by the ratio of two external resistors as shown in Figure 2. The device servos the output to maintain the voltage at the ADJ pin at 1.21V referenced to ground. The current in R1 is then equal to 1.21V/R1 and the current in R2 is the current in R1 plus the ADJ pin bias current. The ADJ pin bias current, 3μA at 25°C, flows through R2 into the ADJ pin. The output voltage can be calculated using the formula in Figure 2. The value of R1 should be less than 4.17k to minimize errors in the output voltage caused by the ADJ pin bias current. Note that in shutdown the output is turned off and the divider current will be zero.



$$V_{OUT} = 1.21V\left(1+\frac{R2}{R1}\right)+(I_{ADJ})(R2)$$

$V_{ADJ} = 1.21V$

$I_{ADJ} = 3\mu A$ AT 25°C

OUTPUT RANGE = 1.21V TO 20V

Figure 2. Adjustable Operation

The adjustable device is tested and specified with the ADJ pin tied to the OUT pin for an output voltage of 1.21V. Specifications for output voltages greater than 1.21V will be proportional to the ratio of the desired output voltage to 1.21V: V_{OUT}/1.21V. For example, load regulation for an output current change of 1mA to 1.5A is –3mV typical at V_{OUT} = 1.21V. At V_{OUT} = 5V, load regulation is:

(5V/1.21V)(–3mV) = –12.4mV

Output Capacitance and Transient Response

The LT1963 regulators are designed to be stable with a wide range of output capacitors. The ESR of the output capacitor affects stability, most notably with small capacitors. A minimum output capacitor of 10μF with an ESR in the range of 50mΩ to 3Ω is recommended to prevent oscillations. Larger values of output capacitance can decrease the peak deviations and provide improved transient response for larger load current changes. Bypass capacitors, used to decouple individual components powered by the LT1963, will increase the effective output capacitor value.

Extra consideration must be given to the use of ceramic capacitors. Ceramic capacitors are manufactured with a variety of dielectrics, each with different behavior across temperature and applied voltage. The most common dielectrics used are specified with EIA temperature characteristic codes of Z5U, Y5V, X5R and X7R. The Z5U and Y5V dielectrics are good for providing high capacitances in a small package, but they tend to have strong voltage and temperature coefficients as shown in Figures 2 and 3. When used with a 5V regulator, a 16V 10μF Y5V capacitor can exhibit an effective value as low as 1μF to 2μF for the DC bias voltage applied and over the operating temperature range. The X5R and X7R dielectrics result in more stable characteristics and are more suitable for use as the output capacitor. The X7R type has better stability across temperature, while the X5R is less expensive and is available in higher values. Care still must be exercised when using X5R and X7R capacitors; the X5R and X7R codes only specify operating temperature range and maximum capacitance change over temperature. Capacitance change due to DC bias with X5R and X7R capacitors is better than Y5V and Z5U capacitors, but can still be significant enough to drop capacitor values below appropriate levels. Capacitor DC bias characteristics tend to

APPLICATIONS INFORMATION

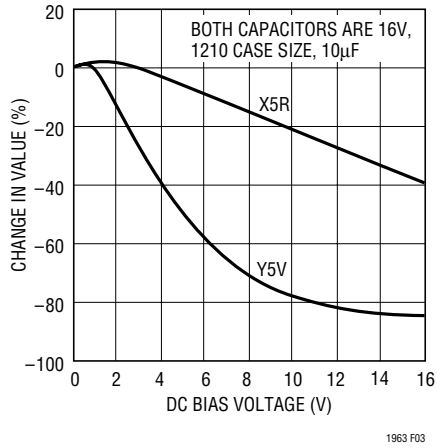


Figure 3. Ceramic Capacitor DC Bias Characteristics

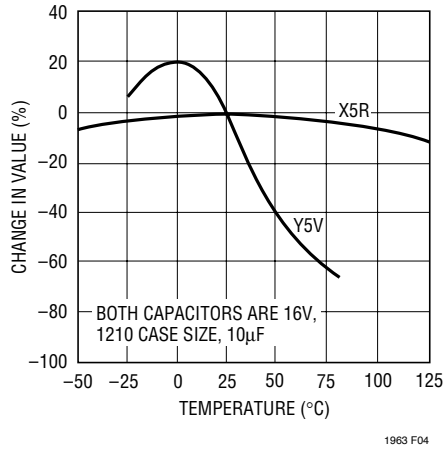


Figure 4. Ceramic Capacitor Temperature Characteristics

improve as component case size increases, but expected capacitance at operating voltage should be verified.

Voltage and temperature coefficients are not the only sources of problems. Some ceramic capacitors have a piezoelectric response. A piezoelectric device generates voltage across its terminals due to mechanical stress, similar to the way a piezoelectric accelerometer or microphone works. For a ceramic capacitor the stress can be induced by vibrations in the system or thermal transients.

Overload Recovery

Like many IC power regulators, the LT1963-X has safe operating area protection. The safe area protection decreases the current limit as input-to-output voltage increases and keeps the power transistor inside a safe operating region for all values of input-to-output voltage. The protection is designed to provide some output current at all values of input-to-output voltage up to the device breakdown.

When power is first turned on, as the input voltage rises, the output follows the input, allowing the regulator to start up into very heavy loads. During the start-up, as the input voltage is rising, the input-to-output voltage differential is small, allowing the regulator to supply large output currents. With a high input voltage, a problem can occur wherein removal of an output short will not allow the output voltage to recover. Other regulators, such as the LT1085, also exhibit this phenomenon, so it is not unique to the LT1963-X.

The problem occurs with a heavy output load when the input voltage is high and the output voltage is low. Common situations are immediately after the removal of a short-circuit or when the shutdown pin is pulled high after the input voltage has already been turned on. The load line for such a load may intersect the output current curve at two points. If this happens, there are two stable output operating points for the regulator. With this double intersection, the input power supply may need to be cycled down to zero and brought up again to make the output recover.

Output Voltage Noise

The LT1963 regulators have been designed to provide low output voltage noise over the 10Hz to 100kHz bandwidth while operating at full load. Output voltage noise is typically 40nV/$\sqrt{\text{Hz}}$ over this frequency bandwidth for the LT1963 (adjustable version). For higher output voltages (generated by using a resistor divider), the output voltage noise will be gained up accordingly. This results in RMS noise over the 10Hz to 100kHz bandwidth of 14μV_{RMS} for the LT1963 increasing to 38μV_{RMS} for the LT1963-3.3.

Higher values of output voltage noise may be measured when care is not exercised with regards to circuit layout and testing. Crosstalk from nearby traces can induce unwanted noise onto the output of the LT1963-X. Power supply ripple rejection must also be considered; the LT1963 regulators do not have unlimited power supply rejection and will pass a small portion of the input noise through to the output.

APPLICATIONS INFORMATION

Thermal Considerations

The power handling capability of the device is limited by the maximum rated junction temperature (125°C). The power dissipated by the device is made up of two components:

1. Output current multiplied by the input/output voltage differential: $(I_{OUT})(V_{IN} – V_{OUT})$, and
2. GND pin current multiplied by the input voltage: $(I_{GND})(V_{IN})$.

The GND pin current can be found using the GND Pin Current curves in the Typical Performance Characteristics. Power dissipation will be equal to the sum of the two components listed above.

The LT1963 series regulators have internal thermal limiting designed to protect the device during overload conditions. For continuous normal conditions, the maximum junction temperature rating of 125°C must not be exceeded. It is important to give careful consideration to all sources of thermal resistance from junction to ambient. Additional heat sources mounted nearby must also be considered.

For surface mount devices, heat sinking is accomplished by using the heat spreading capabilities of the PC board and its copper traces. Copper board stiffeners and plated through-holes can also be used to spread the heat generated by power devices.

The following tables list thermal resistance for several different board sizes and copper areas. All measurements were taken in still air on 1/16" FR-4 board with one ounce copper.

Table 1. Q Package, 5-Lead DD

COPPER AREA		BOARD AREA	THERMAL RESISTANCE (JUNCTION-TO-AMBIENT)
TOPSIDE*	BACKSIDE		
2500mm^2	2500mm^2	2500mm^2	23°C/W
1000mm^2	2500mm^2	2500mm^2	25°C/W
125mm^2	2500mm^2	2500mm^2	33°C/W

* Device is mounted on topside

Table 2. SO-8 Package, 8-Lead SO

COPPER AREA		BOARD AREA	THERMAL RESISTANCE (JUNCTION-TO-AMBIENT)
TOPSIDE*	BACKSIDE		
2500mm^2	2500mm^2	2500mm^2	55°C/W
1000mm^2	2500mm^2	2500mm^2	55°C/W
225mm^2	2500mm^2	2500mm^2	63°C/W
100mm^2	2500mm^2	2500mm^2	69°C/W

* Device is mounted on topside

Table 3. SOT-223 Package, 3-Lead SOT-223

COPPER AREA		BOARD AREA	THERMAL RESISTANCE (JUNCTION-TO-AMBIENT)
TOPSIDE*	BACKSIDE		
2500mm^2	2500mm^2	2500mm^2	42°C/W
1000mm^2	2500mm^2	2500mm^2	42°C/W
225mm^2	2500mm^2	2500mm^2	50°C/W
100mm^2	2500mm^2	2500mm^2	56°C/W
1000mm^2	1000mm^2	1000mm^2	49°C/W
1000mm^2	0mm^2	1000mm^2	52°C/W

* Device is mounted on topside

Table 4. FE Package, 16-Lead TSSOP

COPPER AREA		BOARD AREA	THERMAL RESISTANCE (JUNCTION-TO-AMBIENT)
TOPSIDE*	BACKSIDE		
2500mm^2	2500mm^2	2500mm^2	38°C/W
1000mm^2	2500mm^2	2500mm^2	43°C/W
225mm^2	2500mm^2	2500mm^2	48°C/W
100mm^2	2500mm^2	2500mm^2	60°C/W

* Device is mounted on topside

T Package, 5-Lead TO-220

Thermal Resistance (Junction-to-Case) = 4°C/W

Calculating Junction Temperature

Example: Given an output voltage of 3.3V, an input voltage range of 4V to 6V, an output current range of 0mA to 500mA and a maximum ambient temperature of 50°C, what will the maximum junction temperature be?

The power dissipated by the device will be equal to:

$$I_{OUT(MAX)}(V_{IN(MAX)} – V_{OUT}) + I_{GND}(V_{IN(MAX)})$$

where,

$I_{OUT(MAX)}$ = 500mA
$V_{IN(MAX)}$ = 6V
I_{GND} at (I_{OUT} = 500mA, V_{IN} = 6V) = 10mA

So,

$$P = 500mA(6V – 3.3V) + 10mA(6V) = 1.41W$$

APPLICATIONS INFORMATION

Using a DD package, the thermal resistance will be in the range of 23°C/W to 33°C/W depending on the copper area. So the junction temperature rise above ambient will be approximately equal to:

1.41W(28°C/W) = 39.5°C

The maximum junction temperature will then be equal to the maximum junction temperature rise above ambient plus the maximum ambient temperature or:

T_{JMAX} = 50°C + 39.5°C = 89.5°C

Protection Features

The LT1963 regulators incorporate several protection features which make them ideal for use in battery-powered circuits. In addition to the normal protection features associated with monolithic regulators, such as current limiting and thermal limiting, the devices are protected against reverse input voltages, reverse output voltages and reverse voltages from output to input.

Current limit protection and thermal overload protection are intended to protect the device against current overload conditions at the output of the device. For normal operation, the junction temperature should not exceed 125°C.

The input of the device will withstand reverse voltages of 20V. Current flow into the device will be limited to less than 1mA (typically less than 100µA) and no negative voltage will appear at the output. The device will protect both itself and the load. This provides protection against batteries that can be plugged in backward.

The output of the LT1963 can be pulled below ground without damaging the device. If the input is left open circuit or grounded, the output can be pulled below ground by 20V. For fixed voltage versions, the output will act like a large resistor, typically 5k or higher, limiting current flow to typically less than 600µA. For adjustable versions, the output will act like an open circuit; no current will flow out of the pin. If the input is powered by a voltage source, the output will source the short-circuit current of the device and will protect itself by thermal limiting. In this case, grounding the $\overline{SHDN}$ pin will turn off the device and stop the output from sourcing the short-circuit current.

The ADJ pin of the adjustable device can be pulled above or below ground by as much as 7V without damaging the device. If the input is left open circuit or grounded, the ADJ pin will act like an open circuit when pulled below ground and like a large resistor (typically 5k) in series with a diode when pulled above ground.

In situations where the ADJ pin is connected to a resistor divider that would pull the ADJ pin above its 7V clamp voltage if the output is pulled high, the ADJ pin input current must be limited to less than 5mA. For example, a resistor divider is used to provide a regulated 1.5V output from the 1.21V reference when the output is forced to 20V. The top resistor of the resistor divider must be chosen to limit the current into the ADJ pin to less than 5mA when the ADJ pin is at 7V. The 13V difference between OUT and ADJ pins divided by the 5mA maximum current into the ADJ pin yields a minimum top resistor value of 2.6k.

In circuits where a backup battery is required, several different input/output conditions can occur. The output voltage may be held up while the input is either pulled to ground, pulled to some intermediate voltage, or is left open circuit. Current flow back into the output will follow the curve shown in Figure 5.

When the IN pin of the LT1963 is forced below the OUT pin or the OUT pin is pulled above the IN pin, input current will typically drop to less than 2µA. This can happen if the input of the device is connected to a discharged (low voltage) battery and the output is held up by either a backup battery or a second regulator circuit. The state of the $\overline{SHDN}$ pin will have no effect on the reverse output current when the output is pulled above the input.

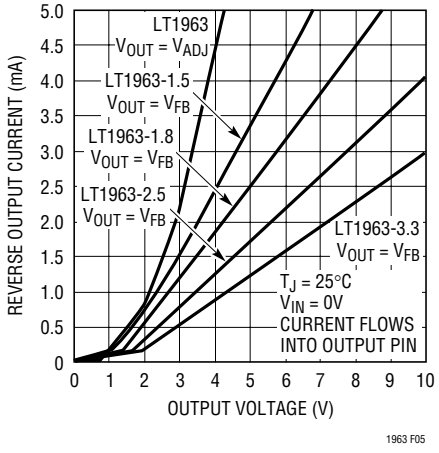
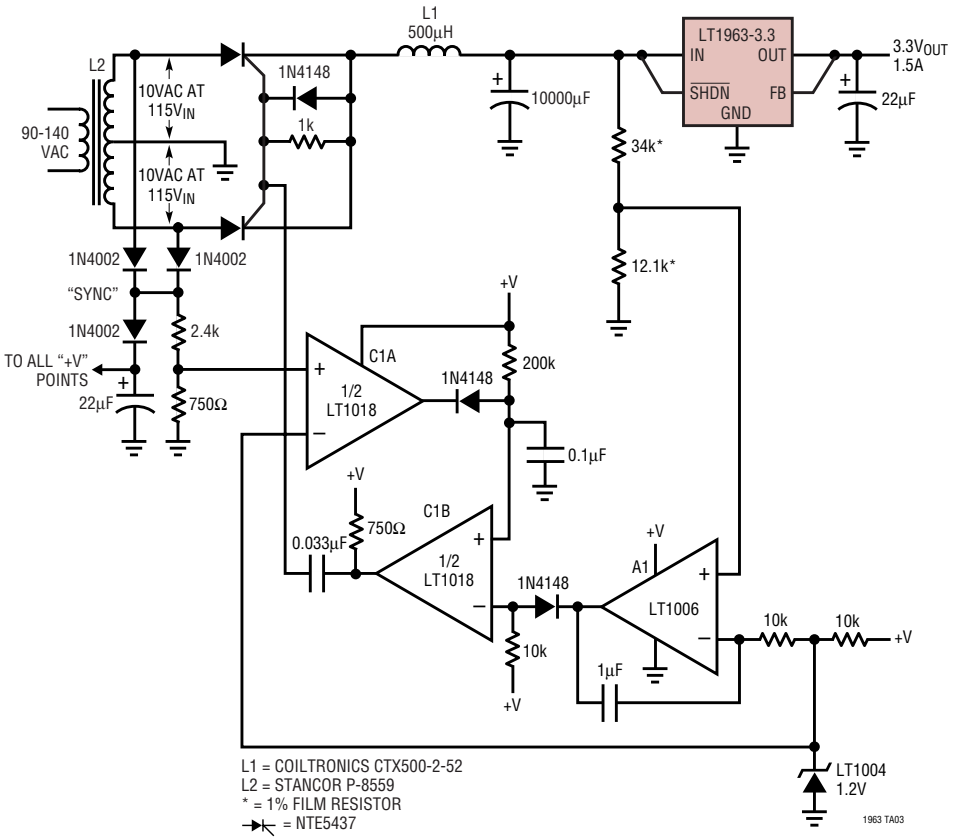


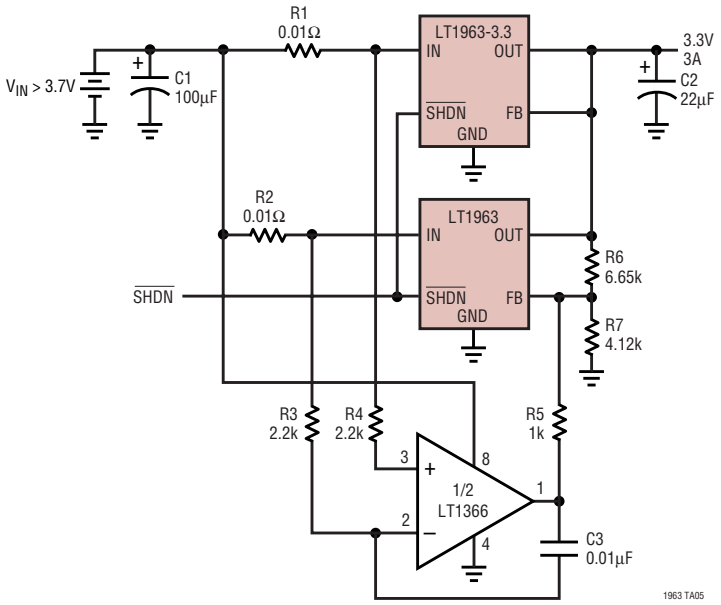
Figure 5. Reverse Output Current

TYPICAL APPLICATIONS

SCR Pre-Regulator Provides Efficiency Over Line Variations

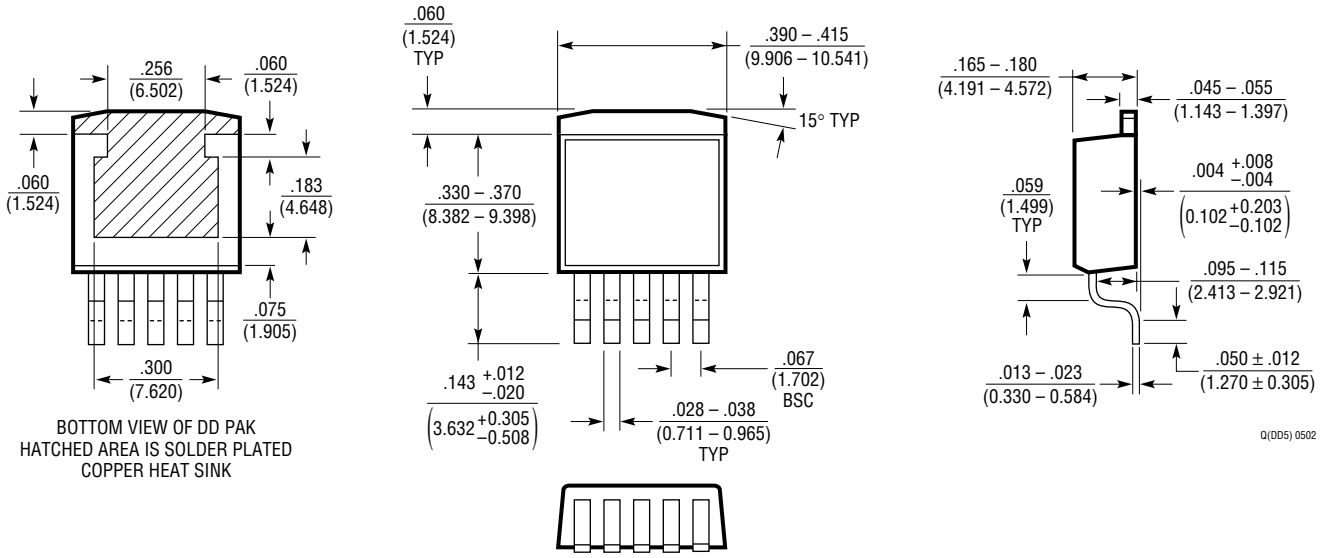


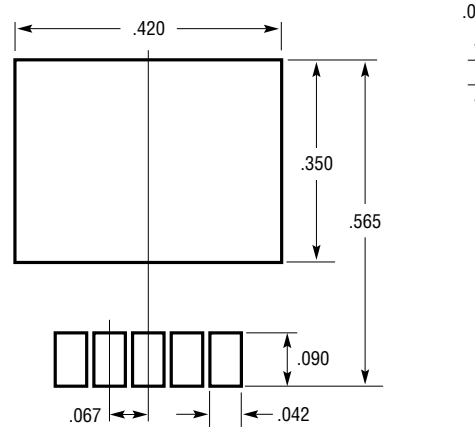
Paralleling of Regulators for Higher Output Current



PACKAGE DESCRIPTION

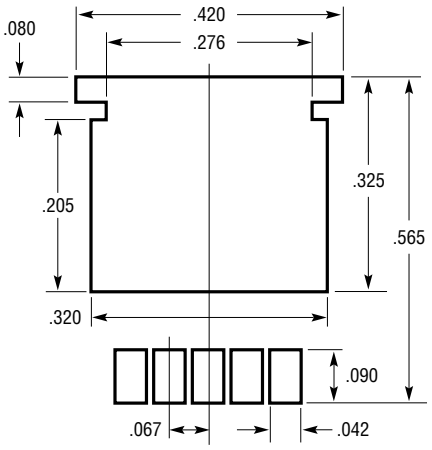
Q Package
5-Lead Plastic DD Pak
(Reference LTC DWG # 05-08-1461)





RECOMMENDED SOLDER PAD LAYOUT

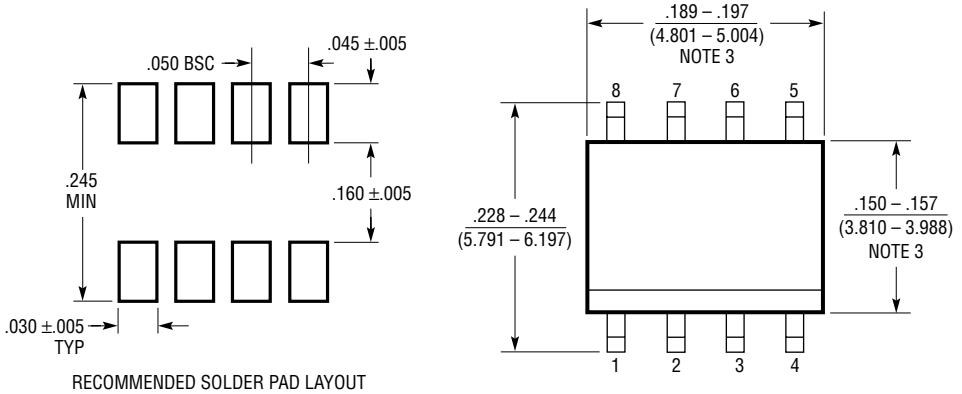
NOTE:
1. DIMENSIONS IN INCH/(MILLIMETER)
2. DRAWING NOT TO SCALE



RECOMMENDED SOLDER PAD LAYOUT
FOR THICKER SOLDER PASTE APPLICATIONS

PACKAGE DESCRIPTION

S8 Package
8-Lead Plastic Small Outline (Narrow .150 Inch)
(Reference LTC DWG # 05-08-1610)

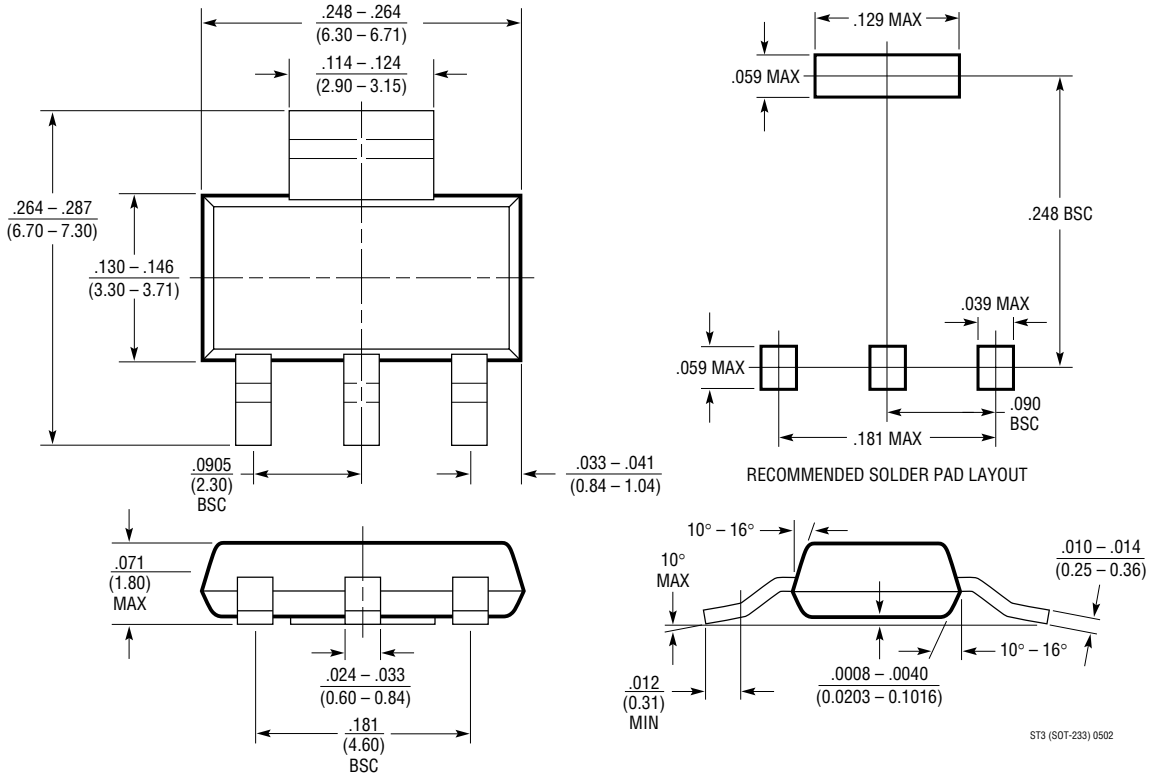


NOTE:
1. DIMENSIONS IN $\frac{\text{INCHES}}{(\text{MILLIMETERS})}$
2. DRAWING NOT TO SCALE
3. THESE DIMENSIONS DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS.
   MOLD FLASH OR PROTRUSIONS SHALL NOT EXCEED .006" (0.15mm)

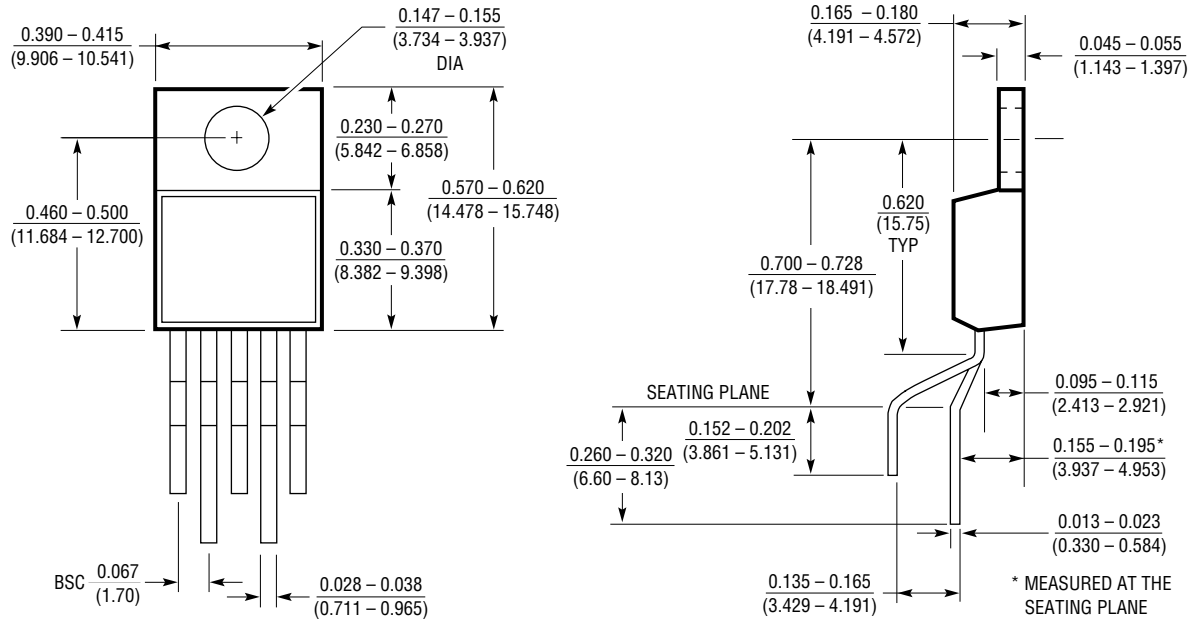
S08 0303

PACKAGE DESCRIPTION

ST Package
3-Lead Plastic SOT-223
(Reference LTC DWG # 05-08-1630)

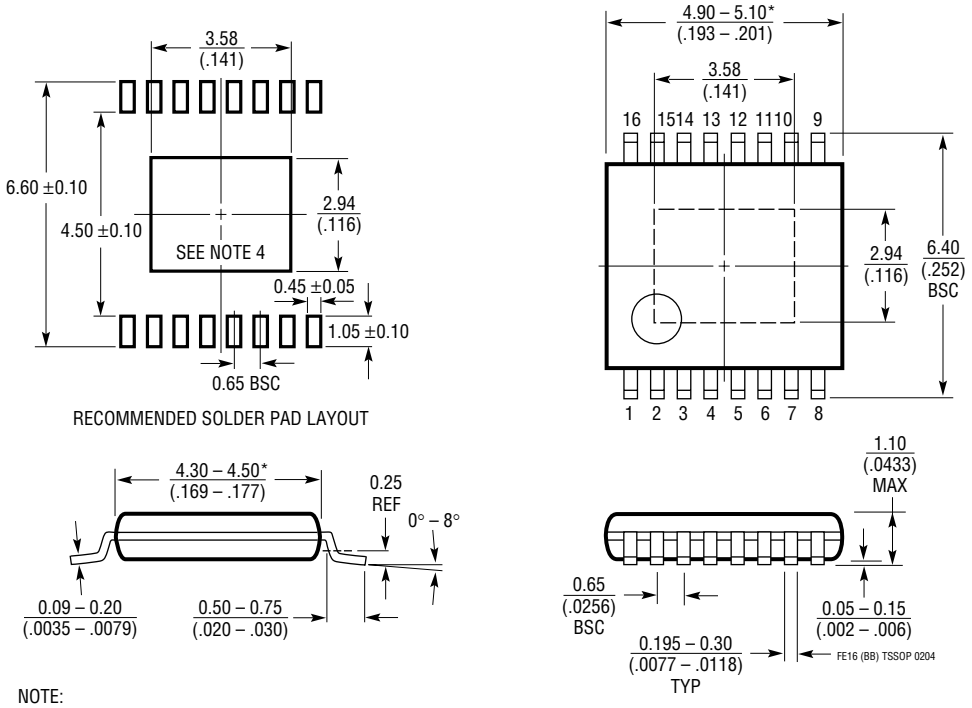


T Package
5-Lead Plastic TO-220 (Standard)
(Reference LTC DWG # 05-08-1421)



PACKAGE DESCRIPTION

FE Package
16-Lead Plastic TSSOP (4.4mm)
(Reference LTC DWG # 05-08-1663)
Exposed Pad Variation BB

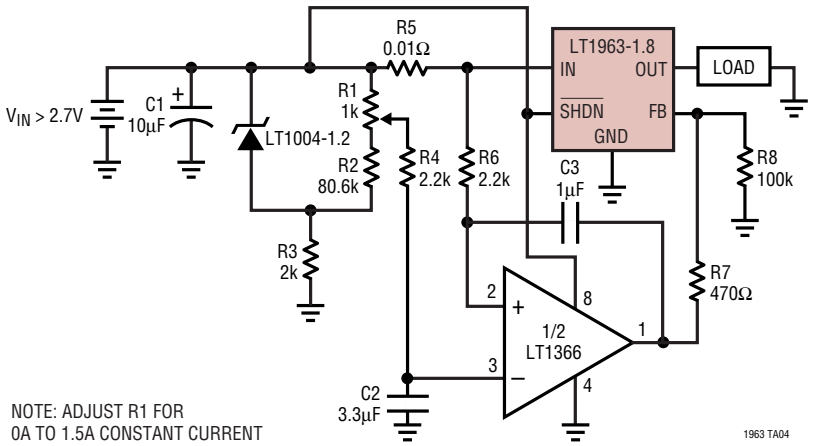


NOTE:
1. CONTROLLING DIMENSION: MILLIMETERS
2. DIMENSIONS ARE IN $\frac{\text{MILLIMETERS}}{(\text{INCHES})}$
3. DRAWING NOT TO SCALE
4. RECOMMENDED MINIMUM PCB METAL SIZE FOR EXPOSED PAD ATTACHMENT
*DIMENSIONS DO NOT INCLUDE MOLD FLASH. MOLD FLASH SHALL NOT EXCEED 0.150mm (.006") PER SIDE

Information furnished by Linear Technology Corporation is believed to be accurate and reliable. However, no responsibility is assumed for its use. Linear Technology Corporation makes no representation that the interconnection of its circuits as described herein will not infringe on existing patent rights.

TYPICAL APPLICATIONS

Adjustable Current Source



RELATED PARTS

PART NUMBER	DESCRIPTION	COMMENTS
LT1129	700mA, Micropower, LDO	V_{IN}: 4.2V to 30V, $V_{OUT(MIN)}$ = 3.75V, V_{DO} = 0.40V, I_Q = 50µA, I_{SD} = 16µA, DD, SOT-223, S8, TO220, TSSOP20 Packages
LT1175	500mA, Micropower Negative LDO	V_{IN}: –20V to –4.3V, $V_{OUT(MIN)}$ = –3.8V, V_{DO} = 0.50V, I_Q = 45µA, I_{SD} = 10µA, DD, SOT-223, S8 Packages
LT1185	3A, Negative LDO	V_{IN}: –35V to –4.2V, $V_{OUT(MIN)}$ = –2.40V, V_{DO} = 0.80V, I_Q = 2.5mA, I_{SD} <1µA, TO220-5 Package
LT1761	100mA, Low Noise Micropower, LDO	V_{IN}: 1.8V to 20V, $V_{OUT(MIN)}$ = 1.22V, V_{DO} = 0.30V, I_Q = 20µA, I_{SD} <1µA, ThinSOT Package
LT1762	150mA, Low Noise Micropower, LDO	V_{IN}: 1.8V to 20V, $V_{OUT(MIN)}$ = 1.22V, V_{DO} = 0.30V, I_Q = 25µA, I_{SD} <1µA, MS8 Package
LT1763	500mA, Low Noise Micropower, LDO	V_{IN}: 1.8V to 20V, $V_{OUT(MIN)}$ = 1.22V, V_{DO} = 0.30V, I_Q = 30µA, I_{SD} <1µA, S8 Package
LT1764/ LT1764A	3A, Low Noise, Fast Transient Response, LDO	V_{IN}: 2.7V to 20V, $V_{OUT(MIN)}$ = 1.21V, V_{DO} = 0.34V, I_Q = 1mA, I_{SD} <1µA, DD, TO220 Packages
LTC1844	150mA, Very Low Drop-Out LDO	V_{IN}: 6.5V to 1.6V, $V_{OUT(MIN)}$ = 1.25V, V_{DO} = 0.08V, I_Q = 40µA, I_{SD} <1µA, ThinSOT Package
LT1962	300mA, Low Noise Micropower, LDO	V_{IN}: 1.8V to 20V, $V_{OUT(MIN)}$ = 1.22V, V_{DO} = 0.27V, I_Q = 30µA, I_{SD} <1µA, MS8 Package
LT1963/ LT1963A	1.5A, Low Noise, Fast Transient Response, LDO	V_{IN}: 2.1V to 20V, $V_{OUT(MIN)}$ = 1.21V, V_{DO} = 0.34V, I_Q = 1mA, I_{SD} <1µA, DD, TO220, SOT Packages
LT1964	200mA, Low Noise Micropower, Negative LDO	V_{IN}: –0.9V to –20V, $V_{OUT(MIN)}$ = –1.21V, V_{DO} = 0.34V, I_Q = 30µA, I_{SD} = 3µA, ThinSOT Package
LT3020	100mA, Low Voltage V_{LDO}	V_{IN}: 0.9V to 10V, $V_{OUT(MIN)}$ = 0.20, V_{DO} = 0.15V, I_Q = 120µA, I_{SD} <3µA, DFN, MS8 Packages
LT3023	Dual, 2x 100mA, Low Noise Micropower, LDO	V_{IN}: 1.8V to 20V, $V_{OUT(MIN)}$ = 1.22V, V_{DO} = 0.30V, I_Q = 40µA, I_{SD} <1µA, DFN, MS10 Packages
LT3024	Dual, 100mA/500mA, Low Noise Micropower, LDO	V_{IN}: 1.8V to 20V, $V_{OUT(MIN)}$ = 1.22V, V_{DO} = 0.30V, I_Q = 60µA, I_{SD} <1µA, DFN, TSSOP Package
LT3150	Fast Transient Response, Low Input Voltage	V_{IN}: –1.4V to 10V, $V_{OUT(MIN)}$ = 1.23V, V_{DO} = 0.13V, I_Q = 12mA, I_{SD} = 25µA, GN16 Package

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