High Input Voltage SMPS Start-up / Linear Regulator

Features

- Accepts inputs from 15V to 450V
- Output currents up to 3.0mA continuous, 30mA peak
- Supply current typically 50µA
- Line regulation typically 0.1mV/V
- Output can be trimmed from 8.0V to 12V
- Output current can be increased to 150mA with external FET

Applications

- Off-line SMPS startup circuits (pulse loads)
- Low power off-line regulators
- Regulators for noisy inputs

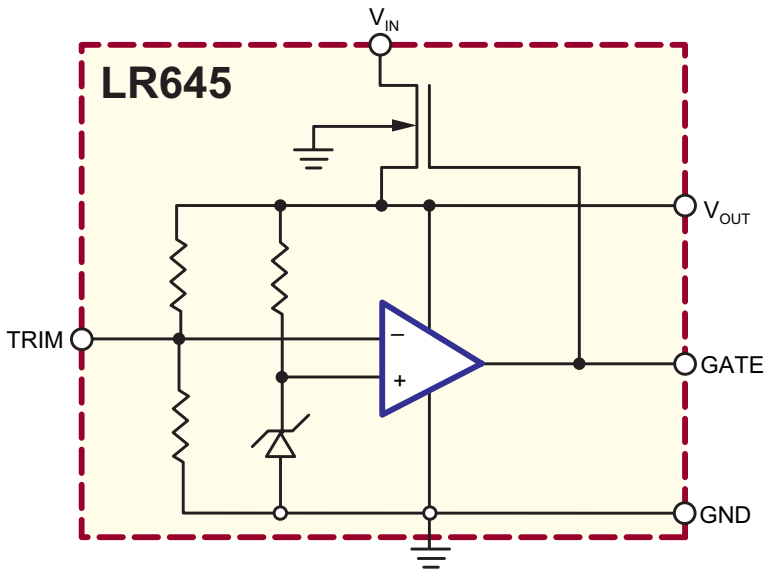
Caution!
The LR645 does NOT provide galvanic isolation. When operated from an AC line, potentially lethal voltages can be present on the IC. Adequate means of protecting the end user from such voltages must be provided by the circuit developer.

General Description

The Supertex LR645 is a high input voltage, low output current linear regulator. It has a 3-terminal fixed output voltage version available in TO-92, TO-220 and SOT-89 packages, as well as an adjustable voltage version available in an 8-lead SOIC package. The 3-terminal version functions like any other low voltage 3-terminal regulator except it allows the use of much higher input voltages. When used in a SMPS start-up circuit, it eliminates the need for large power resistors. In this application, current is drawn from the high voltage line only during start-up. Only leakage current flows after start-up, thereby reducing the continuous power dissipation to a few milliwatts.

The adjustable voltage version allows trimming of the output voltage from 8.0V to 12V. This version can also be connected to an external depletion mode MOSFET for increased output current. When used in conjunction with Supertex depletion mode MOSFET DN2540N5, an output current of up to 150mA is achieved.

Block Diagram



Ordering Information

Device	Package Option			
	TO-92	TO-243AA	TO-220	8-Lead SOIC
LR645	LR645N3	LR645N8	LR645N5	LR645LG
	LR645N3-G	LR645N8-G	LR645N5-G	LR645LG-G

-G indicates package is RoHS compliant ('Green')

Thermal Characteristics

Package	Power Dissipation @T_A = 25°C	θ_{JC} °C/W	θ_{JA} °C/W
SOIC	0.31W	156	400*
TO-92	0.74W	125	170
TO-220	1.8W	8.3	70
TO-243AA	1.6W	15	78*

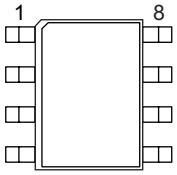
** Mounted on FR4 board; 25mm x 25mm x 1.57mm*
Significant PD increase possible on ceramic substrate

Absolute Maximum Ratings

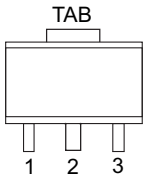
Parameter	Value
Input voltage	450V
Output voltage	15.5V
Operating and storage temperature	-55°C to +150°C
Soldering temperature	300°C

Absolute Maximum Ratings are those values beyond which damage to the device may occur. Functional operation under these conditions is not implied. Continuous operation of the device at the absolute rating level may affect device reliability. All voltages are referenced to device ground.

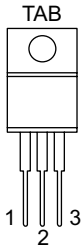
Pin Configurations



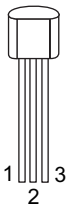
8-Lead SOIC



TO-243AA (SOT-89)



TO-220



TO-92

	$+V_{IN}$	GND	V_{OUT}	TRIM	GATE
TO-92	1	2	3	-	-
TO-243AA	1	2, TAB	3	-	-
TO-220	1	2, TAB	3	-	-
8-Lead SO	1	3	4	5	7

Package Markings



YY = Year Sealed
WW = Week Sealed
L = Lot Number
_____ = "Green" Packaging

8-Lead SOIC



✳ = 2-week alpha date code

TO-243AA

Electrical Characteristics

(Test conditions unless otherwise specified: T_A = 25°C; V_{IN} = 15 to 450V, C_{OUT} = 0.01µF)

Symbol	Parameter	Min	Typ	Max	Units	Conditions
V_{OUT}	Output voltage	9.3	10	10.7	V	No load
	Output voltage over temperature[1]	9.0	10	11.5	V	T_J = - 40°C ≤ to + 125°C, No load
ΔV_{OUT}	Line regulation	-	40	200	mV	V_{IN} = 15V to 400V, No load
	Load regulation	-	150	400	mV	V_{IN} = 50V, I_{OUT} = 0 to 3.0mA
V_{IN}	Operating input voltage range	15	-	450	V	---
I_{INQ}	Input quiescent current	-	50	150	µA	No Load
I_{OFF}	V_{IN} off-state leakage current	-	0.1	10	µA	$V_{AUX} \geq V_{OUT}$ +1V applied to V_{OUT} pin

Symbol	Parameter	Min	Typ	Max	Units	Conditions
I_{AUX}	Input current to V_{OUT}	-	-	200	µA	$V_{AUX} \geq V_{OUT}$ +1V applied to V_{OUT} pin
$\Delta V_{OUT}/\Delta V_{IN}$	Ripple rejection ratio[1]	50	60	-	dB	120Hz, No Load
e_n	Noise voltage[1]	-	25	-	µV	0.01 to 100KHz
I_{PEAK}	Output peak current[2]	-	30	-	mA	C_{OUT} = 10µF, V_{IN} = 400V
V_{AUX}	External voltage applied to V_{OUT}	-	-	13.2	V	---

8-lead, adjustable output voltage version only:

Test conditions unless otherwise specified: T_A = 25°C; V_{IN} = 15 to 450V, C_{OUT} = 0.01µF

V_{OUT}	Output regulation trim range[1]	8	-	12	V	No load
ΔV_{OUT}	Load regulation at 8V trim[1]	-	200	400	mV	V_{IN} = 15V, I_{OUT} = 0 to 1.0mA
	Load regulation at 12V trim[1]	-	100	400	mV	V_{IN} = 50V, I_{OUT} = 0 to 3.0mA

Notes:

1. Guaranteed by design, not tested in production.

2. Pulse test duration < 1.0msec, Duty cycle < 2%

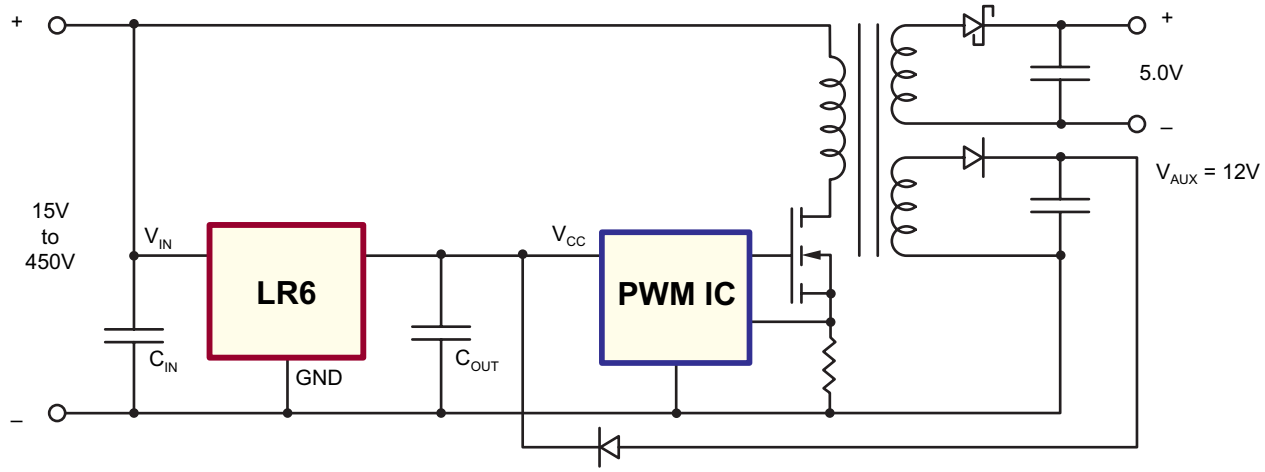
LR645: SMPS Start-Up Circuit

One of the main applications for the LR645 is a start-up circuit for off-line switch-mode power supplies (SMPS), as shown in Figure1. A minimum output capacitance of 0.01µF is recommended for stability. The wide operating input voltage range of the LR645 allows the SMPS to operate and start-up from rectified AC or a DC voltage of 15V to 450V without adjustment.

During start-up, the LR645 powers the V_{CC} line of the PWM IC with a nominal output voltage of 10V. The auxiliary voltage connected through a diode to the V_{OUT} pin of the LR645 will start to increase. When the auxiliary voltage becomes larger than the output voltage the LR645 turns OFF its internal high voltage input line and output voltage, allowing the auxiliary voltage to power the V_{CC} line of the PWM IC. The input current drawn by the LR645 from the high voltage line after start-up will therefore only be leakage current of the internal MOSFET switch, which is typically 0.1µA.

The 3-terminal version shown in Figure 1 has load regulation guaranteed from 0 to 3.0mA at a fixed nominal output voltage of 10V. Applications requiring higher output current and/or a different output voltage can use the 8 pin adjustable version.

Figure 1: SMPS Start-Up Circuit

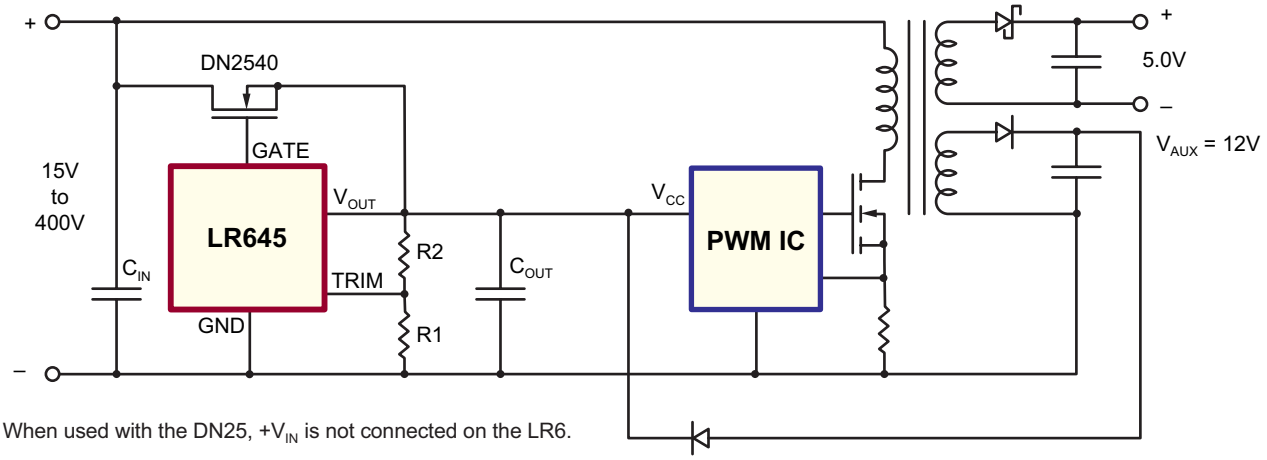


LR645: High Current SMPS Start-Up Circuit

The 8 lead version of the LR645 has connections for an external depletion-mode MOSFET for higher output current and external resistors for adjustable output voltage. As shown in Figure 2, the output current is increased to 150mA by using the Supertex 400V depletion-mode MOSFET DN2540. The maximum operating input voltage will be limited by the drain-to-source breakdown voltage of the external MOSFET, but cannot exceed the 450V rating of the LR645.

The output voltage can be adjusted from 8V to 12V with 2external resistors, R1 and R2. The ratio of R2/R1 determines the output voltage. R2 is connected between the V_{OUT} and TRIM pins. R1 is connected between TRIM and GND pins. Figure 5 is a curve showing output voltage versus resistor ratio R2/R1. The optimum range for R1 + R2 is 200KΩ to 300KΩ. This minimizes loading and optimizes accuracy of the output voltage. Figure 5 uses an R1 + R2 of 250KΩ.

Figure 2: High Current SMPS Start-Up Circuit



Note: When used with the DN25, $+V_{IN}$ is not connected on the LR6.

LR645: Off Line Linear Regulator

Circuits requiring low voltages to operate logic and analog circuits benefit from the LR645. The conventional use of step down transformers can be eliminated, thereby saving space and cost. Some examples of these applications are: proximity controlled light switches, street lamp controls, and low voltage power supplies for appliances such as washing machines, dishwashers, and refrigerators.

The wide operating input voltage range of 15V to 450V as well as the ripple rejection ratio of 50dB minimum allows the use of a small, high voltage input capacitor. The input AC line can be either full-wave or half-wave rectified. A minimum output capacitance of 0.01µF is recommended for output stability.

Figure 3: Cascading for Precision

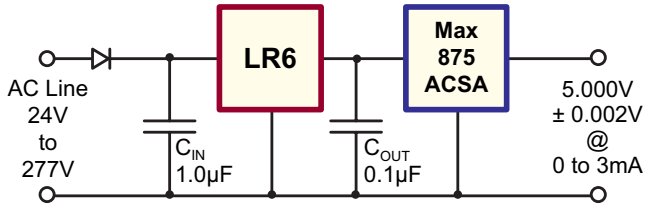


Figure 3 shows the LR645 as a pre-regulator to a precision-regulator for high precision regulation. Higher output current is also possible by using an external depletion-mode MOSFET DN2540N5 as shown in Figure 4.

Power Dissipation Considerations

The LR645 is a true linear regulator. Its power dissipation istherefore a function of input voltage and output load current. Forexample, if the LR645 is providing a continuous load current of 3mAat 10V while its input voltage is 400V, total dissipation in the LR645 will be:

$$P_{DISS} = (V_{IN} - V_{OUT}) \times (I_{OUT} + I_{MAX\ QUIESCENT})$$
$$= (400V - 10V) \times (3.0mA + 150\mu A)$$
$$= 1.23\ Watts$$

The 1.23 watts is for continuous operation. This is within the dissipation capabilities of the TO-220 and SOT-89 packages. See the thermal characteristics chart on page 2 for deratings. For SMPS start-up applications, the output current is usually required only during start-up. This duration depends upon the auxiliary supply output capacitor and C_{OUT}, but is typically a few hundred milliseconds. All package types of the LR645 have been characterized for use with a C_{OUT} of at least 10µF, and an AC line of 277V.

Figure 4: High Current Regulation

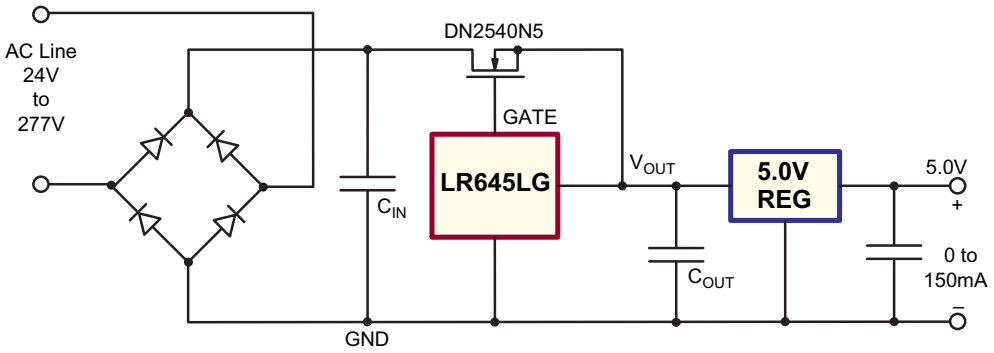
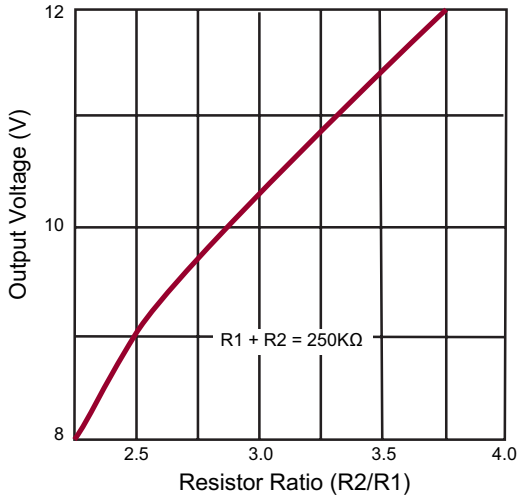
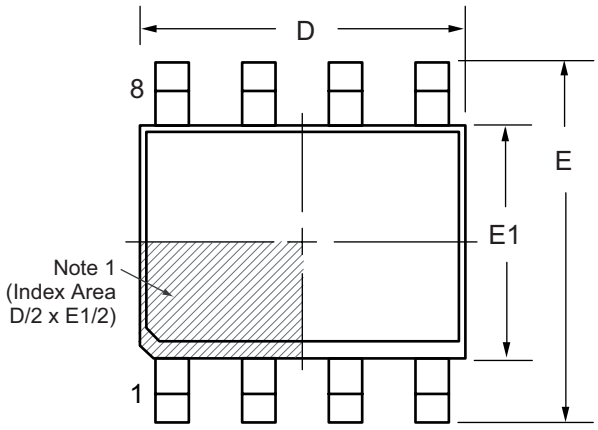


Figure 5: Typical Output Voltage vs Resistor Ratio

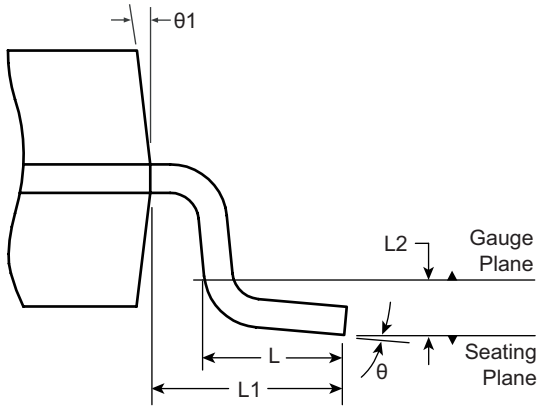


8-Lead SOIC (Narrow Body) Package Outline (LG/TG)

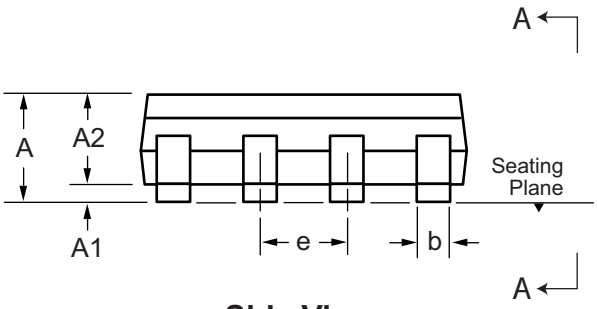
4.9x3.9mm body, 1.75mm height (max), 1.27mm pitch



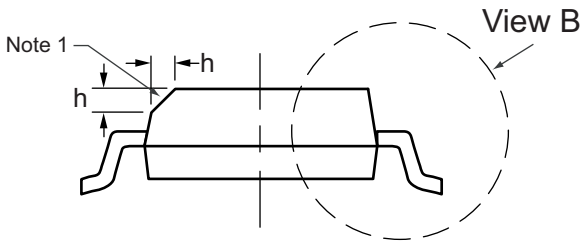
Top View



View B



Side View



View A-A

Note 1:

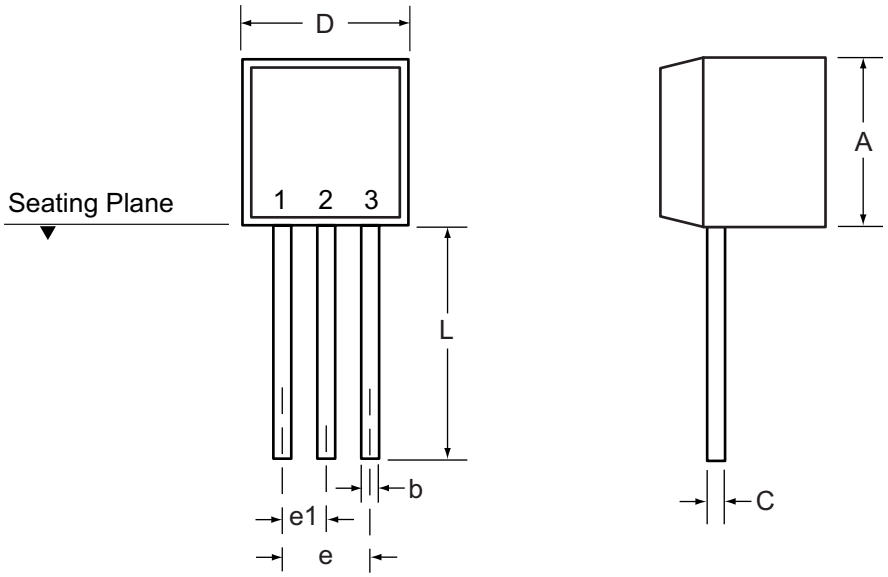
This chamfer feature is optional. If it is not present, then a Pin 1 identifier must be located in the index area indicated.The Pin 1 identifier may be either a mold, or an embedded metal or marked feature.

Symbol		A	A1	A2	b	D	E	E1	e	h	L	L1	L2	θ	θ1
Dimension (mm)	MIN	1.35	0.10	1.25	0.31	4.80	5.80	3.80	1.27 BSC	0.25	0.40	1.04 REF	0.25 BSC	0°	5°
	NOM	-	-	-	-	4.90	6.00	3.90		-	-			-	-
	MAX	1.75	0.25	1.50	0.51	5.00	6.20	4.00		0.50	1.27			8°	15°

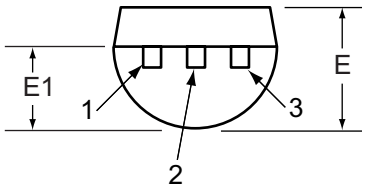
JEDEC Registration MS-012, Variation AA, Issue E, Sept. 2005.

Drawings not to scale.

3-Lead TO-92 Package Outline (N3)



Front View **Side View**

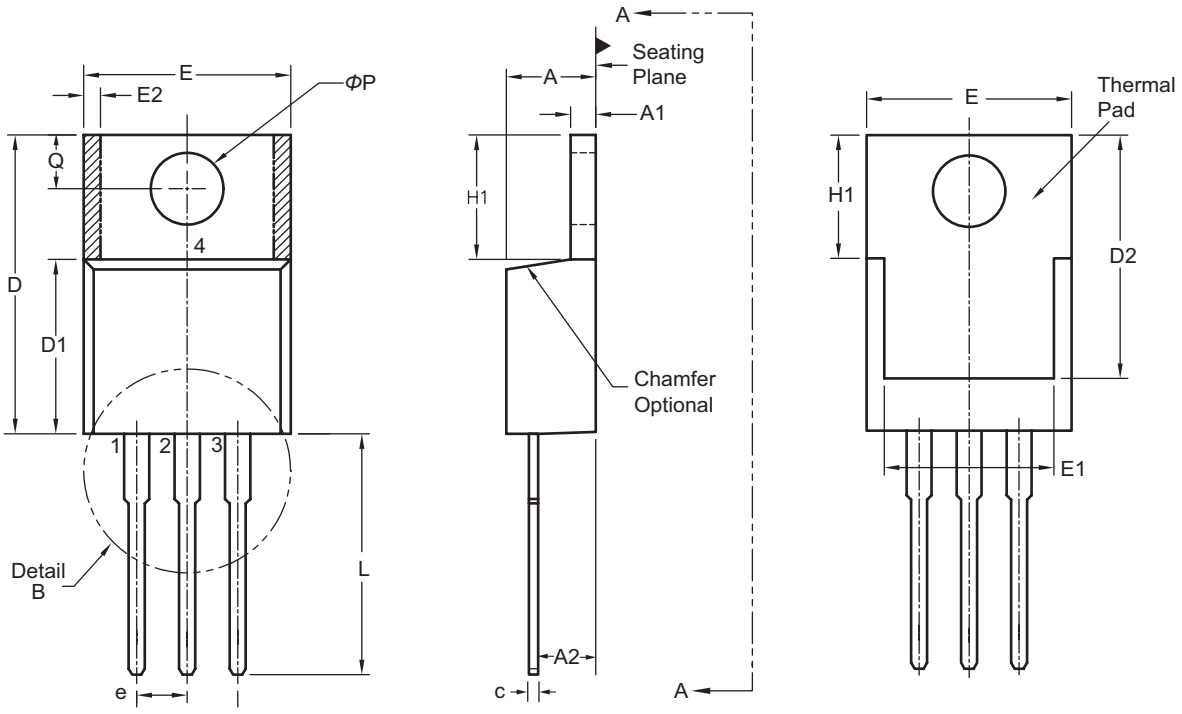


Bottom View

Symbol		A	b	C	D	E	E1	e	e1	L
Dimension (inches)	MIN	.170	.014	.014	.175	.125	.800	.095	.045	.500
	NOM	-	-	-	-	-	-	-	-	-
	MAX	.210	.022	.022	.205	.165	.105	.105	.055	-

Drawings not to scale.

3-Lead TO-220 (Power Package) Package Outline (N5)



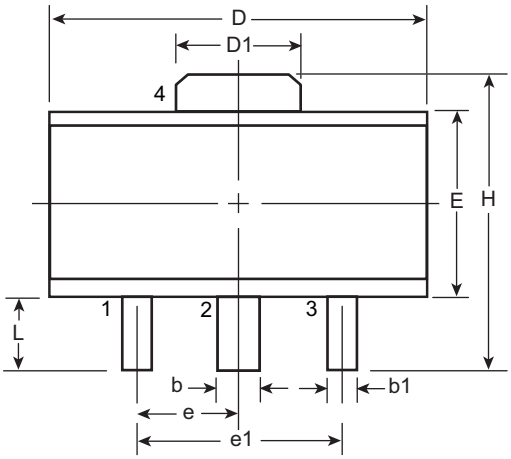
Front View **Side View** **View A - A**

Detail B

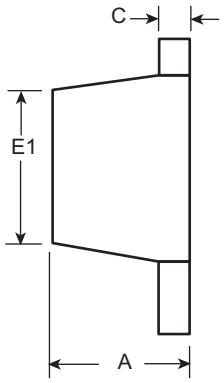
Symbol		A	A1	A2	b	b2	c	D	D1	D2	E	E1	E2	e	H1	L	L1	Q	ΦP
Dimension (inches)	MIN	.140	.020	.080	.015	.045	.014	.560	.330	.480	.380	.270	-	.100 BSC	.230	.500	-	.100	.139
	NOM	-	-	-	.027	.057	-	-	-	-	-	-	-		-	-	-	-	-
	MAX	.190	.055	.115	.040	.070	.024	.650	.355	.507	.420	.350	.030		.270	.580	.250	.135	.161

JEDEC Registration TO-220, Variation AB, Issue K, April 2002.
Drawings not to scale.

3-Lead TO-243AA (SOT-89) Package Outline (N8)



Top View



Side View

Symbol		A	b	b1	C	D	D1	E	E1	e	e1	H	L
Dimensions (mm)	MIN	1.40	0.44	0.36	0.35	4.40	1.62	2.29	2.13	1.50 BSC	3.00 BSC	3.94	0.89
	NOM	-	-	-	-	-	-	-	-			-	-
	MAX	1.60	0.56	0.48	0.44	4.60	1.83	2.60	2.29			4.25	1.20

JEDEC Registration TO-243, Variation AA, Issue C, July 1986.
***Drawings not to scale**.*

(The package drawings in this data sheet may not reflect the most current specifications. For the latest package outline information go to http://www.supertex.com/packaging.html.)

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