LPC2157/2158

Single-chip 16-bit/32-bit microcontrollers; 512 kB flash, with 32 segment x 4 LCD driver

Rev. 02 — 9 February 2009 Product data sheet

1. General description

The LPC2157/2158 is a multi-chip module consisting of a LPC2138/2148 single-chip microcontroller combined with a PCF8576D Universal LCD driver in a low-cost 100-pin package. The LCD driver provides 32 segments and supports from 1 to 4 backplanes. Display overhead is minimized by an on-chip display RAM with auto-increment addressing. Refer to the respective LPC2148 and LPC2138 user manual for details.

2. Features

- 128-bit wide interface/accelerator enables high-speed 60 MHz operation.
  - 32 kB to 40 kB of on-chip static RAM and 512 kB of on-chip flash memory.
- USB 2.0 Full-speed compliant device controller with 2 kB of endpoint RAM.
  - An additional 8 kB of on-chip RAM accessible to USB by DMA (LPC2158 only).
- 32 segment × 4 backplane LCD controller supports from 1 to 4 backplanes.
- Single 10-bit DAC provides variable analog output.
- Low power Real-Time Clock (RTC) with independent power and 32 kHz clock input.
- Multiple serial interfaces including two UARTs (16C550), two Fast I^2C-bus (400 kbit/s), SPI and SSP with buffering and variable data length capabilities.
- Single power supply chip with POR and BOD circuits:
  - CPU operating voltage range of 3.0 V to 3.6 V (3.3 V ± 10 %) with 5 V tolerant I/O pads.
- 100-pin LQFP package with 38 microcontroller I/O pins minimum.
- Individual enable/disable of peripheral functions as well as peripheral clock scaling for additional power optimization.

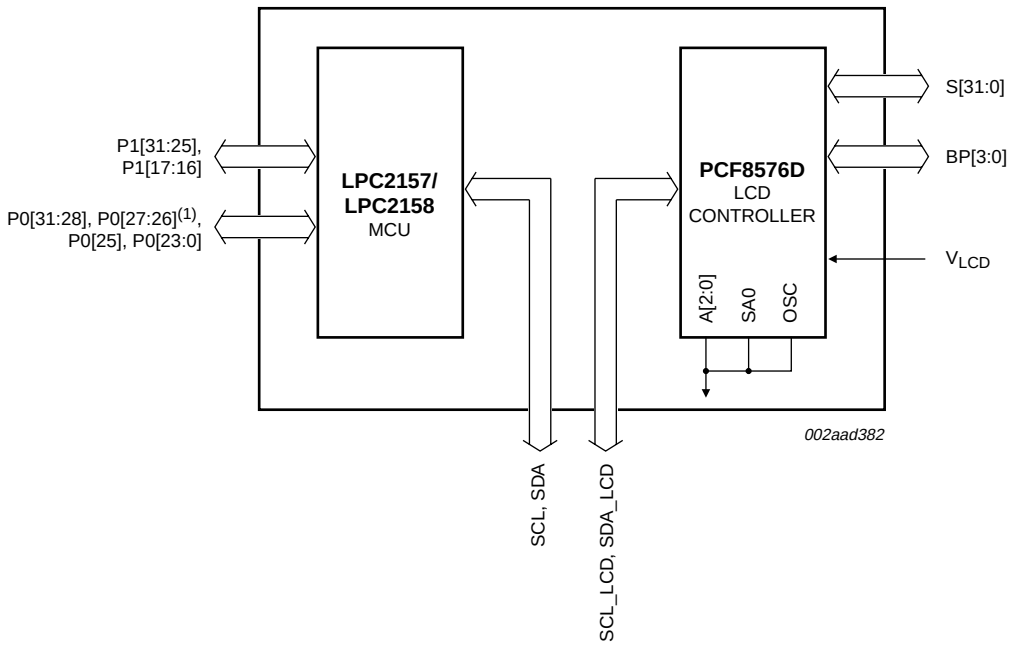
3. Ordering information

Table 1. Ordering information

Type number	Package		
	Name	Description	Version
LPC2157FBD100	LQFP100	plastic low profile quad flat package; 100 leads; body 14 × 14 × 1.4 mm	SOT407-1
LPC2158FBD100	LQFP100	plastic low profile quad flat package; 100 leads; body 14 × 14 × 1.4 mm	SOT407-1

founded by Philips

4. Block diagram



(1) LPC2157 only.

Fig 1. Block diagram of LPC2157/2158

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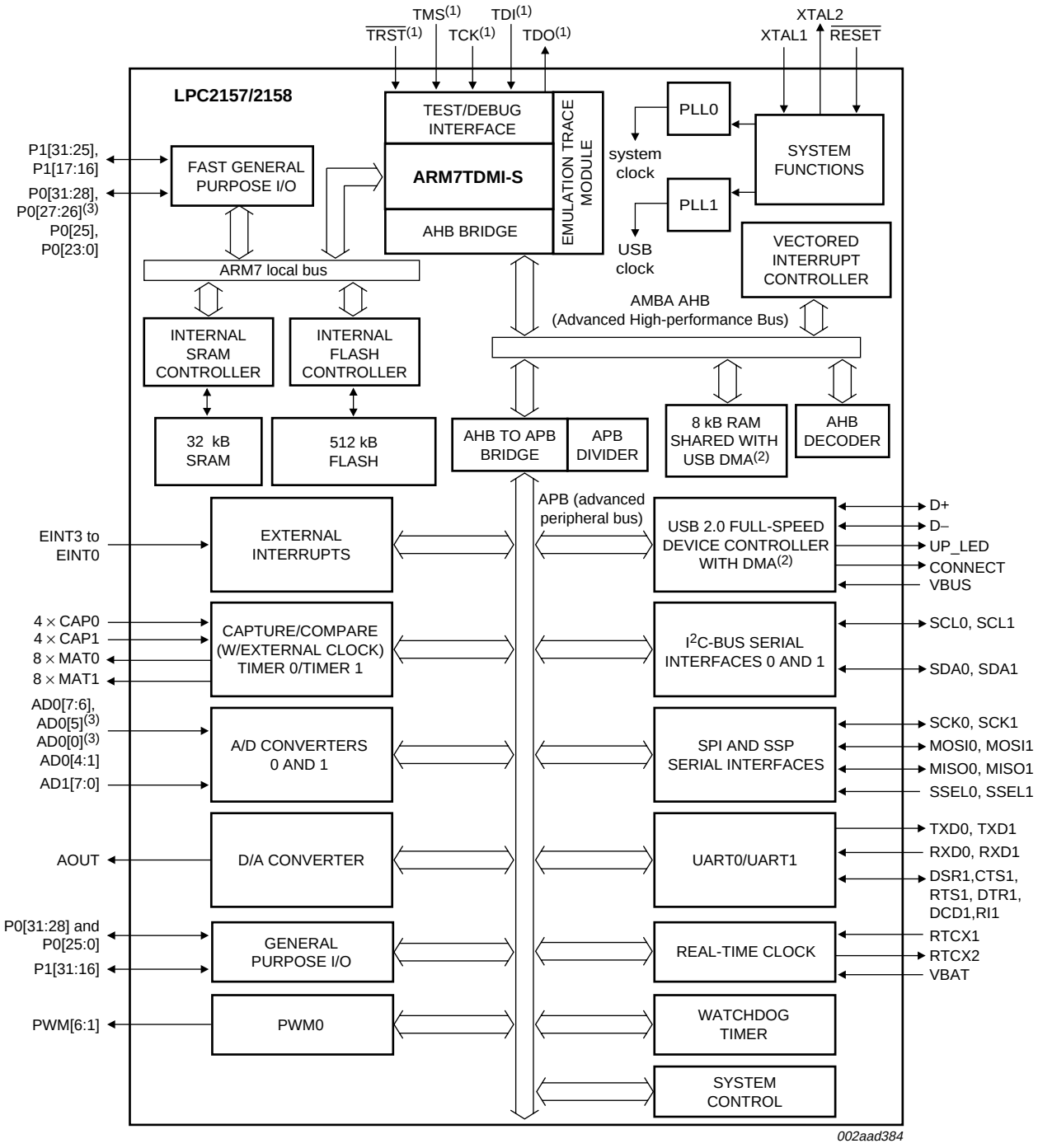

(1) Pins shared with GPIO.

(2) USB DMA controller with 8 kB of RAM accessible as general purpose RAM and/or DMA is available in LPC2158 only.

(3) LPC2157 only.

Fig 2. Microcontroller section block diagram

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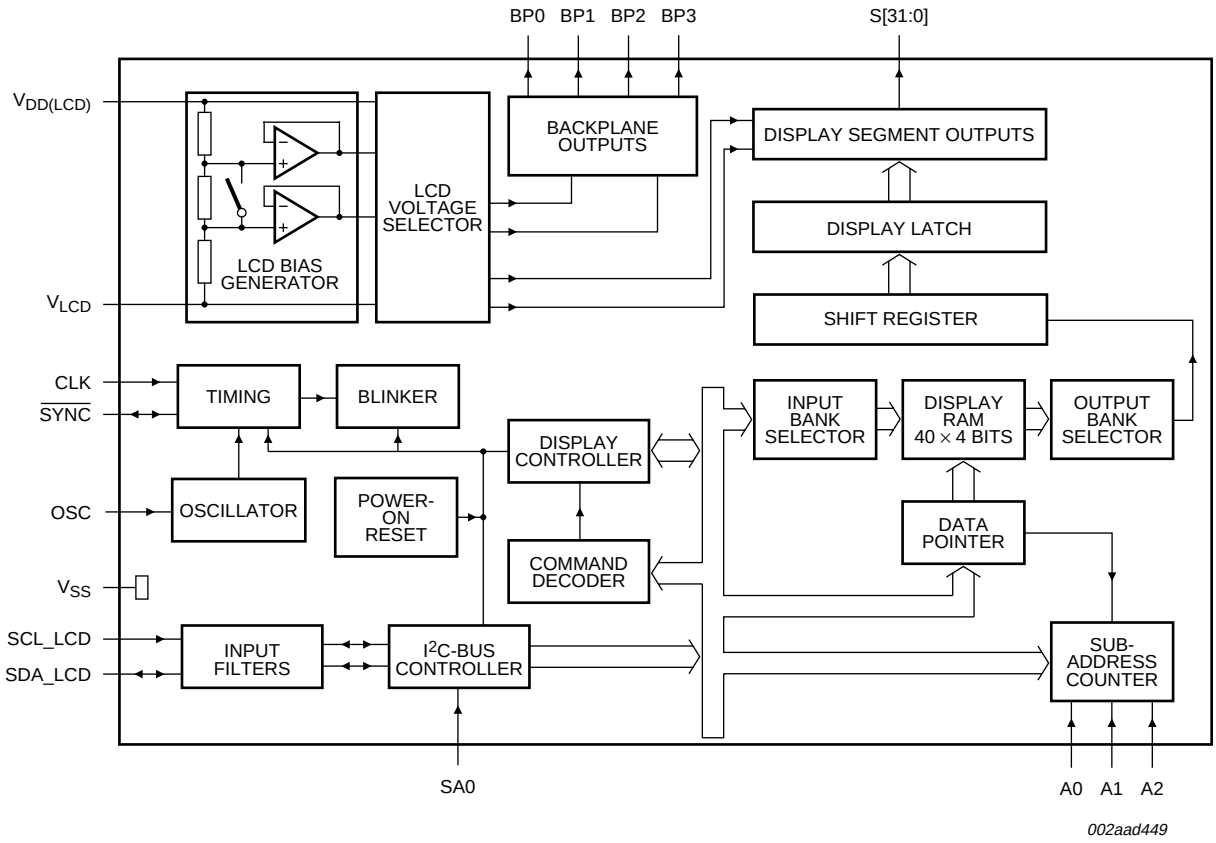

Fig 3. LCD display controller block diagram

5. Pinning information

5.1 Pinning

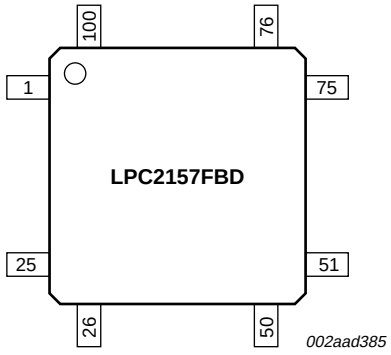

Fig 4. Pin configuration for LPC2157

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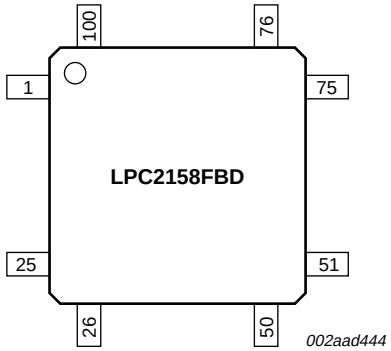

Fig 5. Pin configuration for LPC2158

5.2 Pin description

Table 2. Pin description LPC2157

Symbol	Pin	Type	Description
P0[0] to P0[31]		I/O	**Port 0:** Port 0 is a 32-bit I/O port with individual direction controls for each bit. Total of 31 pins of the Port 0 can be used as a general purpose bidirectional digital I/Os while P0[31] is output only pin. The operation of port 0 pins depends upon the pin function selected via the pin connect block. Pin P0[24] is not available.
P0[0]/TXD0/ PWM1	7[1]	I/O	**P0[0] —** General purpose input/output digital pin (GPIO).
		O	**TXD0 —** Transmitter output for UART0.
		O	**PWM1 —** Pulse Width Modulator output 1.
P0[1]/RXD0/ PWM3/EINT0	9[2]	I/O	**P0[1] —** General purpose input/output digital pin (GPIO).
		I	**RXD0 —** Receiver input for UART0.
		O	**PWM3 —** Pulse Width Modulator output 3.
		I	**EINT0 —** External interrupt 0 input.
P0[2]/SCL0/ CAP0[0]	10[3]	I/O	**P0[2] —** General purpose input/output digital pin (GPIO).
		I/O	**SCL0 —** I^2C0 clock input/output. Open-drain output (for I^2C-bus compliance).
		I	**CAP0[0] —** Capture input for Timer 0, channel 0.
P0[3]/SDA0/ MAT0[0]/EINT1	14[3]	I/O	**P0[3] —** General purpose input/output digital pin (GPIO).
		I/O	**SDA0 —** I^2C0 data input/output. Open-drain output (for I^2C-bus compliance).
		O	**MAT0[0] —** Match output for Timer 0, channel 0.
		I	**EINT1 —** External interrupt 1 input.
P0[4]/SCK0/ CAP0[1]/AD0[6]	15[4]	I/O	**P0[4] —** General purpose input/output digital pin (GPIO).
		I/O	**SCK0 —** Serial clock for SPI0. SPI clock output from master or input to slave.
		I	**CAP0[1] —** Capture input for Timer 0, channel 1.
		I	**AD0[6] —** ADC 0, input 6.
P0[5]/MISO0/ MAT0[1]/AD0[7]	17[4]	I/O	**P0[5] —** General purpose input/output digital pin (GPIO).
		I/O	**MISO0 —** Master In Slave Out for SPI0. Data input to SPI master or data output from SPI slave.
		O	**MAT0[1] —** Match output for Timer 0, channel 1.
		I	**AD0[7] —** ADC 0, input 7.

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Table 2. Pin description LPC2157 *…continued*

Symbol	Pin	Type	Description
P0[6]/MOSI0/ CAP0[2]/AD1[0]	18[4]	I/O	**P0[6] —** General purpose input/output digital pin (GPIO).
		I/O	**MOSI0 —** Master Out Slave In for SPI0. Data output from SPI master or data input to SPI slave.
		I	**CAP0[2] —** Capture input for Timer 0, channel 2.
		I	**AD1[0] —** ADC 1, input 0.
P0[7]/SSEL0/ PWM2/EINT2	19[2]	I/O	**P0[7] —** General purpose input/output digital pin (GPIO).
		I	**SSEL0 —** Slave Select for SPI0. Selects the SPI interface as a slave.
		O	**PWM2 —** Pulse Width Modulator output 2.
		I	**EINT2 —** External interrupt 2 input.
P0[8]/TXD1/ PWM4/AD1[1]	20[4]	I/O	**P0[8] —** General purpose input/output digital pin (GPIO).
		O	**TXD1 —** Transmitter output for UART1.
		O	**PWM4 —** Pulse Width Modulator output 4.
		I	**AD1[1] —** ADC 1, input 1.
P0[9]/RXD1/ PWM6/EINT3	21[2]	I/O	**P0[9] —** General purpose input/output digital pin (GPIO).
		I	**RXD1 —** Receiver input for UART1.
		O	**PWM6 —** Pulse Width Modulator output 6.
		I	**EINT3 —** External interrupt 3 input.
P0[10]/RTS1/ CAP1[0]/AD1[2]	22[4]	I/O	**P0[10] —** General purpose input/output digital pin (GPIO).
		O	**RTS1 —** Request to Send output for UART1.
		I	**CAP1[0] —** Capture input for Timer 1, channel 0.
		I	**AD1[2] —** ADC 1, input 2.
P0[11]/CTS1/ CAP1[1]/SCL1	23[3]	I/O	**P0[11] —** General purpose input/output digital pin (GPIO).
		I	**CTS1 —** Clear to Send input for UART1.
		I	**CAP1[1] —** Capture input for Timer 1, channel 1.
		I/O	**SCL1 —** I^2C1 clock input/output. Open-drain output (for I^2C-bus compliance)
P0[12]/DSR1/ MAT1[0]/AD1[3]	24[4]	I/O	**P0[12] —** General purpose input/output digital pin (GPIO).
		I	**DSR1 —** Data Set Ready input for UART1.
		O	**MAT1[0] —** Match output for Timer 1, channel 0.
		I	**AD1[3] —** ADC 1 input 3.
P0[13]/DTR1/ MAT1[1]/AD1[4]	25[4]	I/O	**P0[13] —** General purpose input/output digital pin (GPIO).
		O	**DTR1 —** Data Terminal Ready output for UART1.
		O	**MAT1[1] —** Match output for Timer 1, channel 1.
		I	**AD1[4] —** ADC 1 input 4.
P0[14]/DCD1/ EINT1/SDA1	26[3]	I/O	**P0[14] —** General purpose input/output digital pin (GPIO).
		I	**DCD1 —** Data Carrier Detect input for UART1.
		I	**EINT1 —** External interrupt 1 input.
		I/O	**SDA1 —** I^2C1 data input/output. Open-drain output (for I^2C-bus compliance). **Note:** LOW on this pin while $\overline{\text{RESET}}$ is LOW forces on-chip bootloader to take over control of the part after reset.

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Table 2. Pin description LPC2157 *…continued*

Symbol	Pin	Type	Description
P0[15]/RI1/ EINT2/AD1[5]	28[4]	I/O	**P0[15] —** General purpose input/output digital pin (GPIO).
		I	**RI1 —** Ring Indicator input for UART1.
		I	**EINT2 —** External interrupt 2 input.
		I	**AD1[5] —** ADC 1, input 5.
P0[16]/EINT0/ MAT0[2]/CAP0[2]	29[2]	I/O	**P0[16] —** General purpose input/output digital pin (GPIO).
		I	**EINT0 —** External interrupt 0 input.
		O	**MAT0[2] —** Match output for Timer 0, channel 2.
		I	**CAP0[2] —** Capture input for Timer 0, channel 2.
P0[17]/CAP1[2]/ SCK1/MAT1[2]	30[1]	I/O	**P0[17] —** General purpose input/output digital pin (GPIO).
		I	**CAP1[2] —** Capture input for Timer 1, channel 2.
		I/O	**SCK1 —** Serial Clock for SSP. Clock output from master or input to slave.
		O	**MAT1[2] —** Match output for Timer 1, channel 2.
P0[18]/CAP1[3]/ MISO1/MAT1[3]	79[1]	I/O	**P0[18] —** General purpose input/output digital pin (GPIO).
		I	**CAP1[3] —** Capture input for Timer 1, channel 3.
		I/O	**MISO1 —** Master In Slave Out for SSP. Data input to SPI master or data output from SSP slave.
		O	**MAT1[3] —** Match output for Timer 1, channel 3.
P0[19]/MAT1[2]/ MOSI1/CAP1[2]	80[1]	I/O	**P0[19] —** General purpose input/output digital pin (GPIO).
		O	**MAT1[2] —** Match output for Timer 1, channel 2.
		I/O	**MOSI1 —** Master Out Slave In for SSP. Data output from SSP master or data input to SSP slave.
		I	**CAP1[2] —** Capture input for Timer 1, channel 2.
P0[20]/MAT1[3]/ SSEL1/EINT3	81[2]	I/O	**P0[20] —** General purpose input/output digital pin (GPIO).
		O	**MAT1[3] —** Match output for Timer 1, channel 3.
		I	**SSEL1 —** Slave Select for SSP. Selects the SSP interface as a slave.
		I	**EINT3 —** External interrupt 3 input.
P0[21]/PWM5/ AD1[6]/CAP1[3]	91[4]	I/O	**P0[21] —** General purpose input/output digital pin (GPIO).
		O	**PWM5 —** Pulse Width Modulator output 5.
		I	**AD1[6] —** ADC 1, input 6.
		I	**CAP1[3] —** Capture input for Timer 1, channel 3.
P0[22]/AD1[7]/ CAP0[0]/ MAT0[0]	92[4]	I/O	**P0[22] —** General purpose input/output digital pin (GPIO).
		I	**AD1[7] —** ADC 1, input 7.
		I	**CAP0[0] —** Capture input for Timer 0, channel 0.
		O	**MAT0[0] —** Match output for Timer 0, channel 0.
P0[23]	84[1]	I/O	**P0[23] —** General purpose input/output digital pin (GPIO).
P0[25]/AD0[4]/ AOUT	97[5]	I/O	**P0[25] —** General purpose input/output digital pin (GPIO).
		I	**AD0[4] —** ADC 0, input 4.
		O	**AOUT —** DAC output.
P0[26]/AD0[5]	98[7]	I/O	**P0[26] —** General purpose input/output digital pin (GPIO).
		I	**AD0[5] —** ADC 0, input 5. This analog input is always connected to its pin.

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Table 2. Pin description LPC2157 *…continued*

Symbol	Pin	Type	Description
P0[27]/AD0[0]/ CAP0[1]/MAT0[1]	99[7]	I/O	**P0[27] —** General purpose input/output digital pin (GPIO).
		I	**AD0[0] —** ADC 0, input 0. This analog input is always connected to its pin.
		I	**CAP0[1] —** Capture input for Timer 0, channel 1.
		O	**MAT0[1] —** Match output for Timer 0, channel 1.
P0[28]/AD0[1]/ CAP0[2]/MAT0[2]	1[4]	I/O	**P0[28] —** General purpose input/output digital pin (GPIO).
		I	**AD0[1] —** ADC 0, input 1.
		I	**CAP0[2] —** Capture input for Timer 0, channel 2.
		O	**MAT0[2] —** Match output for Timer 0, channel 2.
P0[29]/AD0[2]/ CAP0[3]MAT0[3]	2[4]	I/O	**P0[29] —** General purpose input/output digital pin (GPIO).
		I	**AD0[2] —** ADC 0, input 2.
		I	**CAP0[3] —** Capture input for Timer 0, channel 3.
		O	**MAT0[3] —** Match output for Timer 0, channel 3.
P0[30]/AD0[3]/ EINT3/CAP0[0]	3[4]	I/O	**P0[30] —** General purpose input/output digital pin (GPIO).
		I	**AD0[3] —** ADC 0, input 3.
		I	**EINT3 —** External interrupt 3 input.
		I	**CAP0[0] —** Capture input for Timer 0, channel 0.
P0[31]	5[6]	O	**P0[31] —** General purpose output only digital pin.
P1[0] to P1[31]		I/O	**Port 1:** Port 1 is a 32-bit bidirectional I/O port with individual direction controls for each bit. The operation of port 1 pins depends upon the pin function selected via the pin connect block. Pins 0 through 15 and 18 through 24 of port 1 are not available.
P1[16]	4[6]	I/O	**P1[16] —** General purpose input/output digital pin (GPIO).
P1[17]	100[6]	I/O	**P1[17] —** General purpose input/output digital pin (GPIO).
P1[25]/EXTIN0	16[6]	I/O	**P1[25] —** General purpose input/output digital pin (GPIO).
		I	**EXTIN0 —** External Trigger Input. Standard I/O with internal pull-up.
P1[26]/RTCK	12[6]	I/O	**P1[26] —** General purpose input/output digital pin (GPIO).
		I/O	**RTCK —** Returned Test Clock output. Extra signal added to the JTAG port. Assists debugger synchronization when processor frequency varies. Bidirectional pin with internal pull-up. **Note:** LOW on RTCK while $\overline{\text{RESET}}$ is LOW enables pins P1[31:26] to operate as Debug port after reset.
P1[27]/TDO	90[6]	I/O	**P1[27] —** General purpose input/output digital pin (GPIO).
		O	**TDO —** Test Data out for JTAG interface.
P1[28]/TDI	86[6]	I/O	**P1[28] —** General purpose input/output digital pin (GPIO).
		I	**TDI —** Test Data in for JTAG interface.
P1[29]/TCK	82[6]	I/O	**P1[29] —** General purpose input/output digital pin (GPIO).
		I	**TCK —** Test Clock for JTAG interface. This clock must be slower than $\frac{1}{6}$ of the CPU clock (CCLK) for the JTAG interface to operate.
P1[30]/TMS	78[6]	I/O	**P1[30] —** General purpose input/output digital pin (GPIO).
		I	**TMS —** Test Mode Select for JTAG interface.
P1[31]/$\overline{\text{TRST}}$	8[6]	I/O	**P1[31] —** General purpose input/output digital pin (GPIO).
		I	**$\overline{\text{TRST}}$ —** Test Reset for JTAG interface.

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Table 2. Pin description LPC2157 *…continued*

Symbol	Pin	Type	Description
$\overline{\text{RESET}}$	83[8]	I	**External reset input:** A LOW on this pin resets the device, causing I/O ports and peripherals to take on their default states, and processor execution to begin at address 0. TTL with hysteresis, 5 V tolerant.
XTAL1	88[9]	O	Input from the oscillator amplifier.
XTAL2	87[9]	I	Output to the oscillator circuit and internal clock generator circuits.
RTCX1	93[9]	I	Input to the RTC oscillator circuit.
RTCX2	94[9]	O	Output from the RTC oscillator circuit.
V_{SS}	6, 13, 32, 39, 40, 85, 95	I	**Ground:** 0 V reference.
V_{DD}	11, 27, 33	I	**3.3 V power supply:** This is the power supply voltage for the core and I/O ports.
V_{DDA}	96	I	**Analog 3.3 V power supply:** This should be nominally the same voltage as V_{DD} but should be isolated to minimize noise and error. This voltage is only used to power the on-chip ADC(s) and DAC.
$V_{DD(LCD)}$	38	I	**1.8 V to 5.5 V power supply:** Power supply voltage for the PCF8576D.
V_{LCD}	41	I	**LCD power supply:** LCD voltage.
VREF	89	I	**ADC reference voltage:** This should be nominally less than or equal to the V_{DD} voltage but should be isolated to minimize noise and error. Level on this pin is used as a reference for ADC(s) and DAC.
VBAT	31	I	**RTC power supply voltage:** 3.3 V on this pin supplies the power to the RTC.
SDA_LCD	34	I/O	**SDA LCD —** I^2C-bus data signal for the LCD controller.
SCL_LCD	35	I	**SCL LCD —** I^2C-bus clock signal for the LCD controller.
$\overline{\text{SYNC}}$	36	I/O	**$\overline{\text{SYNC}}$ —** cascade synchronization input/output
CLK	37	I/O	**CLK —** external clock input/output
BP0 to BP3	42 to 45	O	**BP0 to BP3:** LCD backplane outputs.
S0 to S31	46 to 77	O	**S0 to S31:** LCD segment outputs.

[1] 5 V tolerant pad providing digital I/O functions with TTL levels and hysteresis and 10 ns slew rate control.

[2] 5 V tolerant pad providing digital I/O functions with TTL levels and hysteresis and 10 ns slew rate control. If configured for an input function, this pad utilizes built-in glitch filter that blocks pulses shorter than 3 ns.

[3] Open-drain 5 V tolerant digital I/O I^2C-bus 400 kHz specification compatible pad. It requires external pull-up to provide an output functionality.

[4] 5 V tolerant pad providing digital I/O (with TTL levels and hysteresis and 10 ns slew rate control) and analog input function. If configured for an input function, this pad utilizes built-in glitch filter that blocks pulses shorter than 3 ns. When configured as an ADC input, digital section of the pad is disabled.

[5] 5 V tolerant pad providing digital I/O (with TTL levels and hysteresis and 10 ns slew rate control) and analog output function. When configured as the DAC output, digital section of the pad is disabled.

[6] 5 V tolerant pad with built-in pull-up resistor providing digital I/O functions with TTL levels and hysteresis and 10 ns slew rate control. The pull-up resistor's value typically ranges from 60 kΩ to 300 kΩ.

[7] Pad is designed in accordance with the Universal Serial Bus (USB) specification, revision 2.0 (Full-speed and Low-speed mode only).

[8] 5 V tolerant pad providing digital input (with TTL levels and hysteresis) function only.

[9] Pad provides special analog functionality.

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Table 3. Pin description LPC2158

Symbol	Pin	Type	Description
P0[0] to P0[31]		I/O	**Port 0:** Port 0 is a 32-bit I/O port with individual direction controls for each bit. Total of 29 pins of the Port 0 can be used as a general purpose bidirectional digital I/Os while P0[31] is output only pin. The operation of port 0 pins depends upon the pin function selected via the pin connect block. Pins P0[24], P0[26] and P0[27] are not available.
P0[0]/TXD0/ PWM1	7[1]	I/O	**P0[0] —** General purpose input/output digital pin (GPIO).
		O	**TXD0 —** Transmitter output for UART0.
		O	**PWM1 —** Pulse Width Modulator output 1.
P0[1]/RXD0/ PWM3/EINT0	9[2]	I/O	**P0[1] —** General purpose input/output digital pin (GPIO).
		I	**RXD0 —** Receiver input for UART0.
		O	**PWM3 —** Pulse Width Modulator output 3.
		I	**EINT0 —** External interrupt 0 input.
P0[2]/SCL0/ CAP0[0]	10[3]	I/O	**P0[2] —** General purpose input/output digital pin (GPIO).
		I/O	**SCL0 —** I^2C0 clock input/output. Open-drain output (for I^2C-bus compliance).
		I	**CAP0[0] —** Capture input for Timer 0, channel 0.
P0[3]/SDA0/ MAT0[0]/EINT1	14[3]	I/O	**P0[3] —** General purpose input/output digital pin (GPIO).
		I/O	**SDA0 —** I^2C0 data input/output. Open-drain output (for I^2C-bus compliance).
		O	**MAT0[0] —** Match output for Timer 0, channel 0.
		I	**EINT1 —** External interrupt 1 input.
P0[4]/SCK0/ CAP0[1]/AD0[6]	15[4]	I/O	**P0[4] —** General purpose input/output digital pin (GPIO).
		I/O	**SCK0 —** Serial clock for SPI0. SPI clock output from master or input to slave.
		I	**CAP0[1] —** Capture input for Timer 0, channel 1.
		I	**AD0[6] —** ADC 0, input 6.
P0[5]/MISO0/ MAT0[1]/AD0[7]	17[4]	I/O	**P0[5] —** General purpose input/output digital pin (GPIO).
		I/O	**MISO0 —** Master In Slave Out for SPI0. Data input to SPI master or data output from SPI slave.
		O	**MAT0[1] —** Match output for Timer 0, channel 1.
		I	**AD0[7] —** ADC 0, input 7.
P0[6]/MOSI0/ CAP0[2]/AD1[0]	18[4]	I/O	**P0[6] —** General purpose input/output digital pin (GPIO).
		I/O	**MOSI0 —** Master Out Slave In for SPI0. Data output from SPI master or data input to SPI slave.
		I	**CAP0[2] —** Capture input for Timer 0, channel 2.
		I	**AD1[0] —** ADC 1, input 0.
P0[7]/SSEL0/ PWM2/EINT2	19[2]	I/O	**P0[7] —** General purpose input/output digital pin (GPIO).
		I	**SSEL0 —** Slave Select for SPI0. Selects the SPI interface as a slave.
		O	**PWM2 —** Pulse Width Modulator output 2.
		I	**EINT2 —** External interrupt 2 input.
P0[8]/TXD1/ PWM4/AD1[1]	20[4]	I/O	**P0[8] —** General purpose input/output digital pin (GPIO).
		O	**TXD1 —** Transmitter output for UART1.
		O	**PWM4 —** Pulse Width Modulator output 4.
		I	**AD1[1] —** ADC 1, input 1.

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Table 3. Pin description LPC2158 *…continued*

Symbol	Pin	Type	Description
P0[9]/RXD1/ PWM6/EINT3	21[2]	I/O	**P0[9] —** General purpose input/output digital pin (GPIO).
		I	**RXD1 —** Receiver input for UART1.
		O	**PWM6 —** Pulse Width Modulator output 6.
		I	**EINT3 —** External interrupt 3 input.
P0[10]/RTS1/ CAP1[0]/AD1[2]	22[4]	I/O	**P0[10] —** General purpose input/output digital pin (GPIO).
		O	**RTS1 —** Request to Send output for UART1.
		I	**CAP1[0] —** Capture input for Timer 1, channel 0.
		I	**AD1[2] —** ADC 1, input 2.
P0[11]/CTS1/ CAP1[1]/SCL1	23[3]	I/O	**P0[11] —** General purpose input/output digital pin (GPIO).
		I	**CTS1 —** Clear to Send input for UART1.
		I	**CAP1[1] —** Capture input for Timer 1, channel 1.
		I/O	**SCL1 —** I^2C1 clock input/output. Open-drain output (for I^2C-bus compliance)
P0[12]/DSR1/ MAT1[0]/AD1[3]	24[4]	I/O	**P0[12] —** General purpose input/output digital pin (GPIO).
		I	**DSR1 —** Data Set Ready input for UART1.
		O	**MAT1[0] —** Match output for Timer 1, channel 0.
		I	**AD1[3] —** ADC 1 input 3.
P0[13]/DTR1/ MAT1[1]/AD1[4]	25[4]	I/O	**P0[13] —** General purpose input/output digital pin (GPIO).
		O	**DTR1 —** Data Terminal Ready output for UART1.
		O	**MAT1[1] —** Match output for Timer 1, channel 1.
		I	**AD1[4] —** ADC 1 input 4.
P0[14]/DCD1/ EINT1/SDA1	26[3]	I/O	**P0[14] —** General purpose input/output digital pin (GPIO).
		I	**DCD1 —** Data Carrier Detect input for UART1.
		I	**EINT1 —** External interrupt 1 input.
		I/O	**SDA1 —** I^2C1 data input/output. Open-drain output (for I^2C-bus compliance). **Note:** LOW on this pin while $\overline{\text{RESET}}$ is LOW forces on-chip bootloader to take over control of the part after reset.
P0[15]/RI1/ EINT2/AD1[5]	28[4]	I/O	**P0[15] —** General purpose input/output digital pin (GPIO).
		I	**RI1 —** Ring Indicator input for UART1.
		I	**EINT2 —** External interrupt 2 input.
		I	**AD1[5] —** ADC 1, input 5.
P0[16]/EINT0/ MAT0[2]/CAP0[2]	29[2]	I/O	**P0[16] —** General purpose input/output digital pin (GPIO).
		I	**EINT0 —** External interrupt 0 input.
		O	**MAT0[2] —** Match output for Timer 0, channel 2.
		I	**CAP0[2] —** Capture input for Timer 0, channel 2.
P0[17]/CAP1[2]/ SCK1/MAT1[2]	30[1]	I/O	**P0[17] —** General purpose input/output digital pin (GPIO).
		I	**CAP1[2] —** Capture input for Timer 1, channel 2.
		I/O	**SCK1 —** Serial Clock for SSP. Clock output from master or input to slave.
		O	**MAT1[2] —** Match output for Timer 1, channel 2.

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Table 3. Pin description LPC2158 *…continued*

Symbol	Pin	Type	Description
P0[18]/CAP1[3]/ MISO1/MAT1[3]	79[1]	I/O	**P0[18] —** General purpose input/output digital pin (GPIO).
		I	**CAP1[3] —** Capture input for Timer 1, channel 3.
		I/O	**MISO1 —** Master In Slave Out for SSP. Data input to SPI master or data output from SSP slave.
		O	**MAT1[3] —** Match output for Timer 1, channel 3.
P0[19]/MAT1[2]/ MOSI1/CAP1[2]	80[1]	I/O	**P0[19] —** General purpose input/output digital pin (GPIO).
		O	**MAT1[2] —** Match output for Timer 1, channel 2.
		I/O	**MOSI1 —** Master Out Slave In for SSP. Data output from SSP master or data input to SSP slave.
		I	**CAP1[2] —** Capture input for Timer 1, channel 2.
P0[20]/MAT1[3]/ SSEL1/EINT3	81[2]	I/O	**P0[20] —** General purpose input/output digital pin (GPIO).
		O	**MAT1[3] —** Match output for Timer 1, channel 3.
		I	**SSEL1 —** Slave Select for SSP. Selects the SSP interface as a slave.
		I	**EINT3 —** External interrupt 3 input.
P0[21]/PWM5/ AD1[6]/CAP1[3]	91[4]	I/O	**P0[21] —** General purpose input/output digital pin (GPIO).
		O	**PWM5 —** Pulse Width Modulator output 5.
		I	**AD1[6] —** ADC 1, input 6.
		I	**CAP1[3] —** Capture input for Timer 1, channel 3.
P0[22]/AD1[7]/ CAP0[0]/ MAT0[0]	92[4]	I/O	**P0[22] —** General purpose input/output digital pin (GPIO).
		I	**AD1[7] —** ADC 1, input 7.
		I	**CAP0[0] —** Capture input for Timer 0, channel 0.
		O	**MAT0[0] —** Match output for Timer 0, channel 0.
P0[23]/V_{BUS}	84[1]	I/O	**P0[23] —** General purpose input/output digital pin (GPIO).
		I	**V_{BUS} —** Indicates the presence of USB bus power. **Note:** This signal must be HIGH for USB reset to occur.
P0[25]/AD0[4]/ AOUT	97[5]	I/O	**P0[25] —** General purpose input/output digital pin (GPIO).
		I	**AD0[4] —** ADC 0, input 4.
		O	**AOUT —** DAC output.
P0[28]/AD0[1]/ CAP0[2]/MAT0[2]	1[4]	I/O	**P0[28] —** General purpose input/output digital pin (GPIO).
		I	**AD0[1] —** ADC 0, input 1.
		I	**CAP0[2] —** Capture input for Timer 0, channel 2.
		O	**MAT0[2] —** Match output for Timer 0, channel 2.
P0[29]/AD0[2]/ CAP0[3]/MAT0[3]	2[4]	I/O	**P0[29] —** General purpose input/output digital pin (GPIO).
		I	**AD0[2] —** ADC 0, input 2.
		I	**CAP0[3] —** Capture input for Timer 0, channel 3.
		O	**MAT0[3] —** Match output for Timer 0, channel 3.
P0[30]/AD0[3]/ EINT3/CAP0[0]	3[4]	I/O	**P0[30] —** General purpose input/output digital pin (GPIO).
		I	**AD0[3] —** ADC 0, input 3.
		I	**EINT3 —** External interrupt 3 input.
		I	**CAP0[0] —** Capture input for Timer 0, channel 0.

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Table 3. Pin description LPC2158 *…continued*

Symbol	Pin	Type	Description
P0[31]/UP_LED/ CONNECT	5[6]	O	**P0[31] —** General purpose output only digital pin.
		O	**UP_LED —** USB GoodLink LED indicator. It is LOW when device is configured (non-control endpoints enabled). It is HIGH when the device is not configured or during global suspend.
		O	**CONNECT —** Signal used to switch an external 1.5 kΩ resistor under the software control. Used with the SoftConnect USB feature. **Important:** This is an digital output only pin. This pin MUST NOT be externally pulled LOW when $\overline{\text{RESET}}$ pin is LOW or the JTAG port will be disabled.
P1[0] to P1[31]		I/O	**Port 1:** Port 1 is a 32-bit bidirectional I/O port with individual direction controls for each bit. The operation of port 1 pins depends upon the pin function selected via the pin connect block. Pins 0 through 15 and 18 through 24 of port 1 are not available.
P1[16]	4[6]	I/O	**P1[16] —** General purpose input/output digital pin (GPIO).
P1[17]	100[6]	I/O	**P1[17] —** General purpose input/output digital pin (GPIO).
P1[25]/EXTIN0	16[6]	I/O	**P1[25] —** General purpose input/output digital pin (GPIO).
		I	**EXTIN0 —** External Trigger Input. Standard I/O with internal pull-up.
P1[26]/RTCK	12[6]	I/O	**P1[26] —** General purpose input/output digital pin (GPIO).
		I/O	**RTCK —** Returned Test Clock output. Extra signal added to the JTAG port. Assists debugger synchronization when processor frequency varies. Bidirectional pin with internal pull-up. **Note:** LOW on RTCK while $\overline{\text{RESET}}$ is LOW enables pins P1[31:26] to operate as Debug port after reset.
P1[27]/TDO	90[6]	I/O	**P1[27] —** General purpose input/output digital pin (GPIO).
		O	**TDO —** Test Data out for JTAG interface.
P1[28]/TDI	86[6]	I/O	**P1[28] —** General purpose input/output digital pin (GPIO).
		I	**TDI —** Test Data in for JTAG interface.
P1[29]/TCK	82[6]	I/O	**P1[29] —** General purpose input/output digital pin (GPIO).
		I	**TCK —** Test Clock for JTAG interface. This clock must be slower than $\frac{1}{6}$ of the CPU clock (CCLK) for the JTAG interface to operate.
P1[30]/TMS	78[6]	I/O	**P1[30] —** General purpose input/output digital pin (GPIO).
		I	**TMS —** Test Mode Select for JTAG interface.
P1[31]/$\overline{\text{TRST}}$	8[6]	I/O	**P1[31] —** General purpose input/output digital pin (GPIO).
		I	**$\overline{\text{TRST}}$ —** Test Reset for JTAG interface.
D+	98[7]	I/O	USB bidirectional D+ line.
D–	99[7]	I/O	USB bidirectional D– line.
$\overline{\text{RESET}}$	83[8]	I	**External reset input:** A LOW on this pin resets the device, causing I/O ports and peripherals to take on their default states, and processor execution to begin at address 0. TTL with hysteresis, 5 V tolerant.
XTAL1	88[9]	O	Input from the oscillator amplifier.
XTAL2	87[9]	I	Output to the oscillator circuit and internal clock generator circuits.
RTCX1	93[9]	I	Input to the RTC oscillator circuit.
RTCX2	94[9]	O	Output from the RTC oscillator circuit.
V_{SS}	6, 13, 32, 39, 40, 85, 95	I	**Ground:** 0 V reference.

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Table 3. Pin description LPC2158 *…continued*

Symbol	Pin	Type	Description
V_{DD}	11, 27, 33	I	**3.3 V power supply:** This is the power supply voltage for the core and I/O ports.
V_{DDA}	96	I	**Analog 3.3 V power supply:** This should be nominally the same voltage as V_{DD} but should be isolated to minimize noise and error. This voltage is only used to power the on-chip ADC(s) and DAC.
$V_{DD(LCD)}$	38	I	**1.8 V to 5.5 V power supply:** Power supply voltage for the PCF8576D.
V_{LCD}	41	I	**LCD power supply:** LCD voltage.
VREF	89	I	**ADC reference voltage:** This should be nominally less than or equal to the V_{DD} voltage but should be isolated to minimize noise and error. Level on this pin is used as a reference for ADC(s) and DAC.
VBAT	31	I	**RTC power supply voltage:** 3.3 V on this pin supplies the power to the RTC.
SDA_LCD	34	I/O	**SDA LCD —** I^2C-bus data signal for the LCD controller.
SCL_LCD	35	I	**SCL LCD —** I^2C-bus clock signal for the LCD controller.
$\overline{SYNC}$	36	I/O	**$\overline{SYNC}$ —** cascade synchronization input/output
CLK	37	I/O	**CLK —** external clock input/output
BP0 to BP3	42 to 45	O	**BP0 to BP3:** LCD backplane outputs.
S0 to S31	46 to 77	O	**S0 to S31:** LCD segment outputs.

[1] 5 V tolerant pad providing digital I/O functions with TTL levels and hysteresis and 10 ns slew rate control.

[2] 5 V tolerant pad providing digital I/O functions with TTL levels and hysteresis and 10 ns slew rate control. If configured for an input function, this pad utilizes built-in glitch filter that blocks pulses shorter than 3 ns.

[3] Open-drain 5 V tolerant digital I/O I^2C-bus 400 kHz specification compatible pad. It requires external pull-up to provide an output functionality.

[4] 5 V tolerant pad providing digital I/O (with TTL levels and hysteresis and 10 ns slew rate control) and analog input function. If configured for an input function, this pad utilizes built-in glitch filter that blocks pulses shorter than 3 ns. When configured as an ADC input, digital section of the pad is disabled.

[5] 5 V tolerant pad providing digital I/O (with TTL levels and hysteresis and 10 ns slew rate control) and analog output function. When configured as the DAC output, digital section of the pad is disabled.

[6] 5 V tolerant pad with built-in pull-up resistor providing digital I/O functions with TTL levels and hysteresis and 10 ns slew rate control. The pull-up resistor's value typically ranges from 60 kΩ to 300 kΩ.

[7] Pad is designed in accordance with the Universal Serial Bus (USB) specification, revision 2.0 (Full-speed and Low-speed mode only).

[8] 5 V tolerant pad providing digital input (with TTL levels and hysteresis) function only.

[9] Pad provides special analog functionality.

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6. Functional description

6.1 Architectural overview

The ARM7TDMI-S is a general purpose 32-bit microprocessor, which offers high performance and very low power consumption. The ARM architecture is based on Reduced Instruction Set Computer (RISC) principles, and the instruction set and related decode mechanism are much simpler than those of microprogrammed Complex Instruction Set Computers (CISC). This simplicity results in a high instruction throughput and impressive real-time interrupt response from a small and cost-effective processor core.

Pipeline techniques are employed so that all parts of the processing and memory systems can operate continuously. Typically, while one instruction is being executed, its successor is being decoded, and a third instruction is being fetched from memory.

The ARM7TDMI-S processor also employs a unique architectural strategy known as Thumb, which makes it ideally suited to high-volume applications with memory restrictions, or applications where code density is an issue.

The key idea behind Thumb is that of a super-reduced instruction set. Essentially, the ARM7TDMI-S processor has two instruction sets:

- The standard 32-bit ARM set.
- A 16-bit Thumb set.

The Thumb set's 16-bit instruction length allows it to approach twice the density of standard ARM code while retaining most of the ARM's performance advantage over a traditional 16-bit processor using 16-bit registers. This is possible because Thumb code operates on the same 32-bit register set as ARM code.

Thumb code is able to provide up to 65 % of the code size of ARM, and 160 % of the performance of an equivalent ARM processor connected to a 16-bit memory system.

6.2 On-chip flash program memory

The LPC2157/2158 incorporate a 512 kB flash memory system. This memory may be used for both code and data storage. Programming of the flash memory may be accomplished in several ways. It may be programmed In System via the serial port. The application program may also erase and/or program the flash while the application is running, allowing a great degree of flexibility for data storage field firmware upgrades, etc. Due to the architectural solution chosen for an on-chip bootloader, flash memory available for user's code on LPC2157/2158 is 500 kB respectively.

The LPC2157/2158 flash memory provides a minimum of 400000 erase/write cycles and 20 years of data-retention.

6.3 On-chip static RAM

On-chip static RAM may be used for code and/or data storage. The SRAM may be accessed as 8-bit, 16-bit, and 32-bit. The LPC2157/2158 provide 32 kB and 40 kB of static RAM.

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In case of LPC2158 only, an 8 kB SRAM block intended to be utilized mainly by the USB can also be used as a general purpose RAM for data storage and code storage and execution.

6.4 Memory map

The LPC2157/2158 memory map incorporates several distinct regions, as shown in Figure 6.

In addition, the CPU interrupt vectors may be remapped to allow them to reside in either flash memory (the default) or on-chip static RAM. This is described in Section 6.19 “System control”.

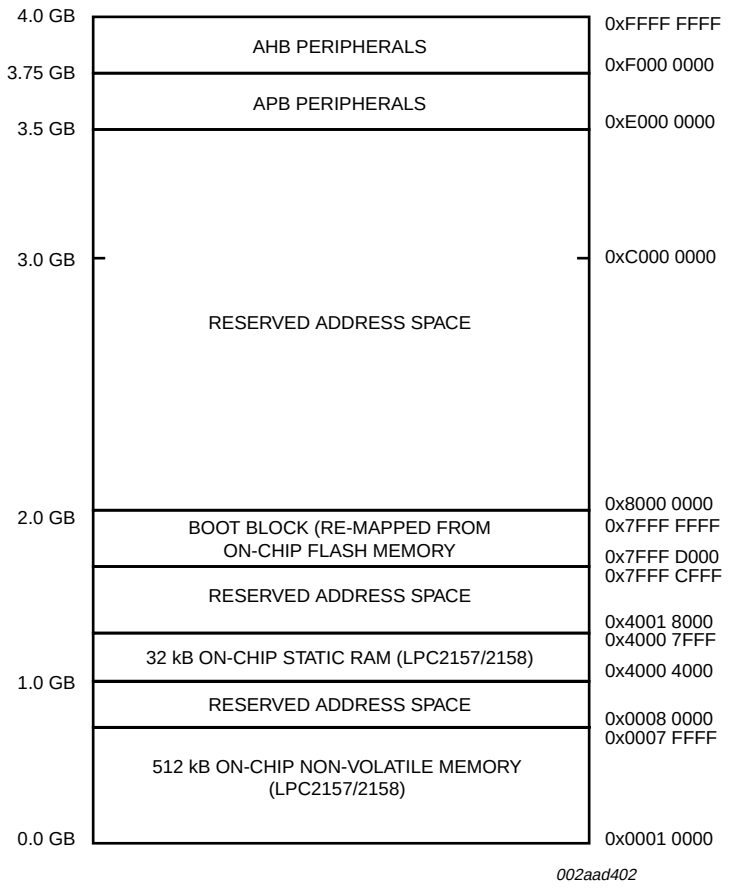

Fig 6. LPC2157/2158 memory map

6.5 Interrupt controller

The Vectored Interrupt Controller (VIC) accepts all of the interrupt request inputs and categorizes them as Fast Interrupt Request (FIQ), vectored Interrupt Request (IRQ), and non-vectored IRQ as defined by programmable settings. The programmable assignment scheme means that priorities of interrupts from the various peripherals can be dynamically assigned and adjusted.

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FIQ has the highest priority. If more than one request is assigned to FIQ, the VIC combines the requests to produce the FIQ signal to the ARM processor. The fastest possible FIQ latency is achieved when only one request is classified as FIQ, because then the FIQ service routine does not need to branch into the interrupt service routine but can run from the interrupt vector location. If more than one request is assigned to the FIQ class, the FIQ service routine will read a word from the VIC that identifies which FIQ source(s) is (are) requesting an interrupt.

Vectored IRQs have the middle priority. Sixteen of the interrupt requests can be assigned to this category. Any of the interrupt requests can be assigned to any of the 16 vectored IRQ slots, among which slot 0 has the highest priority and slot 15 has the lowest.

Non-vectored IRQs have the lowest priority.

The VIC combines the requests from all the vectored and non-vectored IRQs to produce the IRQ signal to the ARM processor. The IRQ service routine can start by reading a register from the VIC and jumping there. If any of the vectored IRQs are pending, the VIC provides the address of the highest-priority requesting IRQs service routine, otherwise it provides the address of a default routine that is shared by all the non-vectored IRQs. The default routine can read another VIC register to see what IRQs are active.

6.5.1 Interrupt sources

Each peripheral device has one interrupt line connected to the Vectored Interrupt Controller, but may have several internal interrupt flags. Individual interrupt flags may also represent more than one interrupt source.

6.6 Pin connect block

The pin connect block allows selected pins of the microcontroller to have more than one function. Configuration registers control the multiplexers to allow connection between the pin and the on chip peripherals. Peripherals should be connected to the appropriate pins prior to being activated, and prior to any related interrupt(s) being enabled. Activity of any enabled peripheral function that is not mapped to a related pin should be considered undefined.

The Pin Control Module with its pin select registers defines the functionality of the microcontroller in a given hardware environment.

After reset all pins of Port 0 and Port 1 are configured as input with the following exceptions: If debug is enabled, the JTAG pins will assume their JTAG functionality. The pins associated with the I^2C0 and I^2C1 interface are open drain.

6.7 Fast general purpose parallel I/O

Device pins that are not connected to a specific peripheral function are controlled by the GPIO registers. Pins may be dynamically configured as inputs or outputs. Separate registers allow setting or clearing any number of outputs simultaneously. The value of the output register may be read back, as well as the current state of the port pins.

LPC2157/2158 introduce accelerated GPIO functions over prior LPC2000 devices:

- GPIO registers are relocated to the ARM local bus for the fastest possible I/O timing.

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- Mask registers allow treating sets of port bits as a group, leaving other bits unchanged.
- All GPIO registers are byte addressable.
- Entire port value can be written in one instruction.

6.7.1 Features

- Bit-level set and clear registers allow a single instruction set or clear of any number of bits in one port.
- Direction control of individual bits.
- Separate control of output set and clear.
- All I/O default to inputs after reset.

6.8 10-bit ADC

The LPC2157/2158 contain two single 10-bit successive approximation ADCs. While ADC0 has eight channels (six channels for LPC2158), ADC1 has eight channels. Therefore, the total number of available ADC inputs for LPC2157 is 16 and for LPC2158 is 14.

6.8.1 Features

- 10-bit successive approximation ADC.
- Measurement range of 0 V to VREF (2.0 V ≤ VREF ≤ V_{DDA}).
- Each converter capable of performing more than 400000 10-bit samples per second.
- Every analog input has a dedicated result register to reduce interrupt overhead.
- Burst conversion mode for single or multiple inputs.
- Optional conversion on transition on input pin or timer match signal.
- Global Start command for both converters.

6.9 10-bit DAC

The DAC enables the LPC2157/2158 to generate a variable analog output. The maximum DAC output voltage is the VREF voltage.

6.9.1 Features

- 10-bit DAC.
- Buffered output.
- Power-down mode available.
- Selectable speed versus power.

6.10 USB 2.0 device controller (LPC2158 only)

The USB is a 4-wire serial bus that supports communication between a host and a number (127 max) of peripherals. The host controller allocates the USB bandwidth to attached devices through a token based protocol. The bus supports hot plugging, unplugging, and dynamic configuration of the devices. All transactions are initiated by the host controller.

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The LPC2158 is equipped with a USB device controller that enables 12 Mbit/s data exchange with a USB host controller. It consists of a register interface, serial interface engine, endpoint buffer memory and DMA controller. The serial interface engine decodes the USB data stream and writes data to the appropriate end point buffer memory. The status of a completed USB transfer or error condition is indicated via status registers. An interrupt is also generated if enabled.

A DMA controller can transfer data between an endpoint buffer and the USB RAM.

6.10.1 Features

- Fully compliant with USB 2.0 Full-speed specification.
- Supports 32 physical (16 logical) endpoints.
- Supports control, bulk, interrupt and isochronous endpoints.
- Scalable realization of endpoints at run time.
- Endpoint maximum packet size selection (up to USB maximum specification) by software at run time.
- RAM message buffer size based on endpoint realization and maximum packet size.
- Supports SoftConnect and GoodLink LED indicator. These two functions are sharing one pin.
- Supports bus-powered capability with low suspend current.
- Supports DMA transfer on all non-control endpoints.
- One duplex DMA channel serves all endpoints.
- Allows dynamic switching between CPU controlled and DMA modes.
- Double buffer implementation for bulk and isochronous endpoints.

6.11 UARTs

The LPC2157/2158 each contain two UARTs. In addition to standard transmit and receive data lines, the UART1 also provides a full modem control handshake interface.

Compared to previous LPC2000 microcontrollers, UARTs in LPC2157/2158 introduce a fractional baud rate generator for both UARTs, enabling these microcontrollers to achieve standard baud rates such as 115200 Bd with any crystal frequency above 2 MHz. In addition, auto-CTS/RTS flow-control functions are fully implemented in hardware.

6.11.1 Features

- 16 B Receive and Transmit FIFOs.
- Register locations conform to 16C550 industry standard.
- Receiver FIFO trigger points at 1 B, 4 B, 8 B and 14 B
- Built-in fractional baud rate generator covering wide range of baud rates without a need for external crystals of particular values.
- Transmission FIFO control enables implementation of software (XON/XOFF) flow control on both UARTs.
- LPC2158 UART1 equipped with standard modem interface signals. This module also provides full support for hardware flow control (auto-CTS/RTS).

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6.12 I²C-bus serial I/O controller

The LPC2157/2158 each contain two I²C-bus controllers.

The I²C-bus is bidirectional, for inter-IC control using only two wires: a serial clock line (SCL), and a serial data line (SDA). Each device is recognized by a unique address and can operate as either a receiver-only device (e.g., an LCD driver or a transmitter with the capability to both receive and send information (such as memory)). Transmitters and/or receivers can operate in either master or slave mode, depending on whether the chip has to initiate a data transfer or is only addressed. The I²C-bus is a multi-master bus, it can be controlled by more than one bus master connected to it.

The I²C-bus implemented in LPC2157/2158 supports bit rates up to 400 kbit/s (Fast I²C-bus).

6.12.1 Features

- Compliant with standard I²C-bus interface.
- Easy to configure as master, slave, or master/slave.
- Programmable clocks allow versatile rate control.
- Bidirectional data transfer between masters and slaves.
- Multi-master bus (no central master).
- Arbitration between simultaneously transmitting masters without corruption of serial data on the bus.
- Serial clock synchronization allows devices with different bit rates to communicate via one serial bus.
- Serial clock synchronization can be used as a handshake mechanism to suspend and resume serial transfer.
- The I²C-bus can be used for test and diagnostic purposes.

6.13 SPI serial I/O controller

The LPC2157/2158 each contain one SPI controller. The SPI is a full duplex serial interface, designed to handle multiple masters and slaves connected to a given bus. Only a single master and a single slave can communicate on the interface during a given data transfer. During a data transfer the master always sends a byte of data to the slave, and the slave always sends a byte of data to the master.

6.13.1 Features

- Compliant with SPI specification.
- Synchronous, Serial, Full Duplex, Communication.
- Combined SPI master and slave.
- Maximum data bit rate of one eighth of the input clock rate.

6.14 SSP serial I/O controller

The LPC2157/2158 each contain one Serial Synchronous Port controller (SSP). The SSP controller is capable of operation on a SPI, 4-wire SSI, or Microwire bus. It can interact with multiple masters and slaves on the bus. However, only a single master and a single

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slave can communicate on the bus during a given data transfer. The SSP supports full duplex transfers, with data frames of 4 bits to 16 bits of data flowing from the master to the slave and from the slave to the master. Often only one of these data flows carries meaningful data.

6.14.1 Features

- Compatible with Motorola's SPI, TI's 4-wire SSI and National Semiconductor's Microwire buses.
- Synchronous serial communication.
- Master or slave operation.
- 8-frame FIFOs for both transmit and receive.
- Four bits to 16 bits per frame.

6.15 General purpose timers/external event counters

The Timer/Counter is designed to count cycles of the peripheral clock (PCLK) or an externally supplied clock and optionally generate interrupts or perform other actions at specified timer values, based on four match registers. It also includes four capture inputs to trap the timer value when an input signal transitions, optionally generating an interrupt. Multiple pins can be selected to perform a single capture or match function, providing an application with 'or' and 'and', as well as 'broadcast' functions among them.

The LPC2157/2158 can count external events on one of the capture inputs if the minimum external pulse is equal or longer than a period of the PCLK. In this configuration, unused capture lines can be selected as regular timer capture inputs, or used as external interrupts.

6.15.1 Features

- A 32-bit timer/counter with a programmable 32-bit prescaler.
- External event counter or timer operation.
- Four 32-bit capture channels per timer/counter that can take a snapshot of the timer value when an input signal transitions. A capture event may also optionally generate an interrupt.
- Four 32-bit match registers that allow:
  - Continuous operation with optional interrupt generation on match.
  - Stop timer on match with optional interrupt generation.
  - Reset timer on match with optional interrupt generation.
- Four external outputs per timer/counter corresponding to match registers, with the following capabilities:
  - Set LOW on match.
  - Set HIGH on match.
  - Toggle on match.
  - Do nothing on match.

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6.16 Watchdog timer

The purpose of the watchdog is to reset the microcontroller within a reasonable amount of time if it enters an erroneous state. When enabled, the watchdog will generate a system reset if the user program fails to 'feed' (or reload) the watchdog within a predetermined amount of time.

6.16.1 Features

- Internally resets chip if not periodically reloaded.
- Debug mode.
- Enabled by software but requires a hardware reset or a watchdog reset/interrupt to be disabled.
- Incorrect/Incomplete feed sequence causes reset/interrupt if enabled.
- Flag to indicate watchdog reset.
- Programmable 32-bit timer with internal prescaler.
- Selectable time period from ($T_{cy(PCLK)} \times 256 \times 4$) to ($T_{cy(PCLK)} \times 2^{32} \times 4$) in multiples of $T_{cy(PCLK)} \times 4$.

6.17 Real-time clock

The RTC is designed to provide a set of counters to measure time when normal or idle operating mode is selected. The RTC has been designed to use little power, making it suitable for battery powered systems where the CPU is not running continuously (Idle mode).

6.17.1 Features

- Measures the passage of time to maintain a calendar and clock.
- Ultra-low power design to support battery powered systems.
- Provides Seconds, Minutes, Hours, Day of Month, Month, Year, Day of Week, and Day of Year.
- Can use either the RTC dedicated 32 kHz oscillator input or clock derived from the external crystal/oscillator input at XTAL1. Programmable reference clock divider allows fine adjustment of the RTC.
- Dedicated power supply pin can be connected to a battery or the main 3.3 V.

6.18 Pulse width modulator

The PWM is based on the standard timer block and inherits all of its features, although only the PWM function is pinned out on the LPC2157/2158. The timer is designed to count cycles of the peripheral clock (PCLK) and optionally generate interrupts or perform other actions when specified timer values occur, based on seven match registers. The PWM function is also based on match register events.

The ability to separately control rising and falling edge locations allows the PWM to be used for more applications. For instance, multi-phase motor control typically requires three non-overlapping PWM outputs with individual control of all three pulse widths and positions.

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Two match registers can be used to provide a single edge controlled PWM output. One match register (MR0) controls the PWM cycle rate, by resetting the count upon match. The other match register controls the PWM edge position. Additional single edge controlled PWM outputs require only one match register each, since the repetition rate is the same for all PWM outputs. Multiple single edge controlled PWM outputs will all have a rising edge at the beginning of each PWM cycle, when an MR0 match occurs.

Three match registers can be used to provide a PWM output with both edges controlled. Again, the MR0 match register controls the PWM cycle rate. The other match registers control the two PWM edge positions. Additional double edge controlled PWM outputs require only two match registers each, since the repetition rate is the same for all PWM outputs.

With double edge controlled PWM outputs, specific match registers control the rising and falling edge of the output. This allows both positive going PWM pulses (when the rising edge occurs prior to the falling edge), and negative going PWM pulses (when the falling edge occurs prior to the rising edge).

6.18.1 Features

- Seven match registers allow up to six single edge controlled or three double edge controlled PWM outputs, or a mix of both types.
- The match registers also allow:
  - Continuous operation with optional interrupt generation on match.
  - Stop timer on match with optional interrupt generation.
  - Reset timer on match with optional interrupt generation.
- Supports single edge controlled and/or double edge controlled PWM outputs. Single edge controlled PWM outputs all go HIGH at the beginning of each cycle unless the output is a constant LOW. Double edge controlled PWM outputs can have either edge occur at any position within a cycle. This allows for both positive going and negative going pulses.
- Pulse period and width can be any number of timer counts. This allows complete flexibility in the trade-off between resolution and repetition rate. All PWM outputs will occur at the same repetition rate.
- Double edge controlled PWM outputs can be programmed to be either positive going or negative going pulses.
- Match register updates are synchronized with pulse outputs to prevent generation of erroneous pulses. Software must ‘release’ new match values before they can become effective.
- May be used as a standard timer if the PWM mode is not enabled.
- A 32-bit Timer/Counter with a programmable 32-bit prescaler.

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6.19 System control

6.19.1 Crystal oscillator

On-chip integrated oscillator operates with external crystal in range of 1 MHz to 25 MHz. The oscillator output frequency is called f_{osc} and the ARM processor clock frequency is referred to as CCLK for purposes of rate equations, etc. f_{osc} and CCLK are the same value unless the PLL is running and connected. Refer to Section 6.19.2 “PLL” for additional information.

6.19.2 PLL

The PLL accepts an input clock frequency in the range of 10 MHz to 25 MHz. The input frequency is multiplied up into the range of 10 MHz to 60 MHz with a Current Controlled Oscillator (CCO). The multiplier can be an integer value from 1 to 32 (in practice, the multiplier value cannot be higher than 6 on this family of microcontrollers due to the upper frequency limit of the CPU). The CCO operates in the range of 156 MHz to 320 MHz, so there is an additional divider in the loop to keep the CCO within its frequency range while the PLL is providing the desired output frequency. The output divider may be set to divide by 2, 4, 8 or 16 to produce the output clock. Since the minimum output divider value is 2, it is insured that the PLL output has a 50 % duty cycle. The PLL is turned off and bypassed following a chip reset and may be enabled by software. The program must configure and activate the PLL, wait for the PLL to Lock, then connect to the PLL as a clock source. The PLL settling time is 100 µs.

6.19.3 Reset and wake-up timer

Reset has two sources on the LPC2157/2158: the $\overline{\text{RESET}}$ pin and watchdog reset. The $\overline{\text{RESET}}$ pin is a Schmitt trigger input pin with an additional glitch filter. Assertion of chip reset by any source starts the Wake-up Timer (see Wake-up Timer description below), causing the internal chip reset to remain asserted until the external reset is de-asserted, the oscillator is running, a fixed number of clocks have passed, and the on-chip flash controller has completed its initialization.

When the internal reset is removed, the processor begins executing at address 0, which is the reset vector. At that point, all of the processor and peripheral registers have been initialized to predetermined values.

The Wake-up Timer ensures that the oscillator and other analog functions required for chip operation are fully functional before the processor is allowed to execute instructions. This is important at power on, all types of reset, and whenever any of the aforementioned functions are turned off for any reason. Since the oscillator and other functions are turned off during Power-down mode, any wake-up of the processor from Power-down mode makes use of the Wake-up Timer.

The Wake-up Timer monitors the crystal oscillator as the means of checking whether it is safe to begin code execution. When power is applied to the chip, or some event caused the chip to exit Power-down mode, some time is required for the oscillator to produce a signal of sufficient amplitude to drive the clock logic. The amount of time depends on many factors, including the rate of V_{DD} ramp (in the case of power on), the type of crystal and its electrical characteristics (if a quartz crystal is used), as well as any other external circuitry (e.g. capacitors), and the characteristics of the oscillator itself under the existing ambient conditions.

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6.19.4 Brownout detector

The LPC2157/2158 include 2-stage monitoring of the voltage on the V_{DD} pins. If this voltage falls below 2.9 V, the BOD asserts an interrupt signal to the VIC. This signal can be enabled for interrupt; if not, software can monitor the signal by reading dedicated register.

The second stage of low voltage detection asserts reset to inactivate the LPC2157/2158 when the voltage on the V_{DD} pins falls below 2.6 V. This reset prevents alteration of the flash as operation of the various elements of the chip would otherwise become unreliable due to low voltage. The BOD circuit maintains this reset down below 1 V, at which point the POR circuitry maintains the overall reset.

Both the 2.9 V and 2.6 V thresholds include some hysteresis. In normal operation, this hysteresis allows the 2.9 V detection to reliably interrupt, or a regularly-executed event loop to sense the condition.

6.19.5 Code security

This feature of the LPC2157/2158 allow an application to control whether it can be debugged or protected from observation.

If after reset on-chip bootloader detects a valid checksum in flash and reads 0x8765 4321 from address 0x1FC in flash, debugging will be disabled and thus the code in flash will be protected from observation. Once debugging is disabled, it can be enabled only by performing a full chip erase using the ISP.

6.19.6 External interrupt inputs

The LPC2157/2158 include up to nine edge or level sensitive external interrupt inputs as selectable pin functions. When the pins are combined, external events can be processed as four independent interrupt signals. The external interrupt inputs can optionally be used to wake-up the processor from Power-down mode.

Additionally capture input pins can also be used as external interrupts without the option to wake the device up from Power-down mode.

6.19.7 Memory mapping control

The Memory Mapping Control alters the mapping of the interrupt vectors that appear beginning at address 0x0000 0000. Vectors may be mapped to the bottom of the on-chip flash memory, or to the on-chip static RAM. This allows code running in different memory spaces to have control of the interrupts.

6.19.8 Power control

The LPC2157/2158 supports two reduced power modes: Idle mode and Power-down mode.

In Idle mode, execution of instructions is suspended until either a reset or interrupt occurs. Peripheral functions continue operation during Idle mode and may generate interrupts to cause the processor to resume execution. Idle mode eliminates power used by the processor itself, memory systems and related controllers, and internal buses.

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In Power-down mode, the oscillator is shut down and the chip receives no internal clocks. The processor state and registers, peripheral registers, and internal SRAM values are preserved throughout Power-down mode and the logic levels of chip output pins remain static. The Power-down mode can be terminated and normal operation resumed by either a reset or certain specific interrupts that are able to function without clocks. Since all dynamic operation of the chip is suspended, Power-down mode reduces chip power consumption to nearly zero.

Selecting an external 32 kHz clock instead of the PCLK as a clock-source for the on-chip RTC will enable the microcontroller to have the RTC active during Power-down mode. Power-down current is increased with RTC active. However, it is significantly lower than in Idle mode.

A Power Control for Peripherals feature allows individual peripherals to be turned off if they are not needed in the application, resulting in additional power savings during active and Idle mode.

6.19.9 APB bus

The APB divider determines the relationship between the processor clock (CCLK) and the clock used by peripheral devices (PCLK). The APB divider serves two purposes. The first is to provide peripherals with the desired PCLK via APB bus so that they can operate at the speed chosen for the ARM processor. In order to achieve this, the APB bus may be slowed down to $\frac{1}{2}$ to $\frac{1}{4}$ of the processor clock rate. Because the APB bus must work properly at power-up (and its timing cannot be altered if it does not work since the APB divider control registers reside on the APB bus), the default condition at reset is for the APB bus to run at $\frac{1}{4}$ of the processor clock rate. The second purpose of the APB divider is to allow power savings when an application does not require any peripherals to run at the full processor rate. Because the APB divider is connected to the PLL output, the PLL remains active (if it was running) during Idle mode.

6.20 Emulation and debugging

The LPC2157/2158 supports emulation and debugging via a JTAG serial port. Debugging functions are multiplexed with GPIOs on Port 1. This means that all communication, timer and interface peripherals residing on Port 0 are available during the development and debugging phase as they are when the application is run in the embedded system itself.

6.20.1 EmbeddedICE

Standard ARM EmbeddedICE logic provides on-chip debug support. The debugging of the target system requires a host computer running the debugger software and an EmbeddedICE protocol convertor. EmbeddedICE protocol convertor converts the remote debug protocol commands to the JTAG data needed to access the ARM core.

The ARM core has a Debug Communications Channel (DCC) function built-in. The DCC allows a program running on the target to communicate with the host debugger or another separate host without stopping the program flow or even entering the debug state. The DCC is accessed as a co-processor 14 by the program running on the ARM7TDMI-S core. The DCC allows the JTAG port to be used for sending and receiving data without affecting the normal program flow. The DCC data and control registers are mapped in to addresses in the EmbeddedICE logic.

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The JTAG clock (TCK) must be slower than $\frac{1}{6}$ of the CPU clock (CCLK) for the JTAG interface to operate.

6.20.2 RealMonitor

RealMonitor is a configurable software module, developed by ARM Inc., which enables real-time debug. It is a lightweight debug monitor that runs in the background while users debug their foreground application. It communicates with the host using the DCC, which is present in the EmbeddedICE logic. The LPC2157/2158 contain a specific configuration of RealMonitor software programmed into the on-chip flash memory.

6.21 LCD driver

6.21.1 General description

The LCD segment driver in the LPC2157/2158 can interface to most LCDs using low multiplex rates. It generates the drive signals for static or multiplexed LCDs containing up to four backplanes and up to 32 segments. The LCD controller communicates to a host using the I^2C-bus. The I^2C-bus clock and data signals for both the microcontroller and the LCD driver are available on the LPC2157/2158 providing system flexibility. Communication overhead to manage the display is minimized by an on-chip display RAM with auto-increment addressing, hardware subaddressing, and display memory switching (static and duplex drive modes). Please refer to PCF8576D data sheet for electrical data.

6.21.2 Functional description

The LCD controller is a versatile peripheral device designed to interface microcontrollers to a wide variety of LCDs. It can directly drive any static or multiplexed LCD containing up to four backplanes and up to 32 segments. The display configurations possible with the LCD controller depend on the number of active backplane outputs required. A selection of display configurations is shown in Table 4. All of these configurations can be implemented in a typical system.

The microcontroller communicates to the LCD controller using the I^2C-bus.The appropriate biasing voltages for the multiplexed LCD waveforms are generated internally. The only other connections required to complete the system are to the power supplies ($V_{DD(LCD)}$, V_{SS} and V_{LCD}) and the LCD panel chosen for the application.

Table 4. Selection of display configurations

Number of		7-segments numeric		14-segments alphanumeric		Dot matrix
Backplanes	Segments	Digits	Indicator symbols	Characters	Indicator symbols	
4	128	16	16	8	16	128
3	96	12	12	6	12	96
2	64	8	8	4	8	64
1	32	4	4	2	4	32

6.21.3 LCD bias voltages

LCD biasing voltages are obtained from an internal voltage divider consisting of three series resistors connected between V_{LCD} and V_{SS}. The LCD voltage can be temperature compensated externally via the supply to pin V_{LCD}. A voltage selector drives the multiplexing of the LCD based on programmable configurations.

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6.21.4 Oscillator

6.21.4.1 Internal clock

An internal oscillator provides the clock signals for the internal logic of the LCD controller and its LCD drive signals. After power-up, pin SDA must be HIGH to guarantee that the clock starts.

6.21.5 Timing

The LCD controller timing controls the internal data flow of the device. This includes the transfer of display data from the display RAM to the display segment outputs. The timing also generates the LCD frame signal whose frequency is derived from the clock frequency. The frame signal frequency is a fixed division of the clock frequency from either the internal or an external clock.

Frame frequency = $f_{osc(ctrl)LCD}/24$.

6.21.6 Display register

A display latch holds the display data while the corresponding multiplex signals are generated. There is a one-to-one relationship between the data in the display latch, the LCD segment outputs, and each column of the display RAM.

6.21.7 Segment outputs

The LCD drive section includes 32 segment outputs S0 to S31. The segment output signals are generated according to the multiplexed backplane signals and the display latch data. When less than 32 segment outputs are required, the unused segment outputs should be left open-circuit.

6.21.8 Backplane outputs

The LCD drive section has four backplane outputs BP0 to BP3. The backplane output signals are generated in accordance with the selected LCD drive mode. If less than four backplane outputs are required, the unused outputs can be left open-circuit. In the 1:3 multiplex drive mode, BP3 carries the same signal as BP1, therefore these two adjacent outputs can be tied together to give enhanced drive capabilities. In the 1:2 multiplex drive mode, BP0 and BP2, BP1 and BP3 respectively carry the same signals and may also be paired to increase the drive capabilities. In the static drive mode the same signal is carried by all four backplane outputs and they can be connected in parallel for very high drive requirements.

6.21.9 Display RAM

The display RAM is a static 32 $\times$ 4-bit RAM which stores LCD data. There is a one-to-one correspondence between the RAM addresses and the segment outputs, and between the individual bits of a RAM word and the backplane outputs. The first RAM column corresponds to the 32 segments for backplane 0 (BP0). In multiplexed LCD applications the segment data of the second, third and fourth column of the display RAM are time-multiplexed with BP1, BP2 and BP3 respectively.

6.21.10 Data pointer

The Display RAM is addressed using the data pointer. Either a single byte or a series of display bytes may be loaded into any location of the display RAM.

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6.21.11 Output bank selector

The LCD controller includes a RAM bank switching feature in the static and 1:2 drive modes. In the static drive mode, the BANK SELECT command may request the contents of bit 2 to be selected for display instead of the contents of bit 0. In 1:2 mode, the contents of bits 2 and 3 may be selected instead of bits 0 and 1. This allows display information to be prepared in an alternative bank and then selected for display when it is assembled.

6.21.12 Input bank selector

The input bank selector loads display data into the display RAM based on the selected LCD drive configuration. The BANK SELECT command can be used to load display data in bit 2 in static drive mode or in bits 2 and 3 in 1:2 mode. The input bank selector functions are independent of the output bank selector.

6.21.13 Blinker

The LCD controller has a very versatile display blinking capability. The whole display can blink at a frequency selected by the BLINK command. Each blink frequency is a multiple integer value of the clock frequency; the ratio between the clock frequency and blink frequency depends on the blink mode selected, as shown in Table 5.

An additional feature allows an arbitrary selection of LCD segments to be blinked in the static and 1:2 drive modes. This is implemented without any communication overheads by the output bank selector which alternates the displayed data between the data in the display RAM bank and the data in an alternative RAM bank at the blink frequency. This mode can also be implemented by the BLINK command.

The entire display can be blinked at a frequency other than the nominal blink frequency by sequentially resetting and setting the display enable bit E at the required rate using the MODE SET command.

Table 5. Blinking frequencies

Blink mode	Normal operating mode ratio	Normal blink frequency
Off	-	blinking off
2 Hz	$f_{osc(ctrl)LCD}/768$	2 Hz
1 Hz	$f_{osc(ctrl)LCD}/1536$	1 Hz
0.5 Hz	$f_{osc(ctrl)LCD}/3072$	0.5 Hz

Blink modes 0.5 Hz, 1 Hz and 2 Hz, and nominal blink frequencies 0.5 Hz, 1 Hz and 2 Hz correspond to an oscillator frequency ($f_{osc(ctrl)LCD}$) of 1536 Hz at pin CLK. The oscillator frequency range is 397 Hz to 3046 Hz.

6.21.13.1 I^2C-bus controller

The LCD controller acts as an I^2C-bus slave receiver. In the LPC2157/2158 the hardware subaddress inputs A0, A1 and A2 are tied to V_{SS} setting the hardware subaddress = 0.

6.21.14 Input filters

To enhance noise immunity in electrically adverse environments, RC low-pass filters are provided on the SDA and SCL lines.

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6.21.15 I²C-bus slave addresses

The I²C-bus slave address is 0111 0000. The LCD controller is a write-only device and will not respond to a read access.

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7. Limiting values

Table 6. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).[1]

Symbol	Parameter	Conditions		Min	Max	Unit
V_{DD}	supply voltage (core and external rail)			–0.5	+3.6	V
V_{DDA}	analog 3.3 V pad supply voltage			–0.5	+4.6	V
$V_{i(VBAT)}$	input voltage on pin VBAT	for the RTC		–0.5	+4.6	V
$V_{i(VREF)}$	input voltage on pin VREF			–0.5	+4.6	V
V_{IA}	analog input voltage	on ADC related pins		–0.5	+5.1	V
V_I	input voltage	5 V tolerant I/O pins; only valid when the V_{DD} supply voltage is present	[2]	–0.5	+6.0	V
		other I/O pins	[2][3]	–0.5	V_{DD} + 0.5	V
I_{DD}	supply current	per supply pin	[4]	-	100	mA
I_{SS}	ground current	per ground pin	[4]	-	100	mA
T_{stg}	storage temperature		[5]	–65	+150	°C
$P_{tot(pack)}$	total power dissipation (per package)	based on package heat transfer, not device power consumption		-	1.5	W

[1] The following applies to the Limiting values:

a) This product includes circuitry specifically designed for the protection of its internal devices from the damaging effects of excessive static charge. Nonetheless, it is suggested that conventional precautions be taken to avoid applying greater than the rated maximum.

b) Parameters are valid over operating temperature range unless otherwise specified. All voltages are with respect to V_{SS} unless otherwise noted.

[2] Including voltage on outputs in 3-state mode.

[3] Not to exceed 4.6 V.

[4] The peak current is limited to 25 times the corresponding maximum current.

[5] Dependent on package type.

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8. Static characteristics

Table 7. Static characteristics

T_{amb} = −40 °C to +85 °C for commercial applications, unless otherwise specified.

Symbol	Parameter	Conditions		Min	Typ[1]	Max	Unit
V_{DD}	supply voltage		[2]	3.0	3.3	3.6	V
V_{DDA}	analog 3.3 V pad supply voltage			3.0	3.3	3.6	V
$V_{i(VBAT)}$	input voltage on pin VBAT		[3]	2.0	3.3	3.6	V
$V_{i(VREF)}$	input voltage on pin VREF			2.5	3.3	V_{DDA}	V
Standard port pins, $\overline{\text{RESET}}$, RTCK							
I_{IL}	LOW-level input current	V_I = 0 V; no pull-up		-	-	3	µA
I_{IH}	HIGH-level input current	$V_I = V_{DD}$; no pull-down		-	-	3	µA
I_{OZ}	OFF-state output current	V_O = 0 V; $V_O = V_{DD}$; no pull-up/down		-	-	3	µA
I_{latch}	I/O latch-up current	$-(0.5V_{DD}) < V_I < (1.5V_{DD})$; T_j < 125 °C		-	-	100	mA
V_I	input voltage	pin configured to provide a digital function	[4][5][6][7]	0	-	5.5	V
V_O	output voltage	output active		0	-	V_{DD}	V
V_{IH}	HIGH-level input voltage			2.0	-	-	V
V_{IL}	LOW-level input voltage			-	-	0.8	V
V_{hys}	hysteresis voltage			0.4	-	-	V
V_{OH}	HIGH-level output voltage	I_{OH} = −4 mA	[8]	V_{DD} − 0.4	-	-	V
V_{OL}	LOW-level output voltage	I_{OL} = −4 mA	[8]	-	-	0.4	V
I_{OH}	HIGH-level output current	$V_{OH} = V_{DD}$ − 0.4 V	[8]	−4	-	-	mA
I_{OL}	LOW-level output current	V_{OL} = 0.4 V	[8]	4	-	-	mA
I_{OHS}	HIGH-level short-circuit output current	V_{OH} = 0 V	[9]	-	-	−45	mA
I_{OLS}	LOW-level short-circuit output current	$V_{OL} = V_{DDA}$	[9]	-	-	50	mA
I_{pd}	pull-down current	V_I = 5 V	[10]	10	50	150	µA
I_{pu}	pull-up current	V_I = 0 V	[11]	−15	−50	−85	µA
		$V_{DD} < V_I$ < 5 V	[10]	0	0	0	µA

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Table 7. Static characteristics *...continued*

T_{amb} = −40 °C to +85 °C for commercial applications, unless otherwise specified.

Symbol	Parameter	Conditions		Min	Typ[1]	Max	Unit
$I_{DD(act)}$	active mode supply current	V_{DD} = 3.3 V; T_{amb} = 25 °C; code `while(1){}` executed from flash, no active peripherals		-	15	50	mA
		CCLK = 10 MHz					
		CCLK = 60 MHz		-	40	70	mA
		V_{DD} = 3.3 V; T_{amb} = 25 °C; code executed from flash; USB enabled and active; all other peripherals disabled		-	27	70	mA
		CCLK = 12 MHz					
		CCLK = 60 MHz		-	57	90	mA
$I_{DD(pd)}$	Power-down mode supply current	V_{DD} = 3.3 V; T_{amb} = 25 °C		-	40	100	µA
		V_{DD} = 3.3 V; T_{amb} = 85 °C		-	250	500	µA
I_{BATpd}	Power-down mode battery supply current	RTC clock = 32 kHz (from RTCX pins); T_{amb} = 25 °C	[12]	-	15	30	µA
		V_{DD} = 3.0 V; $V_{i(VBAT)}$ = 2.5 V					
		V_{DD} = 3.0 V; $V_{i(VBAT)}$ = 3.0 V		-	20	40	µA
I_{BATact}	active mode battery supply current	CCLK = 60 MHz; PCLK = 15 MHz; PCLK enabled to RTCK; RTC clock = 32 kHz (from RTCX pins); T_{amb} = 25 °C	[12]	-	78	-	µA
		V_{DD} = 3.0 V; $V_{i(VBAT)}$ = 3.0 V					
$I_{BATact(opt)}$	optimized active mode battery supply current	PCLK disabled to RTCK in the PCONP register; RTC clock = 32 kHz (from RTCX pins); T_{amb} = 25 °C; $V_{i(VBAT)}$ = 3.3 V	[12][13]	-	23	-	µA
		CCLK = 25 MHz					
		CCLK = 60 MHz		-	30	-	µA
I^2C-bus pins							
V_{IH}	HIGH-level input voltage			$0.7V_{DD}$	-	-	V
V_{IL}	LOW-level input voltage			-	-	$0.3V_{DD}$	V
V_{hys}	hysteresis voltage			-	$0.5V_{DD}$	-	V
V_{OL}	LOW-level output voltage	I_{OLS} = 3 mA	[8]	-	-	0.4	V
I_{LI}	input leakage current	$V_I = V_{DD}$	[14]	-	2	4	µA
		V_I = 5 V		-	10	22	µA
Oscillator pins							
$V_{i(XTAL1)}$	input voltage on pin XTAL1			0	-	1.8	V

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Table 7. Static characteristics *…continued*

T_{amb} = −40 °C to +85 °C for commercial applications, unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ[1]	Max	Unit
$V_{o(XTAL2)}$	output voltage on pin XTAL2		0	-	1.8	V
$V_{i(RTCX1)}$	input voltage on pin RTCX1		0	-	1.8	V
$V_{o(RTCX2)}$	output voltage on pin RTCX2		0	-	1.8	V
USB pins						
I_{OZ}	OFF-state output current	0 V < V_I < 3.3 V	-	-	±10	µA
V_{BUS}	bus supply voltage		-	-	5.25	V
V_{DI}	differential input sensitivity voltage	|(D+) − (D−)|	0.2	-	-	V
V_{CM}	differential common mode voltage range	includes V_{DI} range	0.8	-	2.5	V
$V_{th(rs)se}$	single-ended receiver switching threshold voltage		0.8	-	2.0	V
V_{OL}	LOW-level output voltage	R_L of 1.5 kΩ to 3.6 V	-	-	0.3	V
V_{OH}	HIGH-level output voltage	R_L of 15 kΩ to GND	2.8	-	3.6	V
C_{trans}	transceiver capacitance	pin to GND	-	-	20	pF
Z_{DRV}	driver output impedance for driver which is not high-speed capable	steady state drive [15]	29	-	44	Ω
R_{pu}	pull-up resistance	SoftConnect = ON	1.1	-	1.9	kΩ

[1] Typical ratings are not guaranteed. The values listed are at room temperature (25 °C), nominal supply voltages.

[2] Core and external rail.

[3] The RTC typically fails when $V_{i(VBAT)}$ drops below 1.6 V.

[4] Including voltage on outputs in 3-state mode.

[5] V_{DD} supply voltages must be present.

[6] 3-state outputs go into 3-state mode when V_{DD} is grounded.

[7] Please also see the errata note mentioned in errata sheet.

[8] Accounts for 100 mV voltage drop in all supply lines.

[9] Allowed as long as the current limit does not exceed the maximum current allowed by the device.

[10] Minimum condition for V_I = 4.5 V, maximum condition for V_I = 5.5 V.

[11] Applies to P1[16] to P1[31].

[12] On pin VBAT.

[13] Optimized for low battery consumption.

[14] To V_{SS}.

[15] Includes external resistors of 18 Ω ±1 % on D+ and D−.

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Table 8. ADC static characteristics

V_{DDA} = 2.5 V to 3.6 V; T_{amb} = −40 °C to +85 °C unless otherwise specified; ADC frequency 4.5 MHz.

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
V_{IA}	analog input voltage			0	-	V_{DDA}	V
C_{ia}	analog input capacitance			-	-	1	pF
E_D	differential linearity error	V_{SSA} = 0 V, V_{DDA} = 3.3 V	[1][2]	-	-	±1	LSB
$E_{L(adj)}$	integral non-linearity	V_{SSA} = 0 V, V_{DDA} = 3.3 V	[3]	-	-	±2	LSB
E_O	offset error	V_{SSA} = 0 V, V_{DDA} = 3.3 V	[4]	-	-	±3	LSB
E_G	gain error	V_{SSA} = 0 V, V_{DDA} = 3.3 V	[5]	-	-	±0.5	%
E_T	absolute error	V_{SSA} = 0 V, V_{DDA} = 3.3 V	[6]	-	-	±4	LSB
R_{vsi}	voltage source interface resistance		[7]	-	-	40	kΩ

[1] The ADC is monotonic, there are no missing codes.

[2] The differential linearity error (E_D) is the difference between the actual step width and the ideal step width. See Figure 7.

[3] The integral non-linearity ($E_{L(adj)}$) is the peak difference between the center of the steps of the actual and the ideal transfer curve after appropriate adjustment of gain and offset errors. See Figure 7.

[4] The offset error (E_O) is the absolute difference between the straight line which fits the actual curve and the straight line which fits the ideal curve. See Figure 7.

[5] The gain error (E_G) is the relative difference in percent between the straight line fitting the actual transfer curve after removing offset error, and the straight line which fits the ideal transfer curve. See Figure 7.

[6] The absolute error (E_T) is the maximum difference between the center of the steps of the actual transfer curve of the non-calibrated ADC and the ideal transfer curve. See Figure 7.

[7] See Figure 8.

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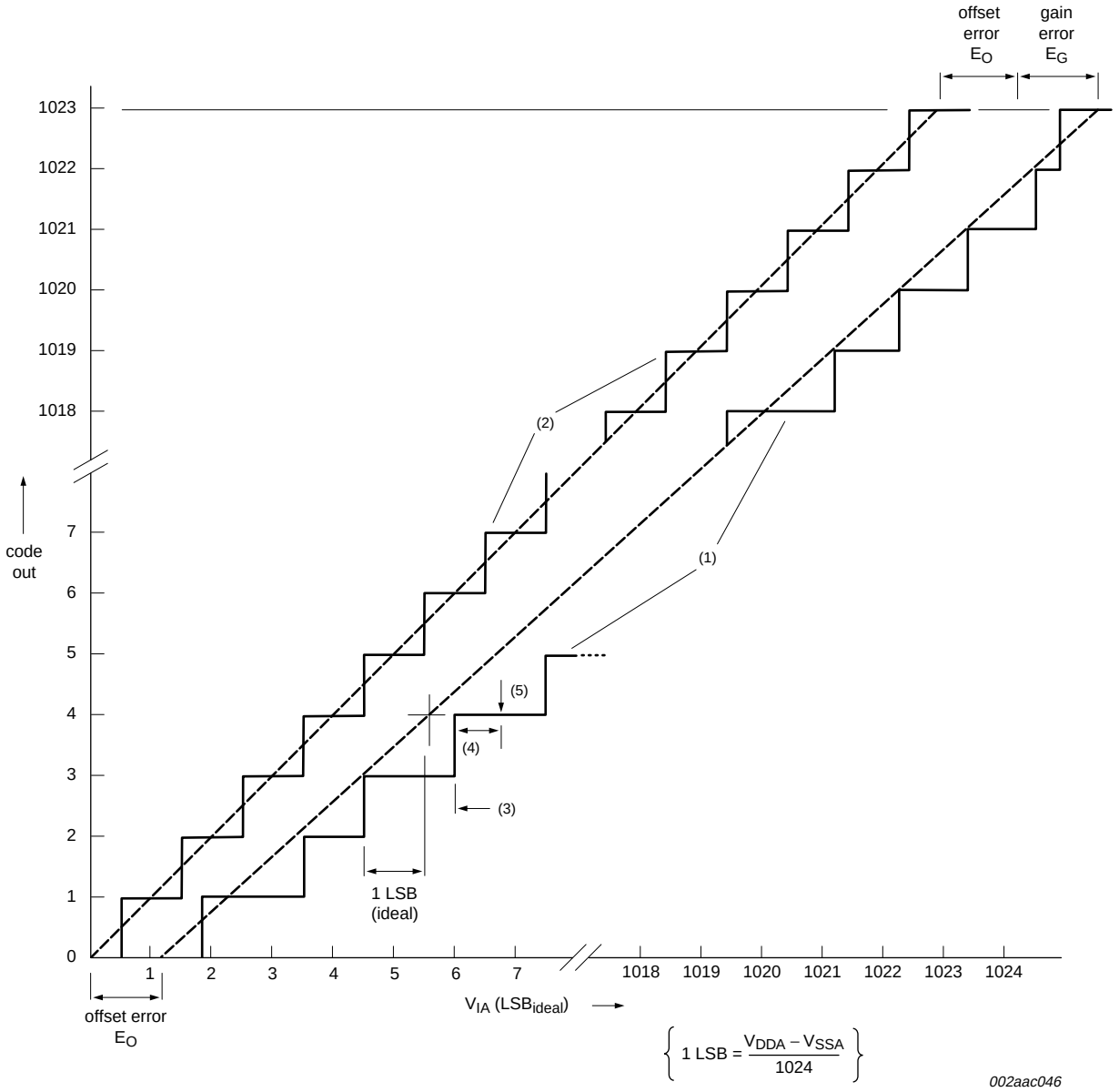

(1) Example of an actual transfer curve.

(2) The ideal transfer curve.

(3) Differential linearity error (E_D).

(4) Integral non-linearity ($E_{L(adj)}$).

(5) Center of a step of the actual transfer curve.

Fig 7. ADC characteristics

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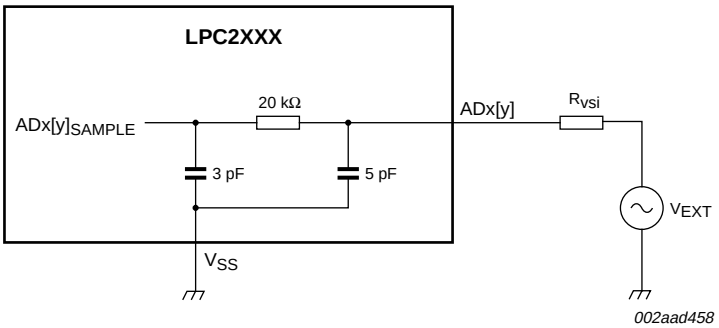

Fig 8. Suggested ADC interface - LPC2157/2158 ADx[y] pin

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9. Dynamic characteristics

Table 9. Dynamic characteristics of USB pins (full-speed)

C_L = 50 pF; R_{pu} = 1.5 kΩ on D+ to V_{DD}, unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
t_r	rise time	10 % to 90 %	4	-	20	ns
t_f	fall time	10 % to 90 %	4	-	20	ns
t_{FRFM}	differential rise and fall time matching	(t_r/t_f)	90	-	110	%
V_{CRS}	output signal crossover voltage		1.3	-	2.0	V
t_{FEOPT}	source SE0 interval of EOP	see Figure 10	160	-	175	ns
t_{FDEOP}	source jitter for differential transition to SE0 transition	see Figure 10	–2	-	+5	ns
t_{JR1}	receiver jitter to next transition		–18.5	-	+18.5	ns
t_{JR2}	receiver jitter for paired transitions	10 % to 90 %	–9	-	+9	ns
t_{EOPR1}	EOP width at receiver	must reject as EOP; see Figure 10	[1] 40	-	-	ns
t_{EOPR2}	EOP width at receiver	must accept as EOP; see Figure 10	[1] 82	-	-	ns

[1] Characterized but not implemented as production test. Guaranteed by design.

Table 10. Dynamic characteristics

T_{amb} = −40 °C to +85 °C for commercial applications, V_{DD} over specified ranges[1]

Symbol	Parameter	Conditions	Min	Typ[2]	Max	Unit
External clock						
f_{osc}	oscillator frequency		10	-	25	MHz
$T_{cy(clk)}$	clock cycle time		40	-	100	ns
t_{CHCX}	clock HIGH time		$T_{cy(clk)} \times 0.4$	-	-	ns
t_{CLCX}	clock LOW time		$T_{cy(clk)} \times 0.4$	-	-	ns
t_{CLCH}	clock rise time		-	-	5	ns
t_{CHCL}	clock fall time		-	-	5	ns
Port pins (P0[2], P0[3], P0[11], and P0[14])						
$t_{r(o)}$	output rise time		-	10	-	ns
$t_{f(o)}$	output fall time		-	10	-	ns
I^2C-bus pins (P0[2], P0[3], P0[11], and P0[14])						
$t_{f(o)}$	output fall time	V_{IH} to V_{IL}	$20 + 0.1 \times C_b$[3]	-	-	ns

[1] Parameters are valid over operating temperature range unless otherwise specified.

[2] Typical ratings are not guaranteed. The values listed are at room temperature (25 °C), nominal supply voltages.

[3] Bus capacitance C_b in pF, from 10 pF to 400 pF.

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9.1 Timing

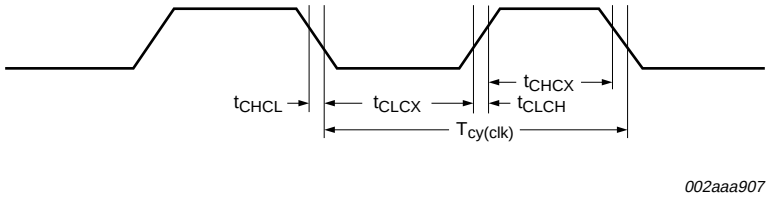

Fig 9. External clock timing (with an amplitude of at least $V_{i(RMS)}$ = 200 mV)

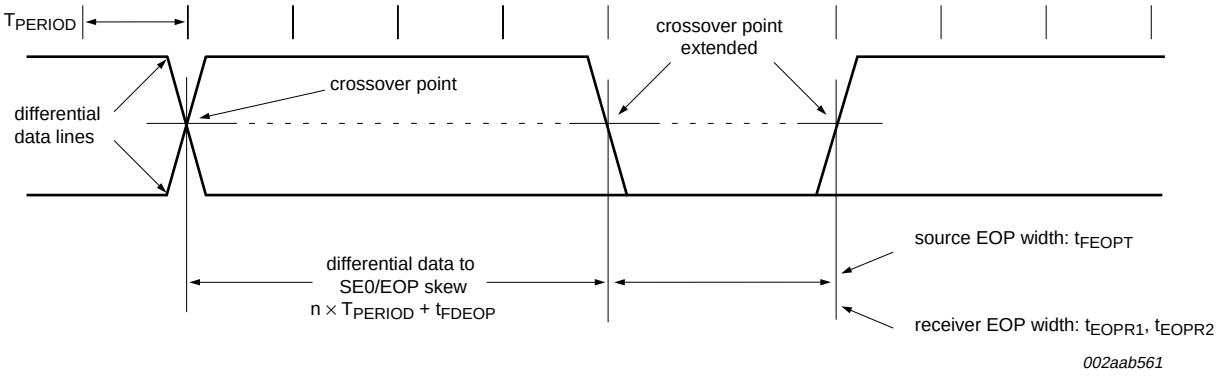

Fig 10. Differential data-to-EOP transition skew and EOP width

10. Application information

10.1 Suggested USB interface solutions

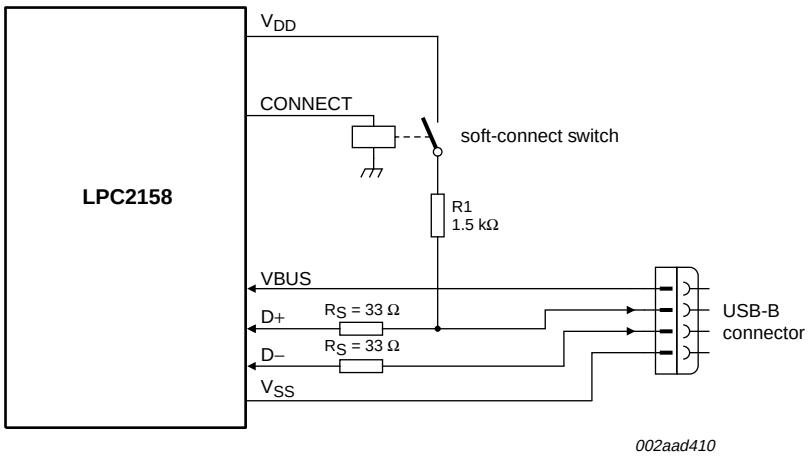

Fig 11. LPC2158 USB interface using the CONNECT function on pin 17

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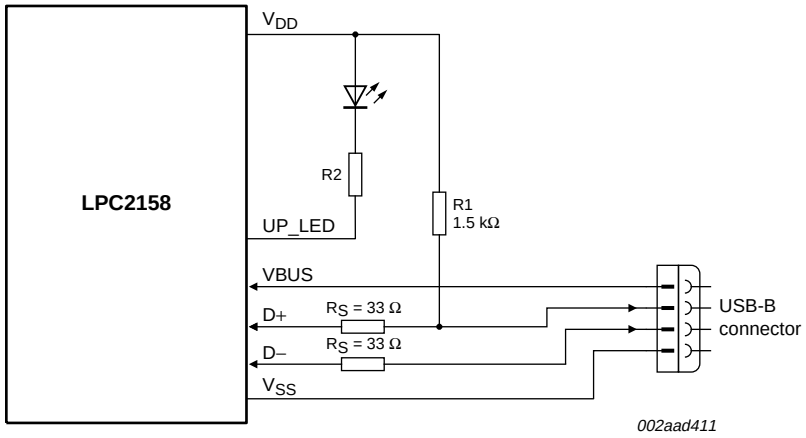

Fig 12. LPC2158 USB interface using the UP_LED function on pin 17

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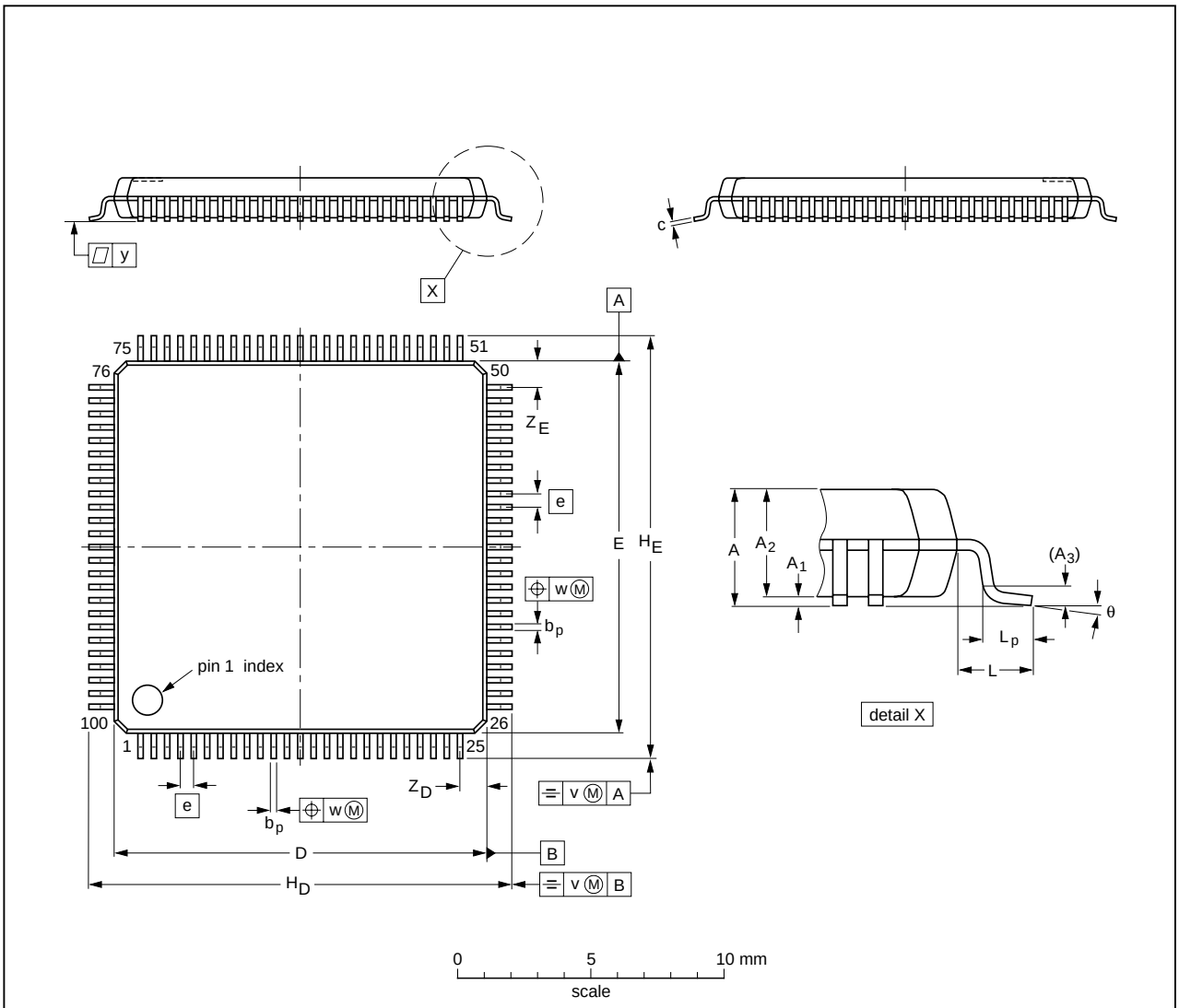
11. Package outline

LQFP100: plastic low profile quad flat package; 100 leads; body 14 x 14 x 1.4 mm **SOT407-1**



DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(1)}$	e	H_D	H_E	L	L_p	v	w	y	$Z_D^{(1)}$	$Z_E^{(1)}$	θ
mm	1.6	0.15 0.05	1.45 1.35	0.25	0.27 0.17	0.20 0.09	14.1 13.9	14.1 13.9	0.5	16.25 15.75	16.25 15.75	1	0.75 0.45	0.2	0.08	0.08	1.15 0.85	1.15 0.85	7° 0°

Note

1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT407-1	136E20	MS-026				~~00-02-01~~ 03-02-20

Fig 13. Package outline SOT407-1 (LQFP100)

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12. Abbreviations

Table 11. Abbreviations

Acronym	Description
ADC	Analog-to-Digital Converter
AHB	Advanced High-performance Bus
AMBA	Advanced Microcontroller Bus Architecture
APB	Advanced Peripheral Bus
BOD	Brown-Out Detection
DAC	Digital-to-Analog Converter
DCC	Debug Communications Channel
DMA	Direct Memory Access
FIFO	First In, First Out
GPIO	General Purpose Input/Output
I/O	Input/Output
ISP	In-System Programming
JTAG	Joint Test Action Group
MCU	Microcontroller Unit
PLL	Phase-Locked Loop
POR	Power-On Reset
PWM	Pulse Width Modulator
RC	Resistance-Capacitance
SPI	Serial Peripheral Interface
SSI	Synchronous Serial Interface
SSP	Synchronous Serial Port
TTL	Transistor-Transistor Logic
UART	Universal Asynchronous Receiver/Transmitter

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13. Revision history

Table 12. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
LPC2157_2158_2	20090209	Product data sheet	-	LPC2157_2158_1
Modifications:	• Section 2 “Features”: removed RC oscillator feature • Section 2 “Features”: added CPU operating voltage feature • Section 5.2 “Pin description”: description pin 82 P1[29]/TCK modified • Section 6.20.1 “EmbeddedICE”: added JTAG clock condition (last paragraph) • Table 7 “Static characteristics”: V_{hys}, 0.4 V moved from Typ to Min column • Table 7 “Static characteristics”: added table note [7]			
LPC2157_2158_1	20081015	Product data sheet	-	-

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14. Legal information

14.1 Data sheet status

Document status[1][2]	Product status[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the Internet at URL http://www.nxp.com.

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