ES_LPC122x

Errata sheet LPC1224/25/26/27

Rev. 1.3 — 13 September 2013 **Errata sheet**

Document information

Info	Content
Keywords	LPC1227FBD64, LPC1227FBD48, LPC1226FBD64, LPC1226FBD48, LPC1225FBD64, LPC1225FBD48, LPC1224FBD64, LPC1224FBD48 errata
Abstract	This errata sheet describes both the known functional problems and any deviations from the electrical specifications known at the release date of this document. Each deviation is assigned a number and its history is tracked in a table.

Revision history

Rev	Date	Description
1.3	20130913	• Added I2C.1.
1.2	20120321	• Corrected initial device revision from '-' to 'A'.
1.1	20120119	• Added ADC.2.
1	20110501	• Initial version.

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1. Product identification

The LPC122x devices typically have the following top-side marking:

LPC122x

/xxx

xxxxxxx

xxYYWWxR[x]

The last letter in the last line (field 'R') will identify the device revision. This Errata Sheet covers the following revisions of the LPC122x:

Table 1. Device revision table

Revision identifier (R)	Revision description
'A'	Initial device revision

Field 'YY' states the year the device was manufactured. Field 'WW' states the week the device was manufactured during that year.

2. Errata overview

Table 2. Functional problems table

Functional problems	Short description	Revision identifier	Detailed description
ADC.1	PIO0_2, PIO1_5 trigger sources do not operate properly	'A'	Section 3.1
ADC.2	A/D Global Data register should not be used with burst mode or hardware triggering.	'A'	Section 3.2
I2C.1	In the slave-transmitter mode, the device set in the monitor mode must write a dummy value of 0xFF into the DAT register.	'A'	Section 3.3
RTC.1	Self-timed wakeup from Deep-Sleep requires WDOsc	'A'	Section 3.4

Table 3. AC/DC deviations table

AC/DC deviations	Short description	Product version(s)	Detailed description
n/a	n/a	n/a	n/a

Table 4. Errata notes table

Errata notes	Short description	Revision identifier	Detailed description
n/a	n/a	n/a	n/a

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3. Functional problems detail

3.1 ADC.1: PIO0_2, PIO1_5 trigger sources to ADC do not operate properly

Introduction:

There are two asynchronous trigger inputs to the analog to digital converter: PIO0_2 and PIO1_5. There are also four timer driven synchronous trigger sources controlled by timer MAT events.

Problem:

Asynchronous trigger events on PIO0_2 and PIO1_5 can be lost by the analog to digital converter. Synchronous sources are unaffected and can be used without issue.

Work-around:

None.

3.2 ADC.2: A/D Global Data register should not be used with burst mode or hardware triggering

Introduction:

On the LPC122x, the START field and the BURST bit in the A/D control register specify whether A/D conversions are initiated via software command, in response to some hardware trigger, or continuously in burst ("hardware-scan") mode. Results of the ADC conversions can be read in one of two ways. One is to use the A/D Global Data Register to read all data from the ADC. Another is to use the individual A/D Channel Data Registers.

Problem:

If the burst mode is enabled (BURST bit set to ‘1’) or if hardware triggering is specified, the A/D conversion results read from the A/D Global Data register could be incorrect. If conversions are only launched directly by software command (BURST bit = '0' and START = ‘001’), the results read from the A/D Global Data register will be correct provided the previous result is read prior to launching a new conversion.

Work-around:

When using either burst mode or hardware triggering, the individual A/D Channel Data registers should be used instead of the A/D Global Data register to read the A/D conversion results.

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3.3 I2C.1: In the slave-transmitter mode, the device set in the monitor mode must write a dummy value of 0xFF into the DAT register

Introduction:

The I2C monitor allows the device to monitor the I2C traffic on the I^2C-bus in a non-intrusive way.

Problem:

In the slave-transmitter mode, the device set in the monitor mode must write a dummy value of 0xFF into the DAT register. If this is not done, the received data from the slave device will be corrupted. To allow the monitor mode to have sufficient time to process the data on the I^2C-bus, the device may need to have the ability to stretch the I2C clock. Under this condition, the I2C monitor mode is not 100 % non-intrusive.

Work-around:

When setting the device in monitor mode, enable the ENA_SCL bit in the MMCTRL register to allow clock stretching.

Software code example to enable the ENA_SCL bit:

```
LPC_I2C_MMCTRL |= (1<<1); //Enable ENA_SCL bit
```

In the I2C ISR routine, for the status code related to the slave-transmitter mode, write the value of 0xFF into the DAT register to prevent data corruption. In order to avoid stretching the SCL clock, the data byte can be saved in a buffer and processed in the Main loop. This ensures the SI flag is cleared as fast as possible.

Software code example for the slave-transmitter mode:

```
case 0xA8:     // Own SLA + R has been received, ACK returned
case 0xB0:
case 0xB8:     // data byte in DAT transmitted, ACK received
case 0xC0:     // (last) data byte transmitted, NACK received
case 0xC8:     // last data byte in DAT transmitted, ACK received
    DataByte = LPC_I2C->DATA_BUFFER;//Save data. Data can be process in Main loop
    LPC_I2C->DAT = 0xFF;            // Pretend to shift out 0xFF
    LPC_I2C->CONCLR = 0x08;         // clear flag SI
break;
```


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3.4 RTC.1: RTC Wake up from Deep-sleep requires use of WDOsc

Introduction:

The LPC122x features the ability to wake up from Deep-sleep mode in a self timed manner using the lower power Real Time Clock (RTC). Once RTC is powered and the clock source is configured, a match event will generate an interrupt and wake the LPC122x.

Problem:

In order to wake from Deep-sleep via RTC, the system must be clocked by the WDOsc while in Deep-Sleep.

Work-around:

Prior to entering Deep-sleep the WDOsc must be powered, and the main clock source selection register must source the main clock with the WDOsc. The WDOsc must be configured to use the lowest operating frequency by selecting the 0.5 MHz input (FREQSEL) and post divide value of 64 (DIVSEL). The Deep-sleep mode configuration register must be written with values corresponding to the "WD oscillator on" column in Table 44 of the User Manual. Refer to the section "Deep-sleep mode" in the Power Management section of the System Control chapter of the User Manual for additional details and restrictions on Deep-sleep.

4. AC/DC deviations detail

4.1 n/a

5. Errata notes detail

5.1 n/a

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