LPC11E3x

32-bit ARM Cortex-M0 microcontroller; up to 128 kB flash; up to 12 kB SRAM and 4 kB EEPROM; USART

Rev. 2.3 — 11 September 2014 Product data sheet

1. General description

The LPC11E3x are an ARM Cortex-M0 based, low-cost 32-bit MCU, designed for 8/16-bit microcontroller applications, offering performance, low power, simple instruction set and memory addressing together with reduced code size compared to existing 8/16-bit architectures.

The LPC11E3x operate at CPU frequencies of up to 50 MHz.

The peripheral complement of the LPC11E3x includes up to 128 kB of flash memory, up to 12 kB of SRAM data memory and 4 kB EEPROM, one Fast-mode Plus I^2C-bus interface, one RS-485/EIA-485 USART with support for synchronous mode and smart card interface, two SSP interfaces, four general purpose counter/timers, a 10-bit ADC, and up to 54 general purpose I/O pins.

The I/O Handler is a software library-supported hardware engine that can be used to add performance, connectivity and flexibility to system designs. It is available on the LPC11E37HFBD64/401. The I/O Handler can emulate serial interfaces such as UART, I^2C, and I^2S with no or very low additional CPU load and can off-load the CPU by performing processing-intensive functions like DMA transfers in hardware. Software libraries for multiple I/O Handler applications are available on http://www.LPCware.com.

2. Features and benefits

- System:
  - ARM Cortex-M0 processor, running at frequencies of up to 50 MHz.
  - ARM Cortex-M0 built-in Nested Vectored Interrupt Controller (NVIC).
  - Non Maskable Interrupt (NMI) input selectable from several input sources.
  - System tick timer.
- Memory:
  - Up to 128 kB on-chip flash program memory with sector (4 kB) and page erase (256 byte) access.
  - 4 kB on-chip EEPROM data memory; byte erasable and byte programmable; on-chip API support.
  - 12 kB SRAM data memory.
  - 16 kB boot ROM.
  - In-System Programming (ISP) and In-Application Programming (IAP) via on-chip bootloader software.
  - ROM-based 32-bit integer division routines.

- Debug options:
  - Standard JTAG (Joint Test Action Group) test interface for BSDL (Boundary Scan Description Language).
  - Serial Wire Debug.
- Digital peripherals:
  - Up to 54 General Purpose I/O (GPIO) pins with configurable pull-up/pull-down resistors, repeater mode, and open-drain mode.
  - Up to 8 GPIO pins can be selected as edge and level sensitive interrupt sources.
  - Two GPIO grouped interrupt modules enable an interrupt based on a programmable pattern of input states of a group of GPIO pins.
  - High-current source output driver (20 mA) on one pin.
  - High-current sink driver (20 mA) on true open-drain pins.
  - Four general purpose counter/timers with a total of up to 8 capture inputs and 13 match outputs.
  - Programmable Windowed WatchDog Timer (WWDT) with a dedicated, internal low-power WatchDog Oscillator (WDO).
- Analog peripherals:
  - 10-bit ADC with input multiplexing among eight pins.
- Serial interfaces:
  - USART with fractional baud rate generation, internal FIFO, a full modem control handshake interface, and support for RS-485/9-bit mode and synchronous mode. USART supports an asynchronous smart card interface (ISO 7816-3).
  - Two SSP controllers with FIFO and multi-protocol capabilities.
  - I^2C-bus interface supporting the full I^2C-bus specification and Fast-mode Plus with a data rate of up to 1 Mbit/s with multiple address recognition and monitor mode.
- I/O Handler for hardware emulation of serial interfaces and DMA; supported through software libraries.(LPC11E37HFBD64/401 only.)
- Clock generation:
  - Crystal Oscillator with an operating range of 1 MHz to 25 MHz (system oscillator).
  - 12 MHz high-frequency Internal RC oscillator (IRC) that can optionally be used as a system clock.
  - Internal low-power, low-frequency WatchDog Oscillator (WDO) with programmable frequency output.
  - PLL allows CPU operation up to the maximum CPU rate with the system oscillator or the IRC as clock sources.
  - Clock output function with divider that can reflect the crystal oscillator, the main clock, the IRC, or the watchdog oscillator.
- Power control:
  - Integrated PMU (Power Management Unit) to minimize power consumption during Sleep, Deep-sleep, Power-down, and Deep power-down modes.
  - Power profiles residing in boot ROM provide optimized performance and minimized power consumption for any given application through one simple function call.
  - Four reduced power modes: Sleep, Deep-sleep, Power-down, and Deep power-down.
  - Processor wake-up from Deep-sleep and Power-down modes via reset, selectable GPIO pins, or the watchdog interrupt.
  - Processor wake-up from Deep power-down mode using one special function pin.

All information provided in this document is subject to legal disclaimers.

© NXP Semiconductors N.V. 2014. All rights reserved.

- Power-On Reset (POR).
- Brownout detect with four separate thresholds for interrupt and forced reset.

- Unique device serial number for identification.
- Single 3.3 V power supply (1.8 V to 3.6 V).
- Temperature range −40 °C to +85 °C.
- Available as LQFP64, LQFP48, and HVQFN33 packages.

3. Applications

- Consumer peripherals
- Medical
- Handheld scanners
- Industrial control

4. Ordering information

Table 1. Ordering information

Type number	Package		
	Name	Description	Version
LPC11E35FHI33/501	HVQFN33	plastic thermal enhanced very thin quad flat package; no leads; 33 terminals; body 5 × 5 × 0.85 mm	n/a
LPC11E36FBD64/501	LQFP64	plastic low profile quad flat package; 64 leads; body 10 × 10 × 1.4 mm	SOT314-2
LPC11E36FHN33/501	HVQFN33	plastic thermal enhanced very thin quad flat package; no leads; 33 terminals; body 7 × 7 × 0.85 mm	n/a
LPC11E37FBD48/501	LQFP48	plastic low profile quad flat package; 48 leads; body 7 × 7 × 1.4 mm	SOT313-2
LPC11E37FBD64/501	LQFP64	plastic low profile quad flat package; 64 leads; body 10 × 10 × 1.4 mm	SOT314-2
LPC11E37HFBD64/401	LQFP64	plastic low profile quad flat package; 64 leads; body 10 × 10 × 1.4 mm	SOT314-2

All information provided in this document is subject to legal disclaimers.

© NXP Semiconductors N.V. 2014. All rights reserved.

4.1 Ordering options

Table 2. Ordering options

Type number	Flash in kB	EEPROM in kB	SRAM0 in kB	SRAM2 in kB	SRAM1 in kB[1]	Total SRAM in kB	I/O Handler	USART	I²C-bus FM+	SSP	ADC channels	GPIO pins
LPC11E35FHI33/501	64	4	8	2	2[1]	12	no	1	1	2	8	26
LPC11E36FBD64/501	96	4	8	2	2[1]	12	no	1	1	2	8	54
LPC11E36FHN33/501	96	4	8	2	2[1]	12	no	1	1	2	8	28
LPC11E37FBD48/501	128	4	8	2	2[1]	12	no	1	1	2	8	40
LPC11E37FBD64/501	128	4	8	2	2[1]	12	no	1	1	2	8	54
LPC11E37HFBD64/401	128	4	8	2	2[2]	10	yes	1	1	2	8	54

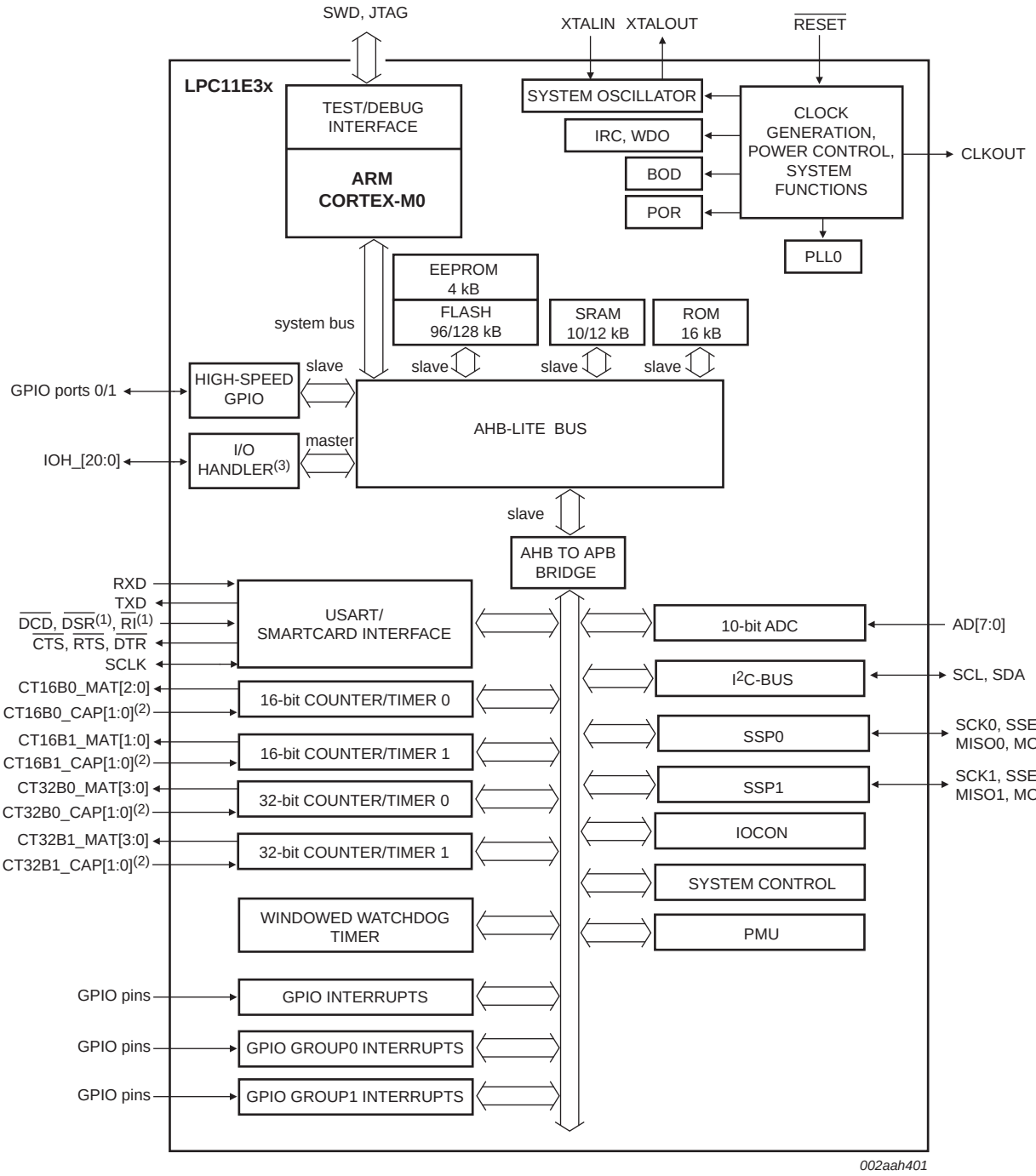
[1] For general-purpose use.

[2] For I/O Handler use only.

All information provided in this document is subject to legal disclaimers.

© NXP Semiconductors N.V. 2014. All rights reserved.

5. Block diagram



(1) Not available on HVQFN33 packages.

(2) CT16B0_CAP1, CT16B1_CAP1 available on LQFP64 packages only; CT32B0_CAP1 available LQFP48, and LQFP64 packages only; CT32B1_CAP1 available in LQFP64 packages only.

(3) LPC11E37HFBD64/401 only.

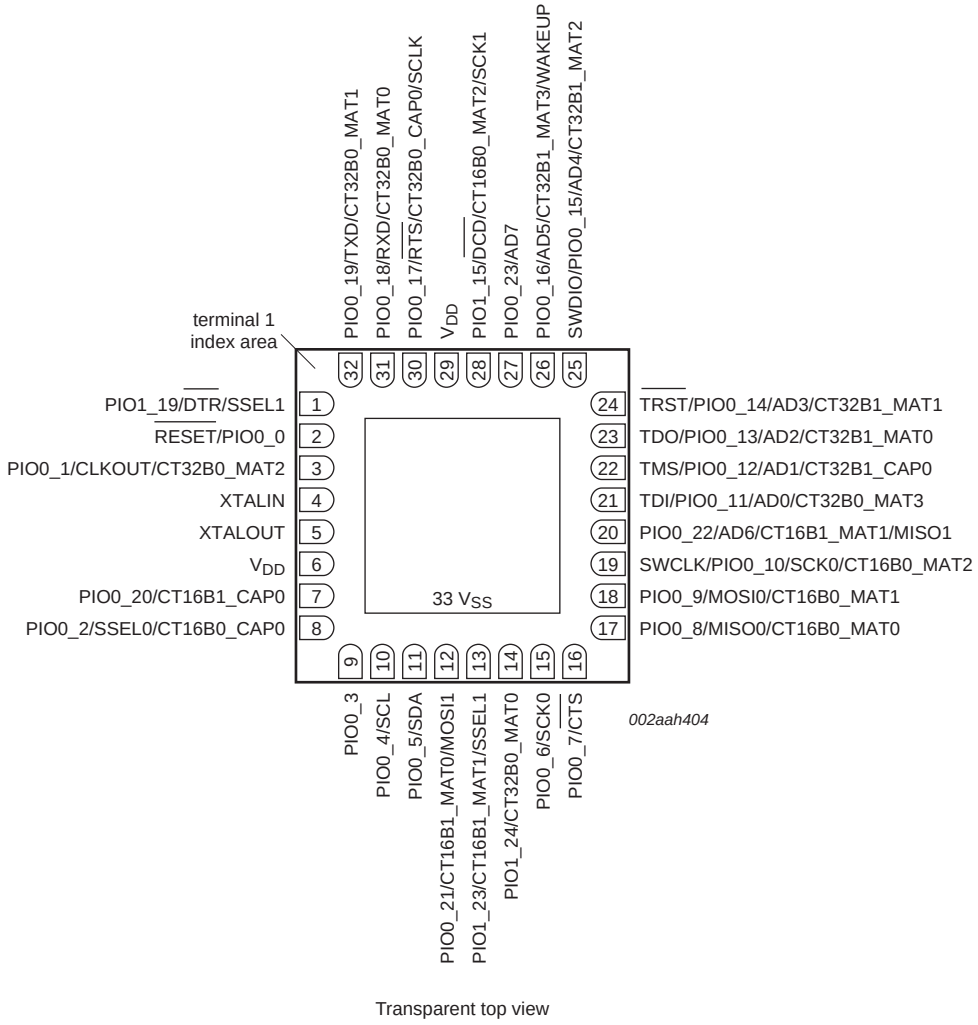
Fig 1. Block diagram

All information provided in this document is subject to legal disclaimers.

© NXP Semiconductors N.V. 2014. All rights reserved.

6. Pinning information

6.1 Pinning



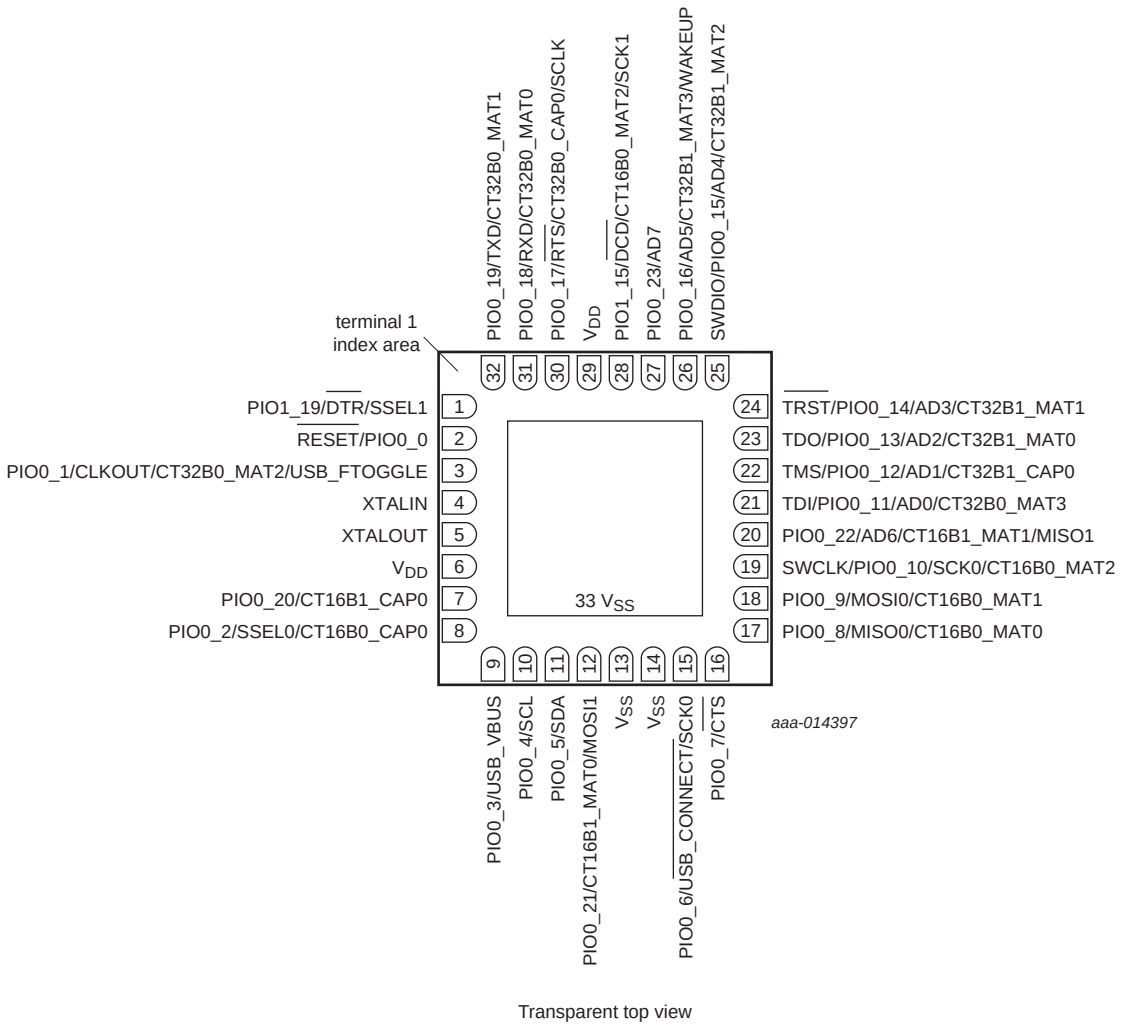
Transparent top view

For parts LPC11E36FHN33/501

Fig 2. Pin configuration (HVQFN33, 7x7)

All information provided in this document is subject to legal disclaimers.

© NXP Semiconductors N.V. 2014. All rights reserved.



Transparent top view

For parts LPC11E35FHI33/501

Fig 3. Pin configuration (HVQFN33, 5x5)

All information provided in this document is subject to legal disclaimers.

© NXP Semiconductors N.V. 2014. All rights reserved.

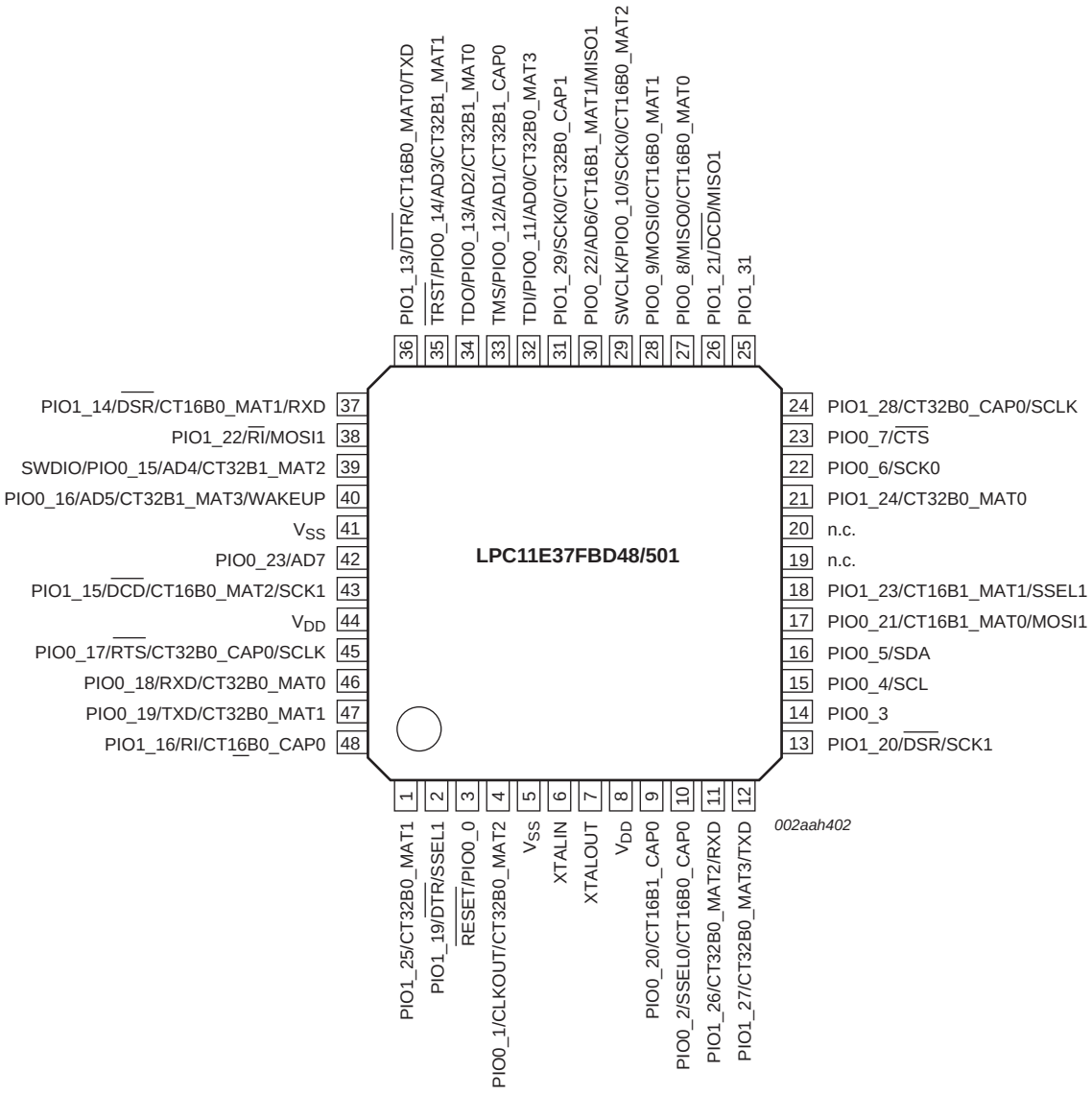
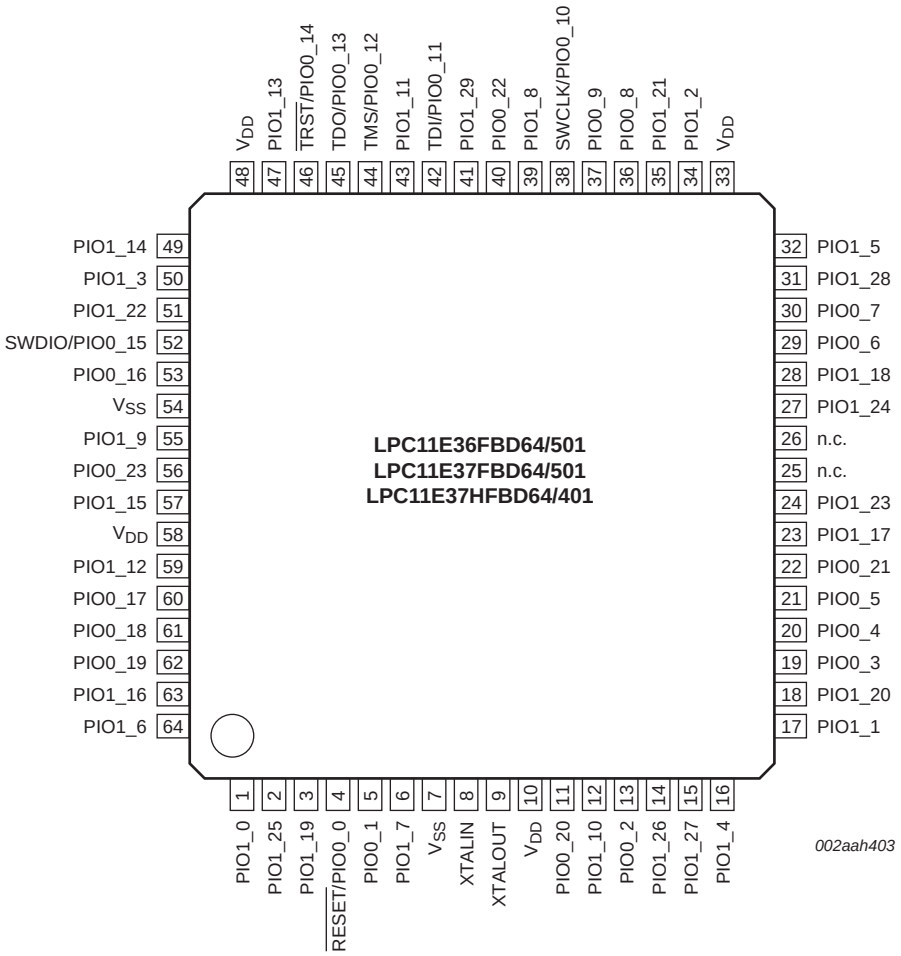


Fig 4. Pin configuration (LQFP48)

All information provided in this document is subject to legal disclaimers.

© NXP Semiconductors N.V. 2014. All rights reserved.



See Table 3 for the full pin name.

Fig 5. Pin configuration (LQFP64)

All information provided in this document is subject to legal disclaimers.

© NXP Semiconductors N.V. 2014. All rights reserved.

6.2 Pin description

Table 3 shows all pins and their assigned digital or analog functions in order of the GPIO port number. The default function after reset is listed first. All port pins have internal pull-up resistors enabled after reset except for the true open-drain pins PIO0_4 and PIO0_5.

Every port pin has a corresponding IOCON register for programming the digital or analog function, the pull-up/pull-down configuration, the repeater, and the open-drain modes.

The USART, counter/timer, and SSP functions are available on more than one port pin.

Table 3. Pin description

Symbol	Pin HVQFN33 (5x5)	Pin HVQFN33 (7x7)	Pin LQFP48	Pin LQFP64		Reset state [1]	Type	Description
$\overline{\text{RESET}}$/PIO0_0	2	2	3	4	[2]	I; PU	I	**$\overline{\text{RESET}}$ —** External reset input with 20 ns glitch filter. A LOW-going pulse as short as 50 ns on this pin resets the device, causing I/O ports and peripherals to take on their default states, and processor execution to begin at address 0. This pin also serves as the debug select input. LOW level selects the JTAG boundary scan. HIGH level selects the ARM SWD debug mode.
						-	I/O	**PIO0_0 —** General purpose digital input/output pin.
PIO0_1/CLKOUT/ CT32B0_MAT2	3	3	4	5	[3]	I; PU	I/O	**PIO0_1 —** General purpose digital input/output pin. A LOW level on this pin during reset starts the ISP command handler.
						-	O	**CLKOUT —** Clockout pin.
						-	O	**CT32B0_MAT2 —** Match output 2 for 32-bit timer 0.
PIO0_2/SSEL0/ CT16B0_CAP0/IOH_0	8	8	10	13	[3]	I; PU	I/O	**PIO0_2 —** General purpose digital input/output pin.
						-	I/O	**SSEL0 —** Slave select for SSP0.
						-	I	**CT16B0_CAP0 —** Capture input 0 for 16-bit timer 0.
						-	I/O	**IOH_0 —** I/O Handler input/output 0. LPC11E37HFBD64/401 only.
PIO0_3/R/IOH_1	9	9	14	19	[3]	I; PU	I/O	**PIO0_3 —** General purpose digital input/output pin.
						-	-	**R —** Reserved.
						-	I/O	**IOH_1 —** I/O Handler input/output 1. LPC11E37HFBD64/401 only.

All information provided in this document is subject to legal disclaimers.

© NXP Semiconductors N.V. 2014. All rights reserved.

Table 3. Pin description

Symbol	Pin HVQFN33 (5x5)	Pin HVQFN33 (7x7)	Pin LQFP48	Pin LQFP64		Reset state [1]	Type	Description
PIO0_4/SCL/IOH_2	10	10	15	20	[4]	I; IA	I/O	**PIO0_4 —** General purpose digital input/output pin (open-drain).
						-	I/O	**SCL —** I^2C-bus clock input/output (open-drain). High-current sink only if I^2C Fast-mode Plus is selected in the I/O configuration register.
						-	I/O	**IOH_2 —** I/O Handler input/output 2. LPC11E37HFBD64/401 only.
PIO0_5/SDA/IOH_3	11	11	16	21	[4]	I; IA	I/O	**PIO0_5 —** General purpose digital input/output pin (open-drain).
						-	I/O	**SDA —** I^2C-bus data input/output (open-drain). High-current sink only if I^2C Fast-mode Plus is selected in the I/O configuration register.
						-	I/O	**IOH_3 —** I/O Handler input/output 3. LPC11E37HFBD64/401 only.
PIO0_6/R/ SCK0/IOH_4	15	15	22	29	[3]	I; PU	I/O	**PIO0_6 —** General purpose digital input/output pin.
						-	-	**R —** Reserved.
						-	I/O	**SCK0 —** Serial clock for SSP0.
						-	I/O	**IOH_4 —** I/O Handler input/output 4. LPC11E37HFBD64/401 only.
PIO0_7/$\overline{\text{CTS}}$/IOH_5	16	16	23	30	[5]	I; PU	I/O	**PIO0_7 —** General purpose digital input/output pin (high-current output driver).
						-	I	**$\overline{\text{CTS}}$ —** Clear To Send input for USART.
						-	I/O	**IOH_5 —** I/O Handler input/output 5. LPC11E37HFBD64/401 only.
PIO0_8/MISO0/ CT16B0_MAT0/R/IOH_6	17	17	27	36	[3]	I; PU	I/O	**PIO0_8 —** General purpose digital input/output pin.
						-	I/O	**MISO0 —** Master In Slave Out for SSP0.
						-	O	**CT16B0_MAT0 —** Match output 0 for 16-bit timer 0.
						-	-	Reserved.
						-	I/O	**IOH_6 —** I/O Handler input/output 6. LPC11E37HFBD64/401 only.
PIO0_9/MOSI0/ CT16B0_MAT1/R/IOH_7	18	18	28	37	[3]	I; PU	I/O	**PIO0_9 —** General purpose digital input/output pin.
						-	I/O	**MOSI0 —** Master Out Slave In for SSP0.
						-	O	**CT16B0_MAT1 —** Match output 1 for 16-bit timer 0.
						-	-	Reserved.
						-	I/O	**IOH_7 —** I/O Handler input/output 7. LPC11E37HFBD64/401 only.

All information provided in this document is subject to legal disclaimers.

© NXP Semiconductors N.V. 2014. All rights reserved.

Table 3. Pin description

Symbol	Pin HVQFN33 (5x5)	Pin HVQFN33 (7x7)	Pin LQFP48	Pin LQFP64		Reset state [1]	Type	Description
SWCLK/PIO0_10/SCK0/ CT16B0_MAT2	19	19	29	38	[3]	I; PU	I	**SWCLK —** Serial wire clock and test clock TCK for JTAG interface.
						-	I/O	**PIO0_10 —** General purpose digital input/output pin.
						-	O	**SCK0 —** Serial clock for SSP0.
						-	O	**CT16B0_MAT2 —** Match output 2 for 16-bit timer 0.
TDI/PIO0_11/AD0/ CT32B0_MAT3	21	21	32	42	[6]	I; PU	I	**TDI —** Test Data In for JTAG interface.
						-	I/O	**PIO0_11 —** General purpose digital input/output pin.
						-	I	**AD0 —** A/D converter, input 0.
						-	O	**CT32B0_MAT3 —** Match output 3 for 32-bit timer 0.
TMS/PIO0_12/AD1/ CT32B1_CAP0	22	22	33	44	[6]	I; PU	I	**TMS —** Test Mode Select for JTAG interface.
						-	I/O	**PIO_12 —** General purpose digital input/output pin.
						-	I	**AD1 —** A/D converter, input 1.
						-	I	**CT32B1_CAP0 —** Capture input 0 for 32-bit timer 1.
TDO/PIO0_13/AD2/ CT32B1_MAT0	23	23	34	45	[6]	I; PU	O	**TDO —** Test Data Out for JTAG interface.
						-	I/O	**PIO0_13 —** General purpose digital input/output pin.
						-	I	**AD2 —** A/D converter, input 2.
						-	O	**CT32B1_MAT0 —** Match output 0 for 32-bit timer 1.
$\overline{\text{TRST}}$/PIO0_14/AD3/ CT32B1_MAT1	24	24	35	46	[6]	I; PU	I	**$\overline{\text{TRST}}$ —** Test Reset for JTAG interface.
						-	I/O	**PIO0_14 —** General purpose digital input/output pin.
						-	I	**AD3 —** A/D converter, input 3.
						-	O	**CT32B1_MAT1 —** Match output 1 for 32-bit timer 1.
SWDIO/PIO0_15/AD4/ CT32B1_MAT2	25	25	39	52	[6]	I; PU	I/O	**SWDIO —** Serial wire debug input/output.
						-	I/O	**PIO0_15 —** General purpose digital input/output pin.
						-	I	**AD4 —** A/D converter, input 4.
						-	O	**CT32B1_MAT2 —** Match output 2 for 32-bit timer 1.

All information provided in this document is subject to legal disclaimers.

© NXP Semiconductors N.V. 2014. All rights reserved.

Table 3. Pin description

Symbol	Pin HVQFN33 (5x5)	Pin HVQFN33 (7x7)	Pin LQFP48	Pin LQFP64		Reset state [1]	Type	Description
PIO0_16/AD5/ CT32B1_MAT3/IOH_8/ WAKEUP	26	26	40	53	[6]	I; PU	I/O	**PIO0_16 —** General purpose digital input/output pin.
						-	I	**AD5 —** A/D converter, input 5.
						-	O	**CT32B1_MAT3 —** Match output 3 for 32-bit timer 1.
						-	I/O	**IOH_8 —** I/O Handler input/output 8. LPC11E37HFBD64/401 only.
						-	I	**WAKEUP —** Deep power-down mode wake-up pin with 20 ns glitch filter. Pull this pin HIGH externally before entering Deep power-down mode, then pull LOW to exit Deep power-down mode. A LOW-going pulse as short as 50 ns wakes up the part.
PIO0_17/$\overline{\text{RTS}}$/ CT32B0_CAP0/SCLK	30	30	45	60	[3]	I; PU	I/O	**PIO0_17 —** General purpose digital input/output pin.
						-	O	**$\overline{\text{RTS}}$ —** Request To Send output for USART.
						-	I	**CT32B0_CAP0 —** Capture input 0 for 32-bit timer 0.
						-	I/O	**SCLK —** Serial clock input/output for USART in synchronous mode.
PIO0_18/RXD/ CT32B0_MAT0	31	31	46	61	[3]	I; PU	I/O	**PIO0_18 —** General purpose digital input/output pin.
						-	I	**RXD —** Receiver input for USART. Used in UART ISP mode.
						-	O	**CT32B0_MAT0 —** Match output 0 for 32-bit timer 0.
PIO0_19/TXD/ CT32B0_MAT1	32	32	47	62	[3]	I; PU	I/O	**PIO0_19 —** General purpose digital input/output pin.
						-	O	**TXD —** Transmitter output for USART. Used in UART ISP mode.
						-	O	**CT32B0_MAT1 —** Match output 1 for 32-bit timer 0.
PIO0_20/CT16B1_CAP0	7	7	9	11	[3]	I; PU	I/O	**PIO0_20 —** General purpose digital input/output pin.
						-	I	**CT16B1_CAP0 —** Capture input 0 for 16-bit timer 1.
PIO0_21/CT16B1_MAT0/ MOSI1	12	12	17	22	[3]	I; PU	I/O	**PIO0_21 —** General purpose digital input/output pin.
						-	O	**CT16B1_MAT0 —** Match output 0 for 16-bit timer 1.
						-	I/O	**MOSI1 —** Master Out Slave In for SSP1.

All information provided in this document is subject to legal disclaimers.

© NXP Semiconductors N.V. 2014. All rights reserved.

Table 3. Pin description

Symbol	Pin HVQFN33 (5x5)	Pin HVQFN33 (7x7)	Pin LQFP48	Pin LQFP64		Reset state [1]	Type	Description
PIO0_22/AD6/ CT16B1_MAT1/MISO1	20	20	30	40	[6]	I; PU	I/O	**PIO0_22 —** General purpose digital input/output pin.
						-	I	**AD6 —** A/D converter, input 6.
						-	O	**CT16B1_MAT1 —** Match output 1 for 16-bit timer 1.
						-	I/O	**MISO1 —** Master In Slave Out for SSP1.
PIO0_23/AD7/IOH_9	27	27	42	56	[6]	I; PU	I/O	**PIO0_23 —** General purpose digital input/output pin.
						-	I	**AD7 —** A/D converter, input 7.
						-	I/O	**IOH_9 —** I/O Handler input/output 9. LPC11E37HFBD64/401 only.
PIO1_0/CT32B1_MAT0/ IOH_10	-	-	-	1	[3]	I; PU	I/O	**PIO1_0 —** General purpose digital input/output pin.
						-	O	**CT32B1_MAT0 —** Match output 0 for 32-bit timer 1.
						-	I/O	**IOH_10 —** I/O Handler input/output 10. LPC11E37HFBD64/401 only.
PIO1_1/CT32B1_MAT1/ IOH_11	-	-	-	17	[3]	I; PU	I/O	**PIO1_1 —** General purpose digital input/output pin.
						-	O	**CT32B1_MAT1 —** Match output 1 for 32-bit timer 1.
						-	I/O	**IOH_11 —** I/O Handler input/output 11. LPC11E37HFBD64/401 only.
PIO1_2/CT32B1_MAT2/ IOH_12	-	-	-	34	[3]	I; PU	I/O	**PIO1_2 —** General purpose digital input/output pin.
						-	O	**CT32B1_MAT2 —** Match output 2 for 32-bit timer 1.
						-	I/O	**IOH_12 —** I/O Handler input/output 12. LPC11E37HFBD64/401 only.
PIO1_3/CT32B1_MAT3/ IOH_13	-	-	-	50	[3]	I; PU	I/O	**PIO1_3 —** General purpose digital input/output pin.
						-	O	**CT32B1_MAT3 —** Match output 3 for 32-bit timer 1.
						-	I/O	**IOH_13 —** I/O Handler input/output 13. (LPC11E37HFBD64/401 only.)
PIO1_4/CT32B1_CAP0/ IOH_14	-	-	-	16	[3]	I; PU	I/O	**PIO1_4 —** General purpose digital input/output pin.
						-	I	**CT32B1_CAP0 —** Capture input 0 for 32-bit timer 1.
						-	I/O	**IOH_14 —** I/O Handler input/output 14. (LPC11E37HFBD64/401 only.)

All information provided in this document is subject to legal disclaimers.

© NXP Semiconductors N.V. 2014. All rights reserved.

Table 3. Pin description

Symbol	Pin HVQFN33 (5x5)	Pin HVQFN33 (7x7)	Pin LQFP48	Pin LQFP64		Reset state [1]	Type	Description
PIO1_5/CT32B1_CAP1/ IOH_15	-	-	-	32	[3]	I; PU	I/O	**PIO1_5 —** General purpose digital input/output pin.
						-	I	**CT32B1_CAP1 —** Capture input 1 for 32-bit timer 1.
						-	I/O	**IOH_15 —** I/O Handler input/output 15. (LPC11E37HFBD64/401 only.)
PIO1_6/IOH_16	-	-	-	64	[3]	I; PU	I/O	**PIO1_6 —** General purpose digital input/output pin.
						-	I/O	**IOH_16 —** I/O Handler input/output 16. (LPC11E37HFBD64/401 only.)
PIO1_7/IOH_17	-	-	-	6	[3]	I; PU	I/O	**PIO1_7 —** General purpose digital input/output pin.
						-	I/O	**IOH_17 —** I/O Handler input/output 17. (LPC11E37HFBD64/401 only.)
PIO1_8/IOH_18	-	-	-	39	[3]	I; PU	I/O	**PIO1_8 —** General purpose digital input/output pin.
						-	I/O	**IOH_18 —** I/O Handler input/output 18. (LPC11E37HFBD64/401 only.)
PIO1_9	-	-	-	55	[3]	I; PU	I/O	**PIO1_9 —** General purpose digital input/output pin.
PIO1_10	-	-	-	12	[3]	I; PU	I/O	**PIO1_10 —** General purpose digital input/output pin.
PIO1_11	-	-	-	43	[3]	I; PU	I/O	**PIO1_11 —** General purpose digital input/output pin.
PIO1_12	-	-	-	59	[3]	I; PU	I/O	**PIO1_12 —** General purpose digital input/output pin.
PIO1_13/$\overline{\text{DTR}}$/ CT16B0_MAT0/TXD	-	-	36	47	[3]	I; PU	I/O	**PIO1_13 —** General purpose digital input/output pin.
						-	O	**$\overline{\text{DTR}}$ —** Data Terminal Ready output for USART.
						-	O	**CT16B0_MAT0 —** Match output 0 for 16-bit timer 0.
						-	O	**TXD —** Transmitter output for USART.
PIO1_14/$\overline{\text{DSR}}$/ CT16B0_MAT1/RXD	-	-	37	49	[3]	I; PU	I/O	**PIO1_14 —** General purpose digital input/output pin.
						-	I	**$\overline{\text{DSR}}$ —** Data Set Ready input for USART.
						-	O	**CT16B0_MAT1 —** Match output 1 for 16-bit timer 0.
						-	I	**RXD —** Receiver input for USART.

All information provided in this document is subject to legal disclaimers.

© NXP Semiconductors N.V. 2014. All rights reserved.

Table 3. Pin description

Symbol	Pin HVQFN33 (5x5)	Pin HVQFN33 (7x7)	Pin LQFP48	Pin LQFP64		Reset state [1]	Type	Description
PIO1_15/$\overline{\text{DCD}}$/ CT16B0_MAT2/SCK1	28	28	43	57	[3]	I; PU	I/O	**PIO1_15 —** General purpose digital input/output pin.
							I	**$\overline{\text{DCD}}$ —** Data Carrier Detect input for USART.
						-	O	**CT16B0_MAT2 —** Match output 2 for 16-bit timer 0.
						-	I/O	**SCK1 —** Serial clock for SSP1.
PIO1_16/$\overline{\text{RI}}$/ CT16B0_CAP0	-	-	48	63	[3]	I; PU	I/O	**PIO1_16 —** General purpose digital input/output pin.
						-	I	**$\overline{\text{RI}}$ —** Ring Indicator input for USART.
						-	I	**CT16B0_CAP0 —** Capture input 0 for 16-bit timer 0.
PIO1_17/CT16B0_CAP1/ RXD	-	-	-	23	[3]	I; PU	I/O	**PIO1_17 —** General purpose digital input/output pin.
						-	I	**CT16B0_CAP1 —** Capture input 1 for 16-bit timer 0.
						-	I	**RXD —** Receiver input for USART.
PIO1_18/CT16B1_CAP1/ TXD	-	-	-	28	[3]	I; PU	I/O	**PIO1_18 —** General purpose digital input/output pin.
						-	I	**CT16B1_CAP1 —** Capture input 1 for 16-bit timer 1.
						-	O	**TXD —** Transmitter output for USART.
PIO1_19/$\overline{\text{DTR}}$/SSEL1	1	1	2	3	[3]	I; PU	I/O	**PIO1_19 —** General purpose digital input/output pin.
						-	O	**$\overline{\text{DTR}}$ —** Data Terminal Ready output for USART.
						-	I/O	**SSEL1 —** Slave select for SSP1.
PIO1_20/$\overline{\text{DSR}}$/SCK1	-	-	13	18	[3]	I; PU	I/O	**PIO1_20 —** General purpose digital input/output pin.
						-	I	**$\overline{\text{DSR}}$ —** Data Set Ready input for USART.
						-	I/O	**SCK1 —** Serial clock for SSP1.
PIO1_21/$\overline{\text{DCD}}$/MISO1	-	-	26	35	[3]	I; PU	I/O	**PIO1_21 —** General purpose digital input/output pin.
						-	I	**$\overline{\text{DCD}}$ —** Data Carrier Detect input for USART.
						-	I/O	**MISO1 —** Master In Slave Out for SSP1.
PIO1_22/$\overline{\text{RI}}$/MOSI1	-	-	38	51	[3]	I; PU	I/O	**PIO1_22 —** General purpose digital input/output pin.
						-	I	**$\overline{\text{RI}}$ —** Ring Indicator input for USART.
						-	I/O	**MOSI1 —** Master Out Slave In for SSP1.

All information provided in this document is subject to legal disclaimers.

© NXP Semiconductors N.V. 2014. All rights reserved.

Table 3. Pin description

Symbol	Pin HVQFN33 (5x5)	Pin HVQFN33 (7x7)	Pin LQFP48	Pin LQFP64		Reset state [1]	Type	Description
PIO1_23/CT16B1_MAT1/ SSEL1	-	13	18	24	[3]	I; PU	I/O	**PIO1_23 —** General purpose digital input/output pin.
						-	O	**CT16B1_MAT1 —** Match output 1 for 16-bit timer 1.
						-	I/O	**SSEL1 —** Slave select for SSP1.
PIO1_24/CT32B0_MAT0	-	14	21	27	[3]	I; PU	I/O	**PIO1_24 —** General purpose digital input/output pin.
						-	O	**CT32B0_MAT0 —** Match output 0 for 32-bit timer 0.
PIO1_25/CT32B0_MAT1	-	-	1	2	[3]	I; PU	I/O	**PIO1_25 —** General purpose digital input/output pin.
						-	O	**CT32B0_MAT1 —** Match output 1 for 32-bit timer 0.
PIO1_26/CT32B0_MAT2/ RXD/IOH_19	-	-	11	14	[3]	I; PU	I/O	**PIO1_26 —** General purpose digital input/output pin.
						-	O	**CT32B0_MAT2 —** Match output 2 for 32-bit timer 0.
						-	I	**RXD —** Receiver input for USART.
						-	I/O	**IOH_19 —** I/O Handler input/output 18. (LPC11E37HFBD64/401 only.)
PIO1_27/CT32B0_MAT3/ TXD/IOH_20	-	-	12	15	[3]	I; PU	I/O	**PIO1_27 —** General purpose digital input/output pin.
						-	O	**CT32B0_MAT3 —** Match output 3 for 32-bit timer 0.
						-	O	**TXD —** Transmitter output for USART.
						-	I/O	**IOH_20 —** I/O Handler input/output 20. (LPC11E37HFBD64/401 only.)
PIO1_28/CT32B0_CAP0/ SCLK	-	-	24	31	[3]	I; PU	I/O	**PIO1_28 —** General purpose digital input/output pin.
						-	I	**CT32B0_CAP0 —** Capture input 0 for 32-bit timer 0.
						-	I/O	**SCLK —** Serial clock input/output for USART in synchronous mode.
PIO1_29/SCK0/ CT32B0_CAP1	-	-	31	41	[3]	I; PU	I/O	**PIO1_29 —** General purpose digital input/output pin.
						-	I/O	**SCK0 —** Serial clock for SSP0.
						-	I	**CT32B0_CAP1 —** Capture input 1 for 32-bit timer 0.
PIO1_31	-	-	25	-	[3]	I; PU	I/O	**PIO1_31 —** General purpose digital input/output pin.
n.c.	-	-	19	25		-	-	Not connected.
n.c.	-	-	20	26		-	-	Not connected.

All information provided in this document is subject to legal disclaimers.

© NXP Semiconductors N.V. 2014. All rights reserved.

Table 3. Pin description

Symbol	Pin HVQFN33 (5x5)	Pin HVQFN33 (7x7)	Pin LQFP48	Pin LQFP64		Reset state [1]	Type	Description
XTALIN	4	4	6	8	[7]	-	-	Input to the oscillator circuit and internal clock generator circuits. Input voltage must not exceed 1.8 V.
XTALOUT	5	5	7	9	[7]	-	-	Output from the oscillator amplifier.
V_{DD}	6; 29	6; 29	8; 44	10; 33; 48; 58		-	-	Supply voltage to the internal regulator, the external rail, and the ADC. Also used as the ADC reference voltage.
V_{SS}	33; 13; 14	33	5; 41	7; 54		-	-	Ground.

[1] Pin state at reset for default function: I = Input; O = Output; PU = internal pull-up enabled; IA = inactive, no pull-up/down enabled; F = floating; If the pins are not used, tie floating pins to ground or power to minimize power consumption.

[2] 5 V tolerant pad. $\overline{\text{RESET}}$ functionality is not available in Deep power-down mode. Use the WAKEUP pin to reset the chip and wake up from Deep power-down mode. An external pull-up resistor is required on this pin for the Deep power-down mode. See Figure 29 for the reset pad configuration.

[3] 5 V tolerant pad providing digital I/O functions with configurable pull-up/pull-down resistors and configurable hysteresis (see Figure 28).

[4] I^2C-bus pins compliant with the I^2C-bus specification for I^2C standard mode, I^2C Fast-mode, and I^2C Fast-mode Plus.

[5] 5 V tolerant pad providing digital I/O functions with configurable pull-up/pull-down resistors and configurable hysteresis (see Figure 28); includes high-current output driver.

[6] 5 V tolerant pad providing digital I/O functions with configurable pull-up/pull-down resistors, configurable hysteresis, and analog input. When configured as a ADC input, digital section of the pad is disabled and the pin is not 5 V tolerant (see Figure 28); includes digital input glitch filter.

[7] When the system oscillator is not used, connect XTALIN and XTALOUT as follows: XTALIN can be left floating or can be grounded (grounding is preferred to reduce susceptibility to noise). Leave XTALOUT floating.

7. Functional description

7.1 On-chip flash programming memory

The LPC11E3x contain up to 128 kB on-chip flash program memory. The flash can be programmed using In-System Programming (ISP) or In-Application Programming (IAP) via the on-chip boot loader software.

The flash memory is divided into 4 kB sectors with each sector consisting of 16 pages. Individual pages can be erased using the IAP erase page command.

7.2 EEPROM

The LPC11E3x contain 4 kB of on-chip byte-erasable and byte-programmable EEPROM data memory. The EEPROM can be programmed using In-Application Programming (IAP) via the on-chip boot loader software.

All information provided in this document is subject to legal disclaimers.

© NXP Semiconductors N.V. 2014. All rights reserved.

7.3 SRAM

The LPC11E3x contain a total of 10 kB (LPC11E37HFBD64/401) or 12 kB on-chip static RAM memory.

On the LPC11E37HFBD64/401, the 2 kB SRAM1 region at location 0x2000 0000 to 0x2000 07FFF is used for the I/O Handler software library. Do not use this memory location for data or other user code.

7.4 On-chip ROM

The on-chip ROM contains the boot loader and the following Application Programming Interfaces (APIs):

- In-System Programming (ISP) and In-Application Programming (IAP) support for flash including IAP erase page command.
- IAP support for EEPROM.
- Power profiles for configuring power consumption and PLL settings.
- 32-bit integer division routines.

7.5 Memory map

The LPC11E3x incorporates several distinct memory regions, shown in the following figures. Figure 6 shows the overall map of the entire address space from the user program viewpoint following reset. The interrupt vector area supports address remapping.

The AHB (Advanced High-performance Bus) peripheral area is 2 MB in size and is divided to allow for up to 128 peripherals. The APB (Advanced Peripheral Bus) peripheral area is 512 kB in size and is divided to allow for up to 32 peripherals. Each peripheral of either type is allocated 16 kB of space. This addressing scheme allows simplifying the address decoding for each peripheral.

All information provided in this document is subject to legal disclaimers.

© NXP Semiconductors N.V. 2014. All rights reserved.

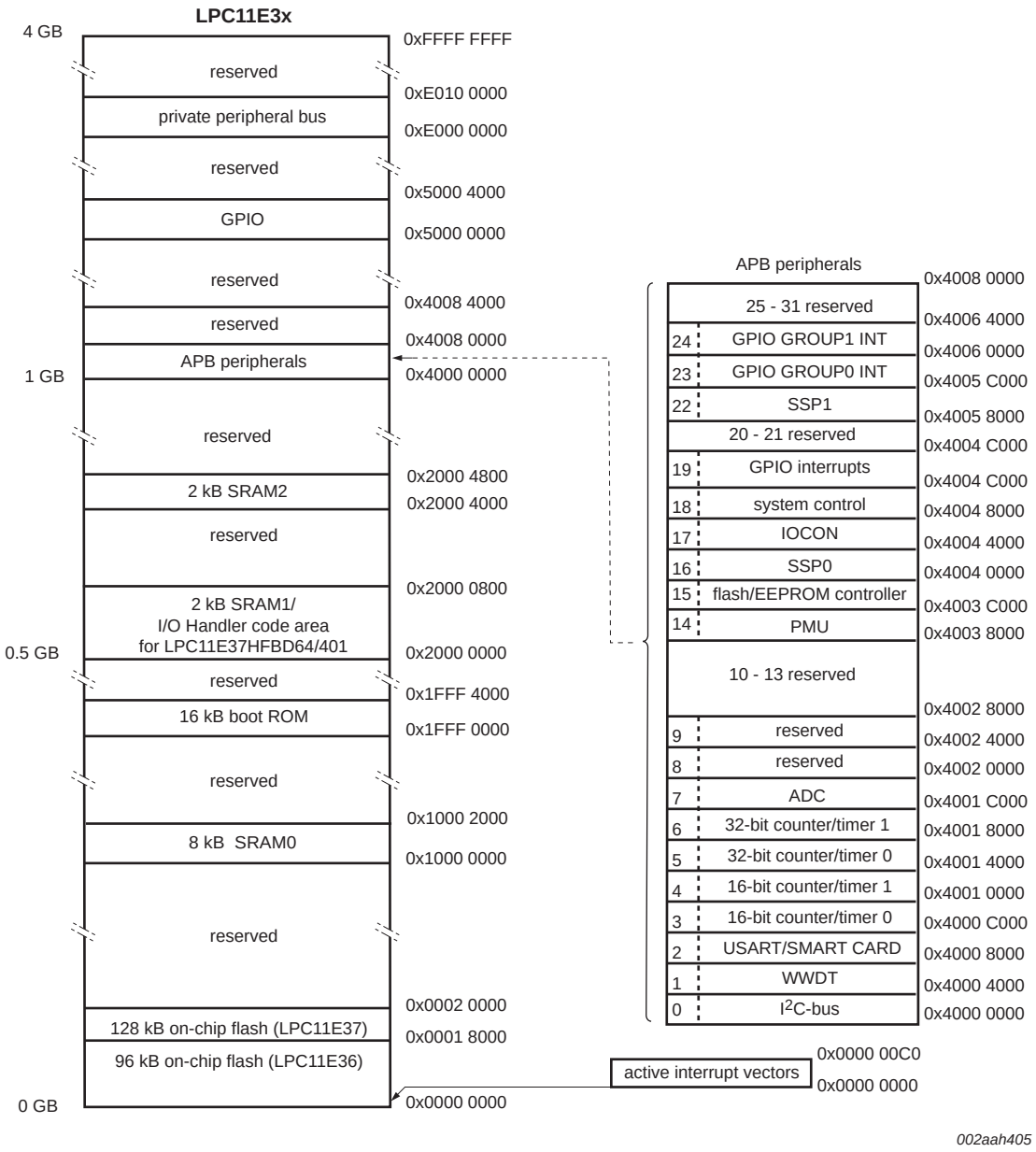


Fig 6. LPC11E3x memory map

7.6 Nested Vectored Interrupt Controller (NVIC)

The Nested Vectored Interrupt Controller (NVIC) is part of the Cortex-M0. The tight coupling to the CPU allows for low interrupt latency and efficient processing of late arriving interrupts.

7.6.1 Features

- Controls system exceptions and peripheral interrupts.
- In the LPC11E3x, the NVIC supports 24 vectored interrupts.

All information provided in this document is subject to legal disclaimers.

© NXP Semiconductors N.V. 2014. All rights reserved.

- Four programmable interrupt priority levels, with hardware priority level masking.
- Software interrupt generation.

7.6.2 Interrupt sources

Each peripheral device has one interrupt line connected to the NVIC but can have several interrupt flags. Individual interrupt flags can also represent more than one interrupt source.

7.7 IOCON block

The IOCON block allows selected pins of the microcontroller to have more than one function. Configuration registers control the multiplexers to allow connection between the pin and the on-chip peripherals.

Connect peripherals to the appropriate pins before activating the peripheral and before enabling any related interrupt. . Activity of any enabled peripheral function that is not mapped to a related pin is treated as undefined.

7.7.1 Features

- Programmable pull-up, pull-down, or repeater mode.
- All GPIO pins (except PIO0_4 and PIO0_5) are pulled up to 3.3 V (V_{DD} = 3.3 V) if their pull-up resistor is enabled.
- Programmable pseudo open-drain mode.
- Programmable 10 ns glitch filter on pins PIO0_22, PIO0_23, and PIO0_11 to PIO0_16. The glitch filter is turned on by default.
- Programmable hysteresis.
- Programmable input inverter.

7.8 General-Purpose Input/Output GPIO

The GPIO registers control device pin functions that are not connected to a specific peripheral function. Pins can be dynamically configured as inputs or outputs. Multiple outputs can be set or cleared in one write operation.

LPC11E3x use accelerated GPIO functions:

- GPIO registers are a dedicated AHB peripheral so that the fastest possible I/O timing can be achieved.
- Entire port value can be written in one instruction.

Any GPIO pin providing a digital function can be programmed to generate an interrupt on a level, a rising or falling edge, or both.

The GPIO block consists of three parts:

1. The GPIO ports.
2. The GPIO pin interrupt block to control eight GPIO pins selected as pin interrupts.
3. Two GPIO group interrupt blocks to control two combined interrupts from all GPIO pins.

All information provided in this document is subject to legal disclaimers.

© NXP Semiconductors N.V. 2014. All rights reserved.

7.8.1 Features

- GPIO pins can be configured as input or output by software.
- All GPIO pins default to inputs with interrupt disabled at reset.
- Pin registers allow pins to be sensed and set individually.
- Up to eight GPIO pins can be selected from all GPIO pins to create an edge- or level-sensitive GPIO interrupt request.
- Any pin or pins in each port can trigger a port interrupt.

7.9 I/O Handler (LPC11E37HFBD64/401 only)

The I/O Handler is a software library-supported hardware engine for emulating serial interfaces and DMA. The I/O Handler can emulate serial interfaces such as UART, I^2C, or I^2S with no or very low additional CPU load. The software libraries are available with supporting application notes from NXP (see http://www.LPCware.com.) LPCXpresso, Keil, and IAR IDEs are supported. I/O Handler library code must be executed from the memory area 0x2000 0000 to 0x2000 07FF. This memory is not available for other use.

For application examples, see Section 11.7 “I/O Handler software library applications”.

7.10 USART

The LPC11E3x contains one USART.

The USART includes full modem control, support for synchronous mode, and a smart card interface. The RS-485/9-bit mode allows both software address detection and automatic address detection using 9-bit mode.

The USART uses a fractional baud rate generator. Standard baud rates such as 115200 Bd can be achieved with any crystal frequency above 2 MHz.

7.10.1 Features

- Maximum USART data bit rate of 3.125 Mbit/s.
- 16 byte receive and transmit FIFOs.
- Register locations conform to 16C550 industry standard.
- Receiver FIFO trigger points at 1 B, 4 B, 8 B, and 14 B.
- Built-in fractional baud rate generator covering wide range of baud rates without a need for external crystals of particular values.
- Fractional divider for baud rate control, auto baud capabilities and FIFO control mechanism that enables software flow control implementation.
- Support for RS-485/9-bit mode.
- Support for modem control.
- Support for synchronous mode.
- Includes smart card interface.

All information provided in this document is subject to legal disclaimers.

© NXP Semiconductors N.V. 2014. All rights reserved.

7.11 SSP serial I/O controller

The SSP controllers operate on a SSP, 4-wire SSI, or Microwire bus. It can interact with multiple masters and slaves on the bus. Only a single master and a single slave can communicate on the bus during a given data transfer. The SSP supports full duplex transfers, with frames of 4 bit to 16 bit of data flowing from the master to the slave and from the slave to the master. In practice, often only one of these data flows carries meaningful data.

7.11.1 Features

- Maximum SSP speed of 25 Mbit/s (master) or 4.17 Mbit/s (slave) (in SSP mode).
- Compatible with Motorola SPI (Serial Peripheral Interface), 4-wire Texas Instruments SSI (Serial Synchronous Interface), and National Semiconductor Microwire buses.
- Synchronous serial communication.
- Master or slave operation.
- 8-frame FIFOs for both transmit and receive.
- 4-bit to 16-bit frame.

7.12 I^2C-bus serial I/O controller

The LPC11E3x contain one I^2C-bus controller.

The I^2C-bus is bidirectional for inter-IC control using only two wires: a Serial CLock line (SCL) and a Serial DAta line (SDA). Each device is recognized by a unique address and can operate as either a receiver-only device (e.g., an LCD driver) or a transmitter with the capability to both receive and send information (such as memory). Transmitters and/or receivers can operate in either master or slave mode, depending on whether the chip has to initiate a data transfer or is only addressed. The I^2C-bus is a multi-master bus, and more than one bus master connected to the interface can be controlled the bus.

7.12.1 Features

- The I^2C-interface is an I^2C-bus compliant interface with open-drain pins. The I^2C-bus interface supports Fast-mode Plus with bit rates up to 1 Mbit/s.
- Easy to configure as master, slave, or master/slave.
- Programmable clocks allow versatile rate control.
- Bidirectional data transfer between masters and slaves.
- Multi-master bus (no central master).
- Arbitration between simultaneously transmitting masters without corruption of serial data on the bus.
- Serial clock synchronization allows devices with different bit rates to communicate via one serial bus.
- Serial clock synchronization can be used as a handshake mechanism to suspend and resume serial transfer.
- The I^2C-bus can be used for test and diagnostic purposes.
- The I^2C-bus controller supports multiple address recognition and a bus monitor mode.

All information provided in this document is subject to legal disclaimers.

© NXP Semiconductors N.V. 2014. All rights reserved.

7.13 10-bit ADC

The LPC11E3x contains one ADC. It is a single 10-bit successive approximation ADC with eight channels.

7.13.1 Features

- 10-bit successive approximation ADC.
- Input multiplexing among 8 pins.
- Power-down mode.
- Measurement range 0 V to V_{DD}.
- 10-bit conversion time $\geq$ 2.44 μs (up to 400 kSamples/s).
- Burst conversion mode for single or multiple inputs.
- Optional conversion on transition of input pin or timer match signal.
- Individual result registers for each ADC channel to reduce interrupt overhead.

7.14 General purpose external event counter/timers

The LPC11E3x includes two 32-bit counter/timers and two 16-bit counter/timers. The counter/timer is designed to count cycles of the system derived clock. It can optionally generate interrupts or perform other actions at specified timer values, based on four match registers. Each counter/timer also includes one capture input to trap the timer value when an input signal transitions, optionally generating an interrupt.

7.14.1 Features

- A 32-bit/16-bit timer/counter with a programmable 32-bit/16-bit prescaler.
- Counter or timer operation.
- Up to two capture channels per timer, that can take a snapshot of the timer value when an input signal transitions. A capture event can also generate an interrupt.
- Four match registers per timer that allow:
  - Continuous operation with optional interrupt generation on match.
  - Stop timer on match with optional interrupt generation.
  - Reset timer on match with optional interrupt generation.
- Up to four external outputs corresponding to match registers, with the following capabilities:
  - Set LOW on match.
  - Set HIGH on match.
  - Toggle on match.
  - Do nothing on match.
- The timer and prescaler can be configured to be cleared on a designated capture event. This feature permits easy pulse-width measurement by clearing the timer on the leading edge of an input pulse and capturing the timer value on the trailing edge.

All information provided in this document is subject to legal disclaimers.

© NXP Semiconductors N.V. 2014. All rights reserved.

7.15 System tick timer

The ARM Cortex-M0 includes a system tick timer (SYSTICK) that is intended to generate a dedicated SYSTICK exception at a fixed time interval (typically 10 ms).

7.16 Windowed WatchDog Timer (WWDT)

The purpose of the WWDT is to prevent an unresponsive system state. If software fails to update the watchdog within a programmable time window, the watchdog resets the microcontroller

7.16.1 Features

- Internally resets chip if not periodically reloaded during the programmable time-out period.
- Optional windowed operation requires reload to occur between a minimum and maximum time period, both programmable.
- Optional warning interrupt can be generated at a programmable time before watchdog time-out.
- Software enables the WWDT, but a hardware reset or a watchdog reset/interrupt is required to disable the WWDT.
- Incorrect feed sequence causes reset or interrupt, if enabled.
- Flag to indicate watchdog reset.
- Programmable 24-bit timer with internal prescaler.
- Selectable time period from ($T_{cy(WDCLK)} \times 256 \times 4$) to ($T_{cy(WDCLK)} \times 2^{24} \times 4$) in multiples of $T_{cy(WDCLK)} \times 4$.
- The Watchdog Clock (WDCLK) source can be selected from the IRC or the dedicated watchdog oscillator (WDO). The clock source selection provides a wide range of potential timing choices of watchdog operation under different power conditions.

7.17 Clocking and power control

7.17.1 Integrated oscillators

The LPC11E3x include three independent oscillators: the system oscillator, the Internal RC oscillator (IRC), and the watchdog oscillator. Each oscillator can be used for more than one purpose as required in a particular application.

Following reset, the LPC11E3x operates from the internal RC oscillator until software switches to a different clock source. The IRC allows the system to operate without any external crystal and the bootloader code to operate at a known frequency.

See Figure 7 for an overview of the LPC11E3x clock generation.

All information provided in this document is subject to legal disclaimers.

© NXP Semiconductors N.V. 2014. All rights reserved.

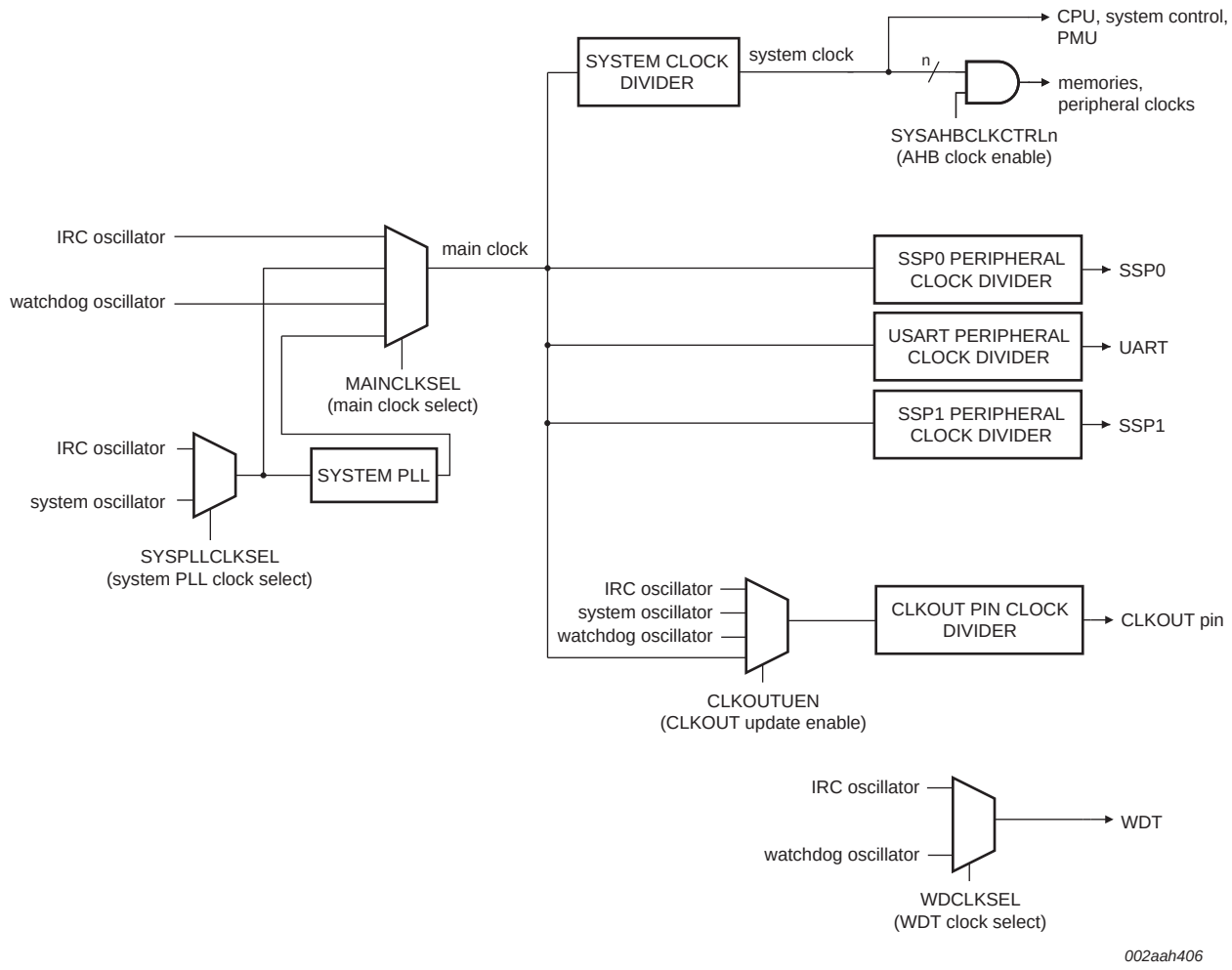


Fig 7. LPC11E3x clocking generation block diagram

7.17.1.1 Internal RC oscillator

The IRC can be used as the clock source for the WDT, and/or as the clock that drives the system PLL and then the CPU. The nominal IRC frequency is 12 MHz.

Upon power-up, any chip reset, or wake-up from Deep power-down mode, the LPC11E3x use the IRC as the clock source. Software can later switch to one of the other available clock sources.

7.17.1.2 System oscillator

The system oscillator can be used as the clock source for the CPU, with or without using the PLL.

The system oscillator operates at frequencies of 1 MHz to 25 MHz. This frequency can be boosted to a higher frequency, up to the maximum CPU operating frequency, by the system PLL.

All information provided in this document is subject to legal disclaimers.

© NXP Semiconductors N.V. 2014. All rights reserved.

7.17.1.3 Watchdog oscillator

The watchdog oscillator can be used as a clock source that directly drives the CPU, the watchdog timer, or the CLKOUT pin. The watchdog oscillator nominal frequency is programmable between 9.4 kHz and 2.3 MHz. The frequency spread over processing and temperature is ±40 % (see also Table 13).

7.17.2 System PLL

The PLL accepts an input clock frequency in the range of 10 MHz to 25 MHz. The input frequency is multiplied up to a high frequency with a Current Controlled Oscillator (CCO). The multiplier can be an integer value from 1 to 32. The CCO operates in the range of 156 MHz to 320 MHz. To support this frequency range, an additional divider keeps the CCO within its frequency range while the PLL is providing the desired output frequency. The output divider can be set to divide by 2, 4, 8, or 16 to produce the output clock. The PLL output frequency must be lower than 100 MHz. Since the minimum output divider value is 2, it is insured that the PLL output has a 50 % duty cycle. The PLL is turned off and bypassed following a chip reset. Software can enable the PLL later. The program must configure and activate the PLL, wait for the PLL to lock, and then connect to the PLL as a clock source. The PLL settling time is 100 μs.

7.17.3 Clock output

The LPC11E3x feature a clock output function that routes the IRC oscillator, the system oscillator, the watchdog oscillator, or the main clock to an output pin.

7.17.4 Wake-up process

The LPC11E3x begin operation by using the 12 MHz IRC oscillator as the clock source at power-up and when awakened from Deep power-down mode. This mechanism allows chip operation to resume quickly. If the application uses the main oscillator or the PLL, software must enable these components and wait for them to stabilize. Only then can the system use the PLL and main oscillator as a clock source.

7.17.5 Power control

The LPC11E3x support various power control features. There are four special modes of processor power reduction: Sleep mode, Deep-sleep mode, Power-down mode, and Deep power-down mode. The CPU clock rate can also be controlled as needed by changing clock sources, reconfiguring PLL values, and/or altering the CPU clock divider value. This power control mechanism allows a trade-off of power versus processing speed based on application requirements. In addition, a register is provided for shutting down the clocks to individual on-chip peripherals. This register allows fine-tuning of power consumption by eliminating all dynamic power use in any peripherals that are not required for the application. Selected peripherals have their own clock divider which provides even better power control.

7.17.5.1 Power profiles

The power consumption in Active and Sleep modes can be optimized for the application through simple calls to the power profile. The power configuration routine configures the LPC11E3x for one of the following power modes:

- Default mode corresponding to power configuration after reset.
- CPU performance mode corresponding to optimized processing capability.

All information provided in this document is subject to legal disclaimers.

© NXP Semiconductors N.V. 2014. All rights reserved.

- Efficiency mode corresponding to optimized balance of current consumption and CPU performance.
- Low-current mode corresponding to lowest power consumption.

In addition, the power profile includes routines to select the optimal PLL settings for a given system clock and PLL input clock.

7.17.5.2 Sleep mode

When Sleep mode is entered, the clock to the core is stopped. Resumption from the Sleep mode does not need any special sequence but re-enabling the clock to the ARM core.

In Sleep mode, execution of instructions is suspended until either a reset or interrupt occurs. Peripheral functions continue operation during Sleep mode and can generate interrupts to cause the processor to resume execution. Sleep mode eliminates dynamic power used by the processor itself, by memory systems and related controllers, and by internal buses.

7.17.5.3 Deep-sleep mode

In Deep-sleep mode, the LPC11E3x is in Sleep-mode and all peripheral clocks and all clock sources are off except for the IRC. The IRC output is disabled unless the IRC is selected as input to the watchdog timer. In addition all analog blocks are shut down and the flash is in stand-by mode. In Deep-sleep mode, the application can keep the watchdog oscillator and the BOD circuit running for self-timed wake-up and BOD protection.

The LPC11E3x can wake up from Deep-sleep mode via reset, selected GPIO pins or a watchdog timer interrupt.

Deep-sleep mode saves power and allows for short wake-up times.

7.17.5.4 Power-down mode

In Power-down mode, the LPC11E3x is in Sleep-mode and all peripheral clocks and all clock sources are off except for watchdog oscillator if selected. In addition all analog blocks and the flash are shut down. In Power-down mode, the application can keep the BOD circuit running for BOD protection.

The LPC11E3x can wake up from Power-down mode via reset, selected GPIO pins or a watchdog timer interrupt.

Power-down mode reduces power consumption compared to Deep-sleep mode at the expense of longer wake-up times.

7.17.5.5 Deep power-down mode

In Deep power-down mode, power is shut off to the entire chip except for the WAKEUP pin. The LPC11E3x can wake up from Deep power-down mode via the WAKEUP pin.

The LPC11E3x can be prevented from entering Deep power-down mode by setting a lock bit in the PMU block. Locking out Deep power-down mode enables the application to keep the watchdog timer or the BOD running at all times.

When entering Deep power-down mode, an external pull-up resistor is required on the WAKEUP pin to hold it HIGH. Pull the $\overline{\text{RESET}}$ pin HIGH to prevent it from floating while in Deep power-down mode.

All information provided in this document is subject to legal disclaimers.

© NXP Semiconductors N.V. 2014. All rights reserved.

7.17.6 System control

7.17.6.1 Reset

Reset has four sources on the LPC11E3x: the $\overline{\text{RESET}}$ pin, the Watchdog reset, power-on reset (POR), and the BrownOut Detection (BOD) circuit. The $\overline{\text{RESET}}$ pin is a Schmitt trigger input pin. Assertion of chip reset by any source, once the operating voltage attains a usable level, starts the IRC and initializes the flash controller.

A LOW-going pulse as short as 50 ns resets the part.

When the internal Reset is removed, the processor begins executing at address 0, which is initially the Reset vector mapped from the boot block. At that point, all of the processor and peripheral registers have been initialized to predetermined values.

In Deep power-down mode, an external pull-up resistor is required on the $\overline{\text{RESET}}$ pin.

7.17.6.2 Brownout detection

The LPC11E3x includes four levels for monitoring the voltage on the V_{DD} pin. If this voltage falls below one of the four selected levels, the BOD asserts an interrupt signal to the NVIC. This signal can be enabled for interrupt in the Interrupt Enable Register in the NVIC to cause a CPU interrupt. Alternatively, software can monitor the signal by reading a dedicated status register. Four additional threshold levels can be selected to cause a forced reset of the chip.

7.17.6.3 Code security (Code Read Protection - CRP)

CRP provides different levels of security in the system so that access to the on-chip flash and use of the Serial Wire Debugger (SWD) and In-System Programming (ISP) can be restricted. Programming a specific pattern into a dedicated flash location invokes CRP. IAP commands are not affected by the CRP.

In addition, ISP entry via the PIO0_1 pin can be disabled without enabling CRP. For details, see the *LPC11Exx user manual*.

There are three levels of Code Read Protection:

1. CRP1 disables access to the chip via the SWD and allows partial flash update (excluding flash sector 0) using a limited set of the ISP commands. This mode is useful when CRP is required and flash field updates are needed but all sectors cannot be erased.
2. CRP2 disables access to the chip via the SWD and only allows full flash erase and update using a reduced set of the ISP commands.
3. Running an application with level CRP3 selected, fully disables any access to the chip via the SWD pins and the ISP. This mode effectively disables ISP override using PIO0_1 pin as well. If necessary, the application must provide a flash update mechanism using IAP calls or using a call to the reinvoke ISP command to enable flash update via the USART.

All information provided in this document is subject to legal disclaimers.

© NXP Semiconductors N.V. 2014. All rights reserved.

CAUTION

If level three Code Read Protection (CRP3) is selected, no future factory testing can be performed on the device.

In addition to the three CRP levels, sampling of pin PIO0_1 for valid user code can be disabled. For details, see the *LPC11Exx user manual*.

7.17.6.4 APB interface

The APB peripherals are located on one APB bus.

7.17.6.5 AHBLite

The AHBLite connects the CPU bus of the ARM Cortex-M0 to the flash memory, the main static RAM, and the ROM.

7.17.6.6 External interrupt inputs

All GPIO pins can be level or edge sensitive interrupt inputs.

All information provided in this document is subject to legal disclaimers.

© NXP Semiconductors N.V. 2014. All rights reserved.

7.18 Emulation and debugging

Debug functions are integrated into the ARM Cortex-M0. Serial wire debug functions are supported in addition to a standard JTAG boundary scan. The ARM Cortex-M0 is configured to support up to four breakpoints and two watch points.

The $\overline{\text{RESET}}$ pin selects between the JTAG boundary scan ($\overline{\text{RESET}}$ = LOW) and the ARM SWD debug ($\overline{\text{RESET}}$ = HIGH). The ARM SWD debug port is disabled while the LPC11E3x is in reset.

To perform boundary scan testing, follow these steps:

1. Erase any user code residing in flash.
2. Power up the part with the $\overline{\text{RESET}}$ pin pulled HIGH externally.
3. Wait for at least 250 μs.
4. Pull the $\overline{\text{RESET}}$ pin LOW externally.
5. Perform boundary scan operations.
6. Once the boundary scan operations are completed, assert the $\overline{\text{TRST}}$ pin to enable the SWD debug mode, and release the $\overline{\text{RESET}}$ pin (pull HIGH).

Remark: The JTAG interface cannot be used for debug purposes.

All information provided in this document is subject to legal disclaimers.

© NXP Semiconductors N.V. 2014. All rights reserved.

8. Limiting values

Table 4. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).[1]

Symbol	Parameter	Conditions		Min	Max	Unit
V_{DD}	supply voltage (core and external rail)		[2]	–0.5	+4.6	V
V_I	input voltage	5 V tolerant digital I/O pins; $V_{DD} \geq 1.8$ V	[5][2]	–0.5	+5.5	V
		$V_{DD} = 0$ V		–0.5	+3.6	V
		5 V tolerant open-drain pins PIO0_4 and PIO0_5	[2][4]	–0.5	+5.5	
V_{IA}	analog input voltage	pin configured as analog input	[2] [3]	–0.5	4.6	V
I_{DD}	supply current	per supply pin		-	100	mA
I_{SS}	ground current	per ground pin		-	100	mA
I_{latch}	I/O latch-up current	$-(0.5V_{DD}) < V_I < (1.5V_{DD})$; $T_j < 125$ °C		-	100	mA
T_{stg}	storage temperature	non-operating	[6]	–65	+150	°C
$T_{j(max)}$	maximum junction temperature			-	150	°C
$P_{tot(pack)}$	total power dissipation (per package)	based on package heat transfer, not device power consumption		-	1.5	W
V_{ESD}	electrostatic discharge voltage	human body model; all pins	[7]	-	+6500	V

[1] The following applies to the limiting values:

a) This product includes circuitry specifically designed for the protection of its internal devices from the damaging effects of excessive static charge. Nonetheless, it is suggested that conventional precautions be taken to avoid applying greater than the rated maximum.

b) Parameters are valid over operating temperature range unless otherwise specified. All voltages are with respect to V_{SS} unless otherwise noted.

c) The limiting values are stress ratings only. Operating the part at these values is not recommended, and proper operation is not guaranteed. The conditions for functional operation are specified in Table 5.

[2] Maximum/minimum voltage above the maximum operating voltage (see Table 5) and below ground that can be applied for a short time (< 10 ms) to a device without leading to irrecoverable failure. Failure includes the loss of reliability and shorter lifetime of the device.

[3] See Table 6 for maximum operating voltage.

[4] V_{DD} present or not present. Compliant with the I^2C-bus standard. 5.5 V can be applied to this pin when V_{DD} is powered down.

[5] Including voltage on outputs in 3-state mode.

[6] The maximum non-operating storage temperature is different than the temperature for required shelf life which should be determined based on required shelf lifetime. Please refer to the JEDEC spec (J-STD-033B.1) for further details.

[7] Human body model: equivalent to discharging a 100 pF capacitor through a 1.5 kΩ series resistor.

All information provided in this document is subject to legal disclaimers.

© NXP Semiconductors N.V. 2014. All rights reserved.

9. Static characteristics

Table 5. Static characteristics

T_{amb} = −40 °C to +85 °C, unless otherwise specified.

Symbol	Parameter	Conditions		Min	Typ[1]	Max	Unit
V_{DD}	supply voltage (core and external rail)			1.8	3.3	3.6	V
I_{DD}	supply current	Active mode; V_{DD} = 3.3 V; T_{amb} = 25 °C; code `while(1){}` executed from flash;					
		system clock = 12 MHz	[2][3][4][5][6]	-	2	-	mA
		system clock = 50 MHz	[3][4][5][6]	-	7	-	mA
		Sleep mode; V_{DD} = 3.3 V; T_{amb} = 25 °C; system clock = 12 MHz	[2][3][4][5][6]	-	1	-	mA
		Deep-sleep mode; V_{DD} = 3.3 V; T_{amb} = 25 °C	[3]	-	300	-	µA
		Power-down mode; V_{DD} = 3.3 V; T_{amb} = 25 °C		-	2	-	µA
		Deep power-down mode; V_{DD} = 3.3 V; T_{amb} = 25 °C	[8]	-	220	-	nA
Standard port pins, $\overline{\text{RESET}}$							
I_{IL}	LOW-level input current	V_I = 0 V; on-chip pull-up resistor disabled		-	0.5	10	nA
I_{IH}	HIGH-level input current	V_I = V_{DD}; on-chip pull-down resistor disabled		-	0.5	10	nA
I_{OZ}	OFF-state output current	V_O = 0 V; V_O = V_{DD}; on-chip pull-up/down resistors disabled		-	0.5	10	nA
V_I	input voltage	pin configured to provide a digital function; $V_{DD} \geq 1.8$ V	[9][10]	0	-	5.0	V
		V_{DD} = 0 V		0	-	3.6	V
V_O	output voltage	output active		0	-	V_{DD}	V
V_{IH}	HIGH-level input voltage			$0.7V_{DD}$	-	-	V
V_{IL}	LOW-level input voltage			-	-	$0.3V_{DD}$	V
V_{hys}	hysteresis voltage			-	0.4	-	V
V_{OH}	HIGH-level output voltage	2.0 V ≤ V_{DD} ≤ 3.6 V; I_{OH} = −4 mA		V_{DD} − 0.4	-	-	V
		1.8 V ≤ V_{DD} < 2.0 V; I_{OH} = −3 mA		V_{DD} − 0.4	-	-	V
V_{OL}	LOW-level output voltage	2.0 V ≤ V_{DD} ≤ 3.6 V; I_{OL} = 4 mA		-	-	0.4	V
		1.8 V ≤ V_{DD} < 2.0 V; I_{OL} = 3 mA		-	-	0.4	V
I_{OH}	HIGH-level output current	V_{OH} = V_{DD} − 0.4 V; 2.0 V ≤ V_{DD} ≤ 3.6 V		−4	-	-	mA
		1.8 V ≤ V_{DD} < 2.0 V		−3	-	-	mA

All information provided in this document is subject to legal disclaimers.

© NXP Semiconductors N.V. 2014. All rights reserved.

Table 5. Static characteristics *...continued*

T_{amb} = −40 °C to +85 °C, unless otherwise specified.

Symbol	Parameter	Conditions		Min	Typ[1]	Max	Unit
I_{OL}	LOW-level output current	V_{OL} = 0.4 V 2.0 V ≤ V_{DD} ≤ 3.6 V		4	-	-	mA
		1.8 V ≤ V_{DD} < 2.0 V		3	-	-	mA
I_{OHS}	HIGH-level short-circuit output current	V_{OH} = 0 V	[11]	-	-	−45	mA
I_{OLS}	LOW-level short-circuit output current	V_{OL} = V_{DD}	[11]	-	-	50	mA
I_{pd}	pull-down current	V_I = 5 V		10	50	150	µA
I_{pu}	pull-up current	V_I = 0 V; 2.0 V ≤ V_{DD} ≤ 3.6 V		−15	−50	−85	µA
		1.8 V ≤ V_{DD} < 2.0 V		−10	−50	−85	µA
		V_{DD} < V_I < 5 V		0	0	0	µA
High-drive output pin (PIO0_7)							
I_{IL}	LOW-level input current	V_I = 0 V; on-chip pull-up resistor disabled		-	0.5	10	nA
I_{IH}	HIGH-level input current	V_I = V_{DD}; on-chip pull-down resistor disabled		-	0.5	10	nA
I_{OZ}	OFF-state output current	V_O = 0 V; V_O = V_{DD}; on-chip pull-up/down resistors disabled		-	0.5	10	nA
V_I	input voltage	pin configured to provide a digital function	[9] [10]	0	-	5.0	V
		V_{DD} = 0 V		0	-	3.6	V
V_O	output voltage	output active		0	-	V_{DD}	V
V_{IH}	HIGH-level input voltage			0.7V_{DD}	-	-	V
V_{IL}	LOW-level input voltage			-	-	0.3V_{DD}	V
V_{hys}	hysteresis voltage			0.4	-	-	V
V_{OH}	HIGH-level output voltage	2.5 V ≤ V_{DD} ≤ 3.6 V; I_{OH} = −20 mA		V_{DD} − 0.4	-	-	V
		1.8 V ≤ V_{DD} < 2.5 V; I_{OH} = −12 mA		V_{DD} − 0.4	-	-	V
V_{OL}	LOW-level output voltage	2.0 V ≤ V_{DD} ≤ 3.6 V; I_{OL} = 4 mA		-	-	0.4	V
		1.8 V ≤ V_{DD} < 2.0 V; I_{OL} = 3 mA		-	-	0.4	V
I_{OH}	HIGH-level output current	V_{OH} = V_{DD} − 0.4 V; 2.5 V ≤ V_{DD} ≤ 3.6 V		20	-	-	mA
		1.8 V ≤ V_{DD} < 2.5 V		12	-	-	mA
I_{OL}	LOW-level output current	V_{OL} = 0.4 V 2.0 V ≤ V_{DD} ≤ 3.6 V		4	-	-	mA
		1.8 V ≤ V_{DD} < 2.0 V		3	-	-	mA
I_{OLS}	LOW-level short-circuit output current	V_{OL} = V_{DD}	[11]	-	-	50	mA
I_{pd}	pull-down current	V_I = 5 V		10	50	150	µA

All information provided in this document is subject to legal disclaimers.

© NXP Semiconductors N.V. 2014. All rights reserved.

Table 5. Static characteristics *…continued*

T_{amb} = −40 °C to +85 °C, unless otherwise specified.

Symbol	Parameter	Conditions		Min	Typ[1]	Max	Unit
I_{pu}	pull-up current	V_I = 0 V 2.0 V ≤ V_{DD} ≤ 3.6 V		−15	−50	−85	µA
		1.8 V ≤ V_{DD} < 2.0 V		−10	−50	−85	µA
		V_{DD} < V_I < 5 V		0	0	0	µA
I^2C-bus pins (PIO0_4 and PIO0_5)							
V_{IH}	HIGH-level input voltage			0.7V_{DD}	-	-	V
V_{IL}	LOW-level input voltage			-	-	0.3V_{DD}	V
V_{hys}	hysteresis voltage			-	0.05V_{DD}	-	V
I_{OL}	LOW-level output current	V_{OL} = 0.4 V; I^2C-bus pins configured as standard mode pins 2.0 V ≤ V_{DD} ≤ 3.6 V		3.5	-	-	mA
		1.8 V ≤ V_{DD} < 2.0 V		3	-	-	
I_{OL}	LOW-level output current	V_{OL} = 0.4 V; I^2C-bus pins configured as Fast-mode Plus pins 2.0 V ≤ V_{DD} ≤ 3.6 V		20	-	-	mA
		1.8 V ≤ V_{DD} < 2.0 V		16	-	-	
I_{LI}	input leakage current	V_I = V_{DD}	[12]	-	2	4	µA
		V_I = 5 V		-	10	22	µA
Oscillator pins							
$V_{i(xtal)}$	crystal input voltage			−0.5	1.8	1.95	V
$V_{o(xtal)}$	crystal output voltage			−0.5	1.8	1.95	V
Pin capacitance							
C_{io}	input/output capacitance	pins configured for analog function		-	-	7.1	pF
		I^2C-bus pins (PIO0_4 and PIO0_5)		-	-	2.5	pF
		pins configured as GPIO		-	-	2.8	pF

[1] Typical ratings are not guaranteed. The values listed are at room temperature (25 °C), nominal supply voltages.

[2] IRC enabled; system oscillator disabled; system PLL disabled.

[3] I_{DD} measurements were performed with all pins configured as GPIO outputs driven LOW and pull-up resistors disabled.

[4] BOD disabled.

[5] All peripherals disabled in the AHBCLKCTRL register. Peripheral clocks to USART, SSP0/1 disabled in the SYSCON block.

[6] Low-current mode PWR_LOW_CURRENT selected when running the set_power routine in the power profiles.

[7] IRC disabled; system oscillator enabled; system PLL enabled.

[8] WAKEUP pin pulled HIGH externally. An external pull-up resistor is required on the $\overline{\text{RESET}}$ pin for the Deep power-down mode.

[9] Including voltage on outputs in 3-state mode.

[10] 3-state outputs go into 3-state mode in Deep power-down mode.

[11] Allowed as long as the current limit does not exceed the maximum current allowed by the device.

[12] To V_{SS}.

All information provided in this document is subject to legal disclaimers.

© NXP Semiconductors N.V. 2014. All rights reserved.

Table 6. ADC static characteristics

T_{amb} = −40 °C to +85 °C unless otherwise specified; ADC frequency 4.5 MHz, V_{DD} = 2.5 V to 3.6 V.

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
V_{IA}	analog input voltage			0	-	V_{DD}	V
C_{ia}	analog input capacitance			-	-	1	pF
E_D	differential linearity error		[1][2]	-	-	±1	LSB
$E_{L(adj)}$	integral non-linearity		[3]	-	-	±1.5	LSB
E_O	offset error		[4]	-	-	±3.5	LSB
E_G	gain error		[5]	-	-	0.6	%
E_T	absolute error		[6]	-	-	±4	LSB
R_{vsi}	voltage source interface resistance			-	-	40	kΩ
R_i	input resistance		[7][8]	-	-	2.5	MΩ

[1] The ADC is monotonic, there are no missing codes.

[2] The differential linearity error (E_D) is the difference between the actual step width and the ideal step width. See Figure 8.

[3] The integral non-linearity ($E_{L(adj)}$) is the peak difference between the center of the steps of the actual and the ideal transfer curve after appropriate adjustment of gain and offset errors. See Figure 8.

[4] The offset error (E_O) is the absolute difference between the straight line which fits the actual curve and the straight line which fits the ideal curve. See Figure 8.

[5] The gain error (E_G) is the relative difference in percent between the straight line fitting the actual transfer curve after removing offset error, and the straight line which fits the ideal transfer curve. See Figure 8.

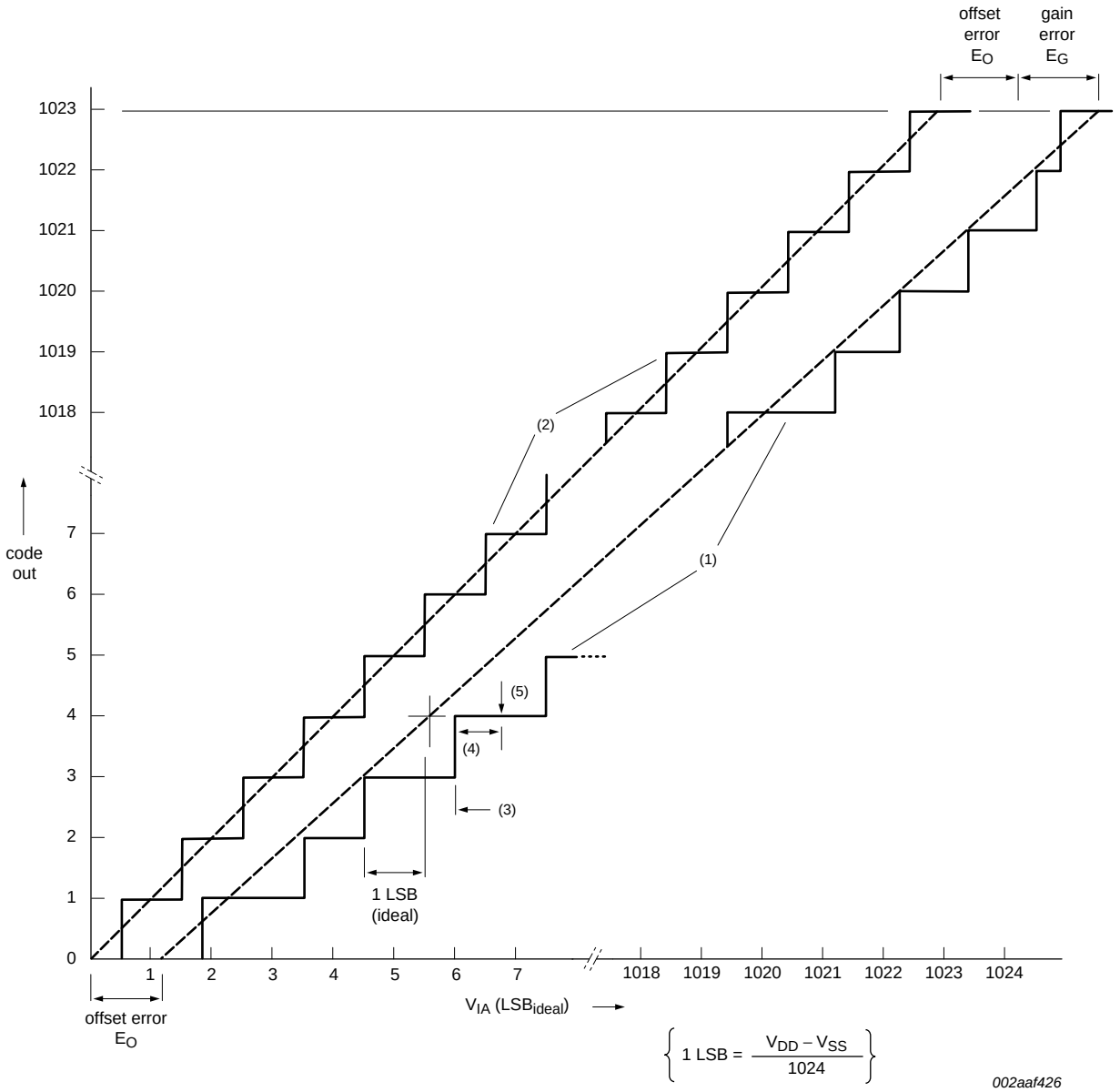
[6] The absolute error (E_T) is the maximum difference between the center of the steps of the actual transfer curve of the non-calibrated ADC and the ideal transfer curve. See Figure 8.

[7] T_{amb} = 25 °C; maximum sampling frequency f_s = 400 kSamples/s and analog input capacitance C_{ia} = 1 pF.

[8] Input resistance R_i depends on the sampling frequency fs: $R_i = 1 / (f_s \times C_{ia})$.

All information provided in this document is subject to legal disclaimers.

© NXP Semiconductors N.V. 2014. All rights reserved.



(1) Example of an actual transfer curve.

(2) The ideal transfer curve.

(3) Differential linearity error (E_D).

(4) Integral non-linearity ($E_{L(adj)}$).

(5) Center of a step of the actual transfer curve.

Fig 8. ADC characteristics

All information provided in this document is subject to legal disclaimers.

© NXP Semiconductors N.V. 2014. All rights reserved.

9.1 BOD static characteristics

Table 7. BOD static characteristics[1]

T_{amb} = 25 °C.

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
V_{th}	threshold voltage	interrupt level 1					
		assertion		-	2.22	-	V
		de-assertion		-	2.35	-	V
		interrupt level 2					
		assertion		-	2.52	-	V
		de-assertion		-	2.66	-	V
		interrupt level 3					
		assertion		-	2.80	-	V
		de-assertion		-	2.90	-	V
		reset level 0					
		assertion		-	1.46	-	V
		de-assertion		-	1.63	-	V
		reset level 1					
		assertion		-	2.06	-	V
		de-assertion		-	2.15	-	V
		reset level 2					
		assertion		-	2.35	-	V
		de-assertion		-	2.43	-	V
		reset level 3					
		assertion		-	2.63	-	V
		de-assertion		-	2.71	-	V

[1] Interrupt levels are selected by writing the level value to the BOD control register BODCTRL, see *the LPC11Exx user manual*.

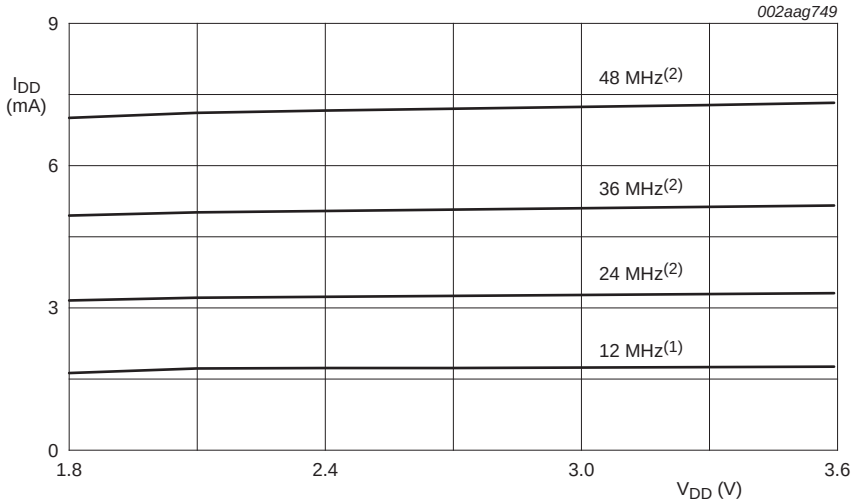
9.2 Power consumption

Power measurements in Active, Sleep, and Deep-sleep modes were performed under the following conditions (see the *LPC11Exx user manual*):

- Configure all pins as GPIO with pull-up resistor disabled in the IOCON block.
- Configure GPIO pins as outputs using the GPIOnDIR registers.
- Write 0 to all GPIOnDATA registers to drive the outputs LOW.

All information provided in this document is subject to legal disclaimers.

© NXP Semiconductors N.V. 2014. All rights reserved.

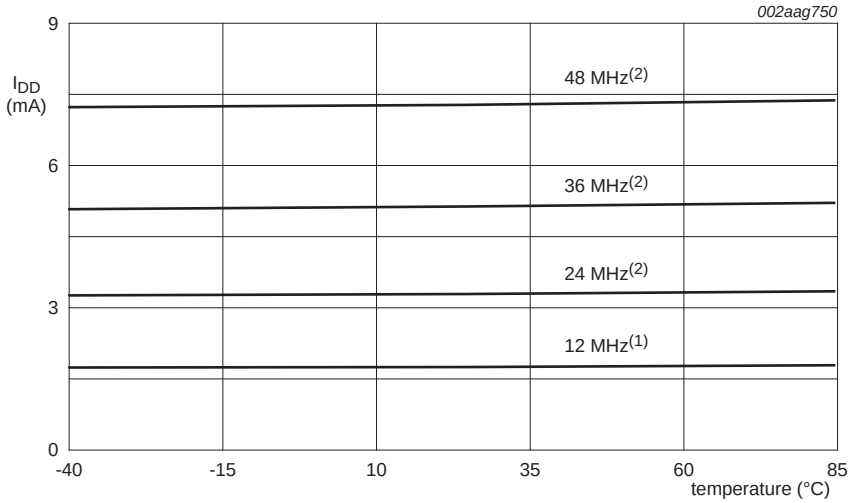


Conditions: T_{amb} = 25 °C; Active mode entered executing code `while(1){}` from flash; internal pull-up resistors disabled; BOD disabled; all peripherals disabled in the SYSAHBCLKCTRL register; all peripheral clocks disabled; low-current mode.

(1) System oscillator and system PLL disabled; IRC enabled.

(2) System oscillator and system PLL enabled; IRC disabled.

Fig 9. Typical supply current versus regulator supply voltage V_{DD} in active mode



Conditions: V_{DD} = 3.3 V; Active mode entered executing code `while(1){}` from flash; internal pull-up resistors disabled; BOD disabled; all peripherals disabled in the SYSAHBCLKCTRL register; all peripheral clocks disabled; low-current mode.

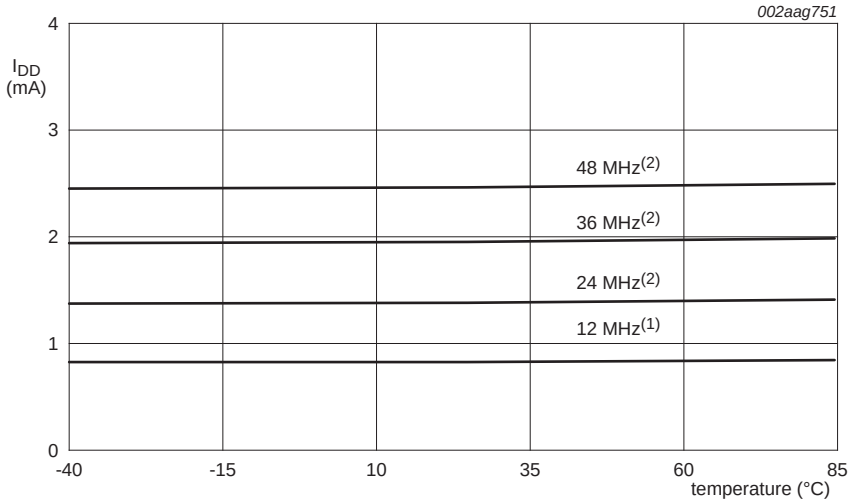
(1) System oscillator and system PLL disabled; IRC enabled.

(2) System oscillator and system PLL enabled; IRC disabled.

Fig 10. Typical supply current versus temperature in Active mode

All information provided in this document is subject to legal disclaimers.

© NXP Semiconductors N.V. 2014. All rights reserved.

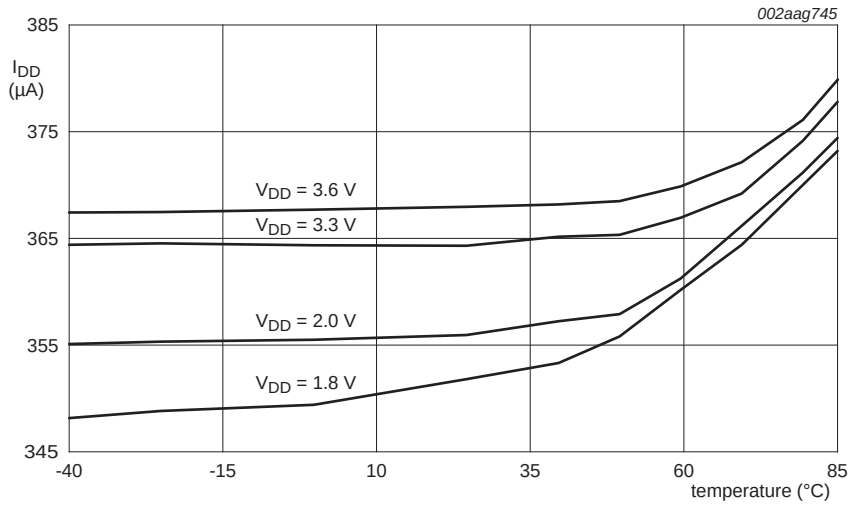


Conditions: V_{DD} = 3.3 V; Sleep mode entered from flash; internal pull-up resistors disabled; BOD disabled; all peripherals disabled in the SYSAHBCLKCTRL register; all peripheral clocks disabled; low-current mode..

(1) System oscillator and system PLL disabled; IRC enabled.

(2) System oscillator and system PLL enabled; IRC disabled.

Fig 11. Typical supply current versus temperature in Sleep mode

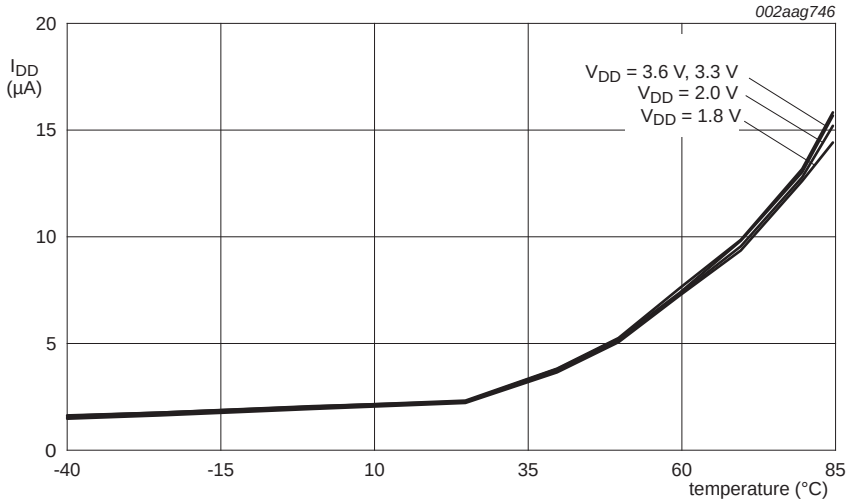


Conditions: BOD disabled; all oscillators and analog blocks turned off in the PDSLEEPCFG register.

Fig 12. Typical supply current versus temperature in Deep-sleep mode

All information provided in this document is subject to legal disclaimers.

© NXP Semiconductors N.V. 2014. All rights reserved.



Conditions: BOD disabled; all oscillators and analog blocks turned off in the PDSLEEPCFG register.

Fig 13. Typical supply current versus temperature in Power-down mode

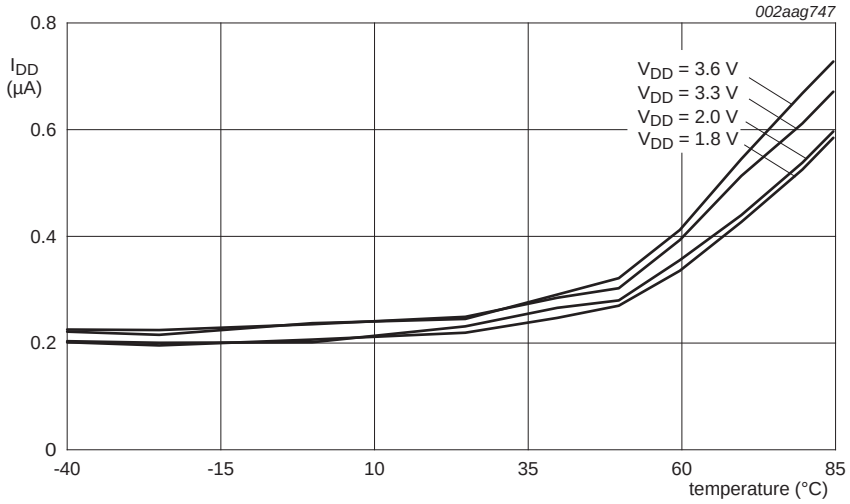


Fig 14. Typical supply current versus temperature in Deep power-down mode

9.3 Peripheral power consumption

The supply current per peripheral is measured as the difference in supply current between the peripheral block enabled and the peripheral block disabled in the SYSAHBCLKCFG and PDRUNCFG (for analog blocks) registers. All other blocks are disabled in both registers and no code is executed. Measured on a typical sample at T_{amb} = 25 °C. Unless noted otherwise, the system oscillator and PLL are running in both measurements.

The supply currents are shown for system clock frequencies of 12 MHz and 48 MHz.

All information provided in this document is subject to legal disclaimers.

© NXP Semiconductors N.V. 2014. All rights reserved.

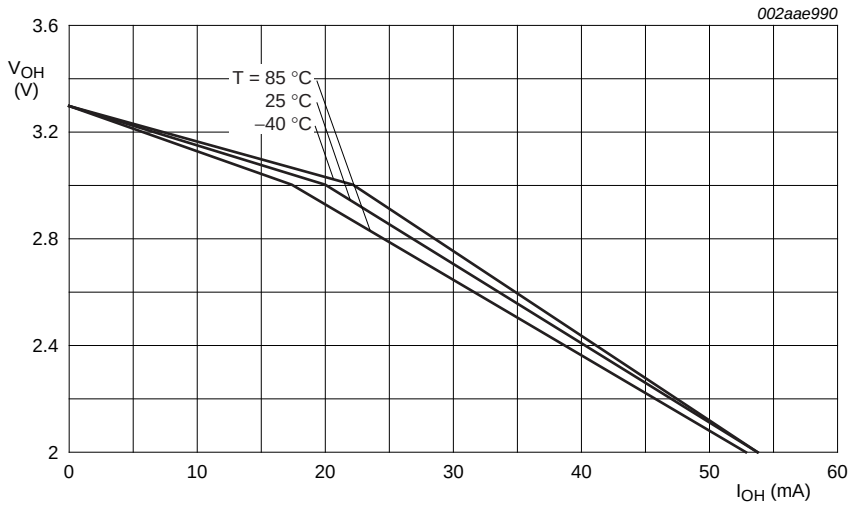
Table 8. Power consumption for individual analog and digital blocks

Peripheral	Typical supply current in mA			Notes
	n/a	12 MHz	48 MHz	
IRC	0.27	-	-	System oscillator running; PLL off; independent of main clock frequency.
System oscillator at 12 MHz	0.22	-	-	IRC running; PLL off; independent of main clock frequency.
Watchdog oscillator at 500 kHz/2	0.004	-	-	System oscillator running; PLL off; independent of main clock frequency.
BOD	0.051	-	-	Independent of main clock frequency.
Main PLL	-	0.21	-	-
ADC	-	0.08	0.29	-
CLKOUT	-	0.12	0.47	Main clock divided by 4 in the CLKOUTDIV register.
CT16B0	-	0.02	0.06	-
CT16B1	-	0.02	0.06	-
CT32B0	-	0.02	0.07	-
CT32B1	-	0.02	0.06	-
GPIO	-	0.23	0.88	GPIO pins configured as outputs and set to LOW. Direction and pin state are maintained if the GPIO is disabled in the SYSAHBCLKCFG register.
IOCONFIG	-	0.03	0.10	-
I^2C	-	0.04	0.13	-
ROM	-	0.04	0.15	-
SPI0	-	0.12	0.45	-
SPI1	-	0.12	0.45	-
UART	-	0.22	0.82	-
WWDT	-	0.02	0.06	Main clock selected as clock source for the WDT.

All information provided in this document is subject to legal disclaimers.

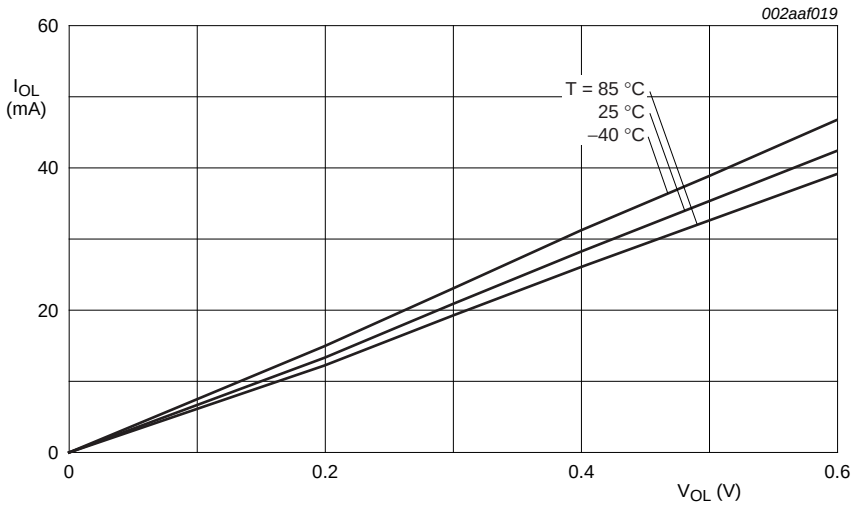
© NXP Semiconductors N.V. 2014. All rights reserved.

9.4 Electrical pin characteristics



Conditions: V_{DD} = 3.3 V; on pin PIO0_7.

Fig 15. High-drive output: Typical HIGH-level output voltage V_{OH} versus HIGH-level output current I_{OH}.

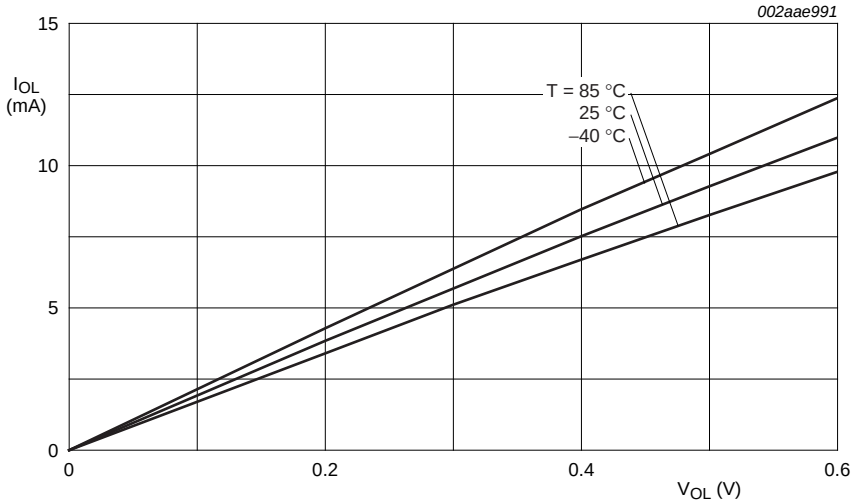


Conditions: V_{DD} = 3.3 V; on pins PIO0_4 and PIO0_5.

Fig 16. I^2C-bus pins (high current sink): Typical LOW-level output current I_{OL} versus LOW-level output voltage V_{OL}

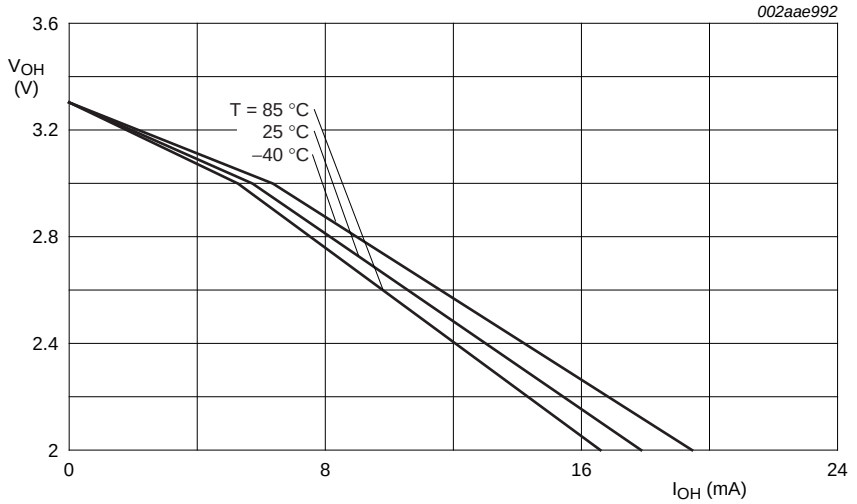
All information provided in this document is subject to legal disclaimers.

© NXP Semiconductors N.V. 2014. All rights reserved.



Conditions: V_{DD} = 3.3 V; standard port pins and PIO0_7.

Fig 17. Typical LOW-level output current I_{OL} versus LOW-level output voltage V_{OL}

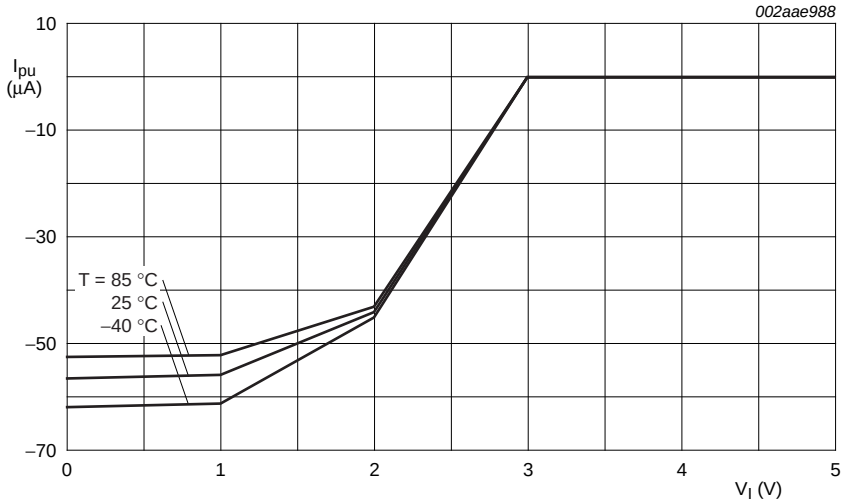


Conditions: V_{DD} = 3.3 V; standard port pins.

Fig 18. Typical HIGH-level output voltage V_{OH} versus HIGH-level output source current I_{OH}

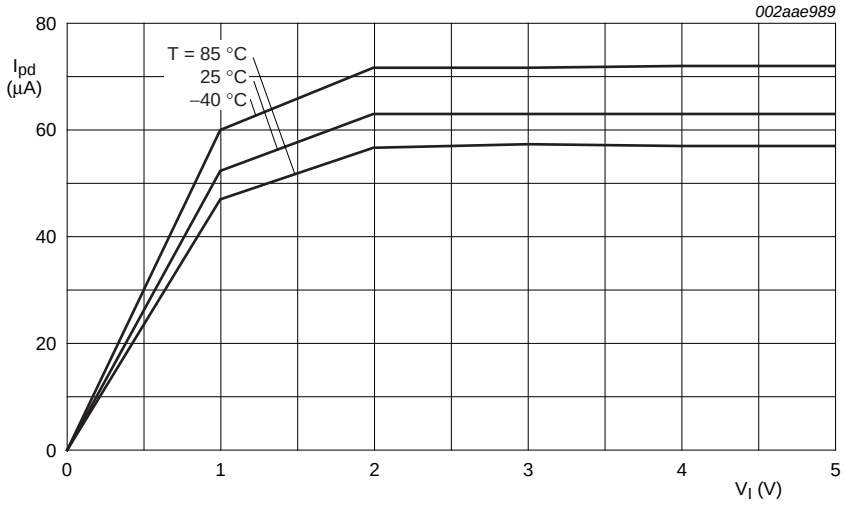
All information provided in this document is subject to legal disclaimers.

© NXP Semiconductors N.V. 2014. All rights reserved.



Conditions: V_{DD} = 3.3 V; standard port pins.

Fig 19. Typical pull-up current I_{pu} versus input voltage V_I



Conditions: V_{DD} = 3.3 V; standard port pins.

Fig 20. Typical pull-down current I_{pd} versus input voltage V_I

All information provided in this document is subject to legal disclaimers.

© NXP Semiconductors N.V. 2014. All rights reserved.

10. Dynamic characteristics

10.1 Flash memory

Table 9. Flash characteristics

T_{amb} = −40 °C to +85 °C, unless otherwise specified.

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
N_{endu}	endurance		[1]	10000	100000	-	cycles
t_{ret}	retention time	powered		10	-	-	years
		unpowered		20	-	-	years
t_{er}	erase time	sector or multiple consecutive sectors		95	100	105	ms
t_{prog}	programming time		[2]	0.95	1	1.05	ms

[1] Number of program/erase cycles.

[2] Programming times are given for writing 256 bytes from RAM to the flash. Data must be written to the flash in blocks of 256 bytes.

Table 10. EEPROM characteristics

T_{amb} = −40 °C to +85 °C; V_{DD} = 2.7 V to 3.6 V. Based on JEDEC NVM qualification. Failure rate < 10 ppm for parts as specified below.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
N_{endu}	endurance		100000	1000000	-	cycles
t_{ret}	retention time	powered	100	200	-	years
		unpowered	150	300	-	years
t_{prog}	programming time	64 bytes	-	2.9	-	ms

10.2 External clock

Table 11. Dynamic characteristic: external clock

T_{amb} = −40 °C to +85 °C; V_{DD} over specified ranges.[1]

Symbol	Parameter	Min	Typ[2]	Max	Unit
f_{osc}	oscillator frequency	1	-	25	MHz
$T_{cy(clk)}$	clock cycle time	40	-	1000	ns
t_{CHCX}	clock HIGH time	$T_{cy(clk)} \times 0.4$	-	-	ns
t_{CLCX}	clock LOW time	$T_{cy(clk)} \times 0.4$	-	-	ns
t_{CLCH}	clock rise time	-	-	5	ns
t_{CHCL}	clock fall time	-	-	5	ns

[1] Parameters are valid over operating temperature range unless otherwise specified.

[2] Typical ratings are not guaranteed. The values listed are at room temperature (25 °C), nominal supply voltages.

All information provided in this document is subject to legal disclaimers.

© NXP Semiconductors N.V. 2014. All rights reserved.

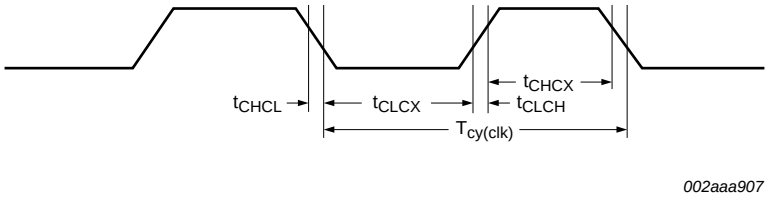


Fig 21. External clock timing (with an amplitude of at least $V_{i(RMS)}$ = 200 mV)

10.3 Internal oscillators

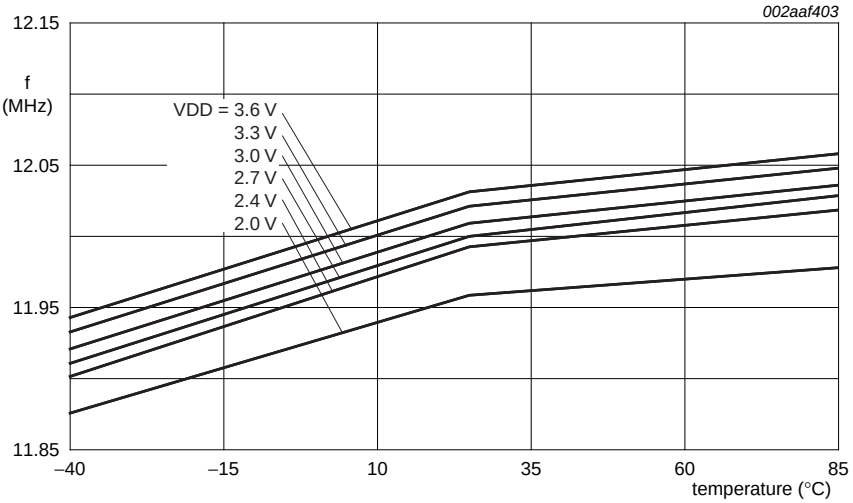
Table 12. Dynamic characteristics: IRC

T_{amb} = −40 °C to +85 °C; 2.7 V ≤ V_{DD} ≤ 3.6 V[1].

Symbol	Parameter	Conditions		Min	Typ[2]	Max	Unit
$f_{osc(RC)}$	internal RC oscillator frequency	-		11.88	12	12.12	MHz

[1] Parameters are valid over operating temperature range unless otherwise specified.

[2] Typical ratings are not guaranteed. The values listed are at room temperature (25 °C), nominal supply voltages.



Conditions: Frequency values are typical values. 12 MHz ± 1 % accuracy is guaranteed for 2.7 V ≤ V_{DD} ≤ 3.6 V and T_{amb} = −40 °C to +85 °C. Variations between parts may cause the IRC to fall outside the 12 MHz ± 1 % accuracy specification for voltages below 2.7 V.

Fig 22. Internal RC oscillator frequency versus temperature

All information provided in this document is subject to legal disclaimers.

© NXP Semiconductors N.V. 2014. All rights reserved.

Table 13. Dynamic characteristics: Watchdog oscillator

Symbol	Parameter	Conditions		Min	Typ[1]	Max	Unit
$f_{osc(int)}$	internal oscillator frequency	DIVSEL = 0x1F, FREQSEL = 0x1 in the WDTOSCCTRL register;	[2][3]	-	9.4	-	kHz
		DIVSEL = 0x00, FREQSEL = 0xF in the WDTOSCCTRL register	[2][3]	-	2300	-	kHz

[1] Typical ratings are not guaranteed. The values listed are at nominal supply voltages.

[2] The typical frequency spread over processing and temperature (T_{amb} = −40 °C to +85 °C) is ±40 %.

[3] See the *LPC11Exx user manual.*

10.4 I/O pins

Table 14. Dynamic characteristics: I/O pins[1]

T_{amb} = −40 °C to +85 °C; 3.0 V ≤ V_{DD} ≤ 3.6 V.

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
t_r	rise time	pin configured as output		3.0	-	5.0	ns
t_f	fall time	pin configured as output		2.5	-	5.0	ns

[1] Applies to standard port pins and $\overline{\text{RESET}}$ pin.

10.5 I²C-bus

Table 15. Dynamic characteristic: I²C-bus pins[1]

T_{amb} = −40 °C to +85 °C.[2]

Symbol	Parameter		Conditions	Min	Max	Unit
f_{SCL}	SCL clock frequency		Standard-mode	0	100	kHz
			Fast-mode	0	400	kHz
			Fast-mode Plus	0	1	MHz
t_f	fall time	[3][4][5][6]	of both SDA and SCL signals Standard-mode	-	300	ns
			Fast-mode	20 + 0.1 × C_b	300	ns
			Fast-mode Plus	-	120	ns
t_{LOW}	LOW period of the SCL clock		Standard-mode	4.7	-	µs
			Fast-mode	1.3	-	µs
			Fast-mode Plus	0.5	-	µs
t_{HIGH}	HIGH period of the SCL clock		Standard-mode	4.0	-	µs
			Fast-mode	0.6	-	µs
			Fast-mode Plus	0.26	-	µs
$t_{HD;DAT}$	data hold time	[3][7][8]	Standard-mode	0	-	µs
			Fast-mode	0	-	µs
			Fast-mode Plus	0	-	µs
$t_{SU;DAT}$	data set-up time	[9][10]	Standard-mode	250	-	ns
			Fast-mode	100	-	ns
			Fast-mode Plus	50	-	ns

[1] See the I²C-bus specification *UM10204* for details.

All information provided in this document is subject to legal disclaimers.

© NXP Semiconductors N.V. 2014. All rights reserved.

[2] Parameters are valid over operating temperature range unless otherwise specified.

[3] A device must internally provide a hold time of at least 300 ns for the SDA signal (with respect to the V_{IH}(min) of the SCL signal) to bridge the undefined region of the falling edge of SCL.

[4] C_b = total capacitance of one bus line in pF.

[5] The maximum t_f for the SDA and SCL bus lines is specified at 300 ns. The maximum fall time for the SDA output stage t_f is specified at 250 ns. This allows series protection resistors to be connected in between the SDA and the SCL pins and the SDA/SCL bus lines without exceeding the maximum specified t_f.

[6] In Fast-mode Plus, fall time is specified the same for both output stage and bus timing. If series resistors are used, designers should allow for this when considering bus timing.

[7] tHD;DAT is the data hold time that is measured from the falling edge of SCL; applies to data in transmission and the acknowledge.

[8] The maximum $t_{HD;DAT}$ could be 3.45 µs and 0.9 µs for Standard-mode and Fast-mode but must be less than the maximum of $t_{VD;DAT}$ or $t_{VD;ACK}$ by a transition time (see *UM10204*). This maximum must only be met if the device does not stretch the LOW period (t_{LOW}) of the SCL signal. If the clock stretches the SCL, the data must be valid by the set-up time before it releases the clock.

[9] tSU;DAT is the data set-up time that is measured with respect to the rising edge of SCL; applies to data in transmission and the acknowledge.

[10] A Fast-mode I²C-bus device can be used in a Standard-mode I²C-bus system but the requirement $t_{SU;DAT}$ = 250 ns must then be met. This will automatically be the case if the device does not stretch the LOW period of the SCL signal. If such a device does stretch the LOW period of the SCL signal, it must output the next data bit to the SDA line $t_{r(max)} + t_{SU;DAT}$ = 1000 + 250 = 1250 ns (according to the Standard-mode I²C-bus specification) before the SCL line is released. Also the acknowledge timing must meet this set-up time.

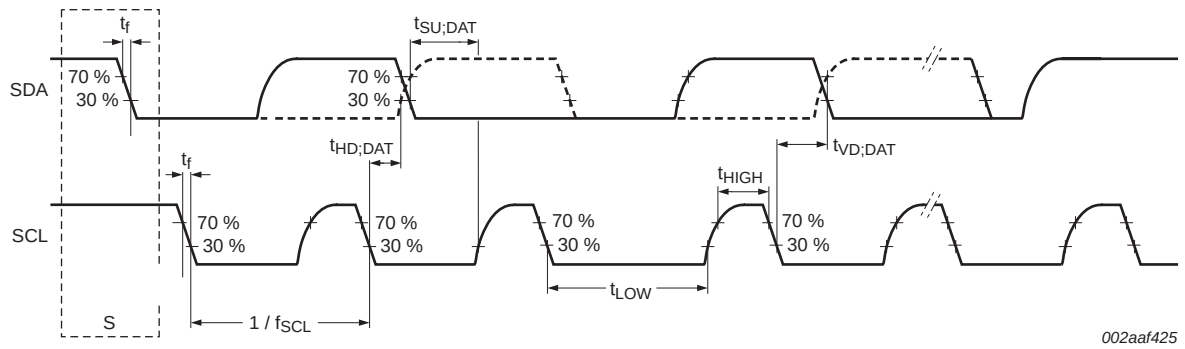


Fig 23. I²C-bus pins clock timing

All information provided in this document is subject to legal disclaimers.

© NXP Semiconductors N.V. 2014. All rights reserved.

10.6 SSP interface

Table 16. Dynamic characteristics of SPI pins in SPI mode

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
SPI master (in SPI mode)							
$T_{cy(clk)}$	clock cycle time	full-duplex mode	[1]	50	-	-	ns
		when only transmitting	[1]	40			ns
t_{DS}	data set-up time	in SPI mode $2.4\ V \leq V_{DD} \leq 3.6\ V$	[2]	15	-	-	ns
		$2.0\ V \leq V_{DD} < 2.4\ V$	[2]	20			ns
		$1.8\ V \leq V_{DD} < 2.0\ V$	[2]	24	-	-	ns
t_{DH}	data hold time	in SPI mode	[2]	0	-	-	ns
$t_{v(Q)}$	data output valid time	in SPI mode	[2]	-	-	10	ns
$t_{h(Q)}$	data output hold time	in SPI mode	[2]	0	-	-	ns
SPI slave (in SPI mode)							
$T_{cy(PCLK)}$	PCLK cycle time			20	-	-	ns
t_{DS}	data set-up time	in SPI mode	[3][4]	0	-	-	ns
t_{DH}	data hold time	in SPI mode	[3][4]	$3 \times T_{cy(PCLK)} + 4$	-	-	ns
$t_{v(Q)}$	data output valid time	in SPI mode	[3][4]	-	-	$3 \times T_{cy(PCLK)} + 11$	ns
$t_{h(Q)}$	data output hold time	in SPI mode	[3][4]	-	-	$2 \times T_{cy(PCLK)} + 5$	ns

[1] $T_{cy(clk)} = (SSPCLKDIV \times (1 + SCR) \times CPSDVSR) / f_{main}$. The clock cycle time derived from the SPI bit rate $T_{cy(clk)}$ is a function of the main clock frequency f_{main}, the SPI peripheral clock divider (SSPCLKDIV), the SPI SCR parameter (specified in the SSP0CR0 register), and the SPI CPSDVSR parameter (specified in the SPI clock prescale register).

[2] $T_{amb} = -40\ °C$ to $85\ °C$.

[3] $T_{cy(clk)} = 12 \times T_{cy(PCLK)}$.

[4] $T_{amb} = 25\ °C$; for normal voltage supply range: $V_{DD} = 3.3\ V$.

All information provided in this document is subject to legal disclaimers.

© NXP Semiconductors N.V. 2014. All rights reserved.

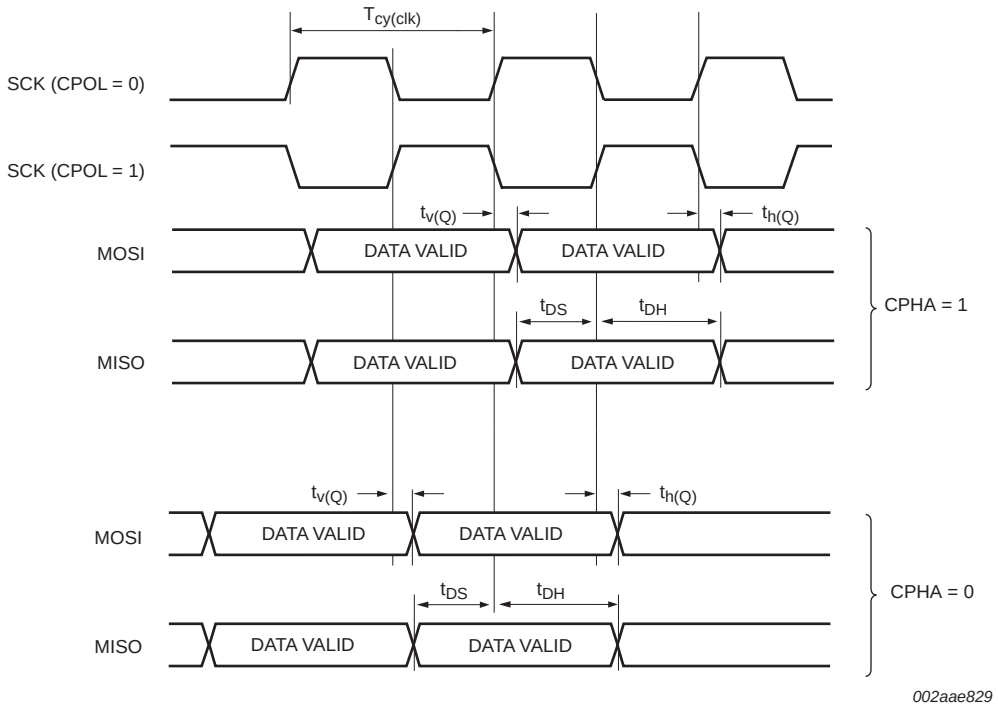


Fig 24. SSP master timing in SPI mode

All information provided in this document is subject to legal disclaimers.

© NXP Semiconductors N.V. 2014. All rights reserved.

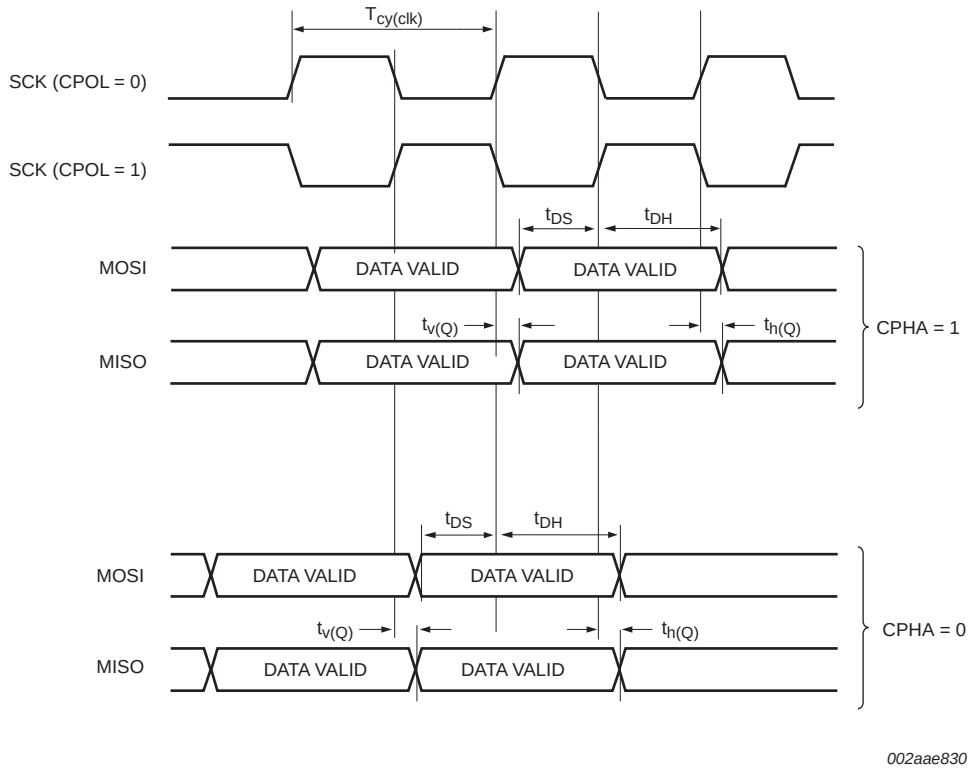


Fig 25. SSP slave timing in SPI mode

All information provided in this document is subject to legal disclaimers.

© NXP Semiconductors N.V. 2014. All rights reserved.

11. Application information

11.1 XTAL input

The input voltage to the on-chip oscillators is limited to 1.8 V. If the oscillator is driven by a clock in slave mode, it is recommended that the input be coupled through a capacitor with C_i = 100 pF. To limit the input voltage to the specified range, choose an additional capacitor to ground C_g which attenuates the input voltage by a factor $C_i/(C_i + C_g)$. In slave mode, a minimum of 200 mV (RMS) is needed.

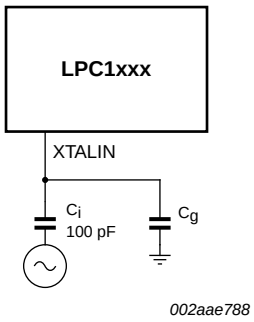


Fig 26. Slave mode operation of the on-chip oscillator

In slave mode, couple the input clock signal with a capacitor of 100 pF (Figure 26), with an amplitude between 200 mV (RMS) and 1000 mV (RMS). This signal corresponds to a square wave signal with a signal swing of between 280 mV and 1.4 V. The XTALOUT pin in this configuration can be left unconnected.

External components and models used in oscillation mode are shown in Figure 27 and in Table 17 and Table 18. Since the feedback resistance is integrated on chip, only a crystal and the capacitances C_{X1} and C_{X2} need to be connected externally in case of fundamental mode oscillation (L, C_L and R_S represent the fundamental frequency). Capacitance C_P in Figure 27 represents the parallel package capacitance and must not be larger than 7 pF. Parameters F_{OSC}, C_L, R_S and C_P are supplied by the crystal manufacturer.

All information provided in this document is subject to legal disclaimers.

© NXP Semiconductors N.V. 2014. All rights reserved.

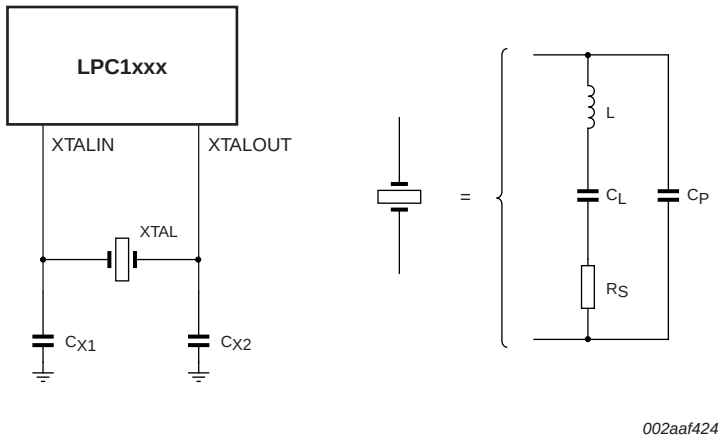


Fig 27. Oscillator modes and models: oscillation mode of operation and external crystal model used for C_{X1}/C_{X2} evaluation

Table 17. Recommended values for C_{X1}/C_{X2} in oscillation mode (crystal and external components parameters) low frequency mode

Fundamental oscillation frequency F_{OSC}	Crystal load capacitance C_L	Maximum crystal series resistance R_S	External load capacitors C_{X1}, C_{X2}
1 MHz to 5 MHz	10 pF	< 300 Ω	18 pF, 18 pF
	20 pF	< 300 Ω	39 pF, 39 pF
	30 pF	< 300 Ω	57 pF, 57 pF
5 MHz to 10 MHz	10 pF	< 300 Ω	18 pF, 18 pF
	20 pF	< 200 Ω	39 pF, 39 pF
	30 pF	< 100 Ω	57 pF, 57 pF
10 MHz to 15 MHz	10 pF	< 160 Ω	18 pF, 18 pF
	20 pF	< 60 Ω	39 pF, 39 pF
15 MHz to 20 MHz	10 pF	< 80 Ω	18 pF, 18 pF

Table 18. Recommended values for C_{X1}/C_{X2} in oscillation mode (crystal and external components parameters) high frequency mode

Fundamental oscillation frequency F_{OSC}	Crystal load capacitance C_L	Maximum crystal series resistance R_S	External load capacitors C_{X1}, C_{X2}
15 MHz to 20 MHz	10 pF	< 180 Ω	18 pF, 18 pF
	20 pF	< 100 Ω	39 pF, 39 pF
20 MHz to 25 MHz	10 pF	< 160 Ω	18 pF, 18 pF
	20 pF	< 80 Ω	39 pF, 39 pF

11.2 XTAL Printed-Circuit Board (PCB) layout guidelines

Follow these guidelines for PCB layout:

- Connect the crystal on the PCB as close as possible to the oscillator input and output pins of the chip.
- Take care that the load capacitors C_{x1}, C_{x2}, and C_{x3} in case of third overtone crystal use have a common ground plane.

All information provided in this document is subject to legal disclaimers.

© NXP Semiconductors N.V. 2014. All rights reserved.

- Connect the external components to the ground plain.
- To keep parasitics and the noise coupled in via the PCB as small as possible, keep loops as small as possible.
- Choose smaller values of C_{x1} and C_{x2} if parasitics of the PCB layout increase.

11.3 Standard I/O pad configuration

Figure 28 shows the possible pin modes for standard I/O pins with analog input function:

- Digital output driver.
- Digital input: Pull-up enabled/disabled.
- Digital input: Pull-down enabled/disabled.
- Digital input: Repeater mode enabled/disabled.
- Analog input.

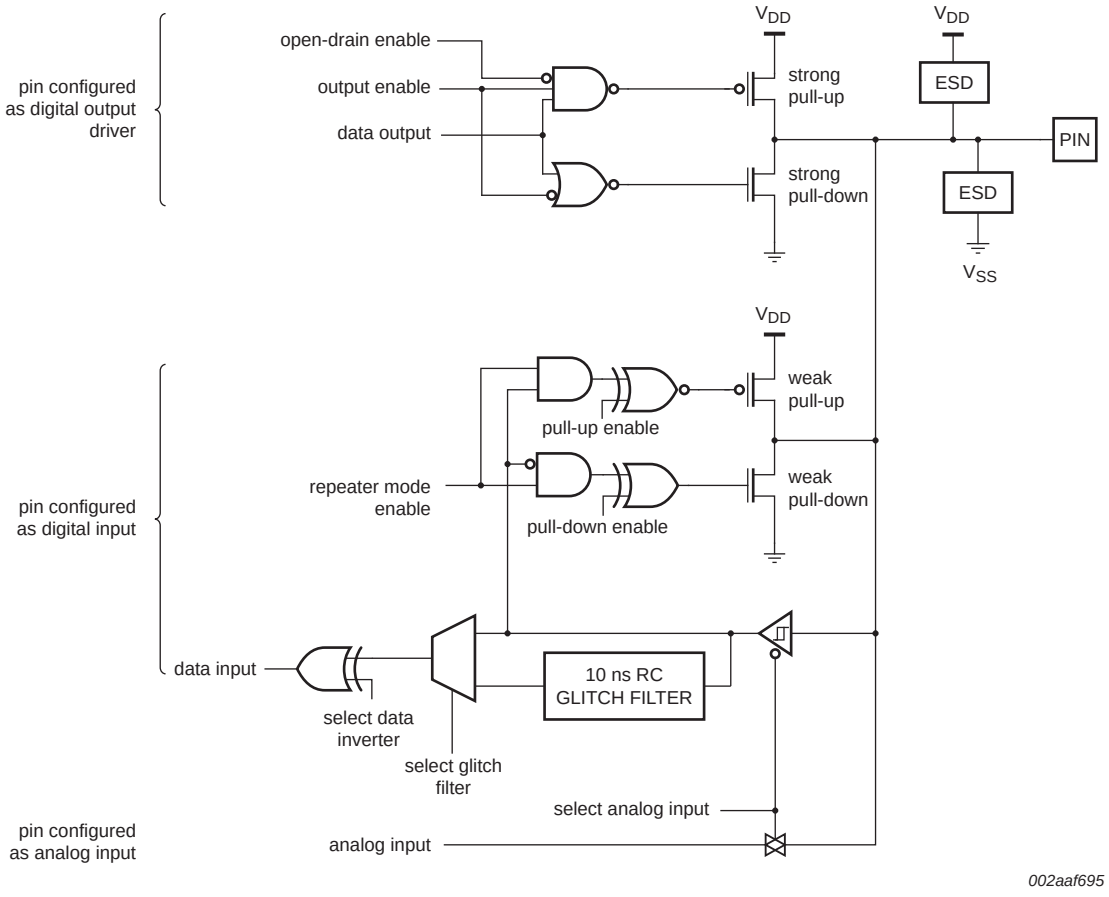


Fig 28. Standard I/O pad configuration

All information provided in this document is subject to legal disclaimers.

© NXP Semiconductors N.V. 2014. All rights reserved.

11.4 Reset pad configuration

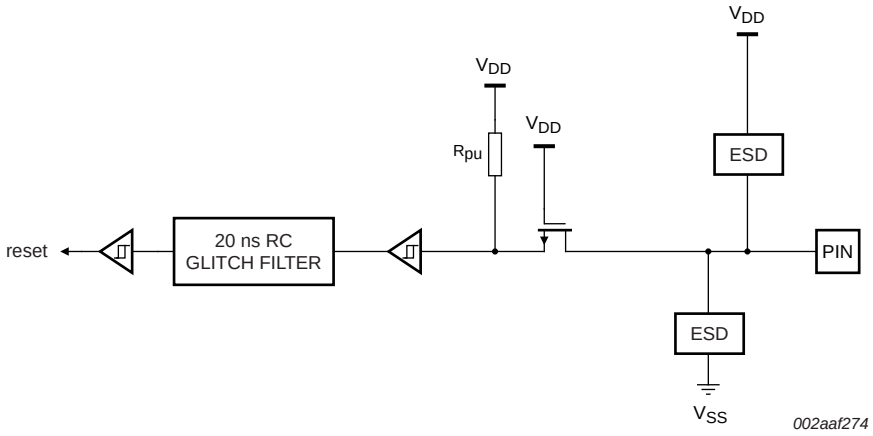


Fig 29. Reset pad configuration

11.5 ADC effective input impedance

A simplified diagram of the ADC input channels can be used to determine the effective input impedance seen from an external voltage source. See Figure 30.

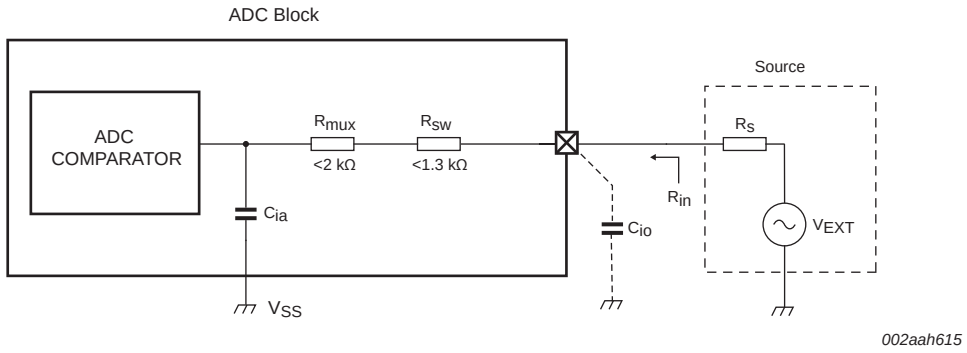


Fig 30. ADC input channel

The effective input impedance, R_{in}, seen by the external voltage source, V_{EXT}, is the parallel impedance of ($(1/f_s \times C_{ia}) + R_{mux} + R_{sw}$) and ($1/f_s \times C_{io}$), and can be calculated using Equation 1 with

f_s = sampling frequency

C_{ia} = ADC analog input capacitance

R_{mux} = analog mux resistance

R_{sw} = switch resistance

C_{io} = pin capacitance

$$R_{in} = \left(\frac{1}{f_s \times C_{ia}} + R_{mux} + R_{sw}\right) \parallel \left(\frac{1}{f_s \times C_{io}}\right) \quad (1)$$

All information provided in this document is subject to legal disclaimers.

© NXP Semiconductors N.V. 2014. All rights reserved.

Under nominal operating condition V_{DD} = 3.3 V and with the maximum sampling frequency fs = 400 kHz, the parameters assume the following values:

C_{ia} = 1 pF (max)

R_{mux} = 2 kΩ (max)

R_{sw} = 1.3 kΩ (max)

C_{io} = 7.1 pF (max)

The effective input impedance with these parameters is R_{in} = 308 kΩ.

11.6 ADC usage notes

The following guidelines show how to increase the performance of the ADC in a noisy environment beyond the ADC specifications listed in Table 6:

- The ADC input trace must be short and as close as possible to the LPC11E3x chip.
- Shield The ADC input traces from fast switching digital signals and noisy power supply lines.
- The ADC and the digital core share the same power supply. Therefore, filter the power supply line adequately.
- To improve the ADC performance in a noisy environment, put the device in Sleep mode during the ADC conversion.

11.7 I/O Handler software library applications

The following sections provide application examples for the I/O Handler software library. All library examples make use of the I/O Handler hardware to extend the functionality of the part through software library calls. The library is available on http://www.LPCware.com.

11.7.1 I/O Handler I^2S

The I/O Handler software library provides functions to emulate an I^2S master transmit interface using the I/O Handler hardware block.

The emulated I^2S interface loops over a 1 kB buffer, transmitting the datawords according to the I^2S protocol. Interrupts are generated every time when the first 512 bytes have been transmitted and when the last 512 bytes have been transmitted. This allows the ARM core to load the free portion of the buffer with new data, thereby enabling streaming audio.

Two channels with 16-bit per channel are supported. The code size of the software library is 1 kB and code must be executed from the SRAM1 memory area reserved for the I/O Handler code.

11.7.2 I/O Handler UART

The I/O Handler UART library emulates one additional full-duplex UART. The emulated UART can be configured for 7 or 8 data bits, no parity and 1 or 2 stop bits. The baud rate is configurable up to 115200 baud. The RXD signal is available on three I/O Handler pins (IOH_6, IOH_16, IOH_20), while TXD and CTS are available on all 21 I/O Handler pins.

The code size of the software library is about 1.2 kB and code must be executed from the SRAM1 memory area reserved for the I/O Handler code.

All information provided in this document is subject to legal disclaimers.

© NXP Semiconductors N.V. 2014. All rights reserved.

11.7.3 I/O Handler I^2C

The I/O Handler I^2C library allows to have an additional I^2C-bus master. I^2C read, I^2C write and combined I^2C read/write are supported. Data is automatically read from and written to user-defined buffers.

The I/O Handler I^2C library combined with the on-chip I^2C module allows to have two distinct I^2C buses, allowing to separate low-speed from high-speed devices or bridging two I^2C buses.

11.7.4 I/O Handler DMA

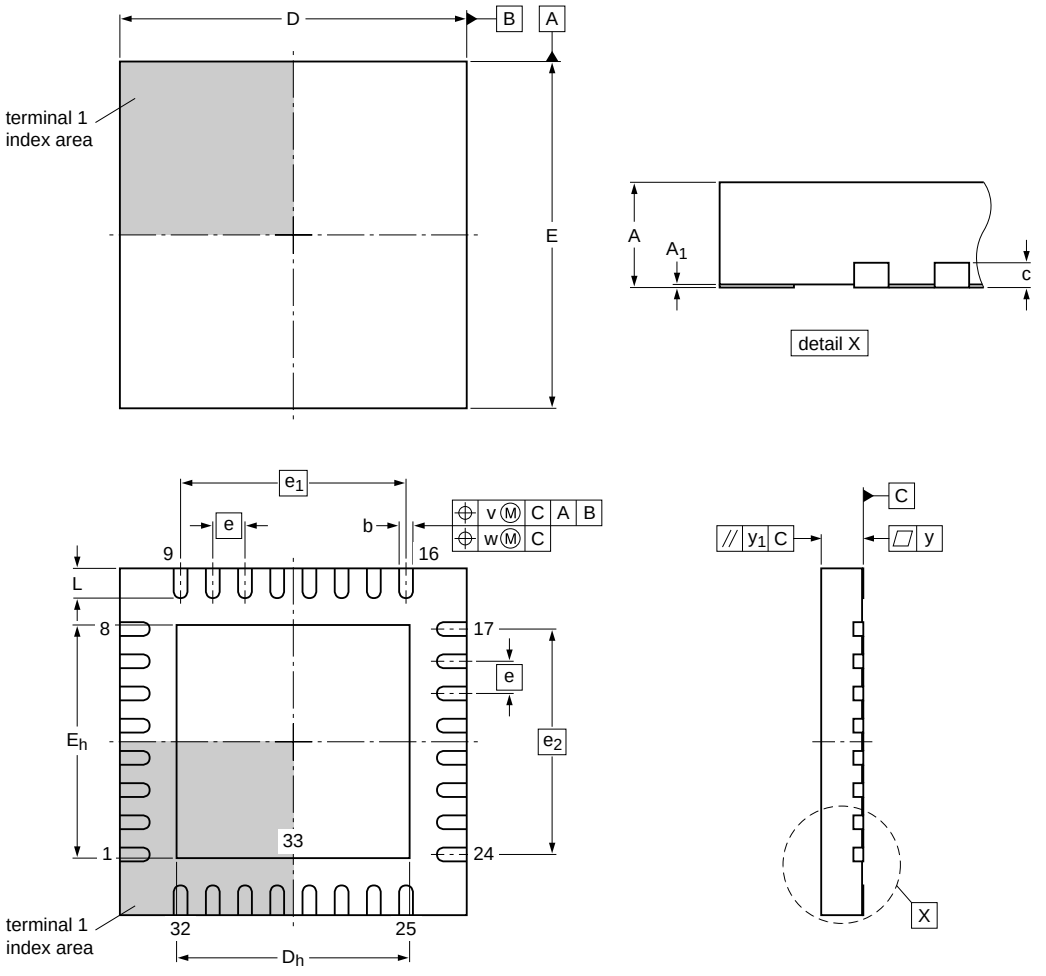
The I/O Handler DMA library offers DMA-like functionality. Four types of transfer are supported: memory to memory, memory to peripheral, peripheral to memory and peripheral to peripheral. Supported peripherals are USART, SSP0/1, ADC and GPIO. DMA transfers can be triggered by the source/target peripheral, software, counter/timer module CT16B1, or I/O Handler pin PIO1_6/IOH_16.

All information provided in this document is subject to legal disclaimers.

© NXP Semiconductors N.V. 2014. All rights reserved.

12. Package outline

HVQFN33: plastic thermal enhanced very thin quad flat package; no leads; 33 terminals; body 7 x 7 x 0.85 mm



Dimensions

Unit		$A^{(1)}$	A_1	b	c	$D^{(1)}$	D_h	$E^{(1)}$	E_h	e	e_1	e_2	L	v	w	y	y_1
	max	1.00	0.05	0.35		7.1	4.85	7.1	4.85				0.75				
mm	nom	0.85	0.02	0.28	0.2	7.0	4.70	7.0	4.70	0.65	4.55	4.55	0.60	0.1	0.05	0.08	0.1
	min	0.80	0.00	0.23		6.9	4.55	6.9	4.55				0.45				

Note

1. Plastic or metal protrusions of 0.075 mm maximum per side are not included.

hvqfn33_po

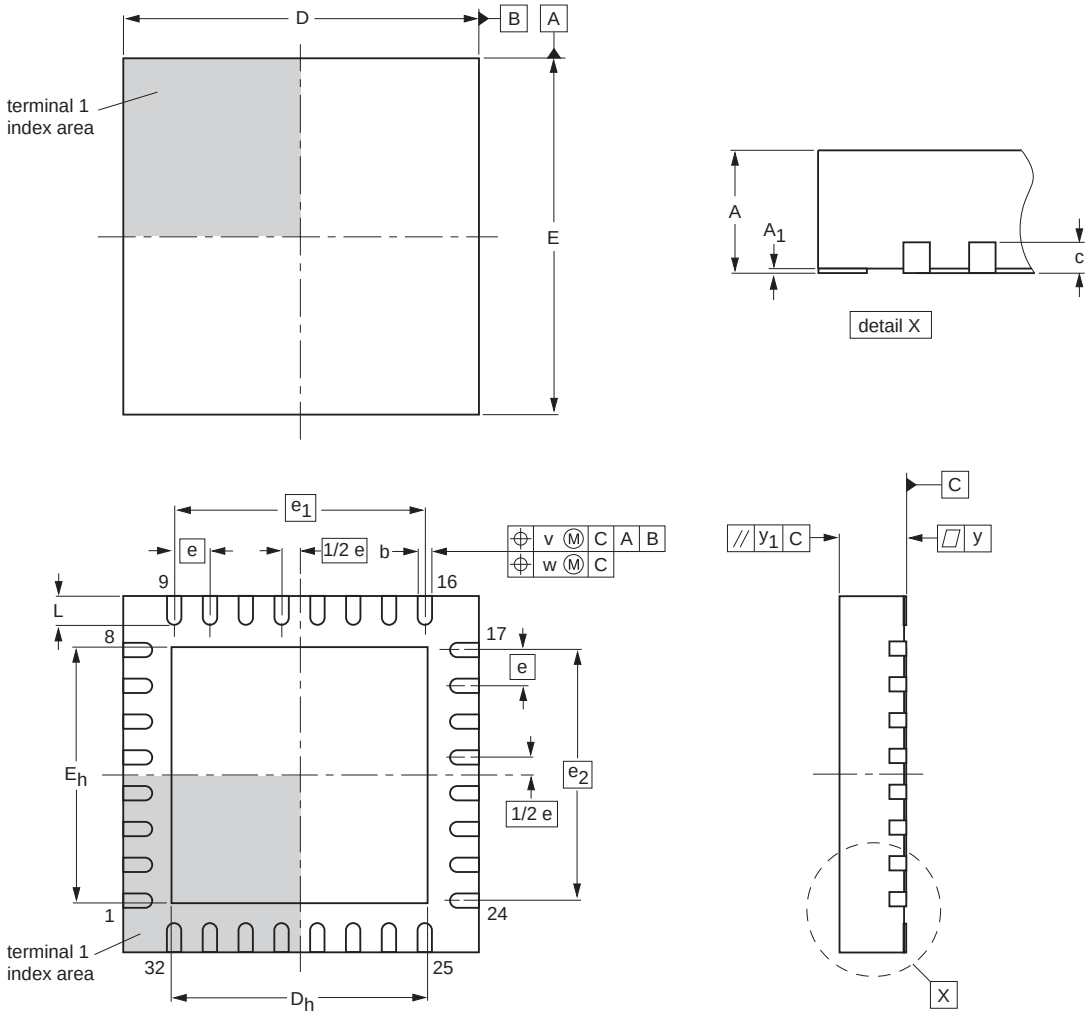
Outline version	References				European projection	Issue date
	IEC	JEDEC	JEITA			
		- - -				~~09-03-17~~ 09-03-23

Fig 31. Package outline HVQFN33 (7 x 7 x 0.85 mm)

All information provided in this document is subject to legal disclaimers.

© NXP Semiconductors N.V. 2014. All rights reserved.

HVQFN33: plastic thermal enhanced very thin quad flat package; no leads; 32 terminals; body 5 x 5 x 0.85 mm



Dimensions (mm are the original dimensions)

Unit[1]		A[1]	A_1	b	c	D[1]	D_h	E[1]	E_h	e	e_1	e_2	L	v	w	y	y_1
mm	max	0.85	0.05	0.30	0.2	5.1	3.75	5.1	3.75	0.5	3.5	3.5	0.5	0.1	0.05	0.05	0.1
	nom																
	min		0.00	0.18		4.9	3.45	4.9	3.45				0.3				

Note

1. Plastic or metal protrusions of 0.075 mm maximum per side are not included.

hvqfn33f_po

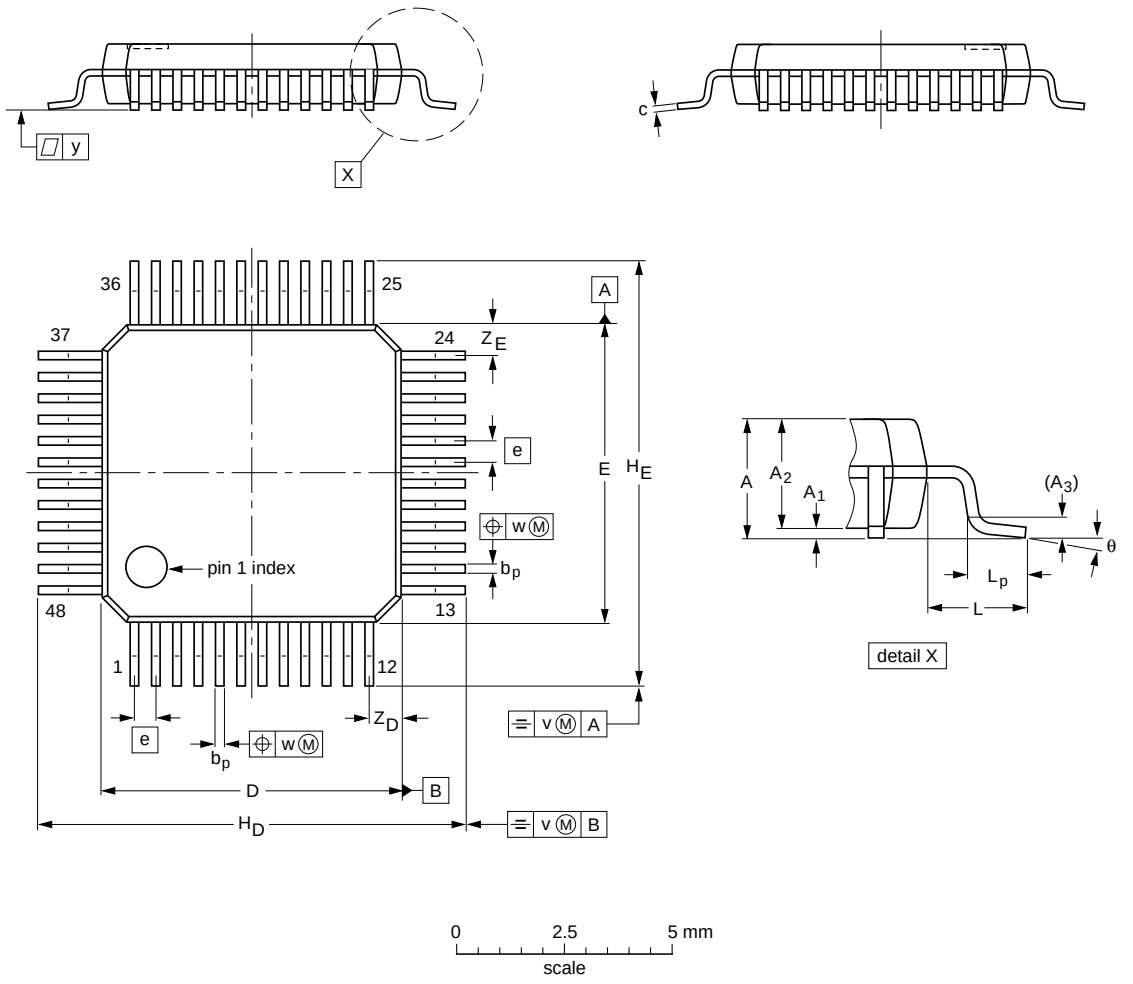
Outline version	References				European projection	Issue date
	IEC	JEDEC	JEITA			
		MO-220				~~11-10-11~~ 11-10-17

Fig 32. Package outline HVQFN33 (5 x 5 x 0.85 mm)

All information provided in this document is subject to legal disclaimers.

© NXP Semiconductors N.V. 2014. All rights reserved.

LQFP48: plastic low profile quad flat package; 48 leads; body 7 x 7 x 1.4 mm **SOT313-2**



DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(1)}$	e	H_D	H_E	L	L_p	v	w	y	$Z_D^{(1)}$	$Z_E^{(1)}$	θ
mm	1.6	0.20 0.05	1.45 1.35	0.25	0.27 0.17	0.18 0.12	7.1 6.9	7.1 6.9	0.5	9.15 8.85	9.15 8.85	1	0.75 0.45	0.2	0.12	0.1	0.95 0.55	0.95 0.55	7^o 0^o

Note

1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

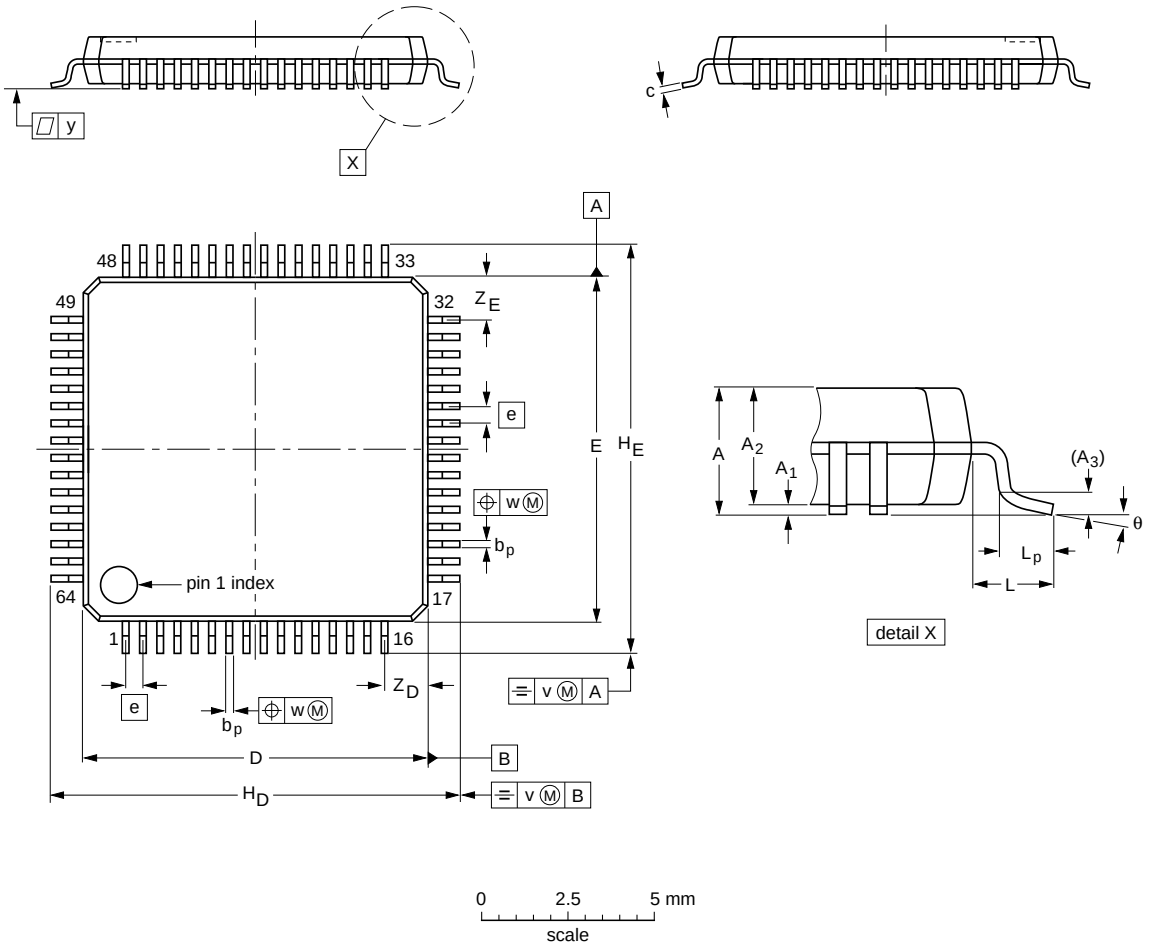
OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT313-2	136E05	MS-026				~~00-01-19~~ 03-02-25

Fig 33. Package outline LQFP48 (SOT313-2)

All information provided in this document is subject to legal disclaimers.

© NXP Semiconductors N.V. 2014. All rights reserved.

LQFP64: plastic low profile quad flat package; 64 leads; body 10 x 10 x 1.4 mm **SOT314-2**



DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(1)}$	e	H_D	H_E	L	L_p	v	w	y	$Z_D^{(1)}$	$Z_E^{(1)}$	θ
mm	1.6	0.20 0.05	1.45 1.35	0.25	0.27 0.17	0.18 0.12	10.1 9.9	10.1 9.9	0.5	12.15 11.85	12.15 11.85	1	0.75 0.45	0.2	0.12	0.1	1.45 1.05	1.45 1.05	7^o 0^o

Note

1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT314-2	136E10	MS-026				~~00-01-19~~ 03-02-25

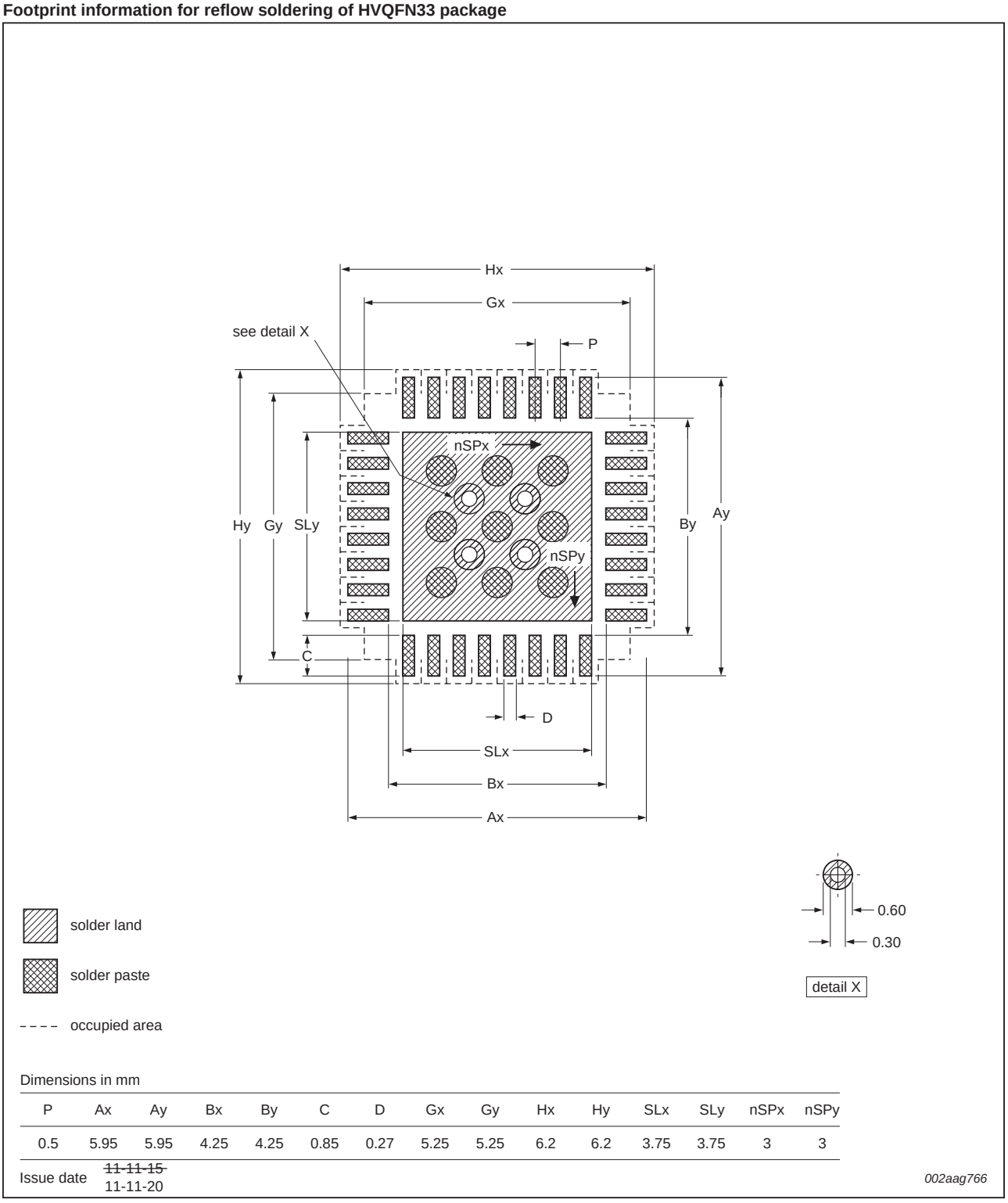
Fig 34. Package outline LQFP64 (SOT314-2)

All information provided in this document is subject to legal disclaimers.

© NXP Semiconductors N.V. 2014. All rights reserved.

13. Soldering

Footprint information for reflow soldering of HVQFN33 package



Dimensions in mm

P	Ax	Ay	Bx	By	C	D	Gx	Gy	Hx	Hy	SLx	SLy	nSPx	nSPy
0.5	5.95	5.95	4.25	4.25	0.85	0.27	5.25	5.25	6.2	6.2	3.75	3.75	3	3

Issue date ~~11-11-15~~ 11-11-20

Fig 35. Reflow soldering for the HVQFN33 (5x5) package

All information provided in this document is subject to legal disclaimers.

© NXP Semiconductors N.V. 2014. All rights reserved.

Footprint information for reflow soldering of HVQFN33 package

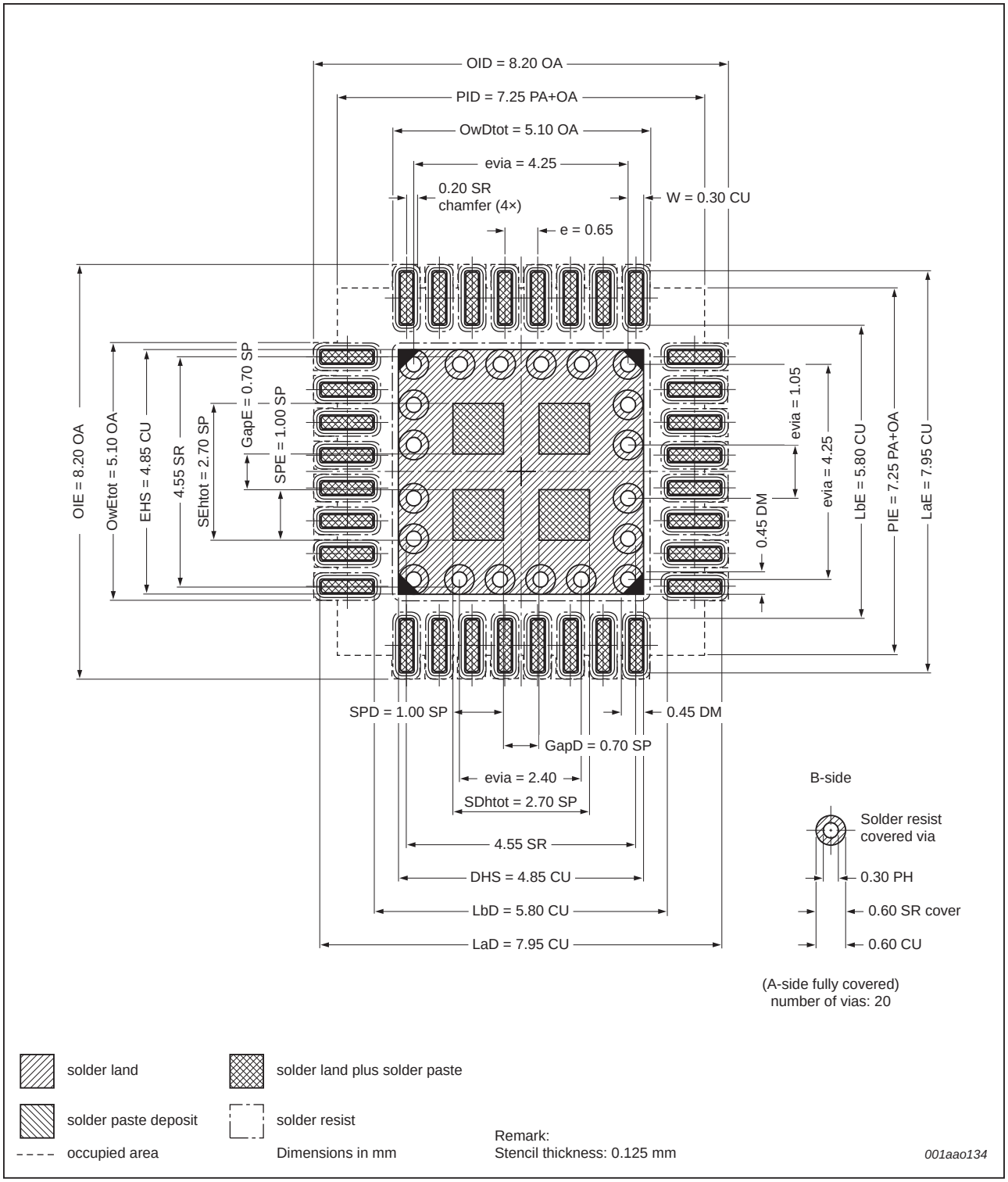
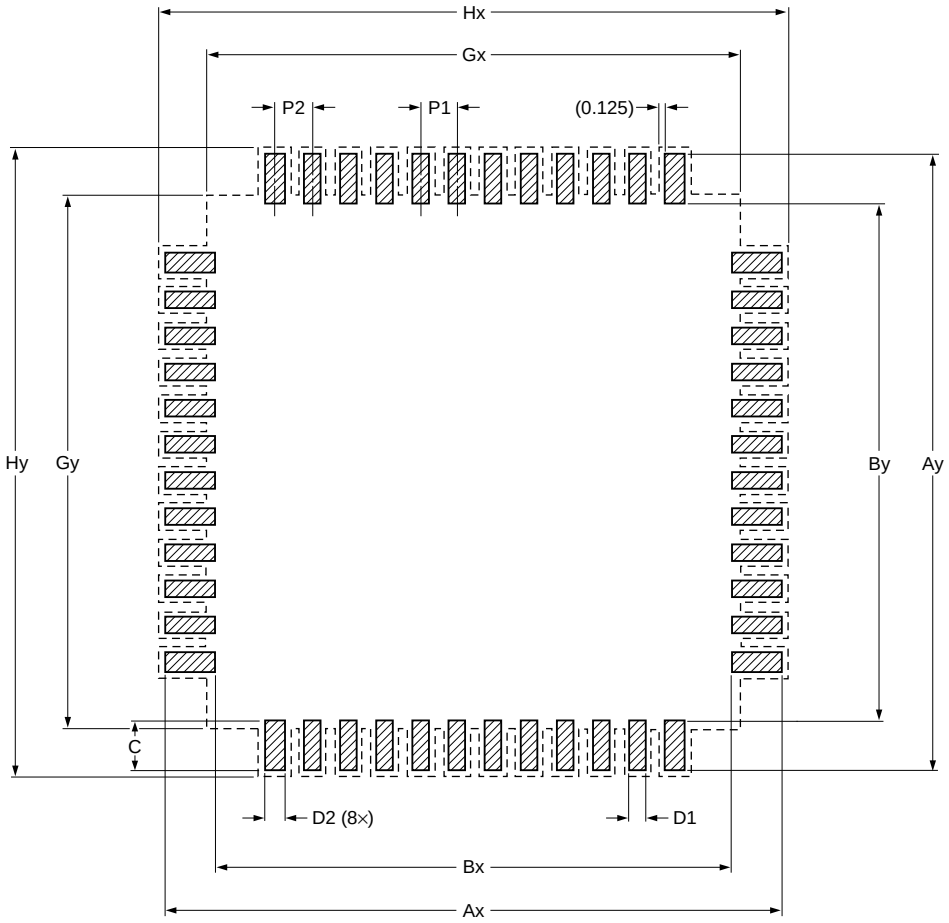


Fig 36. Reflow soldering for the HVQFN33 (7x7) package

All information provided in this document is subject to legal disclaimers.

© NXP Semiconductors N.V. 2014. All rights reserved.

Footprint information for reflow soldering of LQFP48 package **SOT313-2**



Generic footprint pattern

Refer to the package outline drawing for actual layout

solder land

occupied area

DIMENSIONS in mm

P1	P2	Ax	Ay	Bx	By	C	D1	D2	Gx	Gy	Hx	Hy
0.500	0.560	10.350	10.350	7.350	7.350	1.500	0.280	0.500	7.500	7.500	10.650	10.650

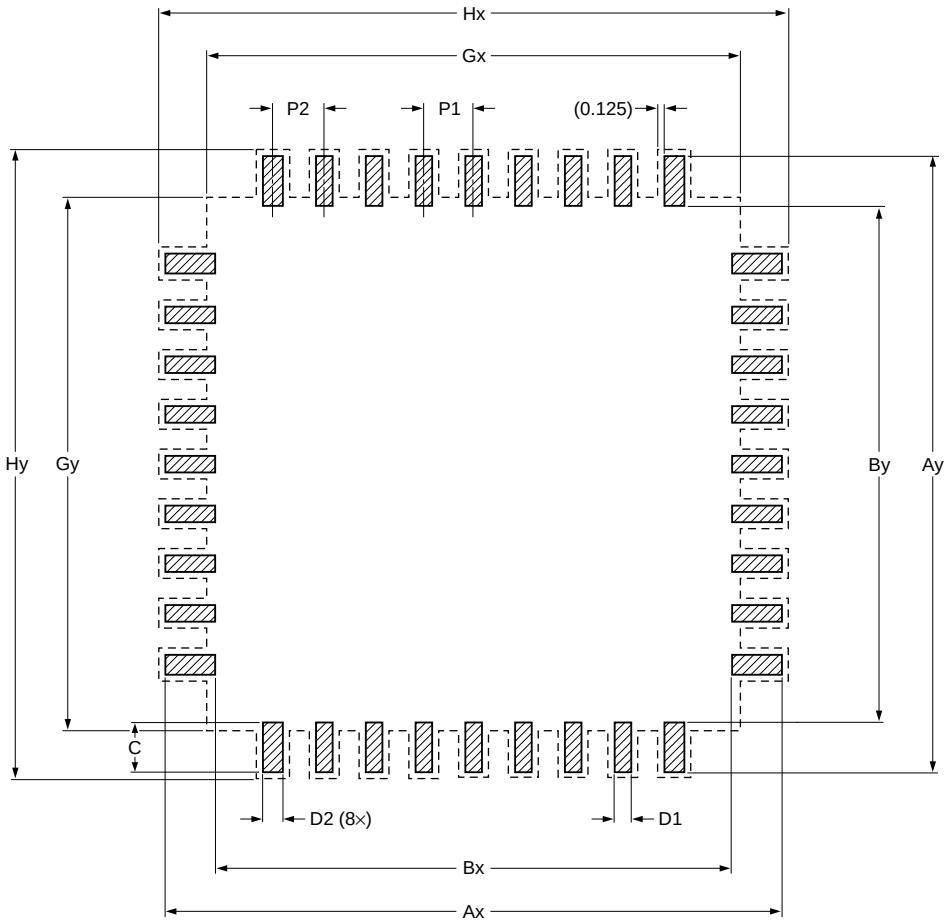
sot313-2_fr

Fig 37. Reflow soldering for the LQFP48 package

All information provided in this document is subject to legal disclaimers.

© NXP Semiconductors N.V. 2014. All rights reserved.

Footprint information for reflow soldering of LQFP64 package **SOT314-2**



Generic footprint pattern

Refer to the package outline drawing for actual layout

solder land

occupied area

DIMENSIONS in mm

P1	P2	Ax	Ay	Bx	By	C	D1	D2	Gx	Gy	Hx	Hy
0.500	0.560	13.300	13.300	10.300	10.300	1.500	0.280	0.400	10.500	10.500	13.550	13.550

sot314-2_fr

Fig 38. Reflow soldering for the LQFP64 package

All information provided in this document is subject to legal disclaimers.

© NXP Semiconductors N.V. 2014. All rights reserved.

14. Revision history

Table 19. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
LPC11E3X v.2.3	20140911	Product data sheet		LPC11E3X v.2.2
Modifications:	Added part LPC11E35FHI33/501.			
LPC11E3X v.2.2	20140114	Product data sheet	-	LPC11E3X v.2.1
Modifications:	ISP mode removed from pin PIO0_3 in Table 3.			
LPC11E3X v.2.1	20131230	Product data sheet	-	LPC11E3X v.2
Modifications:	Add reserved function to pins PIO0_8/MISO0/CT16B0_MAT0/R/IOH_6 and PIO0_9/MOSI0/CT16B0_MAT1/R/IOH_7.			
LPC11E3X v.2	20131121	Product data sheet	-	LPC11E3X v.1.1
Modifications:	• Parts LPC11E3HFBD64/401 added. • 8 kB SRAM block at 0x1000 000 renamed to SRAM0 in Figure 5. • I/O Handler pins added in Table 3. • Typical range of watchdog oscillator frequency changed to 9.4 kHz to 2.3 MHz. • Section 11.7 “I/O Handler software library applications” added. • Condition V_{DD} = 0 V added to Parameter V_I in Table 5 for clarity.			
LPC11E3X v.1.1	20130924	Product data sheet	-	LPC11E3X v.1
Modifications:	• Table 3: Added “5 V tolerant pad” to $\overline{\text{RESET}}$/PIO0_0 table note. • Table 7: Removed BOD interrupt level 0. • Added Section 11.5 “ADC effective input impedance”. • Programmable glitch filter is enabled by default. See Section 7.7.1. • Table 5 “Static characteristics” added Pin capacitance section. • Table 4 “Limiting values”: – Updated V_{DD} min and max. – Updated V_I conditions. • Table 10 “EEPROM characteristics”: – Removed f_{clk} and t_{er}; the user does not have control over these parameters. – Changed the t_{prog} from 1.1 ms to 2.9 ms; the EEPROM IAP always does an erase and program, thus the total program time is $t_{er} + t_{prog}$.			
LPC11E3X v.1	20121107	Objective data sheet	-	-

All information provided in this document is subject to legal disclaimers.

© NXP Semiconductors N.V. 2014. All rights reserved.

15. Legal information

15.1 Data sheet status

Document status[1][2]	Product status[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the Internet at URL http://www.nxp.com.

15.2 Definitions

Draft — The document is a draft version only. The content is still under internal review and subject to formal approval, which may result in modifications or additions. NXP Semiconductors does not give any representations or warranties as to the accuracy or completeness of information included herein and shall have no liability for the consequences of use of such information.

Short data sheet — A short data sheet is an extract from a full data sheet with the same product type number(s) and title. A short data sheet is intended for quick reference only and should not be relied upon to contain detailed and full information. For detailed and full information see the relevant full data sheet, which is available on request via the local NXP Semiconductors sales office. In case of any inconsistency or conflict with the short data sheet, the full data sheet shall prevail.

Product specification — The information and data provided in a Product data sheet shall define the specification of the product as agreed between NXP Semiconductors and its customer, unless NXP Semiconductors and customer have explicitly agreed otherwise in writing. In no event however, shall an agreement be valid in which the NXP Semiconductors product is deemed to offer functions and qualities beyond those described in the Product data sheet.

15.3 Disclaimers

Limited warranty and liability — Information in this document is believed to be accurate and reliable. However, NXP Semiconductors does not give any representations or warranties, expressed or implied, as to the accuracy or completeness of such information and shall have no liability for the consequences of use of such information. NXP Semiconductors takes no responsibility for the content in this document if provided by an information source outside of NXP Semiconductors.

In no event shall NXP Semiconductors be liable for any indirect, incidental, punitive, special or consequential damages (including - without limitation - lost profits, lost savings, business interruption, costs related to the removal or replacement of any products or rework charges) whether or not such damages are based on tort (including negligence), warranty, breach of contract or any other legal theory.

Notwithstanding any damages that customer might incur for any reason whatsoever, NXP Semiconductors' aggregate and cumulative liability towards customer for the products described herein shall be limited in accordance with the *Terms and conditions of commercial sale* of NXP Semiconductors.

Right to make changes — NXP Semiconductors reserves the right to make changes to information published in this document, including without limitation specifications and product descriptions, at any time and without notice. This document supersedes and replaces all information supplied prior to the publication hereof.

Suitability for use — NXP Semiconductors products are not designed, authorized or warranted to be suitable for use in life support, life-critical or safety-critical systems or equipment, nor in applications where failure or malfunction of an NXP Semiconductors product can reasonably be expected to result in personal injury, death or severe property or environmental damage. NXP Semiconductors and its suppliers accept no liability for inclusion and/or use of NXP Semiconductors products in such equipment or applications and therefore such inclusion and/or use is at the customer's own risk.

Applications — Applications that are described herein for any of these products are for illustrative purposes only. NXP Semiconductors makes no representation or warranty that such applications will be suitable for the specified use without further testing or modification.

Customers are responsible for the design and operation of their applications and products using NXP Semiconductors products, and NXP Semiconductors accepts no liability for any assistance with applications or customer product design. It is customer's sole responsibility to determine whether the NXP Semiconductors product is suitable and fit for the customer's applications and products planned, as well as for the planned application and use of customer's third party customer(s). Customers should provide appropriate design and operating safeguards to minimize the risks associated with their applications and products.

NXP Semiconductors does not accept any liability related to any default, damage, costs or problem which is based on any weakness or default in the customer's applications or products, or the application or use by customer's third party customer(s). Customer is responsible for doing all necessary testing for the customer's applications and products using NXP Semiconductors products in order to avoid a default of the applications and the products or of the application or use by customer's third party customer(s). NXP does not accept any liability in this respect.

Limiting values — Stress above one or more limiting values (as defined in the Absolute Maximum Ratings System of IEC 60134) will cause permanent damage to the device. Limiting values are stress ratings only and (proper) operation of the device at these or any other conditions above those given in the Recommended operating conditions section (if present) or the Characteristics sections of this document is not warranted. Constant or repeated exposure to limiting values will permanently and irreversibly affect the quality and reliability of the device.

Terms and conditions of commercial sale — NXP Semiconductors products are sold subject to the general terms and conditions of commercial sale, as published at http://www.nxp.com/profile/terms, unless otherwise agreed in a valid written individual agreement. In case an individual agreement is concluded only the terms and conditions of the respective agreement shall apply. NXP Semiconductors hereby expressly objects to applying the customer's general terms and conditions with regard to the purchase of NXP Semiconductors products by customer.

No offer to sell or license — Nothing in this document may be interpreted or construed as an offer to sell products that is open for acceptance or the grant, conveyance or implication of any license under any copyrights, patents or other industrial or intellectual property rights.

All information provided in this document is subject to legal disclaimers.

© NXP Semiconductors N.V. 2014. All rights reserved.

Export control — This document as well as the item(s) described herein may be subject to export control regulations. Export might require a prior authorization from competent authorities.

Non-automotive qualified products — Unless this data sheet expressly states that this specific NXP Semiconductors product is automotive qualified, the product is not suitable for automotive use. It is neither qualified nor tested in accordance with automotive testing or application requirements. NXP Semiconductors accepts no liability for inclusion and/or use of non-automotive qualified products in automotive equipment or applications.

In the event that customer uses the product for design-in and use in automotive applications to automotive specifications and standards, customer (a) shall use the product without NXP Semiconductors' warranty of the product for such automotive applications, use and specifications, and (b) whenever customer uses the product for automotive applications beyond NXP Semiconductors' specifications such use shall be solely at customer's own risk, and (c) customer fully indemnifies NXP Semiconductors for any liability, damages or failed product claims resulting from customer design and use of the product for automotive applications beyond NXP Semiconductors' standard warranty and NXP Semiconductors' product specifications.

15.4 Trademarks

Notice: All referenced brands, product names, service names and trademarks are the property of their respective owners.

I²C-bus — logo is a trademark of NXP B.V.

16. Contact information

For more information, please visit: **http://www.nxp.com**

For sales office addresses, please send an email to: **salesaddresses@nxp.com**

All information provided in this document is subject to legal disclaimers.

© NXP Semiconductors N.V. 2014. All rights reserved.

17. Contents

1 General description 1
2 Features and benefits 1
3 Applications 3
4 Ordering information 3
4.1 Ordering options 4
5 Block diagram 5
6 Pinning information 6
6.1 Pinning 6
6.2 Pin description 10
7 Functional description 18
7.1 On-chip flash programming memory 18
7.2 EEPROM 18
7.3 SRAM 19
7.4 On-chip ROM 19
7.5 Memory map 19
7.6 Nested Vectored Interrupt Controller (NVIC) 20
7.6.1 Features 20
7.6.2 Interrupt sources 21
7.7 IOCON block 21
7.7.1 Features 21
7.8 General-Purpose Input/Output GPIO 21
7.8.1 Features 22
7.9 I/O Handler (LPC11E37HFBD64/401 only) 22
7.10 USART 22
7.10.1 Features 22
7.11 SSP serial I/O controller 23
7.11.1 Features 23
7.12 I^2C-bus serial I/O controller 23
7.12.1 Features 23
7.13 10-bit ADC 24
7.13.1 Features 24
7.14 General purpose external event counter/timers 24
7.14.1 Features 24
7.15 System tick timer 25
7.16 Windowed WatchDog Timer (WWDT) 25
7.16.1 Features 25
7.17 Clocking and power control 25
7.17.1 Integrated oscillators 25
7.17.1.1 Internal RC oscillator 26
7.17.1.2 System oscillator 26
7.17.1.3 Watchdog oscillator 27
7.17.2 System PLL 27
7.17.3 Clock output 27
7.17.4 Wake-up process 27
7.17.5 Power control 27
7.17.5.1 Power profiles 27
7.17.5.2 Sleep mode 28
7.17.5.3 Deep-sleep mode 28
7.17.5.4 Power-down mode 28
7.17.5.5 Deep power-down mode 28
7.17.6 System control 29
7.17.6.1 Reset 29
7.17.6.2 Brownout detection 29
7.17.6.3 Code security (Code Read Protection - CRP) 29
7.17.6.4 APB interface 30
7.17.6.5 AHBLite 30
7.17.6.6 External interrupt inputs 30
7.18 Emulation and debugging 31
8 Limiting values 32
9 Static characteristics 33
9.1 BOD static characteristics 38
9.2 Power consumption 38
9.3 Peripheral power consumption 41
9.4 Electrical pin characteristics 43
10 Dynamic characteristics 46
10.1 Flash memory 46
10.2 External clock 46
10.3 Internal oscillators 47
10.4 I/O pins 48
10.5 I^2C-bus 48
10.6 SSP interface 50
11 Application information 53
11.1 XTAL input 53
11.2 XTAL Printed-Circuit Board (PCB) layout guidelines 54
11.3 Standard I/O pad configuration 55
11.4 Reset pad configuration 56
11.5 ADC effective input impedance 56
11.6 ADC usage notes 57
11.7 I/O Handler software library applications 57
11.7.1 I/O Handler I^2S 57
11.7.2 I/O Handler UART 57
11.7.3 I/O Handler I^2C 58
11.7.4 I/O Handler DMA 58
12 Package outline 59
13 Soldering 63
14 Revision history 67

continued >>

All information provided in this document is subject to legal disclaimers.

© NXP Semiconductors N.V. 2014. All rights reserved.

15 Legal information 68
15.1 Data sheet status 68
15.2 Definitions 68
15.3 Disclaimers 68
15.4 Trademarks 69
16 Contact information 69
17 Contents 70

Please be aware that important notices concerning this document and the product(s) described herein, have been included in section 'Legal information'.

© NXP Semiconductors N.V. 2014. All rights reserved.

For more information, please visit: http://www.nxp.com
For sales office addresses, please send an email to: salesaddresses@nxp.com

Date of release: 11 September 2014
Document identifier: LPC11E3X