Micro/Mini USB Interface with Integrated 28V Charger

Check for Samples: LP8727

FEATURES

- **USB Multiplexing Switches**
  - **High-Speed USB on USB and UART Inputs**
  - **Negative Voltage Rail on Audio Inputs**
  - **Internal LDO for ID Detection and MIC Bias**
  - **Compatible with USB Charging Specification Rev. 1.1**
  - **DSS Input for Default Switch Connection**
  - **Low-Power MIC Standby Mode**
- **Linear Charge with Single Input**
  - **28 OVP on VBUS Input**
  - **High-Current Mode for Production Test**
  - **Thermal Regulation**
- **Over-Voltage Protected LDO for USB Transceivers and PMU Wakeup**
- **UVLO (Undervoltage Lock Out)**
- **Interrupt Request to Reduce SW Polling**
  - **USB / ID Detection**
  - **SEND / END Button Detection**
  - **Mic Removal**
  - **OVLO / UVLO on VBUS**
  - **Charger Status**
- **Thermal Shutdown Protection**
- **I^2C-compatible Serial Interface**
- **25-Bump 0.4 mm Pitch Thin DSBGA Package**

APPLICATIONS

- **GSM, GPRS, EDGE, CDMA & WCDMA handsets**
- **Portable Media Players / MP3 Players**

DESCRIPTION

The LP8727 is designed to provide automatic multiplexing switches between Micro/Mini USB connector and USB, UART and Audio paths in cellular phone applications. It also contains a single-input Li-Ion battery charger and an overvoltage-protected LDO. Programming is handled via an I^2C-compatible Serial Interface allowing control of charger, multiplexing switches, and reading status information of the device.

The multiplexing switches on USB and UART support high-speed USB, and Audio inputs can be driven to negative voltage rail. The LP8727 is compatible with USB charging specifications rev 1.1 from USB IF.

The Li-Ion charger requires few external components and integrates the power FET. Charging is thermally regulated to obtain the most efficient charging rate for a given ambient temperature. It has Overvoltage Protection (OVP) circuit at the charger input protects the PMU from input voltages up to +28V, eliminating the need for any external protection circuitry.

An overvoltage-protected LDO which can supply up to 50 mA is designed for powering up a low-voltage USB transceiver or waking up a PMU (Power Management Unit) when an external power source (either USB VBUS or wall adapter) is connected to the USB connector.

The LP8727 PMU is available in 25-bump 0.4 mm pitch thin DSBGA package (2.015 mm x 2.015 mm).

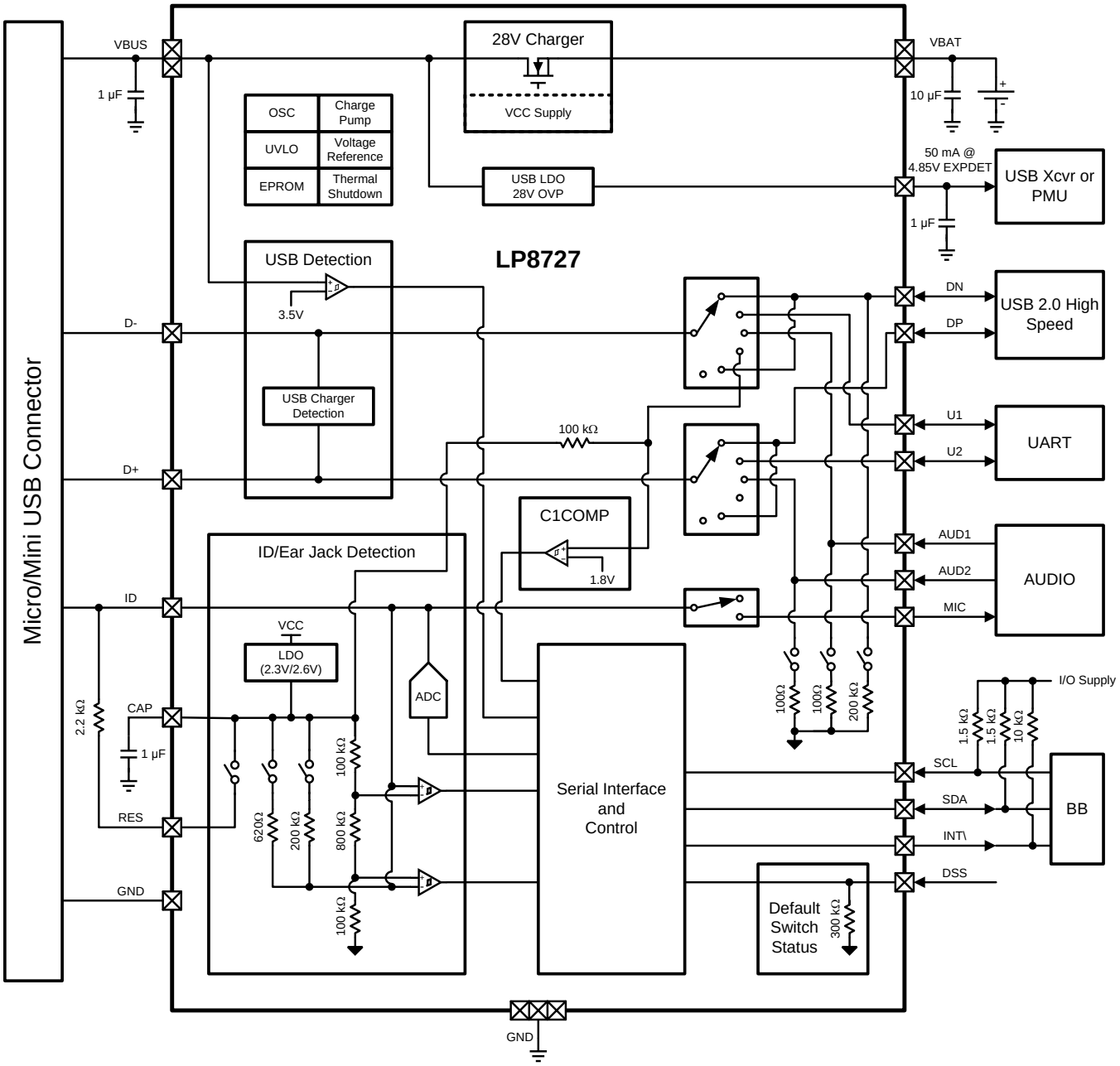
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Typical Application Diagram



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Connection Diagram

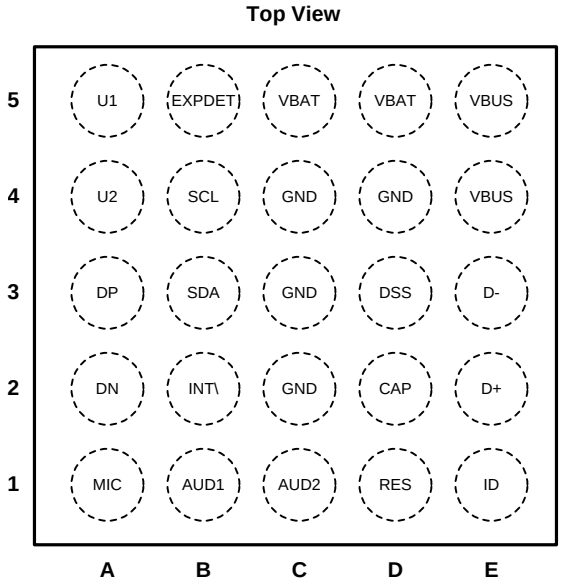


Figure 1. 25-Bump (0.4mm Pitch) DSBGA Package

LP8727 PIN DESCRIPTIONS(1)

PIN NAME	PIN #	TYPE	DESCRIPTION
AUD1	B1	AI	Stereo Audio input (Left).
AUD2	C1	AI	Stereo Audio input (Right).
CAP	D2	A	Internal LDO output. Connect a 1.0 µF ceramic capacitor to GND.
D-	E3	DI/O	Common data I/O. Connect to D- on Mini / Micro USB connector.
D+	E2	DI/O	Common data I/O. Connect to D+ on Mini / Micro USB connector.
DN	A2	DI/O	USB differential data I/O (-).
DP	A3	DI/O	USB differential data I/O (+).
DSS	D3	A	Default switch status input. Internally pulled down with a 300 kΩ resistor. Logic high for UART startup and logic low for USB startup.
EXPDET	B5	P	Overvoltage protected LDO output for low-voltage USB system. Connect a 1.0 µF ceramic capacitor to GND.
GND	C2, C3, C4, D4	G	Ground.
ID	E1	DI	USB ID Input. Connect to ID on Mini / Micro USB connector.
INT\	B2	DO	Open-drain output for interrupt, active low. Typ. 10 kΩ pull-up resistor is required.
MIC	A1	AO	Microphone output.
RES	D1	A	Bias output for ID detection and Microphone. Connect a 2.2 kΩ resistor to ID pin.
SCL	B4	DI	Serial interface clock input. Connect a 1.5 kΩ pullup resistor.
SDA	B3	DI/O	Serial interface data input/output. Connect a 1.5 kΩ pullup resistor.
U1	A5	DI/O	UART data Rx / USB differential data I/O (-).
U2	A4	DI/O	UART data Tx / USB differential data I/O (+).
VBAT	C5, D5	P	Main battery connection. Requires 10 µF ceramic capacitor when a battery is not connected.
VBUS	E4, E5	P	USB VBUS input.

(1) A: Analog Pin, D: Digital Pin, I: Input Pin, DI/O Digital Input/Output Pin, G: Ground, O: Output Pin, I/O: Input/Output Pin, P: Power Connection

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These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

Absolute Maximum Ratings[1][2][3][4]

INPUT VOLTAGE	VBUS to GND		−0.3V to +28V
	VBAT, EXPDET, CAP [wrt. GND]		−0.3V to +6.0V
	SCL, SDA, INT\, DSS [wrt. GND]		−0.3V to (V_{VBAT}+0.3V)
	CP_EN = 1	D+, D−, AUD1, AUD2	−2.1V to (V_{SWPOS}) + 0.3V)
		DP, DN, U1, U2, ID, MIC, RES	−0.3V to (V_{SWPOS}) + 0.3V)
	CP_EN = 0	D+, D−, DP, DN, AUD1, RES	−0.3V to (V_{CC} + 0.3V)
		AUD2, U1, U2, ID, MIC	
TEMPERATURE		Junction Temperature (T_{J-MAX})	150°C
		Storage Temperature Range	−65 to 150°C
		Maximum Lead Temperature(Soldering, 10 sec.)	260°C

(1) Absolute Maximum Ratings are limits beyond which damage to the device may occur. Operating Ratings are conditions under which operation of the device is ensured. Operating Ratings do not imply ensured performance limits. For ensured performance limits and associated test conditions, see the Electrical Characteristics tables.
(2) All voltages are with respect to the potential at the GND pin.
(3) If Military/Aerospace specified devices are required, please contact the TI Sales Office/Distributors for availability and specifications.
(4) Internal thermal shutdown circuitry protects the device fro permanent damage. Thermal shutdown engages at T_J = 150°C (typ.) and disengages at T_J = 130°C. Also engages at 160°C and disengages 115°C.

Operating Ratings[1][2]

INPUT VOLTAGE	VBAT	2.5V to 5.5V
	VBUS	3.5V to 7V
TEMPERATURE	Junction Temperature (T_J) Range	−40°C to 125°C
	Ambient Temperature (T_A) Range[3]	−40°C to 85°C

(1) Absolute Maximum Ratings are limits beyond which damage to the device may occur. Operating Ratings are conditions under which operation of the device is ensured. Operating Ratings do not imply ensured performance limits. For ensured performance limits and associated test conditions, see the Electrical Characteristics tables.
(2) All voltages are with respect to the potential at the GND pin.
(3) In applications where high power dissipation and/or poor package resistance is present, the maximum ambient temperature may have to be de-rated. Maximum ambient temperature (T_A-MAX) is dependent on the maximum operating junction temperature (T_J-MAX), The maximum power dissipation of the device in the application (PD-MAX) and the junction to ambient thermal resistance of the package (θ_{JA}) in the application, as given by the following equation: T_A-MAX = T_J-MAX (θ_{JA} x PD-MAX). Due to the pulsed nature of testing the part, the temp in the Electrical Characteristic table is specified as T_A = T_J.

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ESD Rating(1)

VBUS, VBAT, D+ D−, ID	IEC61000-4-2 In-module	±8kV Contact Discharge
	Testing @ USB Connector	±15kV Air Discharge
Human Body		±2 kV
Machine Model		±150V

(1) The human-body model is 100 pF discharged through 1.5 kΩ. The machine model is a 200 pF capacitor discharged directly into each pin, MIL-STD-883 3015.7.

Thermal Properties

Junction-to-Ambient Thermal Resistance (θ_{JA})(1) Thin DSBGA-25	46°C

(1) Junction-to-ambient thermal resistance is highly application and board layout dependent. In applications where high power dissipation exists, special care must be given to thermal dissipation issues in board design.

Electrical Characteristics(1)(2)

Limits in standard typeface are for T_J = 25°C. Limits in **boldface** type apply over the operating ambient temperature range (−40°C ≤ T_J ≤ +125°C). Unless otherwise noted, specifications apply to the Typical Application Circuit with V_{VBAT} = 3.7V, V_{VBUS} = 5V.

Symbol	Parameter	Conditions	Typ	Min	Max	Units
V_{VBAT}	VBAT Voltage Range			2.5	5.5	V
V_{VBUS}	VBUS Voltage Range			3.5	7	V
V_{CC}	Internal Supply Voltage	V_{VBUS} = 5V	4.2			
		V_{VBUS} = 0V	V_{VBAT}			
V_{SWPOS}	Positive Switch Regulator	V_{VBAT} > 3.6 or V_{VBUS} > 3.6	3.4	3.3	3.6	V
V_{SWNEG}	Negative Switch Regulator	V_{VBAT} > 3.6 or V_{VBUS} > 3.6	−1.8	−2.0	−1.7	V
UNDERVOLTAGE LOCKOUT						
$UVLO_{VBUS}$	Undervoltage Lockout Threshold range	VBUS Rising (Default)	3.9	3.7	4.1	V
		VBUS Falling (Default)	3.7	3.5	3.9	
$UVLO_{VBAT}$	Undervoltage Lockout Threshold range	VBAT Rising (Default)	2.9	2.7	3.1	
		VBAT Falling (Default)	2.7	2.5	2.9	
QUIESCENT CURRENTS						
$I_{VBAT\ (STBY)}$	VBAT Standby I_q	CP_EN = ADC_EN = SEMREM = 0 USB_DET_DIS = 1	3.8		**20**	µA
$I_{VBAT\ (SUP1)}$	VBAT Supply Current1	Register Default @ V_{VBAT} = 3.7V V_{VBUS} = 0V	42		**90**	
$I_{VBAT\ (SUP2)}$	VBAT Supply Current2	Register Default @ V_{VBAT} = 3.7V ADC_EN = SEMREM = 1, V_{VBUS} = 0V	60		**120**	
$I_{VBUS\ (STBY)}$	VBUS Standby I_q	CP_EN = ADC_EN = SEMREM = 0 USB_DET_DIS = CHG_OFF = 1, EXPDET_EN = 0	90		**200**	
$I_{VBUS\ (SUP)}$	VBUS Supply Current	Register Default @V_{VBUS} = 5V, No load on VBAT (No battery)	250		**400**	
LOGIC AND CONTROL INPUTS						
V_{IL}	Input Low Level	SDA, SCL			0.4	V
		DSS			0.4	
V_{IH}	Input High Level	SDA, SCL		1.4		V
		DSS		1.4		
I_{LEAK}	Input Current	All logic inputs Over pin Voltage range	**-5**		**+5**	µA
DSS_{IN}	Input Resistance(2)	DSS Pulldown Resistor to GND	300			kΩ

(1) All voltages are with respect to the potential at the GND pin.
(2) Min and Max limits are specified by design, test or statistical analysis. Typical numbers are not ensured, but do represent the most likely norm.

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Electrical Characteristics[1][2] (continued)

Limits in standard typeface are for T_J = 25°C. Limits in **boldface** type apply over the operating ambient temperature range (−40°C ≤ T_J ≤ +125°C). Unless otherwise noted, specifications apply to the Typical Application Circuit with V_{VBAT} = 3.7V, V_{VBUS} = 5V.

Symbol	Parameter	Conditions	Typ	Min	Max	Units
LOGIC AND CONTROL OUTPUTS						
V_{OL}	Output Low Level	INT\, I_{OUT} = 2mA			0.4	V
		SDA, I_{SINK} = 3mA			0.4	
ID DETECTION LDO						
V_{OUT}	Output Voltage Accuracy	I_{OUT} = 500 µA, V_{OUT} = 2.3V I_{OUT} = 500 µA, V_{OUT} = 2.6V		**-3**	**+3**	%
I_{OUT}	Output Current Rating				1	mA
e_N	Output Noise Voltage	10 Hz ≤ f ≤ 100 kHz C_{OUT} = 1µF[2]	15			μV_{RMS}
PSRR	Power Supply Ripple Rejection Ratio	f = 10 kHz, C_{OUT} = 1µF I_{OUT} = 20 mA[2]	75			dB
C_{OUT}	External Output Capacitance for Stability	See[2]	1.0	0.6	20	µF
EXPDET LDO						
V_{OUT}	Output Voltage Accuracy	I_{OUT} = 1mA, V_{OUT} = 4.85V @ V_{VBUS} = 5V		**-5**	**+3**	%
V_{DO}	Dropout Voltage	I_{OUT} = 50 mA @ V_{VBUS} = 5V	330			mV
$I_{OUT(MAX)}$	Output Current Rating				50	mA
I_{SC}	Short Circuit Current Limit	V_{OUT} = 0V	330			mA
C_{OUT}	External Output Capacitance for Stability	See[3]	1.0	0.6	20	µF

(3) Min and Max limits are specified by design, test or statistical analysis. Typical numbers are not ensured, but do represent the most likely norm.

Multiplexer Switches Electrical Characteristics

Typical values and limits appearing in normal type apply for T_J=25°C. Unless otherwise noted, V_{VBAT} = 3.7V, VBUS is disconnected. Limits appearing in **boldface** type apply over the entire junction temperature range for operation, T_J = −40°C to +125°C.[1]

Symbol	Parameter	Conditions	Typ	Min	Max	Units
$V_{DP,DN}$	Analog Signal Range	CP_EN = 0		0	V_{CC}	V
		CP_EN = 1		0	V_{SWPOS}	
$R_{SWONUSB}$	On Resistance	0V < V_{D+} or V_{D-}< 1V	2.5		6	Ω
$\Delta R_{SWONUSB}$	On Resistance Match Between Channels				0.5	
$R_{FLATUSB}$	On Resistance Flatness		0.5			
$I_{LEAKUSB(OFF)}$	Off Leakage Current[2]	0V < V_{D+} or V_{D-}< 3.3V, CP_EN = 1		−360	360	nA
$I_{LEAKUSB(ON)}$	On Leakage Current[2]			−360	360	
UART ANALOG SWITCHES (U1, U2)						
$V_{U1, U2}$	Analog Signal Range	CP_EN = 0		0	V_{CC}	V
		CP_EN = 1		0	V_{SWPOS}	
$R_{SWONART}$	On Resistance	0V < V_{D+} or V_{D-}< 1V	2.5		6	Ω
$\Delta R_{SWONART}$	On Resistance Match Between Channels				0.5	
$R_{FLATURT}$	On Resistance Flatness		0.5			

(1) Junction-to-ambient thermal resistance is highly application and board layout dependent. In applications where high power dissipation exists, special care must be given to thermal dissipation issues in board design.
(2) Min and Max limits are specified by design, test or statistical analysis. Typical numbers are not ensured, but do represent the most likely norm.

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Multiplexer Switches Electrical Characteristics (continued)

Typical values and limits appearing in normal type apply for T_J=25°C. Unless otherwise noted, V_{VBAT} = 3.7V, VBUS is disconnected. Limits appearing in **boldface** type apply over the entire junction temperature range for operation, T_J = −40°C to +125°C.(1)

Symbol	Parameter	Conditions	Typ	Min	Max	Units
$I_{LEAKUART(OFF)}$	Off Leakage Current(2)	0V < V_{D+} or V_{D-}< 3.3V, CP_EN = 1		−360	360	nA
$I_{LEAKUART(ON)}$	On Leakage Current(2)			−360	360	
AUDIO ANALOG SWITCHES (AUD1, AUD2)						
$V_{AUD1,\ AUD2}$	Analog Signal Range	CP_EN = 0		0	V_{CC}	V
		CP_EN = 1		V_{SWNEG}	V_{SWPOS}	
$R_{SWONAUD}$	On Resistance	−1.8V < V_{D+} or V_{D-}< 1.8V	1.6		3.6	Ω
$\Delta R_{SWONAUD}$	On Resistance Match Between Channels				0.2	
$R_{FLATAUD}$	On Resistance Flatness		0.5			
$I_{LEAKUAUD(OFF)}$	Off Leakage Current(2)	−1.8V < V_{D+} or V_{D-}< 1.8V, CP_EN = 1		−360	360	nA
$I_{LEAKUAUD(ON)}$	On Leakage Current(2)			−360	360	
R_{SHUNT}	Shunt Resistor	I_{SHUNT} = 10 mA	100	30	180	Ω
MIC ANALOG SWITCHES (MIC)						
V_{MIC}	Analog Signal Range	CP_EN = 0		0	V_{CC}	V
		CP_EN = 1		V_{SWNEG}	V_{SWPOS}	
$R_{SWONMIC}$	On Resistance	0V < V_{ID}< 1.6V	3		10	Ω
$R_{FLATMIC}$	On Resistance Flatness		0.8			
$I_{LEAKMIC(OFF)}$	Off Leakage Current(2)			−360	360	nA
$I_{LEAKMIC(ON)}$	On Leakage Current(2)			−360	360	
DYNAMIC						
T_{CP_EN}	Charge Pump Startup Time				1	ms
$T_{MICLPDP}$	MIC Low-Power Detection Pulse Time	MIC_LP = 1, SEMREM = 1	117	50	175	µs
T_{MICLPD}	MIC Low-Power Detection Period		100	45	155	ms
T_{DEB}	Comparator Debounce Time		60	30	100	
T_{ONSW}	Analog Switch Turn-on Time	RL = 50Ω(3)(4)			1	
T_{OFFSW}	Analog Switch Turn-off Time				10	µs
T_{BBM}	Break-Before-Make			0		
V_{ISO}	Off-Isolation(5)	R_L = 50Ω, C_L = 5pF, f= 20 kHz V_{D+} or V_{D-}= $1V_{RMS}$ (6)(4)	−108			dB
V_{CT}	Crosstalk		−107			
$THD+N_{AUD}$	Total Harmonic Distortion Plus Noise AUD1, AUD2	f = 20 Hz to 20 kHz, V V_{D+} or V_{D-}= $0.25V_{RMS}$, R_L = 30Ω, DC Bias = 0V, T = 25°C	0.05			%
	Total Harmonic Distortion Plus Noise MIC	f = 20 Hz to 20 kHz, V V_{D+} or V_{D-}= $0.4V_{RMS}$, R_L = 1kΩ, DC Bias = 0.8V, T = 25°C	0.05			

(3) All timing is measured using 10% and 90% levels.
(4) Min and Max limits are specified by design, test or statistical analysis. Typical numbers are not ensured, but do represent the most likely norm.
(5) Off-isolation = 20log [$V_{D+/D-}$ / ($V_{NO1/2}$or $V_{NC1/2}$), $V_{D+/D-}$ = output, $V_{NO1/2}$ or $V_{NC1/2}$ = input to off switch.
(6) Crosstalk is measured between any two switches.

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Charger Electrical Characteristics

Typical values and limits in standard typeface are for T_J = 25°C. Limits in **boldface** type apply over the entire junction temperature range (−40°C to +125°C).(1)(2)(3)

Symbol	Parameter	Conditions	Typ	Min	Max	Units
V_{OV}	Over Voltage Protection Threshold	Charger input is turned off if voltage is above this threshold	6.9	6.7	7.2	V
V_{OV_HYS}	Over Voltage Protection Threshold Hysteresis		170	120	220	mV
V_{VBUS}	VBUS Operating Range			**4.45**	**6**	V
V_{OK_CHG}	VBUS OK Trip Point	V_{VBUS} - V_{VBAT} (Rising)	250			mV
		V_{VBUS} - V_{VBAT} (Falling)	40			
V_{TERM}	Termination Voltage	V_{TERM} = 4.2V, I_{CHG} = 50 mA		−0.35	+0.35	%
		V_{TERM} is measured at 10% of the programmed I_{CHG} current		**−1**	**+1**	
R_{DSON_CHG}	Charger pass transistor ON resistance	I_{CHG} = 400 mA	250		**400**	mΩ
I_{CHG}	VBUS Programmable Full-Rate Charging Current	4.45V ≤ V_{VBUS} ≤ 6V V_{VBAT} < V_{VBUS} - V_{OK_VBUS} V_{FULL_RATE} < V_{VBAT} < V_{TERM}(4)		**90**	**1100**	mA
	Full-rate charging current tolerance	I_{CHG} = 400 mA		**−5**	**+5**	%
I_{PRECHG}	Pre-charge current	2.2V < V_{VBAT} < V_{FULL_RATE} 80 mA option selected	80	**60**	**100**	mA
$I_{VBUS(MAX)}$	Maximum Input Current	V_{VBUS} - V_{VBAT} ≤ 0.8V			2.3	A
V_{FULL_RATE}	Full-rate Qualification Threshold	V_{VBAT} Rising, Transition from Pre-charge to Full-rate Charging	2.6	**2.5**	**2.7**	V
I_{EOC}	End-of-charge Current, % of Full-rate Current	0.1C option selected	10			%
T_{REG}	Regulated Junction Temperature	115°C option selected(5)	115			°C
DETECTION AND TIMING(5)						
$V_{VBUSDET}$	VBUS Detection Threshold		3.5	**3**	**4**	V
T_{POK}	Power OK Debounce Time	V_{VBUS} > V_{VBAT} + V_{OK_CHG}	30			ms
T_{PRE_FULL}	Debounce Time from Pre-Charge to Full-rate Transition	Pre-charge to full-rate charging transition	55			
T_{EOC}	Debounce Time from CV to End-of-Charge Transition		400			ms
T_{CHG}	Charge Safety Timer	Pre-charge Mode	45			minutes

(1) Junction-to-ambient thermal resistance is highly application and board layout dependent. In applications where high power dissipation exists, special care must be given to thermal dissipation issues in board design.
(2) Dropout voltage is the voltage difference between the input and the output at which the output voltage drops to 100 mV below its nominal value.
(3) The parameters in the electrical characteristic table are tested under open loop conditions at V_{bat} = 3.7 unless otherwise specified. For performance over the input voltage range and closed loop condition, refer to the datasheet curves.
(4) The minimum input voltage equals V_{OUT} (nom) + 0.5V or 2.5V, which ever is greater.
(5) Min and Max limits are specified by design, test or statistical analysis. Typical numbers are not ensured, but do represent the most likely norm.

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LP8727 Control Registers

I²C-Compatible Slave Address: 7'h27 (6)

ADDR	REGISTER	POR DEFAULT	BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0
0x00	DEVICE ID	0011xxxx	**VENDOR ID**				**CHIP_REV**			
0x01	CONTROL1	x0000001	RESV'D	ID_2P2	ID_620	ID_200	VLDO	SEMREN	ADC_EN	CP_EN
0x02	CONTROL2	0000xx01	INTPOL	INT_EN	MIC_LP	CP_AUD	RESV'D	RESV'D	CHG_TYP	USB_DET_DIS
0x03	SW CONTROL	x0000000	RESV'D	MIC_ON	DP2			DM1		
0x04	INT_STAT1	00000000	**CHGDET**	**MR_COMP**	**SEND/END**	**VBUS**	**IDNO**			
0x05	INT_STAT2	00000000	**CHG**	**TSHD**	**TMP**	**OVLO**	**UVLO**	**RESV'D**	**RESV'D**	**RESV'D**
0x06	STATUS1	00000000	**DCPORT**	**CHPORT**	**CHG_STAT**		**RESV'D**	**RESV'D**	**RESV'D**	**C1COMP**
0x07	STATUS2	00000000	**TMP_STAT**			**RESV'D**	**RESV'D**	**RESV'D**	**RESV'D**	**RESV'D**
0x08	CHARGER CONTROL1	010010xx	CHG_EN	EXPDET_EN	PTM	CHG_OFF	IPRECHG		RESV'D	RESV'D
0x09	CHARGER CONTROL2	0010x001	CHG_SET				RESV'D	IMIN_SET		

(6) (**Bolded** locations are Read-Only Bits.)
Resv'd = Reserved

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DETAILED REGISTER DESCRIPTIONS(1)

ADDR	REGISTER NAME	BIT NAME	BIT	POR DEFAULT	DESCRIPTION
0x00	DEVICE ID	CHIP_REV	[3:0]	xxxx	Chip revision.
		VENDOR ID	[7:4]	0011	Texas Instruments vendor ID.
0x01	CONTROL1	CP_EN	0	1	Enable charge pump for analog switch operation. When CP_EN = 0, input signals to the analog switches should not go below GND. 0: Disable 1: Enable
		ADC_EN	1	0	Enable ID detection LDO and internal ADC. 0: Disable 1: Enable
		SEMREN	2	0	Enable ID detection LDO and SEND/END & MR comparators. 0: Disable 1: Enable
		VLDO	3	0	ID detection LDO voltage setting. 0: 2.3V 1: 2.6V
		ID_200	4	0	Connect ID detection LDO to ID pin through an internal 200 kΩ resistor. 0: Disable 1: Enable
		ID_620	5	0	Connect ID detection LDO to ID pin through an internal 620Ω resistor. 0: Disable 1: Enable
		ID_2P2	6	0	Connect ID detection LDO to RES output for microphone biasing. A 2.2 kΩ external resistor is required between RES and ID pins. 0: Disable 1: Enable
		RESERVED	7	x	Not used.

(1) **Bolded** entries are read-only.

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ADDR	REGISTER NAME	BIT NAME	BIT	POR DEFAULT	DESCRIPTION
0x02	CONTROL2	USB_DET_DIS	0	1	Disable USB charger detection. 0: Enable 1: Disable
		CHG_TYP	1	0	Enable charger type detection. CHG_TYP will be automatically set to 0 at the end of detection sequence. 0: Disable 1: Enable
		RESERVED	[3:2]	xx	Not used.
		CP_AUD	4	0	Enable internal 100Ω pull-down resistors on AUD1 and AUD2. 0: Disable 1: Enable
		MIC_LP	5	0	Enable microphone low-power mode. 0: Disable 1: Enable
		INT_EN	6	0	Enable interrupt output. When disabled, INT\ output will be masked and pending interrupts will not be cleared. 0: Disable 1: Enable
		INTPOL	7	0	Interrupt polarity setting. 0: Active low 1: Active high
0x03	SW CONTROL	DM1	[2:0]	000	Set the switch connection to D- pin. 000: D- pin is connected to DN pin. 001: D- pin is connected to U1 pin. 010: D- pin is connected to AUD1 pin. 011: D- pin is connected to C1COMP. 100: D- pin is connected to DN pin regardless of VBUS 101 to 111: Hi-Z
		DP2	[5:3]	000	Set the switch connection to D+ pin. 000: D+ pin is connected to DP pin. 001: D+ pin is connected to U2 pin. 010: D+ pin is connected to AUD2 pin. 011: Hi-Z 100: D+ pin is connected to DP pin regardless of VBUS 101 to 111: Hi-Z
		MIC_ON	6	0	Connect MIC pin to ID pin. 0: Disable 1: Enable
		RESERVED	7	x	Not used.

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ADDR	REGISTER NAME	BIT NAME	BIT	POR DEFAULT	DESCRIPTION
0x04	INT_STAT1	**IDNO**	[3:0]	0000	ADC output with 200 kΩ / 2.2 kΩ / 620Ω of pullup resistor (Activated only when ADC_EN = '1'). Change of IDNO state will trigger assertion of INT\ output. (Refer to Table 1)
		VBUS	4	0	VBUS comparator output. Change of VBUS state will trigger assertion of INT output. 0: $V_{VBUS} < V_{VBUSDET}$ 1: $V_{VBUS} > V_{VBUSDET}$
		SEND/END	5	0	SE comparator output (Activated only when SEMREN = '1). Change of SEND/END state will trigger assertion of INT\ output. 0: $V_{MIC} > V_{SEND/END}$ 1: $V_{MIC} < V_{SEND/END}$
		MR_COMP	6	0	MR comparator output (Activated only when SEMREN = '1'). Change of MR_COMP state will trigger assertion of INT\ output. 0: $V_{MIC} < V_{MR_COMP}$ 1: $V_{MIC} > V_{MR_COMP}$
		CHG_DET	7	0	Charger detection is completed. Change of CHG_DET state will trigger assertion of INT\ output. 0: VBUS is not present or no charger is detected. 1: Charger is detected.
0x05	INT_STAT2	**RESERVED**	[2:0]	000	Not used.
		UVLO	3	0	0: $V_{VBUS} > UVLO_{USB}$ 1: $V_{VBUS} < UVLO_{USB}$
		OVLO	4	0	0: $V_{VBUS} < V_{OV}$ 1: $V_{VBUS} > V_{OV}$
		TMP	5	0	0: TMP_STAT state is not changed. 1: TMP_STAT state is changed.
		TSHD	6	0	0: Thermal shutdown is not triggered. 1: Thermal shutdown is triggered.
		CHG	7	0	0: CHG_STAT state is not changed. 1: CHG_STAT state is changed.
0x06	STATUS1	**C1COMP**	0	0	C1COMP output. 0: $V_{D-} < V_{D-DET}$ 1: $V_{D-} > V_{D-DET}$
		RESERVED	[3:1]	000	Not used.
		CHG_STAT	[5:4]	00	Charger status. 00: Pre-charge 01: CC 10: CV 11: EOC
		CHPORT	6	0	0: High-current USB Host/Hub is not detected. 1: High-current USB Host/Hub is detected.
		DCPORT	7	0	0: Dedicated charger is not detected. 1: Dedicated charger is detected.

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ADDR	REGISTER NAME	BIT NAME	BIT	POR DEFAULT	DESCRIPTION
0x07	STATUS2	**RESERVED**	[4:0]	00000	Not used.
		TMP_STAT	[7:5]	000	Die temperature. 000: 75°C 001: 95°C 010: 115°C 011: 135°C 100: Reserved 101: Reserved 110: Reserved 111: Reserved
0x08	CHARGER CONTROL1	RESERVED	[1:0]	xx	Not used.
		IPRECHG	[3:2]	10	Pre-charge current setting. 00: 40 mA 01: 60 mA 10: 80 mA 11: 100 mA
		CHG_OFF	4	0	Charger block disable. 0: Enable 1: Disable
		PTM	5	0	Enable PTM (Production Test Mode). 0: Disable 1: Enable
		EXPDET_EN	6	1	Enable EXPDET LDO. 0: Disable 1: Enable
		CHG_EN	7	0	Charger stop / start control. 0: Stop charging (Force EOC). 1: Start charging (Restart).
0x09	CHARGER CONTROL2	IMIN_SET	[2:0]	001	EOC level setting. 000: 5% 001: 10% 010: 16% 011: 20% 100: 25% 101: 33% 110: 50%
		RESERVED	3	x	Not used.
		CHG_SET	[7:4]	0010	Charging current setting. 0000: 90 mA 0001: 100 mA 0010: 400 mA 0011: 450 mA 0100: 500 mA 0101: 600 mA 0110: 700 mA 0111: 800 mA 1000: 900 mA 1001: 1000 mA

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Operation Description

MULTIPLEXING SWITCHES

The LP8727 supports USB High-speed, UART and stereo audio & microphone by providing automatic multiplexing switches between Micro/Mini USB connector and USB, UART and Audio paths in cellular phone applications. The LP8727 detects the external devices which can be connected to Micro/Mini USB connector and informs the processor the detection result by generating an interrupt. But, the LP8727 does not automatically change the state of switch mux when the external device is detected. The processor is responsible to change the state of switch mux via I^2C.

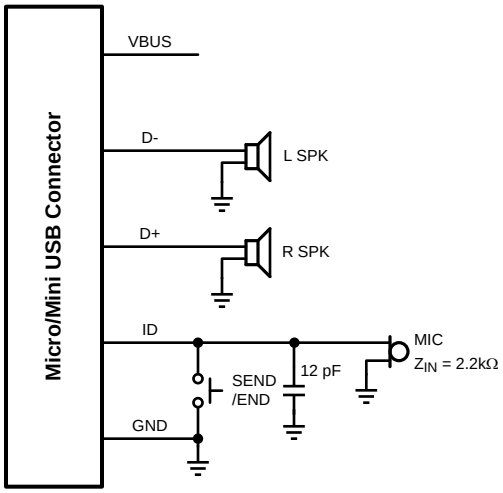


Figure 2. Stereo Audio & MIC Connection

DEFAULT SWITCH STATUS

The LP8727 can configure default switch connection at startup to either USB or UART by the DSS input. The DSS input has a 300 kΩ of internal pulldown resistor. When DSS is logic low (connected to GND or left floating), the default switch connection is set to USB. For UART startup, the DSS should be pulled high to VBAT through an external 300 kΩ pull-up resistor. The status of DSS input is monitored from the startup of device and will be latched at the first rising edge of SCL input. The status of DSS input is monitored and latched at the 1st rising edge of sCL input.

HIGH-IMPEDANCE MODE

If the LP8727 is powered from VBAT (VBUS is not present), the default switch connections for D+, D- and ID should be Hi-Z regardless of DSS status until USB & ID detection is done. The high-impedance mode should also be controlled via I^2C.

LOW-POWER MODE

The LP8727 is designed to support low-power modes by CP_EN, ADC_EN and SEMREN bits on CONTROL1 register. The ID detection LDO is controlled by either ADC_EN or SEMREN bits.

- CP_EN: When CP_EN bit is set to ‘1’, the charge pump is enabled and this allows the audio signal inputs (AUD1 and AUD2) to be driven to negative voltage rail.
- ADC_EN: When ADC_EN bit is set to ‘1’, ID detection LDO and the internal ADC are enabled. When ADC_EN is ‘0’, IDNO bits (ADC output) will be 4’h0000 and INT\ will not be asserted. Any pending interrupts due to a change in the ADC output will not be cleared and must be cleared manually by reading INT_STATx registers.
- SEMREN: When SEMREN bit is set to ‘1’, ID detection LDO and the internal comparators for SEND/END and microphone removal detections are enabled. When SEMREN is ‘0’, the SEND/END and MR_COMP registers will be set to ‘0’ and INT\ will not be asserted. Any pending interrupts due to a change in the SEND/END or MR_COMP comparators will not be cleared and must be cleared manually by reading INT_STATx registers.

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SEND/END BUTTON AND MICROPHONE REMOVAL DETECTION

The LP8727 supports SEND/END button and microphone removal detection features by monitoring voltage on ID pin. When the microphone is connected to ID pin, it is biased by RES output through an external 2.2 kΩ resistor. In the event of removal of the microphone, the voltage on ID pin will go as high as the bias voltage which is typically 2.3V, and this event will be detected by a comparator. The threshold for microphone removal detection will be set to 90% of the bias voltage.

Headset accessories have a push button switch (SEND/END) between the ID pin and GND. In case that SEND/END button is pressed, the voltage on ID pin will drop down to GND potential, and an internal comparator is used to detect this event. The typical threshold of SEND/END button detection is set to 10% of the bias voltage.

Both cases will generate interrupts to the host processor.

MICROPHONE LOW-POWER MODE

When the microphone is connected, it is powered from RES output through an external 2.2 kΩ (typ.) resistor. In case that the microphone is connected but not active, the LP8727 allows reducing the power dissipation at the microphone, while it is still supporting SEND/END button and microphone removal detection.

During the microphone low-power mode, the internal 200 kΩ resistor will be turned on for immediate microphone removal detection, and RES output will cycling ON and OFF with a short period of time for SEND/END detection.

The microphone low-power mode is enabled by MIC_LP bit, and interrupts will be generated by SEND/END and MR_COMP events.

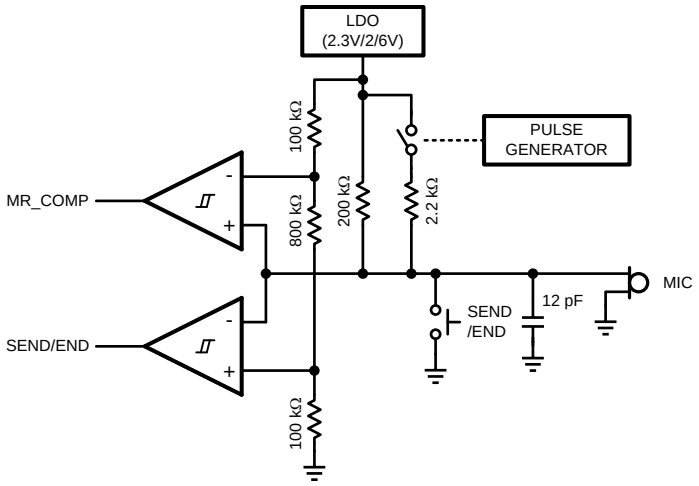


Figure 3. MIC Low-Power Operation

EXPDET LDO

The EXPDET is overvoltage protected LDO output for low-voltage USB transceiver on the processor, or it can be used as a startup trigger signal for the PMU.

The EXPDET LDO is directly powered from VBUS and can withstand up to 28V. The typical output voltage is set to 4.85V and it is designed to supply up to 50 mA. For stable operation, a 1µF ceramic capacitor is required at the output.

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INTERRUPT STATUS

The LP8727 has 2 interrupt status registers, INT_STAT1 and INT_STAT2. These interrupt conditions are generated from VBUS comparator, D+/D− & ID detection, changes of SEND/END & MR_COMP states and charger events. When any of these interrupt conditions occur, then the open drain output (INT\) will be brought low. This signals to the BB processor that an interrupt has occurred. The BB processor will then read all two INT_STAT1 and INT_STAT2 registers sequentially through the serial interface to determine which bit caused the interrupt. Once the status register indicates the actual interrupt condition starts to be read, the INT\ output will be brought high immediately. However, INT_STAT1 and INT_STAT2 registers will not be cleared after being read by the BB processor and will always represent the current status.

INT\ OUTPUT

A serial interface read of each of the interrupt status registers immediately pulls up INT\ output. If an interrupt is captured during a read sequence, the INT\ will not go low until at least 24 serial clocks (SCL) have occurred. Any pending interrupts will be cleared once the LP8727 goes into SHUTDOWN mode.

DEVICE STATUS

The LP8727 has 2 device status registers, STATUS1 and STATUS2. These registers can be read via the serial interface in much the same way as the interrupt status registers.

These registers will not be cleared on a read and will always represent the current state.

Device Identification

The LP8727 can recognize various accessories attached to Micro/Mini USB connector by detecting VBUS, D+, D− and ID pins. The detection comparators have a 60 ms of debounce timer. The device identification flow is shown in Figure 4.

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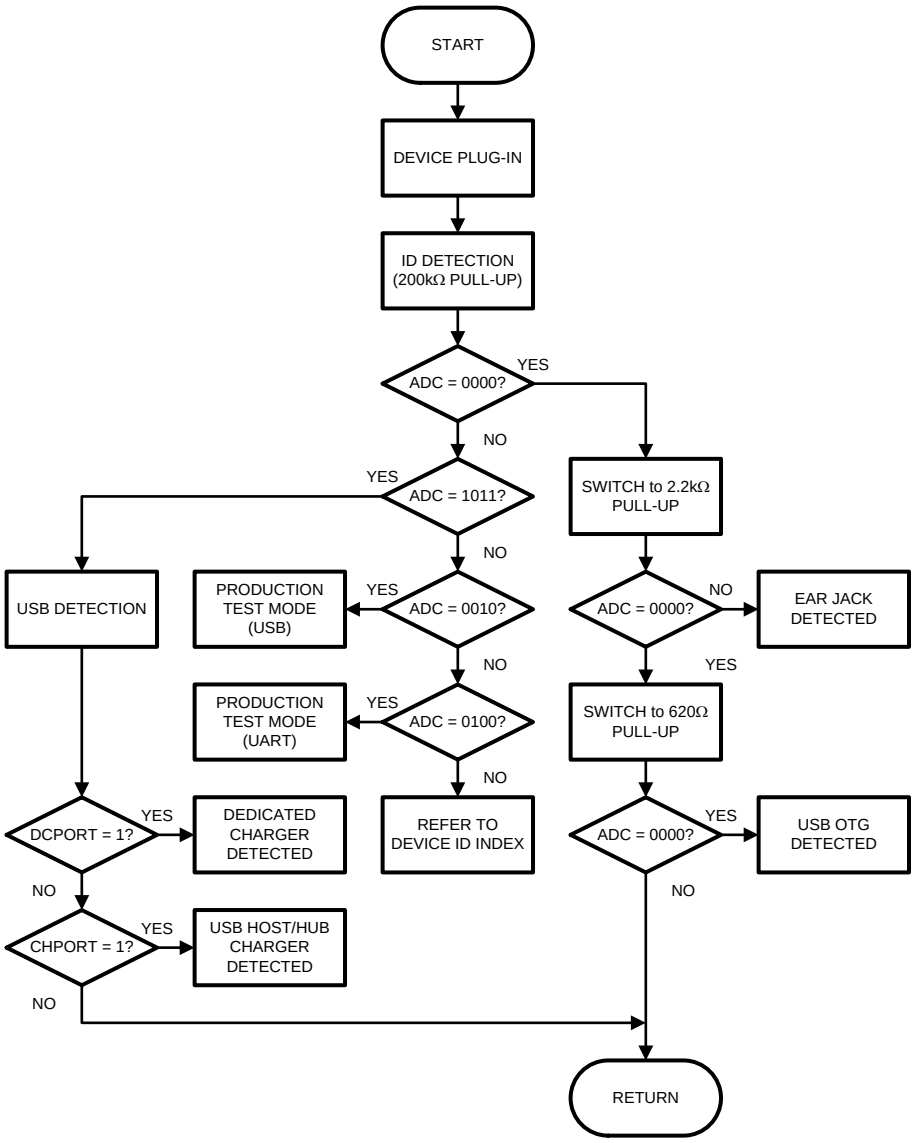


Figure 4. Device Identification Diagram

ID DETECTION

When the external device is connected to Micro/Mini USB connector, the LP8727 reads the voltage of ID pin using an ADC while the ID pin is pulled up to the output of ID DETECTION LDO (typ. 2.3V) through the internal 200 kΩ resistor. If ADC value code is 4'h0000, the LP8727 will change the pullup resistor from 200 kΩ to 2.2 kΩ and eventually to 620Ω step-by-step for detecting microphone and USB OTG. In case that the first ADC reading gives 4'h1011, then the LP8727 will start USB detection according to USB Battery Charging Specification Revision 1.1.

Table 1. Device Indentification Index

ADC VALUE	ADC VOLTAGE	ID RESISTOR [kΩ]	D+ CONDITION	D−CONDITION	VBUS [V]	FUNCTION
DETECTION VALUES with 200 kΩ PULL-UP RESISTOR						
1011	100%	OPEN	15 kΩ to GND	15 kΩ to GND	5	USB Cable
1011	100%	OPEN	Shorted to D−	Shorted to D+	5.6	TA Charger
1010	81.90%	910				Reserved

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Table 1. Device Indentification Index (continued)

ADC VALUE	ADC VOLTAGE	ID RESISTOR [kΩ]	D+ CONDITION	D−CONDITION	VBUS [V]	FUNCTION
1001	75.60%	620				Reserved
1000	68.20%	430				Reserved
0111	62.20%	330				Reserved
0110	54.50%	240				Reserved
0101	47.40%	180			5	TA for North America
0100	39.40%	130	TX	RX	5	UART (Factory)
0011	33.30%	100				Reserved
0010	21.90%	56	D+	D-	5	USB (Factory)
0001	12.50%	28.7				VZW
0000	0%	MIC	Speaker	Speaker		Microphone
0000	0%	GND	D+	D-		USB OTG
DETECTION VALUES with 2.2 kΩ PULL-UP RESISTOR						
1011 to 1000	100% to 68.2%					Reserved
0111 to 0100	62.2% to 39.4%					Typical Microphone
001 to 0001	33.3% to 12.5%					Reserved
0000	0%	GND	D+	D-		USB OTG
DETECTION VALUES with 620Ω PULL-UP RESISTOR						
1011 to 0001	100% to 12.5%					Reserved
0000	0%	GND	D+	D−		USB OTG

USB DETECTION

The LP8727 can detect dedicated charger, standard downstream port and charging downstream port based on USB Battery Charging Specification Revision 1.1. In order to avoid false detection before data (D+ and D−) connection, the LP8727 supports ‘Data Contact Detect’ feature.

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Operating Characteristics

USB Eye Diagram (480 MHz)

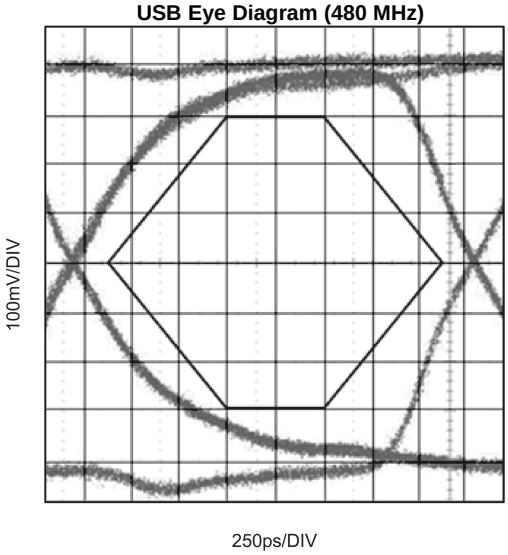


Figure 5.

UART Eye Diagram (480 MHz)

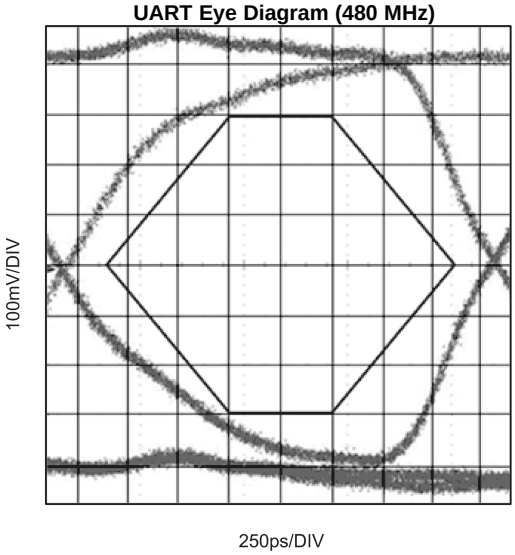


Figure 6.

USB Frequency Response (10 MHz - 1GHz)

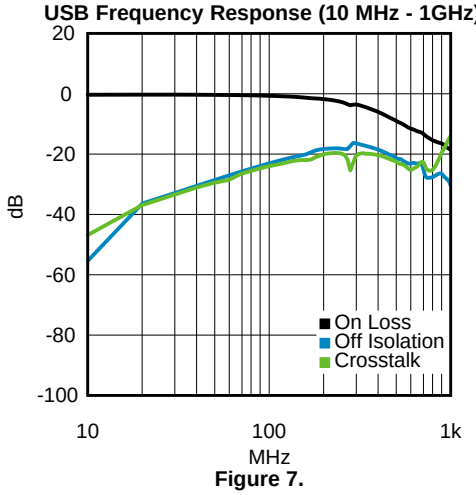


Figure 7.

UART Frequency Response (10 MHz - 1GHz)

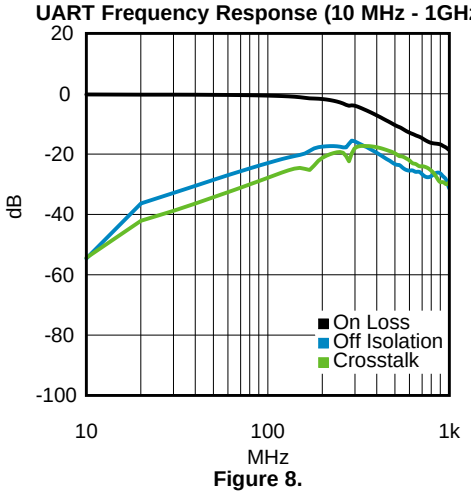


Figure 8.

Audio Frequency Response (10 MHz - 1GHz)

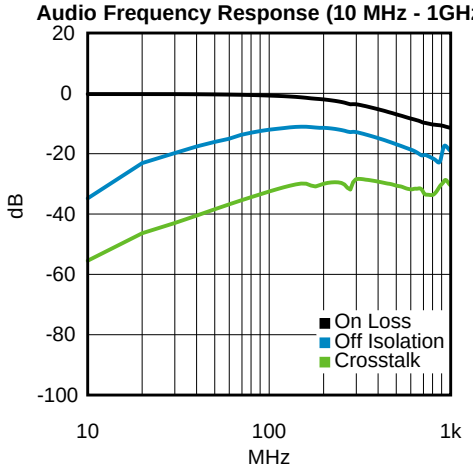


Figure 9.

AUD1 THD+N (R_L = 30Ω)

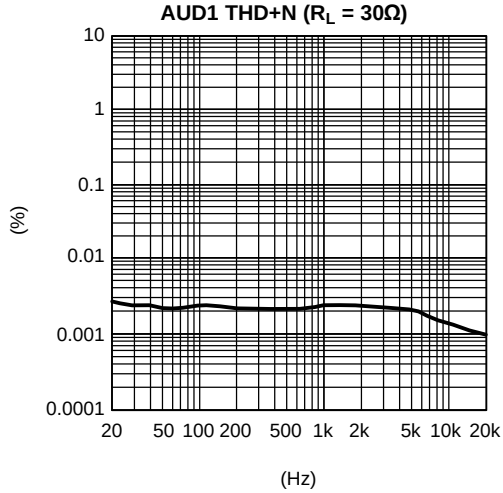


Figure 10.

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Operating Characteristics (continued)

AUD2 THD+N (R_L = 30Ω)

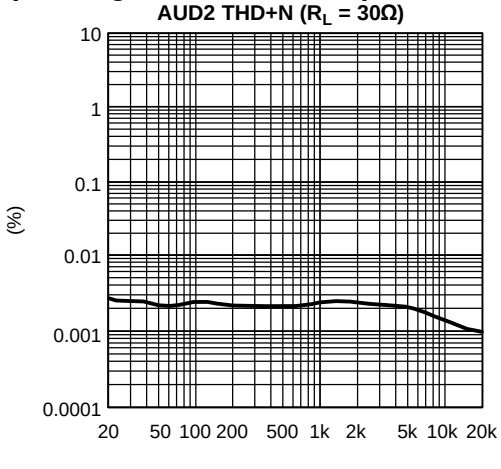


Figure 11.

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SINGLE INPUT LINEAR CHARGER

The LP8727 has a built-in Li-Ion/Li-Poly battery management system. Its main features are:

- Single-input linear charger
- Wide array of battery charging current options
- Flexible charging cycle control
- Thermal regulation
- Safety timer in Pre-charge mode

BATTERY CHARGER FUNCTION

A charge management system allowing safe charge and maintenance of a Li-Ion battery is implemented on the LP8727.

Following the correct detection of a voltage at the charger input, the charger enters pre-charge mode. In this mode the battery is charged with a small constant current. Pre-charge settings are available in register 0x08, and these values are remembered as long as the LP8727 is on. I_{PRECHG} bits select the battery current in pre-charge mode. If battery reaches the level set by $V_{FULLRATE}$, then the charger will move on to full charging mode. $T_{PRECHARGE}$ sets the maximum pre-charge time, after which the battery will be isolated, protecting it from further charging.

In full charging mode full-rate constant current is applied to the battery, to raise the voltage to the termination level. The charging current is programmable via CHG_SET bits. When termination voltage is reached, the charger is in constant voltage mode, and a constant voltage is maintained. After reaching the end-of-charge condition, the charge management isolates the battery and enters the maintenance mode.

Maintenance mode enables the battery voltage to be maintained at the correct level. If restart conditions have been met, then the charge cycle is re-initiated to re-establish the termination voltage level.

END-OF-CHARGE AND RESTART

When EOC condition is met, the LP8727 will generate an interrupt to the processor and the processor is responsible to control the charger operation (top-off or maintenance mode) via I^2C.

Once the charger goes into maintenance mode (stop charging), the processor is also responsible for monitoring the battery voltage and restarting the charger when the battery voltage drops to restart voltage.

PRODUCTION TEST MODE (PTM)

When PTM bit is set, then the charger enters special high-load mode. In this mode the charger should be able to supply up to 2.3A.

OVER-VOLTAGE PROTECTION

A built-in over-voltage protection (OVP) ensures that the charger can withstand high voltages (up to 28V) on VBUS input. When VBUS voltage exceeds the OVP threshold (typ. 6.9V), the charger operation is disabled in order to protect the charger from breakdown. When VBUS voltage drops below the OVP threshold, the charger automatically resumes its charging function.

THERMAL REGULATION

When the die temperature of the charger reaches the thermal regulation threshold (typ. 115°C), the thermal regulation loop dynamically reduces the charging current to prevent the charger from being overheated. As the die temperature drops below the thermal regulation threshold, the charging current will be automatically increased back to the programmed charging current setting.

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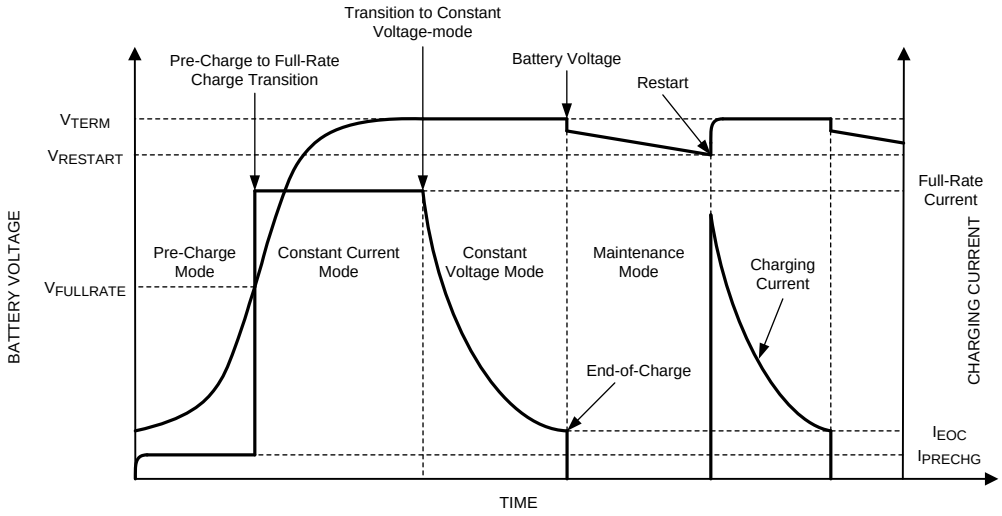


Figure 12. Li-Ion Charging Profile

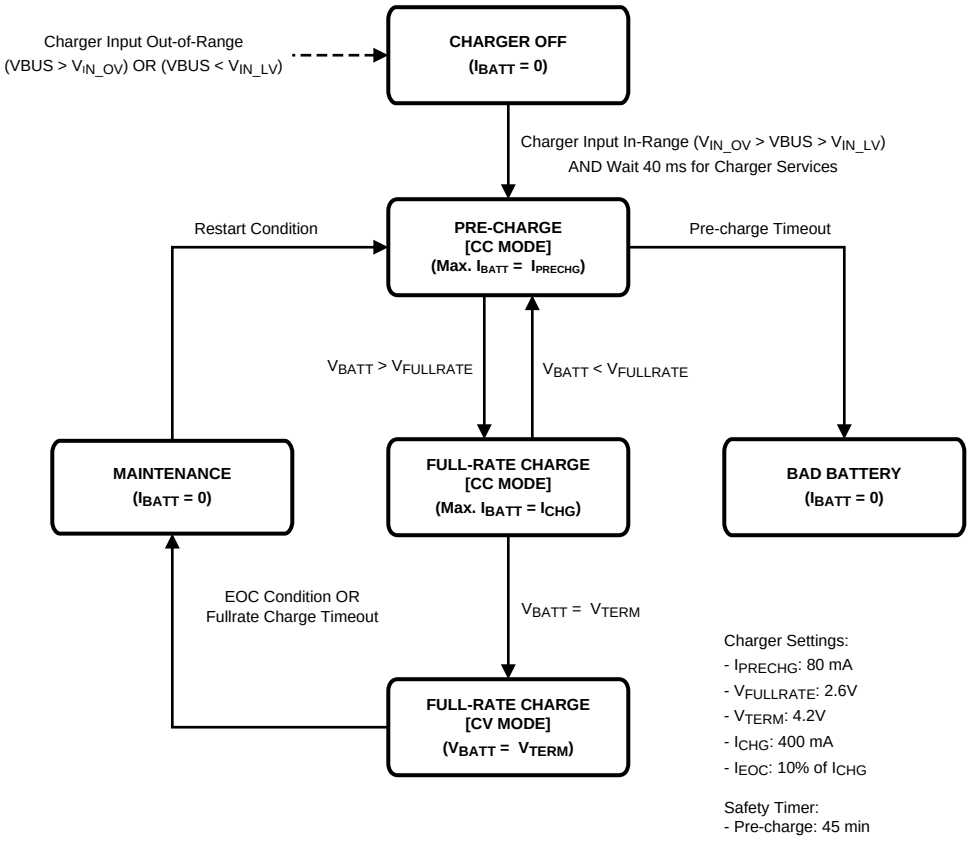


Figure 13. Charger Operation Diagram

UVLO Operation

UVLO measures system voltages on VBUS and VBAT inputs and compares it to selected voltages. The function uses 2 comparators. These comparators are combined into UVLO_N state, which can affect startup, cause shutdown or generate interrupt. UVLO_N state can change on following conditions:

- If system voltage is lower than UVLO and OPVM, then UVLO_N state is set to '0'; and

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- If system voltage is higher than UVLO and OPVM, then UVLO_N state is set to '1'.

Using different values for UVLO and OPVM provides a window for voltage drops under high-load working conditions.

UVLO_N state '0' indicates that the voltage is below normal working range, so the system is not allowed to start up. This state can also cause the system to shut down.

UVLO_N state '1' indicates that the voltage is in normal working range, so the system is allowed to start up and operate.

State transition '1' → '0' causes an UVLO interrupt, which can be sent to INT\ output.

Support Functions

REFERENCE

The LP8727 has internal reference block creating all necessary references and biasing for all blocks.

OSCILLATOR

There is internal oscillator giving clock to the logic control.

V_{VBAT} = 3.7V

PARAMETER	TYP	MIN	MAX	UNIT
Oscillator Frequency	31	29	33	kHz

THERMAL SHUTDOWN

The thermal shutdown (TSHD) function monitors the chip temperature to protect the chip from temperature damage caused by excessive power dissipation. When the chip temperature exceeds 160°C, “1” is written to TSHD bit on INT_STAT2 register and INT\ is pulled to low and then the LP8727 will initiates SHUTDOWN. The STARTUP operation after TSHD trigger can be initiated only after the chip has cooled down to the +115°C threshold.

PARAMETER	TYP	UNIT
TSDH(1)	160	°C
TSDH Hysteresis(1)	45	

(1) specified by design.

CHIP TEMPERATURE MONITOR

The LP8727 supports the chip temperature monitoring feature. When the chip temperature reaches each temperature threshold, TMP bit on INT_STAT2 will be set to “1”, and it will pull INT\ output low. The chip temperature can be obtained by reading TMP_STAT bits on STATUS2 register.

TMP_STAT	000	001	010	011
TEMPERATURE	75°C	95°C	115°C	125°C

I²C-Compatible Serial Bus Interface

INTERFACE BUS OVERVIEW

The I²C-compatible synchronous serial interface provides access to the programmable functions and registers on the device.

This protocol uses a two-wire interface for bi-directional communications between the ICs connected to the bus. The two interface lines are the Serial Data Line (SDA), and the Serial Clock Line (SCL). These lines should be connected to a positive supply, via a pull-up resistor of 1.5 kΩ and remain HIGH even when the bus is idle.

Every device on the bus is assigned a unique address and acts as either a Master or a Slave depending on whether it generates or receives the SCL.

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DATA TRANSACTIONS

One data bit is transferred during each clock pulse. Data is sampled during the high state of the SCL. Consequently, throughout the clock's high period, the data should remain stable. Any changes on the SDA line during the high state of the SCL and in the middle of a transaction, aborts the current transaction. New data should be sent during the low SCL state. This protocol permits a single data line to transfer both command/control information and data using the synchronous serial clock.

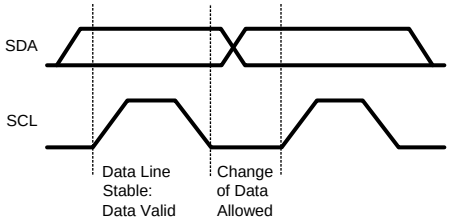


Figure 14. Bit Transfer

Each data transaction is composed of a Start Condition, a number of byte transfers (set by the software) and a Stop Condition to terminate the transaction. Every byte written to the SDA bus must be 8 bits long and is transferred with the most significant bit first. After each byte, an Acknowledge signal must follow. The following sections provide further details of this process.

START AND STOP

The Master device on the bus always generates the Start-and-Stop Conditions (control codes). After a Start Condition is generated, the bus is considered busy, and it retains this status until a certain time after a Stop Condition is generated. A high-to-low transition of the data line (SDA) while the clock (SCL) is high indicates a Start Condition. A low-to-high transition of the SDA line while the SCL is high indicates a Stop Condition.

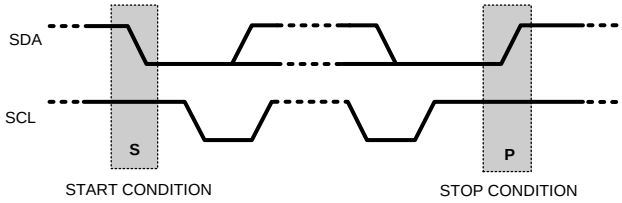


Figure 15. Start-and-Stop Conditions

In addition to the first Start Condition, a repeated Start Condition can be generated in the middle of a transaction. This allows another device to be accessed, or a register read cycle.

ACKNOWLEDGE CYCLE

The Acknowledge Cycle consists of two signals: the acknowledge clock pulse the master sends with each byte transferred, and the acknowledge signal sent by the receiving device. The master generates the acknowledge clock pulse on the ninth clock pulse of the byte transfer. The transmitter releases the SDA line (permits it to go high) to allow the receiver to send the acknowledge signal. The receiver must pull down the SDA line during the acknowledge clock pulse and ensure that SDA remains low during the high period of the clock pulse, thus signaling the correct reception of the last data byte and its readiness to receive the next byte.

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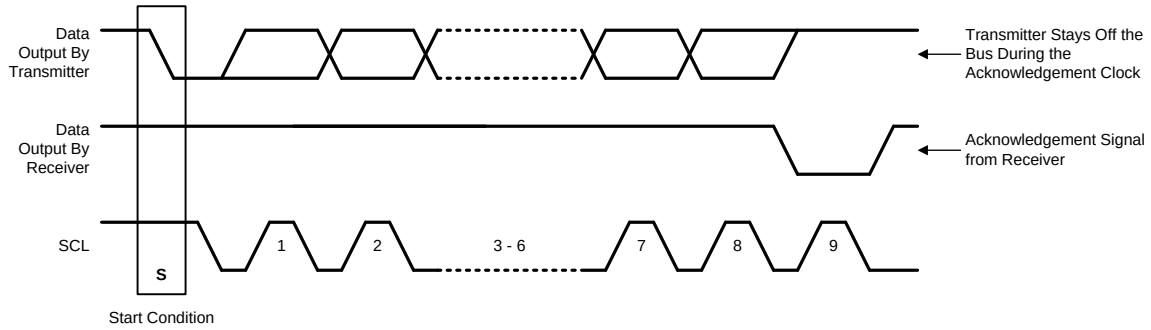


Figure 16. Bus Acknowledge Cycle

”ACKNOWLEDGE AFTER EVERY BYTE” RULE

The master generates an acknowledge clock pulse after each byte transfer. The receiver sends an acknowledge signal after every byte received.

There is one exception to the “acknowledge after every byte” rule.

When the master is the receiver, it must indicate to the transmitter an end of data by not-acknowledging (“negative acknowledge”) the last byte clocked out of the slave. This “negative acknowledge” still includes the acknowledge clock pulse (generated by the master), but the SDA line is not pulled down.

ADDRESSING TRANSFER FORMATS

Each device on the bus has a unique slave address. The slave address of the LP8727 is 7’h27 (0100111).

Before any data is transmitted, the master transmits the address of the slave being addressed. The slave device should send an acknowledge signal on the SDA line, once it recognizes its address.

The slave address is the first seven bits after a Start Condition. The direction of the data transfer (R/W) depends on the bit sent after the slave address — the eighth bit. When the slave address is sent, each device in the system compares this slave address with its own. If there is a match, the device considers itself addressed and sends an acknowledge signal. Depending upon the state of the R/W bit (1: Read, 0: Write), the device acts as a transmitter or a receiver.

CONTROL REGISTER WRITE CYCLE

- Master device generates start condition.
- Master device sends slave address (7 bits) and the data direction bit (r/w = '0').
- Slave device sends acknowledge signal if the slave address is correct.
- Master sends control register address (8 bits).
- Slave sends acknowledge signal.
- Master sends data byte to be written to the addressed register.
- Slave sends acknowledge signal.
- If master will send further data bytes the control register address will be incremented by one after acknowledge signal.
- Write cycle ends when the master creates stop condition.

CONTROL REGISTER READ CYCLE

- Master device generates a start condition.
- Master device sends slave address (7 bits) and the data direction bit (r/w = '0').
- Slave device sends acknowledge signal if the slave address is correct.
- Master sends control register address (8 bits).
- Slave sends acknowledge signal.
- Master device generates repeated start condition.
- Master sends the slave address (7 bits) and the data direction bit (r/w = “1”).

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- Slave sends acknowledge signal if the slave address is correct.
- Slave sends data byte from addressed register.
- If the master device sends acknowledge signal, the control register address will be incremented by one. Slave device sends data byte from addressed register.
- Read cycle ends when the master does not generate acknowledge signal after data byte and generates stop condition.

	Address Mode
Data Read	<Start Condition> <Slave Address><r/w = '0'>[Ack] <Register Addr.>[Ack] <Repeated Start Condition> <Slave Address><r/w = '1'>[Ack] [Register Data]<Ack or NAck> … additional reads from subsequent register address possible <Stop Condition>
Data Write	<Start Condition> <Slave Address><r/w = '0'>[Ack] <Register Addr.>[Ack] <Register Data>[Ack] … additional writes to subsequent register address possible <Stop Condition>
< > Data from master [ ] Data from slave	

REGISTER READ AND WRITE DETAIL

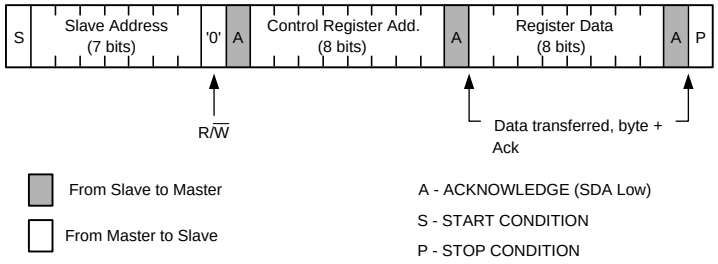


Figure 17. Register Write Format

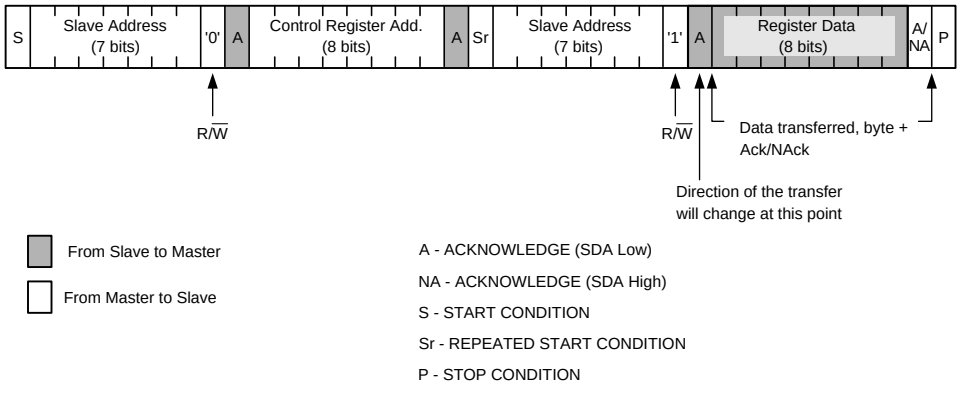


Figure 18. Register Read Format

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REVISION HISTORY

Changes from Original (May 2013) to Revision A	Page
• Changed layout of National Data Sheet to TI format	26

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PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
LP8727TME-B/NOPB	ACTIVE	DSBGA	YFQ	25	250	Green (RoHS & no Sb/Br)	SNAGCU	Level-1-260C-UNLIM	-40 to 85	27-B	Samples
LP8727TME/NOPB	ACTIVE	DSBGA	YFQ	25	250	Green (RoHS & no Sb/Br)	SNAGCU	Level-1-260C-UNLIM	-40 to 85	8727	Samples
LP8727TMX-B/NOPB	ACTIVE	DSBGA	YFQ	25	3000	Green (RoHS & no Sb/Br)	SNAGCU	Level-1-260C-UNLIM	-40 to 85	27-B	Samples
LP8727TMX/NOPB	ACTIVE	DSBGA	YFQ	25	3000	Green (RoHS & no Sb/Br)	SNAGCU	Level-1-260C-UNLIM	-40 to 85	8727	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

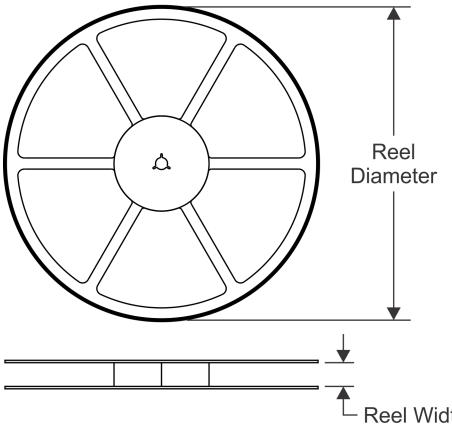
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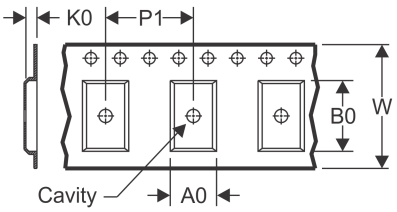
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TAPE AND REEL INFORMATION

REEL DIMENSIONS

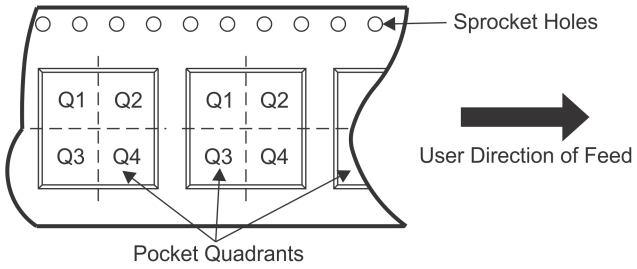


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

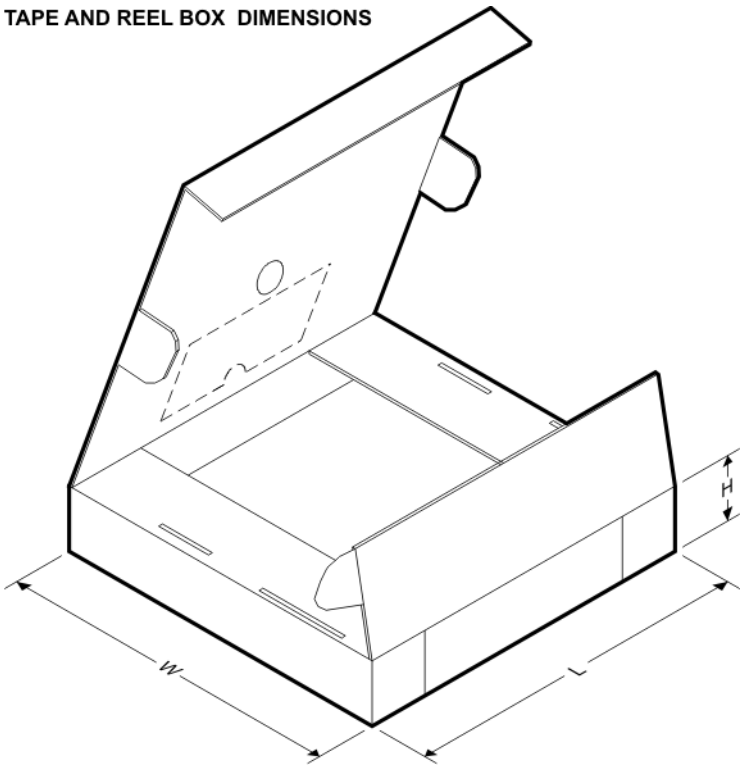
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
LP8727TME-B/NOPB	DSBGA	YFQ	25	250	178.0	8.4	2.08	2.08	0.76	4.0	8.0	Q1
LP8727TME/NOPB	DSBGA	YFQ	25	250	178.0	8.4	2.08	2.08	0.76	4.0	8.0	Q1
LP8727TMX-B/NOPB	DSBGA	YFQ	25	3000	178.0	8.4	2.08	2.08	0.76	4.0	8.0	Q1
LP8727TMX/NOPB	DSBGA	YFQ	25	3000	178.0	8.4	2.08	2.08	0.76	4.0	8.0	Q1

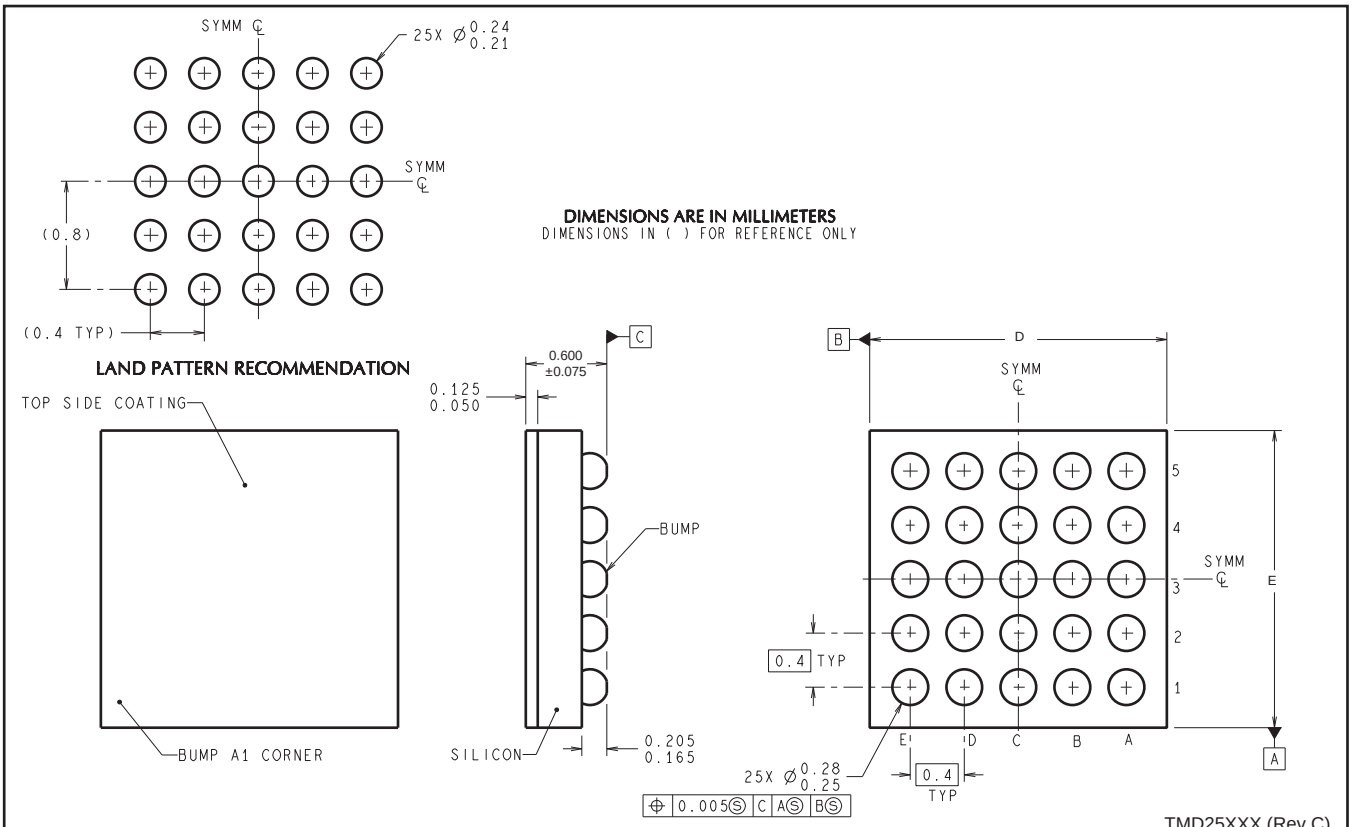
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
LP8727TME-B/NOPB	DSBGA	YFQ	25	250	210.0	185.0	35.0
LP8727TME/NOPB	DSBGA	YFQ	25	250	210.0	185.0	35.0
LP8727TMX-B/NOPB	DSBGA	YFQ	25	3000	210.0	185.0	35.0
LP8727TMX/NOPB	DSBGA	YFQ	25	3000	210.0	185.0	35.0

YFQ0025



D: Max = 2.04 mm, Min = 1.98 mm

E: Max = 2.04 mm, Min = 1.98 mm

4215084/A 12/12

NOTES: A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.
B. This drawing is subject to change without notice.

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