LP8720 One Step-Down DC-DC and Five Linear Regulators with I²C-Compatible Interface

Check for Samples: LP8720

FEATURES

- **5 Low Noise LDO's for up to 300 mA**
- **One High-Efficiency Synchronous Magnetic Buck Regulator, I_{OUT} 400 mA**
  - **High Efficiency PFM Mode @Low I_{OUT}**
  - **Auto Mode PFM/PWM Switch**
  - **Low Inductance 2.2 µH @ 2 MHz Clock**
  - **Dynamic Voltage Scale Control**
- **I²C-Compatible Interface for the Controlling of Internal Registers**
- **20-Bump 2.5 x 2.0 mm DSBGA Package**

KEY SPECIFICATIONS

- **Programmable V_{OUT} from 0.8V to 2.3V on DC-DC**
- **Automatic Soft Start on DC-DC**
- **200 mV Typ Dropout Voltage at 300 mA on LDO's**
- **2% (Typ) Output Voltage Accuracy on LDO's**

APPLICATIONS

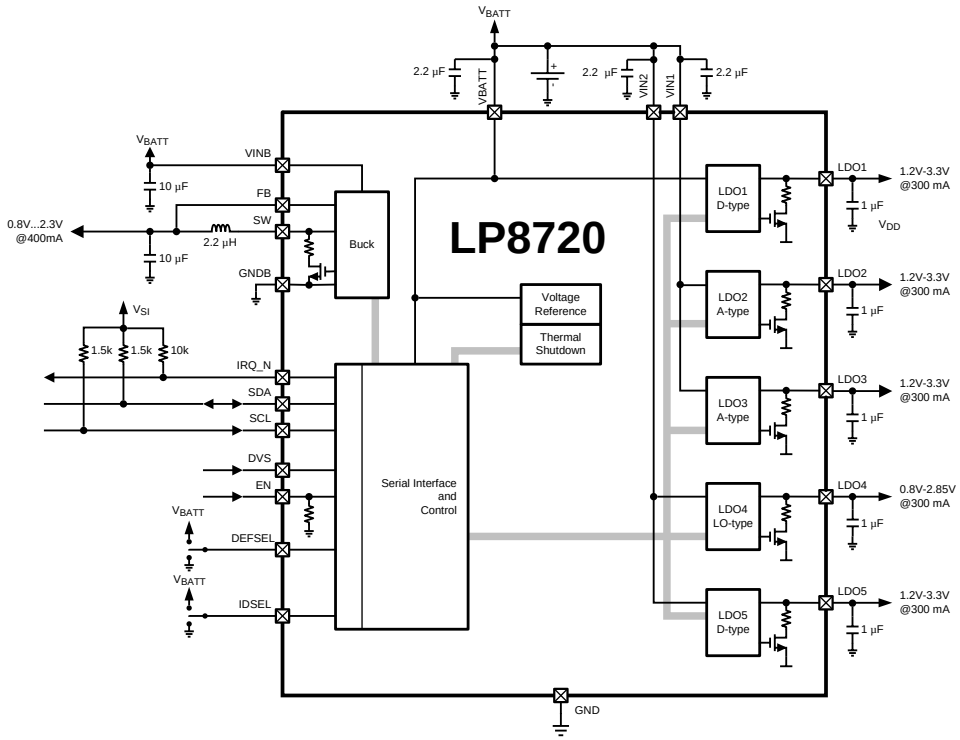
- **Cellular Handsets**
- **Portable Hand-Held Products**

DESCRIPTION

The LP8720 is a multi-function, programmable Power Management Unit, optimized for sub block power requirement solutions. This device integrates one highly efficient 400 mA step-down DC-DC converter with Dynamic Voltage Scale (DVS), five low-noise low dropout (LDO) voltage regulators, and a 400 KHz I²C-compatible interface to allow a host controller access to the internal control registers of the LP8720. Additionally, the LP8720 features programmable power-on sequencing.

LDO regulators provide high PSRR and low noise ideally suited for supplying power to both analog and digital loads. The package will be the smallest 2.5 mm x 2.0 mm 20-bump DSBGA package.

Typical Application Diagram



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Device Pin Diagram (20-Bump DSBGA)

Top View

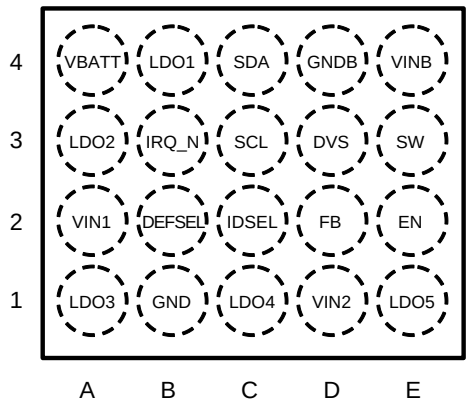


Figure 1. Package Number YZR002011A

LP8720 PIN DESCRIPTIONS(1)

Pin Number	Name	Type	Description
A4	VBATT	P	Battery Input for LDO1 and all internal circuitry.
E4	VINB	P	Battery Input for Buck.
A2	VIN1	P	Battery Input for LDO2 and LDO3.
D1	VIN2	P	Battery Input for LDO4 and LDO5.
B4	LDO1	A	LDO1 Output.
A3	LDO2	A	LDO2 Output.
A1	LDO3	A	LDO3 Output.
C1	LDO4	A	LDO4 Output.
E1	LDO5	A	LDO5 Output.
E3	SW	A	Buck Output.
D2	FB	A	Buck Feedback.
D4	GNDB	G	Power Ground for Buck.
B1	GND	G	IC Ground.
C4	SDA	DI/O	I^2C-compatible Serial Interface Data Input/Output. Open Drain output, external pull up resistor is needed, typ 1.5 kΩ. If not in use then hard wire to GND.
C3	SCL	DI	I^2C-compatible Serial Interface Clock input. External pull-up resistor is needed, typ 1.5 kΩ. If not in use then hard-wire to GND.
B3	IRQ_N	DO	Interrupt output, active LOW. Open Drain output, external pull-up resistor is needed, typ 10 kΩ. If not in use then hard-wire to GND or leave floating.
E2	EN	DI	Enable. EN=LO standby. EN=HI power on. Internal pull-down resistor 500 kΩ. **If not in use then hard wire to VBATT.**
B2	DEFSEL	DI	Control input that sets the default voltages and startup sequence. Must be hard wired to BATT or GND or left floating (Hi-Z) for specific application. When DEFSEL= VBATT then setup 1 is used for default voltages and startup sequence. When DEFSEL= GND then setup 2 is used for default voltages and startup sequence. When DEFSEL= floating (Hi-Z) setup 3 is used for default voltages and startup sequence.
C2	IDSEL	DI	Control input that sets the slave address for serial interface. Must be hard-wired to BATT or GND or left floating (Hi-Z) for specific application. When IDSEL= VBATT then slave address is 7h'7F. When IDSEL= floating (Hi-Z) then slave address is 7h'7C. When IDSEL= GND then slave address is 7h'7D.

(1) **A:**Analog Pin **D:** Digital Pin **I:** Input Pin **DI/O:** Digital Input/Output Pin **G:**Ground Pin **O:** Output Pin **P:** Power Connection

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LP8720 PIN DESCRIPTIONS(1) (continued)

Pin Number	Name	Type	Description
D3	DVS	DI	Dynamic Voltage Scaling. When DVS=HI then Buck voltage set BUCK_V1 is in use. When DVS=LO then Buck voltage set BUCK_V2 is in use. Buck voltage set BUCK_V1 should be higher than Buck voltage set BUCK_V2. **If not in use then hard wire to VBATT or GND.**

Device Description

Operation Modes

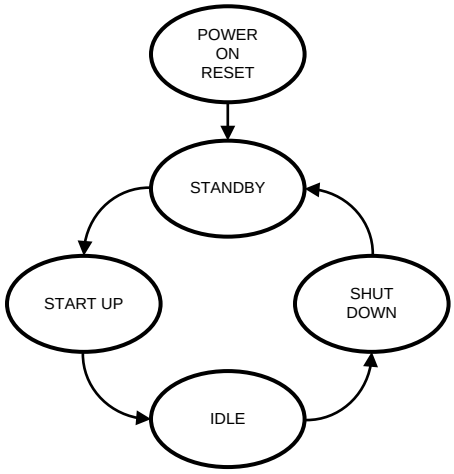
POWER-ON-RESET: After VBATT gets above POR higher threshold, the DEFSEL pin and IDSEL pin are read. All internal registers of LP8720 then are reset to the default values; after that the LP8720 goes to STANDBY mode. This process duration max is 500 µs.

STANDBY: In STANDBY mode only serial interface is working and all other PMU functions are disabled – PMU is in low-power condition. In STANDBY mode the LP8720 can be (re)configured via Serial Interface.

STARTUP: STARTUP sequence is defined by registers contents. STARTUP sequence starts:
1) If rising edge on EN pin.
2) After cooling down from thermal shutdown event if EN = HI.
It is not recommended to write to LP8720 registers during startup. If doing so then current startup sequence may become undefined.

IDLE: PMU will enter into IDLE mode (normal operating mode) after end of startup sequence. In IDLE mode all LDO's and BUCK can be enabled/disabled via Serial Interface. Also in IDLE mode LP8720 can be (re)configured via Serial Interface.

SHUTDOWN: SHUTDOWN sequence is "reverse order of startup sequence," and this is defined by registers contents. SHUTDOWN starts:
1) If falling edge on EN pin.
2) If temperature exceeds thermal shutdown threshold TSD +160°C.
It is not recommended to write to LP8720 registers during SHUTDOWN. If doing so then current SHUTDOWN sequence may become undefined.



Additional Functions

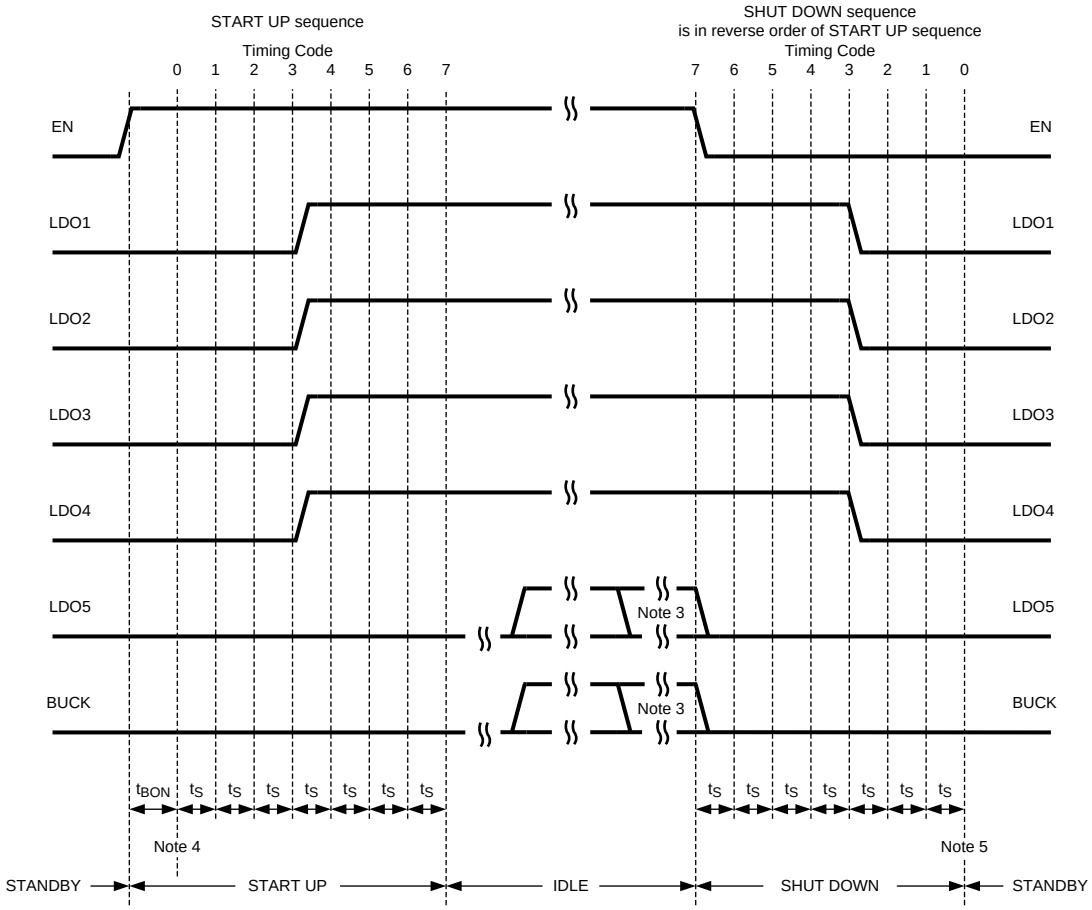
SLEEP: If sum of all LDOs' load currents and BUCK load current is no higher than 5 mA , the user can put PMU to SLEEP. In SLEEP PMU GND current is minimized, and LDO's and BUCK cannot be loaded with bigger current.
There are 2 possibilities to use SLEEP:
1) Control via Serial Interface.
2) Control by DVS pin.

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DVS: Dynamic Voltage Scaling allows using 2 voltage sets for BUCK. There are 2 possibilities to use DVS:
1) Control via Serial Interface.
2) Control by DVS pin.

INTERRUPT: If interrupt is not masked, the PMU forces IRQ_N low if the temperature crosses the TSD_EW limit (thermal shutdown early warning) or/and a thermal shutdown event has taken place. IRQ_N is released by reading Interrupt register.

Power-On and Power-Off Sequences



t_{BON} 150 µs – Reference and bias turn ON. Min 100 µs max 200 µs.

t_S 25 µs – time step. Time step accuracy is defined by OSC frequency accuracy.

(1) STARTUP and SHUTDOWN sequences are defined by registers. Sequences given here are valid if there the registers are not rewritten via Serial Interface.

(2) The timing showed here define time points when LDO's and BUCK are enabled/disabled. Enabling /disabling process duration depends on loading conditions. Buck startup duration is 140 µs for no load. LDO startup duration is no more than 35 µs. For details please see LDO's and BUCK Electrical Specifications.

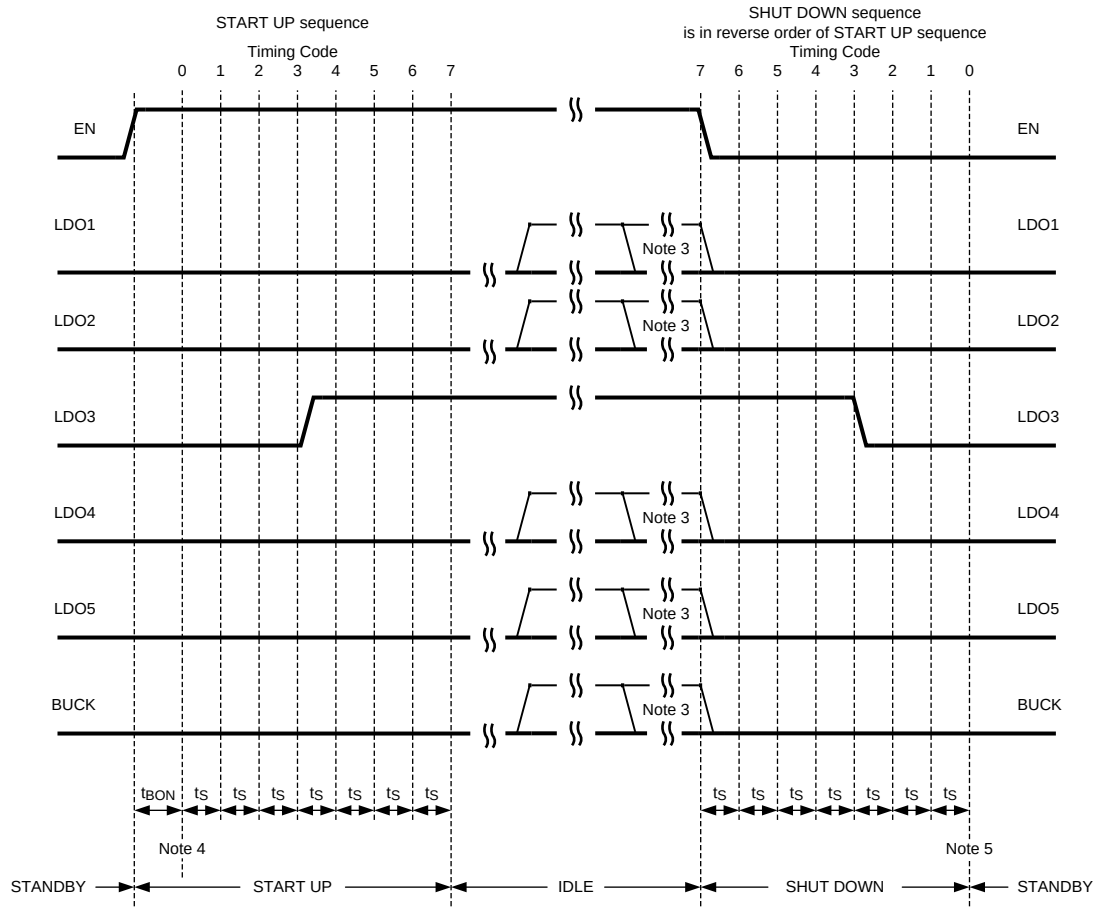
(3) LDO5 and BUCK are disabled. If LDO5 and/or BUCK are enabled via Serial Interface, and startup sequence is not changed via Serial interface, then LDO5 and BUCK are disabled with no delay from falling edge on EN pin.

(4) At this time point registers 0x09 and 0x0C are reset to POR default values.

(5) At this time point registers 0x00, 0x01, 0x02, 0x03, 0x04, 0x05, 0x06, 0x07 and 0x08 are reset to POR default values.

Figure 2. Startup Sequence if DEFSEL=VBATT or DEFSEL=Hi-Z

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t_{BON} 150 µs – Reference and bias turn ON. Min 100 µs max 200 µs.

t_S 25 µs – time step. Time step accuracy is defined by OSC frequency accuracy.

(1) STARTUP and SHUTDOWN sequences are defined by registers. Sequences given here are valid if there the registers are not rewritten via Serial Interface.

(2) The timing showed here define time points when LDO's and BUCK are enabled/disabled. Enabling /disabling process duration depends on loading conditions. Buck startup duration is 140 µs for no load. LDO startup duration is no more than 35 µs. For details please see LDO's and BUCK Electrical Specifications.

(3) LDO1, LDO2, LDO4, LDO5 and BUCK are disabled. If LDO1, LDO2, LDO4, LDO5 and/or BUCK are enabled via Serial Interface and startup sequence is not changed via Serial interface, then LDO1, LDO2, LDO4, LDO5 and BUCK are disabled with no delay from falling edge on EN-pin.

(4) At this time point registers 0x09 and 0x0C are reset to POR default values.

(5) At this time point registers 0x00, 0x01, 0x02, 0x03, 0x04, 0x05, 0x06, 0x07 and 0x08 are reset to POR default values.

Figure 3. Startup Sequence if DEFSEL=GND

Table 1. Startup Sequence(1)

DEFSEL	Startup Sequence	Shutdown Sequence
VBATT	LDO1, 2, 3, 4 enable same time. LDO5 and BUCK enable via Serial Interface.	In reverse order of startup sequence.
GND	LDO3 enable. LDO1, 2, 4, 5 and BUCK enable via Serial Interface .	In reverse order of startup sequence.
Hi-Z	LDO1, 2, 3, 4 enable same time. LDO5 and BUCK enable via Serial Interface.	In reverse order of startup sequence.

(1) When IDSEL= VBATT then slave address is 7h'7F.
When IDSEL= floating (Hi-Z) then slave address is 7h'7C.
When IDSEL= GND then slave address is 7h'7D.

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Table 2. Default Output Voltages(1)(2)

Output	Max Current [mA]	Default output Voltage [V] and default ON/OFF if EN=HI		
		DEFSEL=VBATT	DEFSEL=GND	DEFSEL=Hi-Z
LDO1	300	3.0 ON	3.0 OFF	2.8 ON
LDO2	300	2.6 ON	3.0 OFF	2.6 ON
LDO3	300	1.8 ON	2.6 ON	1.8 ON
LDO4	300	1.0 ON	2.6 OFF	1.2 ON
LDO5	300	3.3 OFF	3.3 OFF	3.3 OFF
BUCK	400	1.0 OFF	1.2/1.3[1)] OFF	1.2 OFF

(1) BUCK voltage is 1.2V if DVS=LO and 1.3V if DVS=HI.
(2) When IDSEL= VBATT then slave address is 7h'7F
When IDSEL= floating (Hi-Z) then slave address is 7h'7C
When IDSEL= GND then slave address is 7h'7D

Table 3. Control Register Map(1)

Addr	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	POR default DEFSEL		
										VBATT	GND	Hi-Z
0x00	GENERAL_ SETTINGS						EXT_DVS_ CONTROL	EXT_SLEEP_ CONTROL	SHORT_ TIMESTEP	0000 0001	0000 0101	0000 0001
0x01	LDO1_ SETTINGS	LDO1_ T[2]	LDO1_ T[1]	LDO1_ T[0]	LDO1_ V[4]	LDO1_ V[3]	LDO1_ V[2]	LDO1_ V[1]	LDO1_ V[0]	0111 1101	1111 1101	0111 1001
0x02	LDO2_ SETTINGS	LDO2_ T[2]	LDO2_ T[1]	LDO2_ T[0]	LDO2_ V[4]	LDO2_ V[3]	LDO2_ V[2]	LDO2_ V[1]	LDO2_ V[0]	0111 0101	1111 1101	0111 0101
0x03	LDO3_ SETTINGS	LDO3_ T[2]	LDO3_ T[1]	LDO3_ T[0]	LDO3_ V[4]	LDO3_ V[3]	LDO3_ V[2]	LDO3_ V[1]	LDO3_ V[0]	0110 1100	0111 0101	0110 1100
0x04	LDO4_ SETTINGS	LDO4_ T[2]	LDO4_ T[1]	LDO4_ T[0]	LDO4_ V[4]	LDO4_ V[3]	LDO4_ V[2]	LDO4_ V[1]	LDO4_ V[0]	0110 0011	1111 1010	0110 0101
0x05	LDO5_ SETTINGS	LDO5_ T[2]	LDO5_ T[1]	LDO5_ T[0]	LDO5_ V[4]	LDO5_ V[3]	LDO5_ V[2]	LDO5_ V[1]	LDO5_ V[0]	1111 1111	1111 1111	1111 1111
0x06	BUCK_ SETTINGS1	BUCK_ T[2]	BUCK_ T[1]	BUCK_ T[0]	BUCK_ V1[4]	BUCK_ V1[3]	BUCK_ V1[2]	BUCK_ V1[1]	BUCK_ V1[0]	1110 0101	1110 1011	1110 1001
0x07	BUCK_ SETTINGS2			FORCE_ PWM	BUCK_ V2[4]	BUCK_ V2[3]	BUCK_ V2[2]	BUCK_ V2[1]	BUCK_ V2[0]	0000 0101	0000 1001	0000 1001
0x08	ENABLE_ BITS	DVS_ V2/V1	SLEEP_ MODE	BUCK_ EN	LDO5_ EN	LDO4_ EN	LDO3_ EN	LDO2_ EN	LDO1_ EN	1000 1111	1000 0100	1000 1111
0x09	PULLDOWN_ BITS	APU_ TSD		BUCK_ PULLDOWN	LDO5_ PULLDOWN	LDO4_ PULLDOWN	LDO3_ PULLDOWN	LDO2_ PULLDOWN	LDO1_ PULLDOWN	0011 1111	0011 1111	0011 1111
0x0A	STATUS_ BITS							TSD	TSD_EW	0000 0000	0000 0000	0000 0000
0x0B	INTERRUPT_ BITS(2)							TSD_ INT	TSD_EW_ INT	0000 0000	0000 0000	0000 0000
0x0C	INTERRUPT_ MASK(2)							TSD_ MASK	TSD_EW_ MASK	0000 0011	0000 0011	0000 0011

(1) When IDSEL= VBATT then slave address is 7h'7F.
When IDSEL= floating (Hi-Z) then slave address is 7h'7C.
When IDSEL= GND then slave address is 7h'7D.
(2) Registers STATUS_BITS 0x0A and INTERRUPT_BITS 0x0B are read only.

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Table 4. Register 0x00

EXT_DVS_CONTROL	1 – DVS pin control: • DVS = HI then BUCK_V1[4:0] • DVS = LO then BUCK_V2[4:0] 0 – Serial interface control: • DVS_V2/V1 = 1 then BUCK_V1[4:0] • DVS_V2/V1 = 0 then BUCK_V2[4:0]
EXT_SLEEP_CONTROL	1 – DVS-pin control: • DVS = HI then normal • DVS = LO then SLEEP 0 – Serial interface control: • SLEEP_MODE = 0 then normal • SLEEP_MODE = 1 then SLEEP
SHORT_TIMESTEP	1 – time step t_S = 25 µs 0 – time step t_S= 50 µs By request time step 100 µs/200 µs is available.

Table 5. Registers 0x01 – 0x07

LDO1_V[4:0] LDO2_V[4:0] LDO3_V[4:0] LDO5_V[4:0]	00000 – 1.20V 00001 – 1.25V 00010 – 1.30V 00011 – 1.35V 00100 – 1.40V 00101 – 1.45V 00110 – 1.50V 00111 – 1.55V	01000 – 1.60V 01001 – 1.65V 01010 – 1.70V 01011 – 1.75V 01100 – 1.80V 01101 – 1.85V 01110 – 1.90V 01111 – 2.00V	10000 – 2.10V 10001 – 2.20V 10010 – 2.30V 10011 – 2.40V 10100 – 2.50V 10101 – 2.60V 10110 – 2.65V 10111 – 2.70V	11000 – 2.75V 11001 – 2.80V 11010 – 2.85V 11011 – 2.90V 11100 – 2.95V 11101 – 3.00V 11110 – 3.10V 11111 – 3.30V
LDO4_V[4:0]	00000 – 0.80V 00001 – 0.85V 00010 – 0.90V 00011 – 1.00V 00100 – 1.10V 00101 – 1.20V 00110 – 1.25V 00111 – 1.30V	01000 – 1.35V 01001 – 1.40V 01010 – 1.45V 01011 – 1.50V 01100 – 1.55V 01101 – 1.60V 01110 – 1.65V 01111 – 1.70V	10000 – 1.75V 10001 – 1.80V 10010 – 1.85V 10011 – 1.90V 10100 – 2.00V 10101 – 2.10V 10110 – 2.20V 10111 – 2.30V	11000 – 2.40V 11001 – 2.50V 11010 – 2.60V 11011 – 2.65V 11100 – 2.70V 11101 – 2.75V 11110 – 2.80V 11111 – 2.85V
BUCK_V1[4:0] BUCK_V2[4:0]	0000 External resistor divider 00001 – 0.80V 00010 – 0.85V 00011 – 0.90V 00100 – 0.95V 00101 – 1.00V 00110 – 1.05V 00111 – 1.10V	01000 – 1.15V 01001 – 1.20V 01010 – 1.25V 01011 – 1.30V 01100 – 1.35V 01101 – 1.40V 01110 – 1.45V 01111 – 1.50V	10000 – 1.55V 10001 – 1.60V 10010 – 1.65V 10011 – 1.70V 10100 – 1.75V 10101 – 1.80V 10110 – 1.85V 10111 – 1.90V	11000 – 1.95V 11001 – 2.00V 11010 – 2.05V 11011 – 2.10V 11100 – 2.15V 11101 – 2.20V 11110 – 2.25V 11111 – 2.30V
	BUCK_V1[4:0] should be higher (or equal) than BUCK_V2[4:0].			
LDO1_T[2:0] LDO2_T[2:0] LDO3_T[2:0] LDO4_T[2:0] LDO5_T[2:0] BUCK_T[2:0]	000 – startup delay 0 001 – startup delay = 1 * time step t_S 010 – startup delay = 2 * time step t_S 011 – startup delay = 3 * time step t_S		100 – startup delay = 4 * time step t_S 101 – startup delay = 5 * time step t_S 110 – startup delay = 6 * time step t_S 111 – NO startup	
	For proper startup operation “111 NO startup” should have corresponding bit in ENABLE_BITS register 0x08 set to 0 (disable).			
FORCE_PWM	1 – Buck is forced to work in PWM mode 0 – Buck works in automatic PFM/PWM selection mode.			

Table 6. Register 0x08

LDO1_EN LDO2_EN LDO3_EN LDO4_EN LDO5_EN BUCK_EN	In STANDBY mode 1 – During next startup sequence will be enabled. 0 – During next startup sequence will be NOT enabled. For proper operation output having “111 NO startup” should have corresponding enable bit 0 (disable).	In IDLE mode the bit has immediate effect. 1 – Enable 0 – Disable
SLEEP_MODE	1 – SLEEP 0 – normal This bit has effect only if EXT_SLEEP_CONTROL=0 (register 0x00)	
DVS_V2/V1	1 – buck voltage is BUCK_V1[4:0] 0 – buck voltage is BUCK_V2[4:0] This bit has effect only if EXT_DVS_CONTROL=0 (register 0x00)	

Table 7. Register 0x09

LDO1_PULLDOWN LDO2_PULLDOWN LDO3_PULLDOWN LDO4_PULLDOWN LDO5_PULLDOWN BUCK_PULLDOWN	1 – pull-down enabled 0 – pull-down disabled
APU_TSD	This bit defines either to reset registers or not before LP8720 automatically starts startup sequence from Thermal Shutdown after cooling down if EN-pin is High. 1 – No change to registers – registers content stays the same as before Thermal Shutdown. 0 – Reset registers to default values before startup from Thermal Shutdown.

Table 8. Register 0x0A (Read Only)

TSD	1 – device is in Thermal Shutdown. 0 – device is NOT in Thermal Shutdown .
TSD_EW	1 – device temperature is higher than Thermal Shutdown Early Warning threshold. 0 – device temperature is lower than Thermal Shutdown Early Warning threshold.

Table 9. Register 0x0B (Read Only)

TSD_INT	1 – Interrupt that was caused by Thermal Shutdown 0 – No Interrupt that was caused by Thermal Shutdown
TSD_EW	1 – Interrupt that was caused by Thermal Shutdown Early Warning 0 – No Interrupt that was caused by Thermal Shutdown Early Warning

Table 10. Register 0x0C

TSD_MASK	1 – TSD interrupt is masked 0 – TSD interrupt is NOT masked
TSD_EW_MASK	1 – TSD_EW interrupt is masked 0 – TSD_EW interrupt is NOT masked

Support Functions

Reference

The LP8720 has an internal reference block creating all necessary references and biasing for all blocks.

Oscillator

There is an internal oscillator giving clock to the bucks and to logic control.

Parameter	Typ	Min	Max	Unit
Oscillator frequency	2.0	1.9	2.1	MHz

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Thermal Shutdown

The Thermal Shutdown (TSD) function monitors the chip temperature to protect the chip from temperature damage caused eg. by excessive power dissipation. The temperature monitoring function has two threshold values, TSD and TSD_EW, that result in protective actions.

When TSD_EW +125ºC is exceeded, IRQ_N is set to low, and “1” is written to the TSD_EW bit in both the STATUS register and in INTERRUPT register.

If the temperature exceeds TSD +160ºC, then PMU initiates Emergency Shutdown.

The POWER-UP operation after Thermal Shutdown can be initiated only after the chip has cooled down to the +115ºC threshold.

Parameter	Typ	Unit
TSD(1)	160	°C
TSD_EW(1)	125	°C
TSD_EW Hysteresis(1)	10	°C

(1) Ensured by design.

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

Absolute Maximum Ratings(1)(2)(3)

V_{BATT} = VINB, VBATT	-0.3V to +6V
VIN1, VIN2	-0.3V to V_{BATT}+0.15V, max 6V
All other pins	-0.3V to V_{BATT}+0.3V, max 6V
Junction Temperature (TJ-MAX)	150ºC
Storage Temperature	-40 to 150ºC
Maximum Continuous Power Dissipation, P_{D-MAX}(4)	1.75 W
ESD(5)	2 kV HBM
	200V MM

(1) Absolute Maximum Ratings are limits beyond which damage to the device may occur. Operating Ratings are conditions under which operation of the device is specified. Operating Ratings do not imply ensured performance limits. For specified performance limits and associated test conditions, see the Electrical Characteristics tables.
(2) If Military/Aerospace specified devices are required, please contact the TI Sales Office/ Distributors for availability and specifications.
(3) All voltages are with respect to the potential at the GND pin.
(4) The Absolute Maximum power dissipation depends on the ambient temperature and can be calculated using the formula $P = (T_J - T_A)/\theta_{JA}$, (eq. 1) where T_J is the junction temperature, T_A is the ambient temperature, and θ_{JA} is the junction-to-ambient thermal resistance. The 1.75-W rating appearing under Absolute Maximum Ratings results from substituting the Absolute Maximum junction temperature, 150ºC for T_J, 70ºC for T_A, and 45°C/W for θ_{JA}. More power can be dissipated safely at ambient temperatures below 70°C. Less power can be dissipated safely at ambient temperatures above 70°C. The Absolute Maximum power dissipation can be increased by 22 mW for each degree below 70°C, and it must be de-rated by 22 mW for each degree above 70ºC.
(5) The human-body model is 100 pF discharged through 1.5 kΩ. The machine model is a 200-pF capacitor discharged directly into each pin, MIL-STD-883 3015.7.

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Operating Ratings(1)(2)

V_{BATT} = VINB, VBATT	2.7 to 4.5V
VIN1, VIN2	2.5V to V_{BATT}
All input-only pins	0V to V_{BATT}
Junction Temperature (T_J)	-40 to 125ºC
Ambient Temperature (T_A)	-40 to 85ºC
Maximum Power Dissipation (T_A = 70ºC)(3)	1.2 W

(1) Absolute Maximum Ratings are limits beyond which damage to the device may occur. Operating Ratings are conditions under which operation of the device is specified. Operating Ratings do not imply ensured performance limits. For specified performance limits and associated test conditions, see the Electrical Characteristics tables.
(2) All voltages are with respect to the potential at the GND pin.
(3) Like the Absolute Maximum power dissipation, the maximum power dissipation for operation depends on the ambient temperature. The 1.2W rating for DSBGA 20 appearing under Operating Ratings results from substituting the maximum junction temperature for operation, 125°C, for T_J, 70°C for T_A, and 45°C/W for θ_{JA} into (eg. 1) above. More power can be dissipated at ambient temperatures below 70°C. Less power can be dissipated at ambient temperatures above 70°C. The maximum power dissipation for operation can be increased by 22mW for each degree below 70°C, and it must be de-rated by 22 mW for each degree above 70°C.

Thermal Properties(1)

Junction-to-Ambient Thermal Resistance (θ_{JA}) (Jedec Standard Thermal PCB) 20-bump DSBGA package	45°C/W

(1) Junction-to-ambient thermal resistance is highly application and board-layout dependent. In applications where high maximum power dissipation exists, special care must be paid to thermal dissipation issues in board design.

Current Consumption

Unless otherwise noted, V_{VBATT} = V_{VINB} =V_{VIN1} = V_{VIN2} = 3.6V, GND = GNDB = 0V, C_{VBATT} = C_{VIN1}= C_{VIN2} = 2.2 µF, C_{VINB} = 10 µF. Typical values and limits appearing in normal type apply for T_J = 25°C. Limits appearing in **boldface** type apply over the entire junction temperature range for operation, T_J= -40 to +125°C(1)

Parameter		Test Conditions	Typ	Limit		Units
				Min	Max	
$I_{Q(STANDBY)}$	Battery Standby Current	V_{BATT} = 3.6V	0.7		5	µA
$I_{Q(SLEEP)}$	Battery Current in SLEEP Mode @ 0 load	BUCK and all LDO's enabled	190		**270**	µA
$I_{Q(SLEEP)}$	Battery Current in SLEEP Mode @ 0 load	LDO1, LDO2, LDO3 and LDO4 enabled	170			µA
$I_{Q(SLEEP)}$	Battery Current in SLEEP Mode @ 0 load	LDO3 enabled	100		**150**	µA
$I_{Q(SLEEP)}$	Battery Current in SLEEP Mode @ 0 load	LDO1 and BUCK enabled	100			µA
I_Q	Battery Current @ 0 load	BUCK and all LDO's enabled	270		**400**	µA
I_Q	Battery Current @ 0 load	LDO1, LDO2, LDO3 and LDO4 enabled	230			µA
I_Q	Battery Current @ 0 load	LDO3 enabled	120		**200**	µA
I_Q	Battery Current @ 0 load	LDO1 and BUCK enabled	120			µA

(1) All limits are specified. All electrical characteristics having room-temperature limits are tested during production with T_J = 25°C. All hot and cold limits are ensured by correlating the electrical characteristics to process and temperature variations and applying statistical process control.

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Power-On Reset(1)

Unless otherwise noted, V_{VBATT} = V_{VINB} = V_{VIN1} =V_{VIN2} = 3.6V, GND = GNDB = 0V, C_{VBATT} =C_{VIN1}= C_{VIN2}=2.2 µF, C_{VINB} = 10 µF. Typical values and limits appearing in normal type apply for T_J = 25°C. Limits appearing in **boldface** type apply over the entire junction temperature range for operation, T_J= -40 to +125°C. (1)

Parameter		Test Conditions	Typ	Limit		Units
				Min	Max	
V_{POR_HI}	POR higher threshold	V_{VBATT} rising	2.2	2.0	2.4	V
V_{POR_LO}	POR lower threshold	V_{VBATT} falling (2)	1.4			V

(1) All limits are specified. All electrical characteristics having room-temperature limits are tested during production with T_J = 25°C. All hot and cold limits are ensured by correlating the electrical characteristics to process and temperature variations and applying statistical process control.
(2) Ensured by design.

Logic and Control

Unless otherwise noted, V_{VBATT} = V_{VINB} = V_{VIN1} = V_{VIN2} = 3.6V, GND=GNDB=0V, C_{VBATT} =C_{VIN1}= C_{VIN2} = 2.2 µF, C_{VINB} = 10 µF. Typical values and limits appearing in normal type apply for T_J=25°C. Limits appearing in **boldface** type apply over the entire junction temperature range for operation, T_J= -40 to +125°C (1)

Parameter		Test Conditions	Typ	Limit		Units
				Min	Max	
Logic and Control Inputs						
VIL	Input Low Level	EN, SCL, SDA, DVS			**0.4**	V
VIH	Input High Level	EN, SCL, SDA, DVS		**1.2**		V
IIL	Input Current	All logic inputs		**-5**	**+5**	µA
RPD	Pull-Down Resistance	From EN to GND	550	**300**	**900**	kΩ
Logic and Control Outputs						
VOL	Output Low Level	IRQ_N, SDA, I_{OUT} = 2 mA			**0.4**	V
VOH	Output High Level	IRQ_N, SDA are Open drain outputs.		**NA**		µA

(1) All limits are specified. All electrical characteristics having room-temperature limits are tested during production with T_J = 25°C. All hot and cold limits are ensured by correlating the electrical characteristics to process and temperature variations and applying statistical process control.

Buck Converter

Unless otherwise noted, V_{VBATT} = V_{VINB} = V_{VIN1} = V_{VIN2} = 3.6V, GND = GNDB = 0V, C_{VBATT} = C_{VIN1} = C_{VIN2} = 2.2 µF, C_{VINB} = 10 µF. Typical values and limits appearing in normal type apply for T_J=25°C. Limits appearing in **boldface** type apply over the entire junction temperature range for operation, T_J= -40 to +125°C (1) (2)

Parameter		Test Conditions	Typ	Limit		Units
				Min	Max	
V_{FB}	Feedback Voltage	3.0V ≤ V_{IN} ≤ 4.5V external resistor divider	0.5	**0.485**	**0.515**	V
V_{BUCK}	Output Voltage, PWM Mode	3.0V ≤ V_{IN} ≤ 4.5V	1.2	**1.164**	**1.236**	V
$V_{VOUT,PFM}$	Output Voltage regulation in PFM mode relative to regulation in PWM mode	See (3)	1.5%			
V_{OUT}	Line Regulation	3.0V ≤ V_{IN} ≤ 4.5V I_{OUT} = 10 mA	0.14			%/V
V_{OUT}	Load Regulation	100mA ≤ I_{OUT} ≤ 300mA	0.09			%/mA
I_{LIM_PWM}	Switch Peak Current Limit	PWM Mode @ 400 mA 3.0V ≤ V_{IN} ≤ 4.5V	900	**500**		mA
$R_{DSON(P)}$	P channel FET on resistance	V_{IN} = 3.6V, I_D = 100 mA	310		**500**	mΩ
$R_{DSON(N)}$	N channel FET on resistance		160		**300**	mΩ

(1) All limits are specified. All electrical characteristics having room-temperature limits are tested during production with T_J = 25°C. All hot and cold limits are ensured by correlating the electrical characteristics to process and temperature variations and applying statistical process control.
(2) Ensured for output voltages no less than 1.0V
(3) Ensured by design.

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Buck Converter (continued)

Unless otherwise noted, $V_{VBATT} = V_{VINB} = V_{VIN1} = V_{VIN2} = 3.6V$, GND = GNDB = 0V, $C_{VBATT} = C_{VIN1} = C_{VIN2} = 2.2\ \mu F$, $C_{VINB} = 10\ \mu F$. Typical values and limits appearing in normal type apply for T_J=25°C. Limits appearing in **boldface** type apply over the entire junction temperature range for operation, T_J= -40 to +125°C(1)(2)

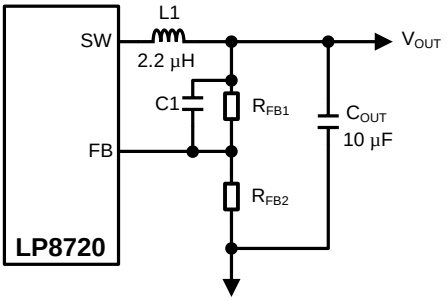
Parameter		Test Conditions	Typ	Limit		Units
				Min	Max	
f_{OSC}	Internal Oscillator Frequency	PWM Mode	2	1.9 **1.7**	2.1 **2.3**	MHz
Efficiency		I_{OUT} = 5 mA, PFM-mode V_{OUT} = 1.2V(3)	88%			
		I_{OUT} = 200 mA, PWM-mode V_{OUT} = 1.2V(3)	90%			
T_{STUP}	Startup Time	I_{OUT} = 0, V_{OUT} = 1.2V(3)	140			µs

Table 11. Buck Output Voltage Programming in Register 0x06 and 0x07

BUCK1_Vx	V_{OUT}	BUCK1_Vx	V_{OUT}
5h'00	External resistor divider	5h'10	1.55
5h'01	0.80	5h'11	1.60
5h'02	0.85	5h'12	1.65
5h'03	0.90	5h'13	1.70
5h'04	0.95	5h'14	1.75
5h'05	1.00	5h'15	1.80
5h'06	1.05	5h'16	1.85
5h'07	1.10	5h'17	1.90
5h'08	1.15	5h'18	1.95
5h'09	1.20	5h'19	2.00
5h'0A	1.25	5h'1A	2.05
5h'0B	1.30	5h'1B	2.10
5h'0C	1.35	5h'1C	2.15
5h'0D	1.40	5h'1D	2.20
5h'0E	1.45	5h'1E	2.25
5h'0F	1.50	5h'1F	2.30

Output Voltage Selection Using External Resistor Divider

Buck1 output voltage can be programmed via the selection of the external feedback resistor network.



V_{OUT} will be adjusted to make the voltage at FB equal to 0.5V. The resistor from FB to ground R_{FB2} should be around 200 kΩ to keep the current drawn through the resistor network to a minimum but large enough that it is not susceptible to noise. With R_{FB2}= 200 kΩ and V_{FB} at 0.5V, the current through the resistor feedback network will be 2.5 µA.

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The formula for output voltage selection is

$$V_{OUT} = V_{FB} \times \left(1 + \frac{R_{FB1}}{R_{FB2}}\right)$$

- V_{OUT} – output voltage
- V_{FB} – feedback voltage (0.5V)

(1)

For any out voltage greater than or equal to 0.8V a transfer function zero should be added by the addition of a capacitor C1. The formula for calculation of C1 is:

$$C1 = \frac{1}{(2 \times \pi \times R_{FB1} \times 45 \times 10^{3})}$$

(2)

For recommended component values see the table below.

V_{OUT} [V]	R_{FB1} [kΩ]	R_{FB2} [kΩ]	C1 [pF]	L [µH]	C_{OUT} [µF]
1.0	200	200	18	2.2	10
1.2	280	200	12	2.2	10
1.4	360	200	10	2.2	10
1.5	360	180	10	2.2	10
1.6	440	200	8.2	2.2	10
1.85	540	200	6.8	2.2	10

LDO's

There are, all together, 5 LDO's in the LP8720 grouped as:

- A-type LDO's (LDO2, 3)
- D-type LDO's (LDO1, 5)
- LO-type LDO (LDO 4)

The A-type LDO's are optimized for supplying of analog loads and have ultra low noise (15 μV_{RMS}) and excellent PSRR (70 dB) performance.

The D-type LDO's are optimized for good dynamic performance to supply different fast changing (digital) loads.

The LO-type LDO is optimized for low output voltage and for good dynamic performance to supply different fast changing (digital) loads.

All LDO's can be programmed through serial interface for 32 different output voltage values, which are summarized in the Ouput Voltage Programming tables below.

At the PMU power on, LDO's start up according to the selected startup sequence, and the default voltages after startup sequence depend on startup setup. See section Power-On and Power-Off Sequences for details.

For stability all LDO's have to be connected to output an external capacitor C_{OUT} with recommended value of 1 µF. It is important to select the type of capacitor which capacitance will in no case (voltage, temperature, etc) be outside of limits specified in the LDO Electrical Characteristics.

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Table 12. LDO1, 2, 3 and 5 Output Voltage Programming

Data Code LDOx_V	LDOx [V]	Data Code LDOx_V	LDOx [V]
5h'00	1.20	5h'10	2.10
5h'01	1.25	5h'11	2.20
5h'02	1.30	5h'12	2.30
5h'03	1.35	5h'13	2.40
5h'04	1.40	5h'14	2.50
5h'05	1.45	5h'15	2.60
5h'06	1.50	5h'16	2.65
5h'07	1.55	5h'17	2.70
5h'08	1.60	5h'18	2.75
5h'09	1.65	5h'19	2.80
5h'0A	1.70	5h'1A	2.85
5h'0B	1.75	5h'1B	2.90
5h'0C	1.80	5h'1C	2.95
5h'0D	1.85	5h'1D	3.00
5h'0E	1.90	5h'1E	3.10
5h'0F	2.00	5h'1F	3.30

Table 13. LDO4 Output Voltage Programming

Data Code LDO4_V	LDO4 [V]	Data Code LDO4_V	LDO4 [V]
5h'00	0.80	5h'10	1.75
5h'01	0.85	5h'11	1.80
5h'02	0.90	5h'12	1.85
5h'03	1.00	5h'13	1.90
5h'04	1.10	5h'14	2.00
5h'05	1.20	5h'15	2.10
5h'06	1.25	5h'16	2.20
5h'07	1.30	5h'17	2.30
5h'08	1.35	5h'18	2.40
5h'09	1.40	5h'19	2.50
5h'0A	1.45	5h'1A	2.60
5h'0B	1.50	5h'1B	2.65
5h'0C	1.55	5h'1C	2.70
5h'0D	1.60	5h'1D	2.75
5h'0E	1.65	5h'1E	2.80
5h'0F	1.70	5h'1F	2.85

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A-Type LDO Electrical Characteristics

Unless otherwise noted, $V_{VBATT} = V_{VINB} = V_{VIN1} = V_{VIN2} = 3.6V$, GND = GNDB = 0V, $C_{VBATT} = C_{VIN1} = C_{VIN2} = 2.2\ \mu F$, $C_{VINB} = 10\ \mu F$. Typical values and limits appearing in normal type apply for T_J=25°C. Limits appearing in **boldface** type apply over the entire junction temperature range for operation, T_J= -40 to +125°C(1)

Parameter		Test Conditions	LDO#	Typ	Limit		Units
					Min	Max	
V_{OUT}	Output Voltage Accuracy	I_{OUT} = 1mA, V_{OUT} = 2.85V	2,3		-2%	+2%	
					-3%	**+3%**	
I_{SC}	Output Current Limit	V_{OUT} = 0V	2,3	600			mA
V_{DO}	Dropout Voltage	$I_{OUT} = I_{MAX}$(2)	2,3	200		**400**	mV
ΔV_{OUT}	Line Regulation	V_{OUT} + 0.5V ≤ V_{IN} ≤ 4.5V $I_{OUT} = I_{MAX}$	2,3	1			mV
	Load Regulation	1 mA ≤ I_{OUT} ≤ I_{MAX}	2,3	5			mV
e_N	Output Noise Voltage	10Hz ≤ f ≤ 100kHz C_{OUT} = 1 µF(3)	2,3	15			μV_{RMS}
PSRR	Power Supply Ripple Rejection Ratio	f = 10 kHz, C_{OUT} = 1 µF, I_{OUT} = 20 mA(3)	2,3	70			dB
$t_{startup}$	Startup Time from Shutdown	C_{OUT} = 1 µF, $I_{OUT} = I_{MAX}$(3)	2,3	35			µs
$V_{Transient}$	Startup Transient Overshoot	C_{OUT} = 1 µF, $I_{OUT} = I_{MAX}$(3)	2,3			**30**	mV
C_{OUT}	External output capacitance for stability		2,3	1.0	**0.5**	**20**	µF

(1) All limits are specified. All electrical characteristics having room-temperature limits are tested during production with T_J = 25°C. All hot and cold limits are ensured by correlating the electrical characteristics to process and temperature variations and applying statistical process control.
(2) Dropout voltage is the input-to-output voltage difference at which the output voltage is 100mV below its nominal value. This specification does not apply in cases it implies operation with an input voltage below the 2.5V minimum appearing under Operating Ratings. For example, this specification does not apply for devices having 1.5V outputs because the specification would imply operation with an input voltage at or about 1.5V.
(3) Ensured by design.

D-Type and LO-Type LDO Electrical Characteristics

Unless otherwise noted, $V_{VBATT} = V_{VINB} = V_{VIN1} = V_{VIN2} = 3.6V$, GND = GNDB = 0V, $C_{VBATT} = C_{VIN1} = C_{VIN2} = 2.2\ \mu F$, $C_{VINB} = 10\ \mu F$. Typical values and limits appearing in normal type apply for T_J = 25°C. Limits appearing in **boldface** type apply over the entire junction temperature range for operation, T_J= -40 to +125°C(1)

Parameter		Test Conditions	LDO#	Typ	Limit		Units
					Min	Max	
V_{OUT}	Output Voltage Accuracy	I_{OUT} = 1mA, V_{OUT} = 2.85V	1,5		-2%	+2%	
					-3%	**+3%**	
		I_{OUT} = 1mA, V_{OUT} = 1.20V	4		-2%	+2%	
					-3%	**+3%**	
		I_{OUT} = 1mA, V_{OUT} = 2.60V	4		-3%	+3%	
					-4%	**+4%**	
I_{SC}	Output Current Limit	V_{OUT} = 0V	1,4,5	600			mA
V_{DO}	Dropout Voltage	$I_{OUT} = I_{MAX}$(2)	1,4,5	190		**400**	mV
ΔV_{OUT}	Line Regulation	V_{OUT} + 0.5V ≤ V_{IN} ≤ 4.5V $I_{OUT} = I_{MAX}$	1,4,5	2			mV
	Load Regulation	1mA ≤ I_{OUT} ≤ I_{MAX}	1,4,5	5			mV
e_N	Output Noise Voltage	10Hz ≤ f ≤ 100kHz, C_{OUT} = 1 µF(3)	1,4,5	100			μV_{RMS}

(1) All limits are specified. All electrical characteristics having room-temperature limits are tested during production with T_J = 25°C. All hot and cold limits are ensured by correlating the electrical characteristics to process and temperature variations and applying statistical process control.
(2) Dropout voltage is the input-to-output voltage difference at which the output voltage is 100mV below its nominal value. This specification does not apply in cases it implies operation with an input voltage below the 2.5V minimum appearing under Operating Ratings. For example, this specification does not apply for devices having 1.5V outputs because the specification would imply operation with an input voltage at or about 1.5V.
(3) Ensured by design.

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D-Type and LO-Type LDO Electrical Characteristics (continued)

Unless otherwise noted, $V_{VBATT} = V_{VINB} = V_{VIN1} = V_{VIN2} = 3.6V$, GND = GNDB = 0V, $C_{VBATT} = C_{VIN1} = C_{VIN2} = 2.2\ \mu F$, $C_{VINB} = 10\ \mu F$. Typical values and limits appearing in normal type apply for $T_J = 25°C$. Limits appearing in **boldface** type apply over the entire junction temperature range for operation, T_J= -40 to +125°C(1)

Parameter		Test Conditions	LDO#	Typ	Limit		Units
					Min	Max	
PSRR	Power Supply Ripple Rejection Ratio	f =10 kHz, C_{OUT} = 1 µF, I_{OUT} = 20 mA(3)	1,4,5	55			dB
$t_{startup}$	Startup Time from Shutdown	C_{OUT} = 1 µF, $I_{OUT} = I_{MAX}$(3)	1,4,5	35			µs
$V_{Transient}$	Startup Transient Overshoot	C_{OUT} = 1µF, $I_{OUT} = I_{MAX}$(3)	1,4,5			**30**	mV
C_{OUT}	External output capacitance for stability		1,4,5	1.0	**0.5**	**20**	µF

Serial Interface

Unless otherwise noted, $V_{VBATT} = V_{VINB} = V_{VIN1} = V_{VIN2} = 3.6V$, GND = GNDB = 0V, $C_{VBATT} = C_{VIN1} = C_{VIN2} = 2.2\ \mu F$, $C_{VINB} = 10\ \mu F$. Typical values and limits appearing in normal type apply for T_J= 25°C. Limits appearing in **boldface** type apply over the entire junction temperature range for operation, T_J= -40 to +125°C(1)(2)

Parameter		Test Conditions	Typ	Limit		Units
				Min	Max	
f_{CLK}	Clock Frequency				400	kHz
t_{BF}	Bus-Free Time between START and STOP			1.3		µs
t_{HOLD}	Hold Time Repeated START Condition			0.6		µs
t_{CLK-LP}	CLK Low Period			1.3		µs
t_{CLK-HP}	CLK High Period			0.6		µs
t_{SU}	Set-Up Time Repeated START Condition			0.6		µs
$t_{DATA-HOLD}$	Data Hold Time			50		ns
$t_{DATA-SU}$	Data Set-Up Time			100		ns
t_{SU}	Set-Up Time for STOP Condition			0.6		µs
t_{TRANS}	Maximum Pulse Width of Spikes that Must Be Suppressed by the Input Filter of Both DATA and CLK Signals		50			ns

(1) All limits are specified. All electrical characteristics having room-temperature limits are tested during production with T_J = 25°C. All hot and cold limits are ensured by correlating the electrical characteristics to process and temperature variations and applying statistical process control.
(2) Ensured by design.

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I²C-COMPATIBLE SERIAL BUS INTERFACE

Interface Bus Overview

The I²C compatible synchronous serial interface provides access to the programmable functions and registers on the device.

This protocol uses a two-wire interface for bi-directional communications between the IC's connected to the bus. The two interface lines are the Serial Data Line (SDA), and the Serial Clock Line (SCL). These lines should be connected to a positive supply, via a pull-up resistor of 1.5 kΩ, and remain HIGH even when the bus is idle.

Every device on the bus is assigned a unique address and acts as either a Master or a Slave depending on whether it generates or receives the serial clock (SCL).

Data Transactions

One data bit is transferred during each clock pulse. Data is sampled during the high state of the serial clock (SCL). Consequently, throughout the clock's high period, the data should remain stable. Any changes on the SDA line during the high state of the SCL and in the middle of a transaction, aborts the current transaction. New data should be sent during the low SCL state. This protocol permits a single data line to transfer both command/control information and data using the synchronous serial clock.

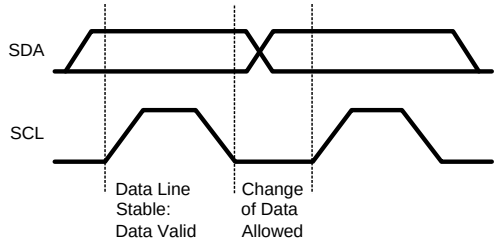


Figure 4. Bit Transfer

Each data transaction is composed of a Start Condition, a number of byte transfers (set by the software) and a Stop Condition to terminate the transaction. Every byte written to the SDA bus must be 8 bits long and is transferred with the most significant bit first. After each byte, an Acknowledge signal must follow. The following sections provide further details of this process.

Start and Stop

The Master device on the bus always generates the Start and Stop Conditions (control codes). After a Start Condition is generated, the bus is considered busy and it retains this status until a certain time after a Stop Condition is generated. A high-to-low transition of the data line (SDA) while the clock (SCL) is high indicates a Start Condition. A low-to-high transition of the SDA line while the SCL is high indicates a Stop Condition.

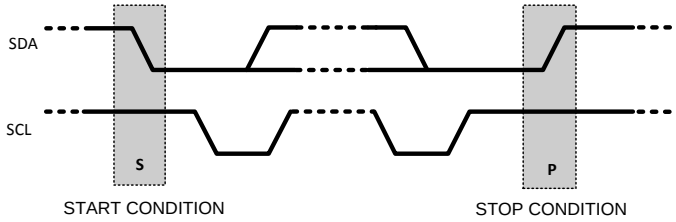


Figure 5. Start and Stop Conditions

In addition to the first Start Condition, a repeated Start Condition can be generated in the middle of a transaction. This allows another device to be accessed, or a register read cycle.

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Acknowledge Cycle

The Acknowledge Cycle consists of two signals: the acknowledge clock pulse the master sends with each byte transferred, and the acknowledge signal sent by the receiving device.

The master generates the acknowledge clock pulse on the ninth clock pulse of the byte transfer. The transmitter releases the SDA line (permits it to go high) to allow the receiver to send the acknowledge signal. The receiver must pull down the SDA line during the acknowledge clock pulse and ensure that SDA remains low during the high period of the clock pulse, thus signaling the correct reception of the last data byte and its readiness to receive the next byte.

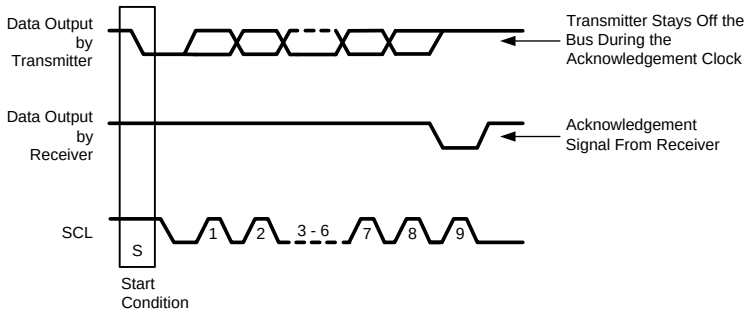


Figure 6. Bus Acknowledge Cycle

”Acknowledge After Every Byte” Rule

The master generates an acknowledge clock pulse after each byte transfer. The receiver sends an acknowledge signal after every byte received.

There is one exception to the “acknowledge after every byte” rule.

When the master is the receiver, it must indicate to the transmitter an end of data by not-acknowledging (“negative acknowledge”) the last byte clocked out of the slave. This “negative acknowledge” still includes the acknowledge clock pulse (generated by the master), but the SDA line is not pulled down.

Addressing Transfer Formats

Each device on the bus has a unique slave address. The LP8720 operates as a slave device. Slave address is selectable by IDSEL-pin.

- When IDSEL= VBATT then slave address is 7h’7F.
- When IDSEL= floating (Hi-Z) then slave address is 7h’7C.
- When IDSEL= GND then slave address is 7h’7D.

Before any data is transmitted, the master transmits the address of the slave being addressed. The slave device should send an acknowledge signal on the SDA line, once it recognizes its address.

The slave address is the first seven bits after a Start Condition. The direction of the data transfer (R/W) depends on the bit sent after the slave address — the eighth bit.

When the slave address is sent, each device in the system compares this slave address with its own. If there is a match, the device considers itself addressed and sends an acknowledge signal. Depending upon the state of the R/W bit (1:read, 0:write), the device acts as a transmitter or a receiver.

Control Register Write Cycle

- Master device generates start condition.
- Master device sends slave address (7 bits) and the data direction bit (r/w = '0').
- Slave device sends acknowledge signal if the slave address is correct.
- Master sends control register address (8 bits).
- Slave sends acknowledge signal.
- Master sends data byte to be written to the addressed register.

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- Slave sends acknowledge signal.
- If master will send further data bytes the control register address will be incremented by one after acknowledge signal.
- Write cycle ends when the master creates stop condition.

Control Register Read Cycle

- Master device generates a start condition.
- Master device sends slave address (7 bits) and the data direction bit (r/w = '0').
- Slave device sends acknowledge signal if the slave address is correct.
- Master sends control register address (8 bits).
- Slave sends acknowledge signal.
- Master device generates repeated start condition.
- Master sends the slave address (7 bits) and the data direction bit (r/w = “1”).
- Slave sends acknowledge signal if the slave address is correct.
- Slave sends data byte from addressed register.
- If the master device sends acknowledge signal, the control register address will be incremented by one. Slave device sends data byte from addressed register.
- Read cycle ends when the master does not generate acknowledge signal after data byte and generates stop condition.

	Address Mode
Data Read	<Start Condition> <Slave Address><r/w = ‘0’>[Ack] <Register Addr.>[Ack] <Repeated Start Condition> <Slave Address><r/w = ‘1’>[Ack] [Register Data]<Ack or NAck> … additional reads from subsequent register address possible <Stop Condition>
Data Write	<Start Condition> <Slave Address><r/w = ‘0’>[Ack] <Register Addr.>[Ack] <Register Data>[Ack] … additional writes to subsequent register address possible <Stop Condition>
< > Data from master [ ] Data from slave	

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Register Read and Write Detail

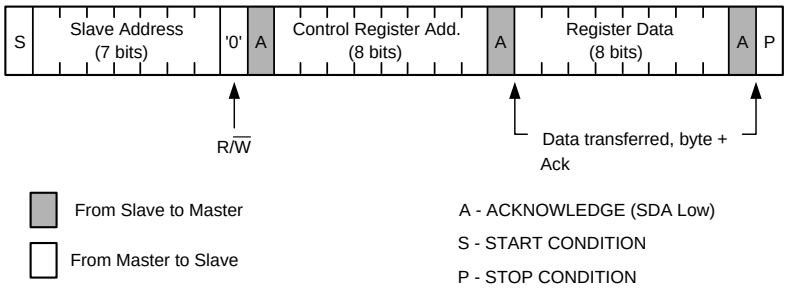


Figure 7. Register Write Format

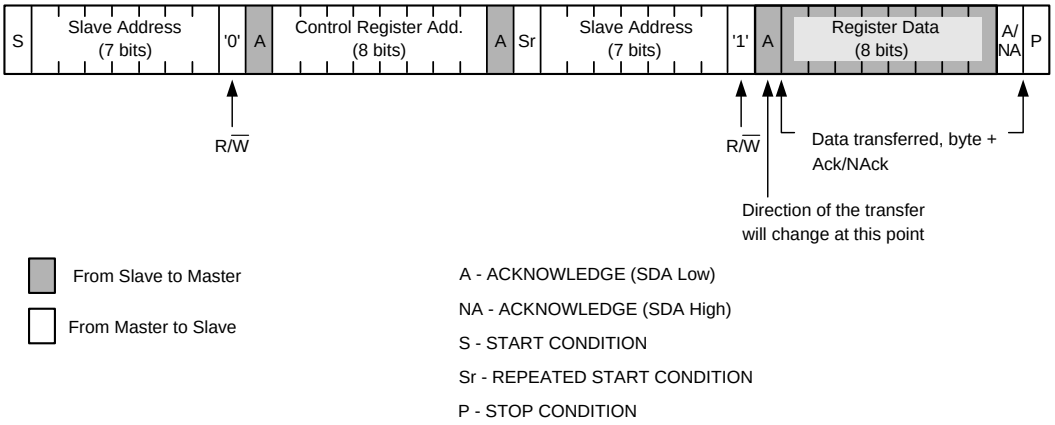


Figure 8. Register Read Format

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REVISION HISTORY

Changes from Revision A (May 2013) to Revision B	Page
• Changed layout of National Data Sheet to TI format	20

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PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
LP8720TLE/NOPB	ACTIVE	DSBGA	YZR	20	250	RoHS & Green	SNAGCU	Level-1-260C-UNLIM	-40 to 125	8720	Samples
LP8720TLX/NOPB	ACTIVE	DSBGA	YZR	20	3000	RoHS & Green	SNAGCU	Level-1-260C-UNLIM	-40 to 125	8720	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

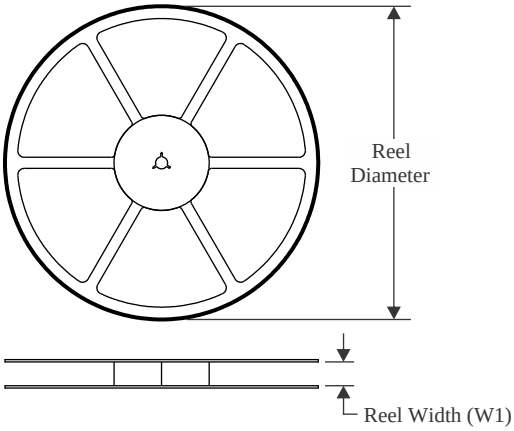
(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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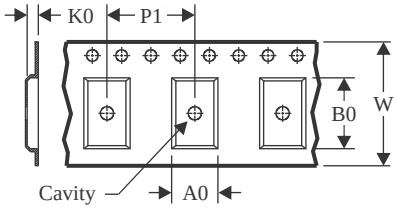
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TAPE AND REEL INFORMATION

REEL DIMENSIONS

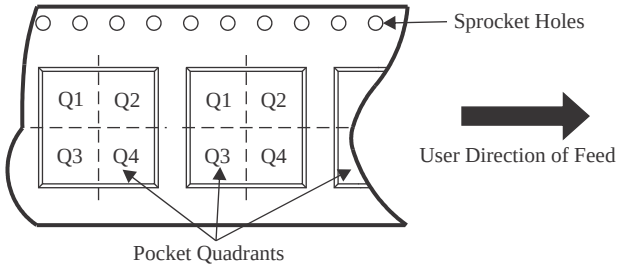


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

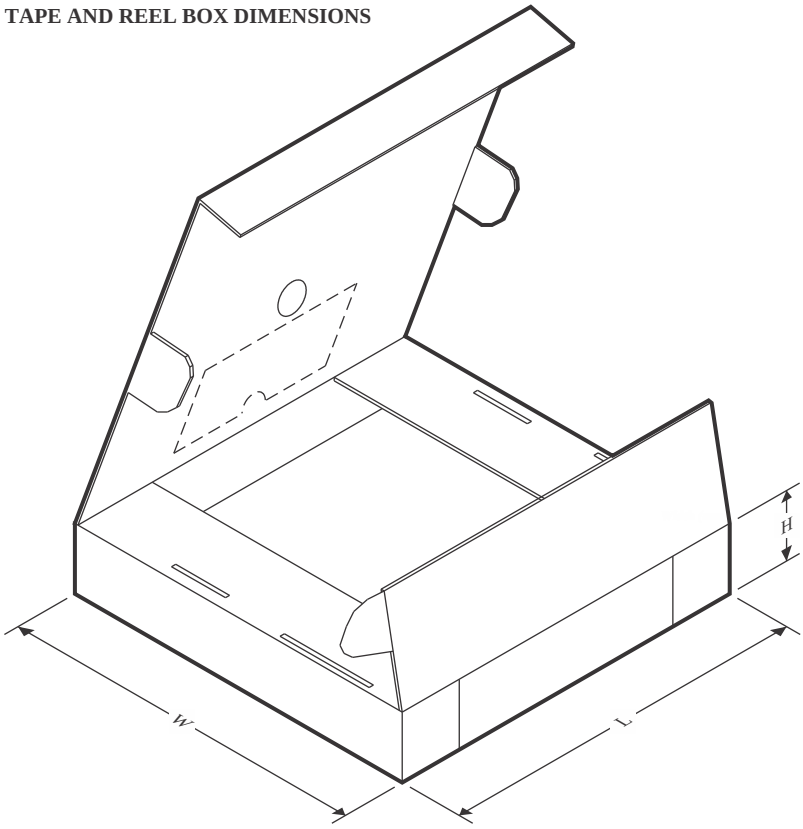
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
LP8720TLE/NOPB	DSBGA	YZR	20	250	178.0	8.4	2.18	2.69	0.76	4.0	8.0	Q1
LP8720TLX/NOPB	DSBGA	YZR	20	3000	178.0	8.4	2.18	2.69	0.76	4.0	8.0	Q1

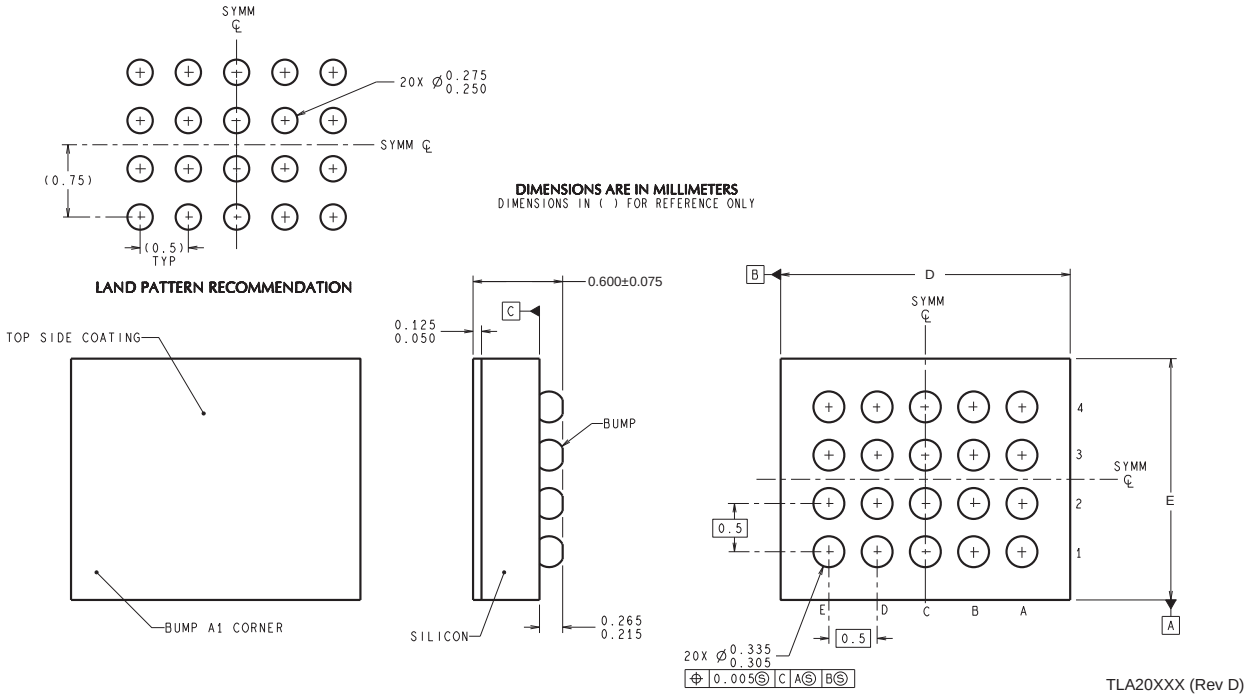
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
LP8720TLE/NOPB	DSBGA	YZR	20	250	208.0	191.0	35.0
LP8720TLX/NOPB	DSBGA	YZR	20	3000	208.0	191.0	35.0

YZR0020



D: Max = 2.49 mm, Min = 2.43 mm

E: Max = 1.99 mm, Min = 1.93 mm

4215053/A 12/12

NOTES: A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.
B. This drawing is subject to change without notice.

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