National Semiconductor

October 2003

LP8340
Low Dropout, Low I_Q, 1.0A CMOS Linear Regulator

General Description

The LP8340 low-dropout CMOS linear regulator is available in 5V, 3.3V, 2.5V, 1.8V and adjustable output versions. Packaged in the 6ld LLP package and 3ld DPAK. The LP8340 can deliver up to 1.0A output current.

Typical dropout voltage is 420mV at 1.0A for the 5.0V version, 540mV at 1.0A for the 3.3V version, 670mV at 1.0A for the 2.5V version and 680mV at 800mA for the 1.8V version.

The LP8340 includes a zener trimmed bandgap voltage reference, foldback current limiting and thermal overload limiting.

The LP8340 features a PMOS output transistor which unlike PNP type low dropout regulators requires no base drive current. This allows the device ground current to remain less than 50µA over operating temperature, supply voltage and irrespective of the load current.

Features

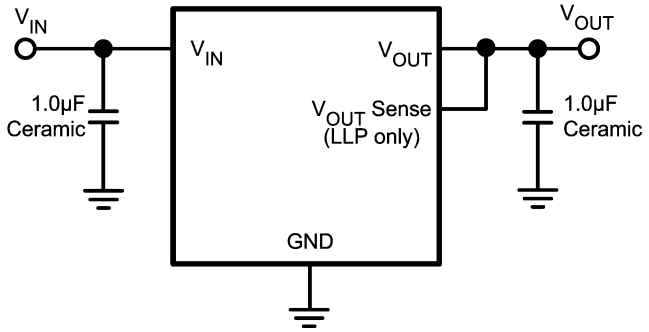
- ±1.5% Typical V_{OUT} tolerance
- 420mV Typical Dropout @ 1.0A (V_O = 5V)
- Wide Operating Range 2.7V to 10V
- Internal 1.0A PMOS Output Transistor
- 19µA Typical Quiescent Current
- Thermal Overload Limiting
- Foldback Current Limiting
- Zener Trimmed Bandgap Reference
- Space saving LLP package
- Temperature Range
  - — LP8340C 0˚C to 125˚C
  - — LP8340I –40˚C to 125˚C

Applications

- Hard Disk Drives
- Notebook Computers
- Battery Powered Electronics
- Portable Instrumentation

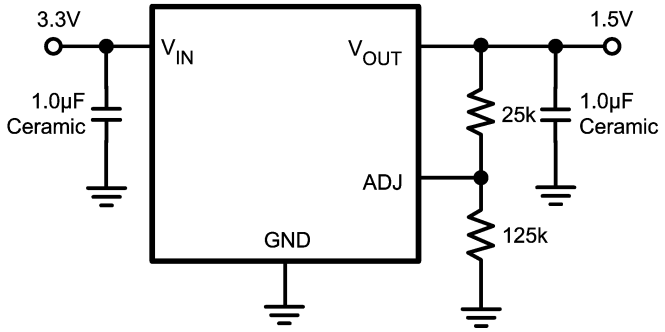
Typical Applications

Fixed V_{OUT}



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Adjustable V_{OUT}



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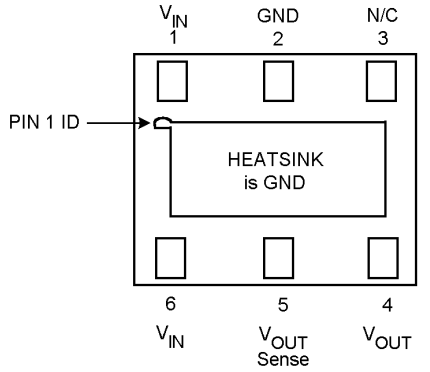
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Ordering Information

Package	Part Number	Package Marking	Transport Media	NSC Drawing
6-Pin LLP	LP8340CLD-ADJ	L041B	1k Units Tape and Reel	LDE06A
	LP8340CLDX-ADJ		4.5k Units Tape and Reel	
	LP8340CLD-1.8	L042B	1k Units Tape and Reel	
	LP8340CLDX-1.8		4.5k Units Tape and Reel	
	LP8340CLD-2.5	L043B	1k Units Tape and Reel	
	LP8340CLDX-2.5		4.5k Units Tape and Reel	
	LP8340CLD-3.3	L051B	1k Units Tape and Reel	
	LP8340CLDX-3.3		4.5k Units Tape and Reel	
	LP8340CLD-5.0	L044B	1k Units Tape and Reel	
	LP8340CLDX-5.0		4.5k Units Tape and Reel	
	LP8340ILD-ADJ	L078B	1k Units Tape and Reel	
	LP8340ILDX-ADJ		4.5k Units Tape and Reel	
	LP8340ILD-1.8	L079B	1k Units Tape and Reel	
	LP8340ILDX-1.8		4.5k Units Tape and Reel	
	LP8340ILD-2.5	L080B	1k Units Tape and Reel	
	LP8340ILDX-2.5		4.5k Units Tape and Reel	
	LP8340ILD-3.3	L081B	1k Units Tape and Reel	
	LP8340ILDX-3.3		4.5k Units Tape and Reel	
	LP8340ILD-5.0	L082B	1k Units Tape and Reel	
	LP8340ILDX-5.0		4.5k Units Tape and Reel	
3-Pin DPAK	LP8340CDT-1.8	LP8340CDT-1.8	75 Units/Rail	TD03B
	LP8340CDTX-1.8		2.5k Units Tape and Reel	
	LP8340CDT-2.5	LP8340CDT-2.5	75 Units/Rail	
	LP8340CDTX-2.5		2.5k Units Tape and Reel	
	LP8340CDT-3.3	LP8340CDT-3.3	75 Units/Rail	
	LP8340CDTX-3.3		2.5k Units Tape and Reel	
	LP8340CDT-5.0	LP8340CDT-5.0	75 Units/Rail	
	LP8340CDTX-5.0		2.5k Units Tape and Reel	
	LP8340IDT-1.8	LP8340IDT-1.8	75 Units/Rail	
	LP8340IDTX-1.8		2.5k Units Tape and Reel	
	LP8340IDT-2.5	LP8340IDT-2.5	75 Units/Rail	
	LP8340IDTX-2.5		2.5k Units Tape and Reel	
	LP8340IDT-3.3	LP8340IDT-3.3	75 Units/Rail	
	LP8340IDTX-3.3		2.5k Units Tape and Reel	
	LP8340IDT-5.0	LP8340IDT-5.0	75 Units/Rail	
	LP8340IDTX-5.0		2.5k Units Tape and Reel	

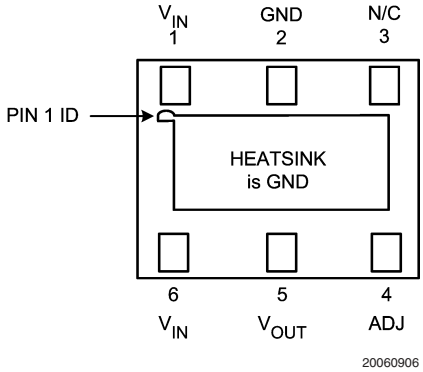
Connection Diagrams

6-Pin LLP
FIXED OUTPUT VOLTAGE



Bottom View

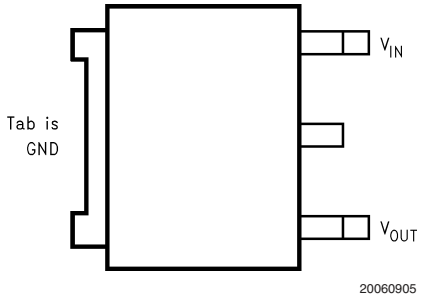
6-Pin LLP
ADJUSTABLE OUTPUT VOLTAGE



Bottom View

Note: V_{IN} Pins (Pin 1 & 6) must be connected together externally for full 1 amp operation (500mA max per pin).
V_{OUT} Sense (Pin 5) must be connected to V_{OUT} (Pin 4).

T0-252



Top View

Absolute Maximum Ratings (Notes 1, 2)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

V_{IN}, V_{OUT}, V_{OUT} Sense, ADJ	−0.3V to 12V
Storage Temperature Range	−65˚C to 160˚C
Junction Temperature (T_J)	150˚C
Power Dissipation	(Note 3)
ESD Rating	
Human Body Model (Note 6)	2kV
Machine Model	200V

Operating Ratings (Notes 1, 2)

Supply Voltage	2.7 to 10V
Temperature Range	
LP8340C	0˚C to 125˚C
LP8340I	−40˚C to 125˚C

LP8340C Electrical Characteristics

Unless otherwise specified all limits guaranteed for $V_{IN} = V_O + 1V$, $C_{IN} = C_{OUT} = 10\mu F$, $T_J = 25˚C$. **Boldface** limits apply over the full operating temperature range of $T_J = 0˚C$ to 125˚C

Symbol	Parameter	Conditions	Min (Note 5)	Typ (Note 4)	Max (Note 5)	Units
V_{IN}	Input Voltage	LP8340-ADJ,1.8, 2.5	**2.7**		**10**	V
		LP8340-3.3, 5.0			**10**	
V_{OUT}	Output Voltage	LP8340-ADJ, ADJ = OUT				V
		I_{OUT} = 10mA, V_{IN} = 2.7V, T_J = 25˚C	1.231	1.250	1.269	
		100µA ≤I_{OUT}≤ 800mA, 3.0V ≤V_{IN}≤V_{OUT} +4V	**1.213**		**1.288**	
		800mA <I_{OUT} ≤1.0A, 3.2V ≤V_{IN} ≤V_{OUT} +4V	**1.213**		**1.288**	
		LP8340-1.8				V
		I_{OUT} = 10mA, V_{IN} = 2.8V, T_J = 25˚C	1.773	1.800	1.827	
		100µA ≤I_{OUT} ≤800mA, 3.2V ≤V_{IN}≤6V	**1.746**		**1.854**	
		800mA <I_{OUT} ≤1.0A, 3.4V ≤V_{IN} ≤6V	**1.746**		**1.854**	
		LP8340-2.5				V
		I_{OUT} = 10mA, V_{IN} = 3.8V, T_J = 25˚C	2.463	2.500	2.538	
		100µA ≤I_{OUT} ≤1.0A, 3.8V ≤V_{IN} ≤6.5V	**2.425**		**2.575**	
		LP8340-3.3				V
		I_{OUT} = 10mA, V_{IN} = 4.3V T_J = 25˚C	3.250	3.300	3.350	
		100µA ≤I_{OUT} ≤1.0A, 4.3V ≤V_{IN} ≤7.5V	**3.201**		**3.399**	
		LP8340-5.0				V
		I_{OUT} = 10mA, V_{IN} = 6V, T_J = 25˚C	4.925	5.000	5.075	
		100µA ≤I_{OUT} ≤1.0A, 6V ≤V_{IN} ≤9V	**4.850**		**5.150**	
ΔV_O	Load Regulation	LP8340-ADJ, ADJ=OUT				mV
		I_{OUT} = 1mA to 1.0A, V_{IN} = 3.2V		6	**25**	
		LP8340-1.8				
		I_{OUT} = 1mA to 1.0A, V_{IN} = 3.4V		8	**30**	
		LP8340-2.5				
		I_{OUT} = 1mA to 1.0A, V_{IN} = 3.5V		15	**50**	
		LP8340-3.3				
		I_{OUT} = 1mA to 1.0A, V_{IN} = 4.3V		20	**75**	
		LP8340-5.0				
		I_{OUT} = 1mA to 1.0A, V_{IN} = 6V		25	**100**	
ΔV_O	Line Regulation	V_{OUT} + 0.5V ≤V_{IN} ≤10V, I_{OUT} = 25mA (Note 7)		4	**15**	mV

LP8340C Electrical Characteristics (Continued)

Unless otherwise specified all limits guaranteed for $V_{IN} = V_O + 1V$, $C_{IN} = C_{OUT} = 10\mu F$, $T_J = 25^\circ C$. **Boldface** limits apply over the full operating temperature range of $T_J = 0^\circ C$ to $125^\circ C$

Symbol	Parameter	Conditions	Min (Note 5)	Typ (Note 4)	Max (Note 5)	Units
$V_{IN} - V_O$	Dropout Voltage (Note 7) (Note 8)	LP8340-1.8 I_{OUT} = 800mA		680	**1400**	mV
		LP8340-2.5 I_{OUT} = 800mA		550	**1000**	
		LP8340-2.5 I_{OUT} = 1.0A		670	**1300**	
		LP8340-3.3 LP8340-ADJ, V_{OUT} = 3.3V, I_{OUT} = 800mA		420	**800**	
		LP8340-3.3 LP8340-ADJ, I_{OUT} = 1.0A		540	**1000**	
		LP8340-5.0 I_{OUT} = 800mA		330	**650**	
		LP8340-5.0 I_{OUT} = 1.0A		420	**800**	
I_Q	Quiescent Current	$V_{IN} \leq 10V$		19	**50**	µA
	Minimum Load Current	$V_{IN} - V_{OUT} \leq 4V$			**100**	µA
I_{LIMIT}	Foldback Current Limit	$V_{IN} - V_{OUT} > 5V$		450		mA
		$V_{IN} - V_{OUT} < 4V$		1600		
	Ripple Rejection Ratio	V_{IN} (dc) = V_{OUT} + 2V V_{IN} (ac) = 1 V_{P-P} @ 120Hz	**48**	55		dB
T_{SD}	Thermal Shutdown Temp. Thermal Shutdown Hyst.			160 10		°C
	ADJ Input Leakage Current	V_{ADJ} = 1.5V or 0V		±0.01	±100	nA
	V_{OUT} Leakage Current	LP8340-ADJ ADJ = OUT, V_{OUT} = 2V, V_{IN} = 10V			10	µA
		LP8340-1.8, V_{OUT} = 2.5V, V_{IN} = 10V			10	
		LP8340-2.5, V_{OUT} = 3.5V, V_{IN} = 10V			10	
		LP8340-3.3, V_{OUT} = 4V, V_{IN} = 10V			10	
		LP8340-5.0, V_{OUT} = 6V, V_{IN} = 10V			10	
e_n	Output Noise	10Hz to 10kHz, R_L = 1kΩ, C_{OUT} = 10µF		250		µVrms

LP8340I Electrical Characteristics

Unless otherwise specified all limits guaranteed for $V_{IN} = V_O + 1V$, $C_{IN} = C_{OUT} = 10\mu F$, $T_J = 25^\circ C$. **Boldface** limits apply over the full operating temperature range of $T_J = -40^\circ C$ to $125^\circ C$

Symbol	Parameter	Conditions	Min (Note 5)	Typ (Note 4)	Max (Note 5)	Units
V_{IN}	Input Voltage	LP8340-ADJ,1.8, 2.5	**2.7**		**10**	V
		LP8340-3.3, 5.0			**10**	

LP8340I Electrical Characteristics (Continued)

Unless otherwise specified all limits guaranteed for $V_{IN} = V_O + 1V$, $C_{IN} = C_{OUT} = 10\mu F$, $T_J = 25^\circ C$. **Boldface** limits apply over the full operating temperature range of $T_J = -40^\circ C$ to $125^\circ C$

Symbol	Parameter	Conditions	Min (Note 5)	Typ (Note 4)	Max (Note 5)	Units
V_{OUT}	Output Voltage	LP8340-ADJ, ADJ = OUT				
		I_{OUT} = 10mA, V_{IN} = 2.7V, $T_J = 25^\circ C$	1.231	1.250	1.269	V
		100µA ≤I_{OUT}≤ 800mA, 3.0V ≤V_{IN}≤V_{OUT} +4V	**1.213**		**1.288**	
		800mA <I_{OUT} ≤1.0A, 3.2V ≤V_{IN} ≤V_{OUT} +4V	**1.213**		**1.288**	
		LP8340-1.8				
		I_{OUT} = 10mA, V_{IN} = 2.8V, $T_J = 25^\circ C$	1.773	1.800	1.827	V
		100µA ≤I_{OUT} ≤800mA, 3.2V ≤V_{IN}≤6V	**1.746**		**1.854**	
		800mA <I_{OUT} ≤1.0A, 3.4V ≤V_{IN} ≤6V	**1.746**		**1.854**	
		LP8340-2.5				
		I_{OUT} = 10mA, V_{IN} = 3.8V, $T_J = 25^\circ C$	2.463	2.500	2.538	V
		100µA ≤I_{OUT} ≤1.0A, 3.8V ≤V_{IN} ≤6.5V	**2.425**		**2.575**	
		LP8340-3.3				
		I_{OUT} = 10mA, V_{IN} = 4.3V $T_J = 25^\circ C$	3.250	3.300	3.350	V
		100µA ≤I_{OUT} ≤1.0A, 4.3V ≤V_{IN} ≤7.5V	**3.201**		**3.399**	
		LP8340-5.0				
		I_{OUT} = 10mA, V_{IN} = 6V, $T_J = 25^\circ C$	4.925	5.000	5.075	V
		100µA ≤I_{OUT} ≤1.0A, 6V ≤V_{IN} ≤9V	**4.850**		**5.150**	
ΔV_O	Load Regulation	LP8340-ADJ, ADJ=OUT				
		I_{OUT} = 1mA to 1.0A, V_{IN} = 3.2V		6	**25**	
		LP8340-1.8				
		I_{OUT} = 1mA to 1.0A, V_{IN} = 3.4V		8	**30**	
		LP8340-2.5				mV
		I_{OUT} = 1mA to 1.0A, V_{IN} = 3.5V		15	**50**	
		LP8340-3.3				
		I_{OUT} = 1mA to 1.0A, V_{IN} = 4.3V		20	**75**	
		LP8340-5.0				
		I_{OUT} = 1mA to 1.0A, V_{IN} = 6V		25	**100**	
ΔV_O	Line Regulation	V_{OUT} + 0.5V ≤V_{IN} ≤10V, I_{OUT} = 25mA (Note 7)		4	**15**	mV
$V_{IN} - V_O$	Dropout Voltage (Note 7) (Note 8)	LP8340-1.8				
		I_{OUT} = 800mA		680	**1400**	
		LP8340-2.5				
		I_{OUT} = 800mA		550	**1000**	
		LP8340-2.5				
		I_{OUT} = 1.0A		670	**1300**	
		LP8340-3.3				mV
		LP8340-ADJ, V_{OUT} = 3.3V, I_{OUT} = 800mA		420	**800**	
		LP8340-3.3				
		LP8340-ADJ, I_{OUT} = 1.0A		540	**1000**	
		LP8340-5.0				
		I_{OUT} = 800mA		330	**650**	
		LP8340-5.0				
		I_{OUT} = 1.0A		420	**800**	
I_Q	Quiescent Current	V_{IN} ≤10V		19	**50**	µA
	Minimum Load Current	$V_{IN} - V_{OUT}$ ≤4V			**100**	µA
I_{LIMIT}	Foldback Current Limit	$V_{IN} - V_{OUT}$ >5V		450		mA
		$V_{IN} - V_{OUT}$ <4V		1600		
	Ripple Rejection Ratio	V_{IN} (dc) = V_{OUT} + 2V V_{IN} (ac) = 1 V_{P-P} @ 120Hz	**48**	55		dB

LP8340I Electrical Characteristics (Continued)

Unless otherwise specified all limits guaranteed for $V_{IN} = V_O + 1V$, $C_{IN} = C_{OUT} = 10\mu F$, $T_J = 25^\circ C$. **Boldface** limits apply over the full operating temperature range of $T_J = -40^\circ C$ to $125^\circ C$

Symbol	Parameter	Conditions	Min (Note 5)	Typ (Note 4)	Max (Note 5)	Units
T_{SD}	Thermal Shutdown Temp. Thermal Shutdown Hyst.			160 10		˚C
	ADJ Input Leakage Current	V_{ADJ} = 1.5V or 0V		±0.01	±100	nA
	V_{OUT} Leakage Current	LP8340-ADJ ADJ = OUT, V_{OUT} = 2V, V_{IN} = 10V			10	µA
		LP8340-1.8, V_{OUT} = 2.5V, V_{IN} = 10V			10	
		LP8340-2.5, V_{OUT} = 3.5V, V_{IN} = 10V			10	
		LP8340-3.3, V_{OUT} = 4V, V_{IN} = 10V			10	
		LP8340-5.0, V_{OUT} = 6V, V_{IN} = 10V			10	
e_n	Output Noise	10Hz to 10kHz, R_L = 1kΩ, C_{OUT} = 10µF		250		µVrms

Note 1: Absolute Maximum ratings indicate limits beyond which damage may occur. Electrical specifications do not apply when operating the device outside of its rated operating conditions.

Note 2: All voltages are with respect to the potential at the ground pin.

Note 3: Maximum Power dissipation for the device is calculated using the following equations:

$$P_D = \frac{T_{J(MAX)} - T_A}{\theta_{JA}}$$

where $T_{J(MAX)}$ is the maximum junction temperature, T_A is the ambient temperature, and θ_{JA} is the junction-to-ambient thermal resistance. The value of the θ_{JA} for the LLP package is specifically dependant on the PCB trace area, trace material, and the number of layers and thermal vias. For improved thermal resistance and power dissipation for the LLP package, refer to Application Note AN-1187.

Note 4: Typical Values represent the most likely parametric norm.

Note 5: All limits are guaranteed by testing or statistical analysis.

Note 6: Human body model 1.5kΩ in series with 100pF.

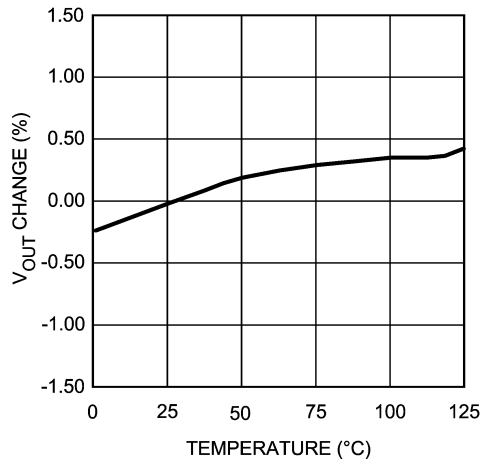
Note 7: Condition does not apply to input voltages below 2.7V since this is the minimum input operating voltage.

Note 8: Dropout voltage is measured by reducing V_{IN} until V_O drops 100mV from its normal value.

Typical Performance Characteristics

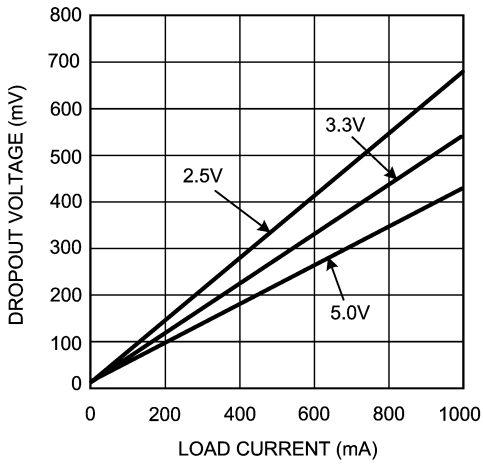
Unless otherwise specified, $V_{IN} = V_O + 1.5V$, $C_{IN} = C_{OUT} = 10\mu F$ X7R ceramic, $T_J = 25^\circ C$

Output Voltage Change vs. Temperature



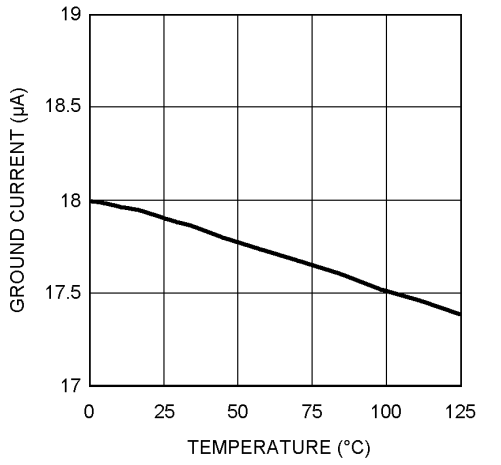
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Dropout Voltage vs. Load Current



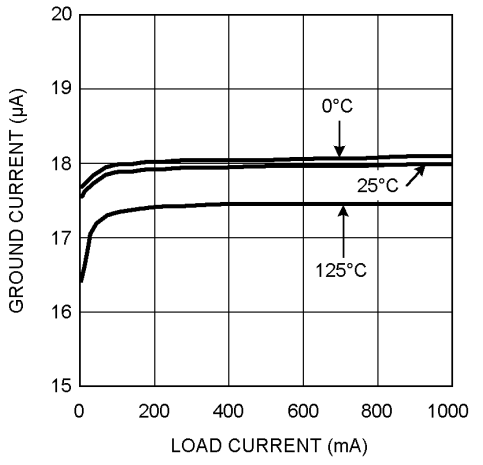
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Ground Current vs. Temperature (I_{LOAD} = 1A)



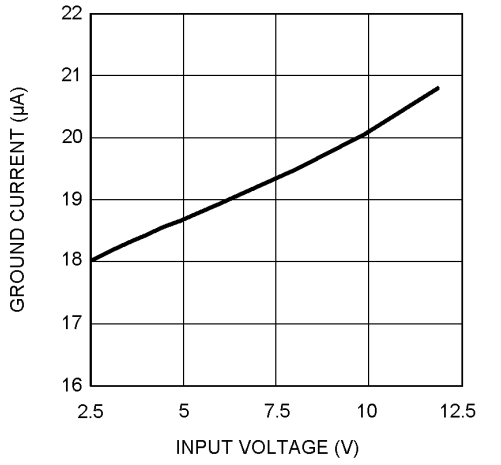
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Ground Current vs. Load Current



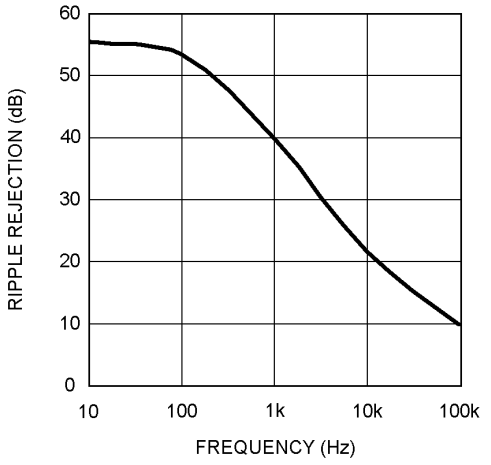
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Ground Current vs. Input Voltage



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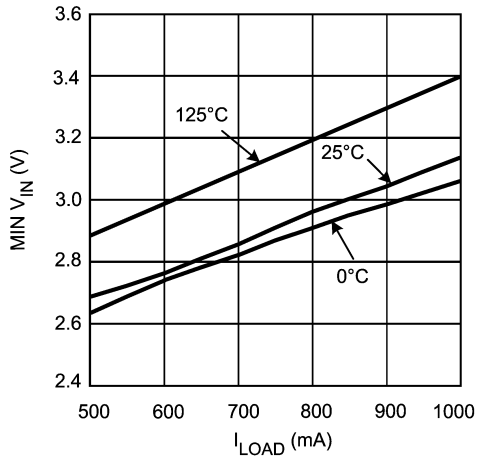
Ripple Rejection Ratio vs. Frequency



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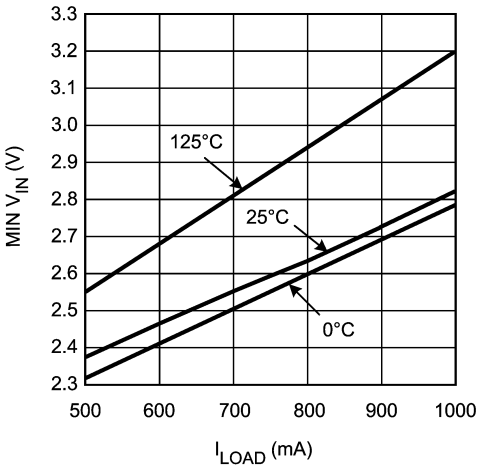
Typical Performance Characteristics (Continued)

LP8340-1.8V Min V_{IN}



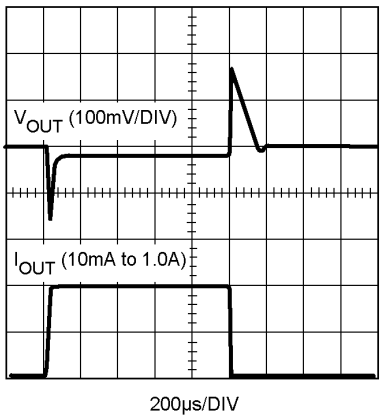
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LP8340-ADJ Min V_{IN}



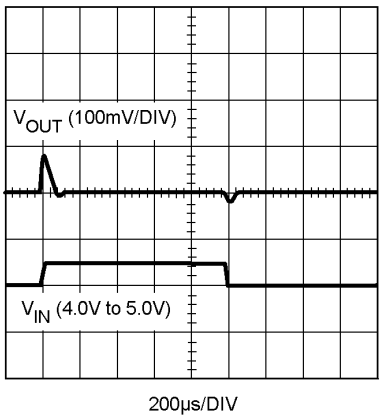
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Load Transient Response



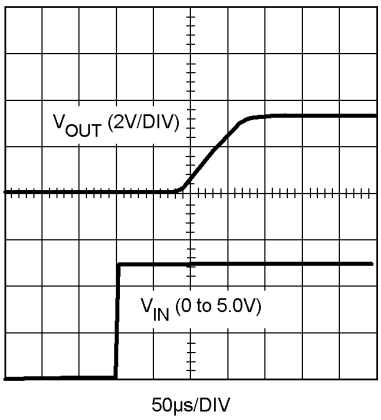
20060913

Line Transient Response (I_{LOAD} = 10mA)



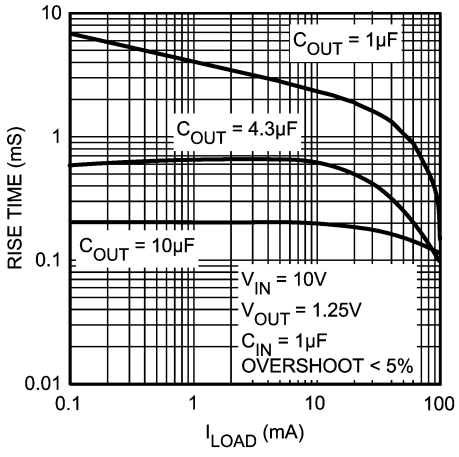
20060914

Start-up Response



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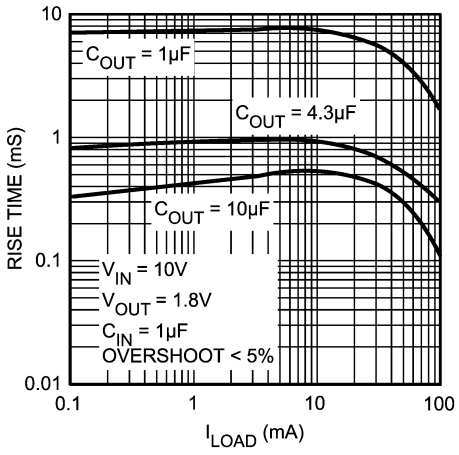
Minimum Input Voltage Rise Time



20060921

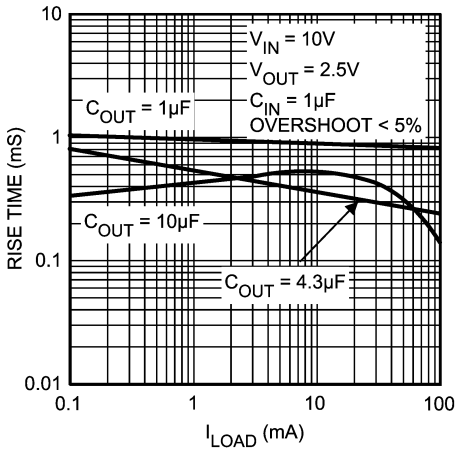
Typical Performance Characteristics (Continued)

Minimum Input Voltage Rise Time



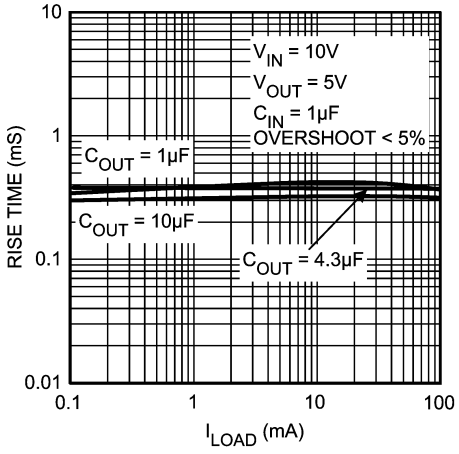
20060922

Minimum Input Voltage Rise Time



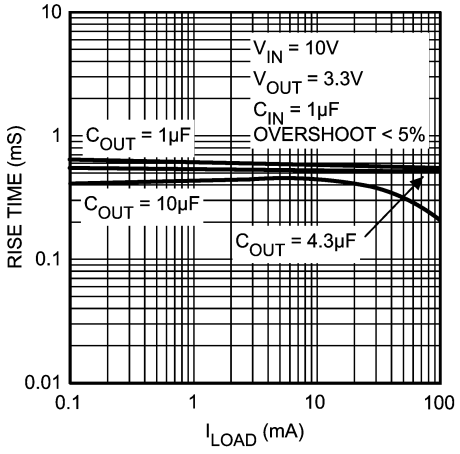
20060923

Minimum Input Voltage Rise Time



20060924

Minimum Input Voltage Rise Time



20060925

Applications Section

GENERAL INFORMATION

The LP8340 is a low-dropout, low quiescent current linear regulator. As shown in *Figure 1* it consists of a 1.25V reference, error amplifier, MOSFET driver, PMOS pass transistor and for the fixed output versions, an internal feedback network (R_1/R_2). In addition, the device is protected from overload by a thermal shutdown circuit and a foldback current limit circuit

The 1.25V reference is connected to the inverting input of the error amplifier. Regulation of the output voltage is achieved by means of negative feedback to the non-inverting input of the error amplifier. Feedback resistors R_1 and R_2 are either internal or external to the device, depending on whether it is a fixed voltage version or the adjustable version. The negative feedback and high open loop gain of the error amplifier cause the two inputs of the error amp to be virtually equal in voltage. If the output voltage changes due to load changes, the error amplifier and MOSFET driver provide the appropriate drive to the pass transistor to maintain the error amplifier's inputs as virtually equal.

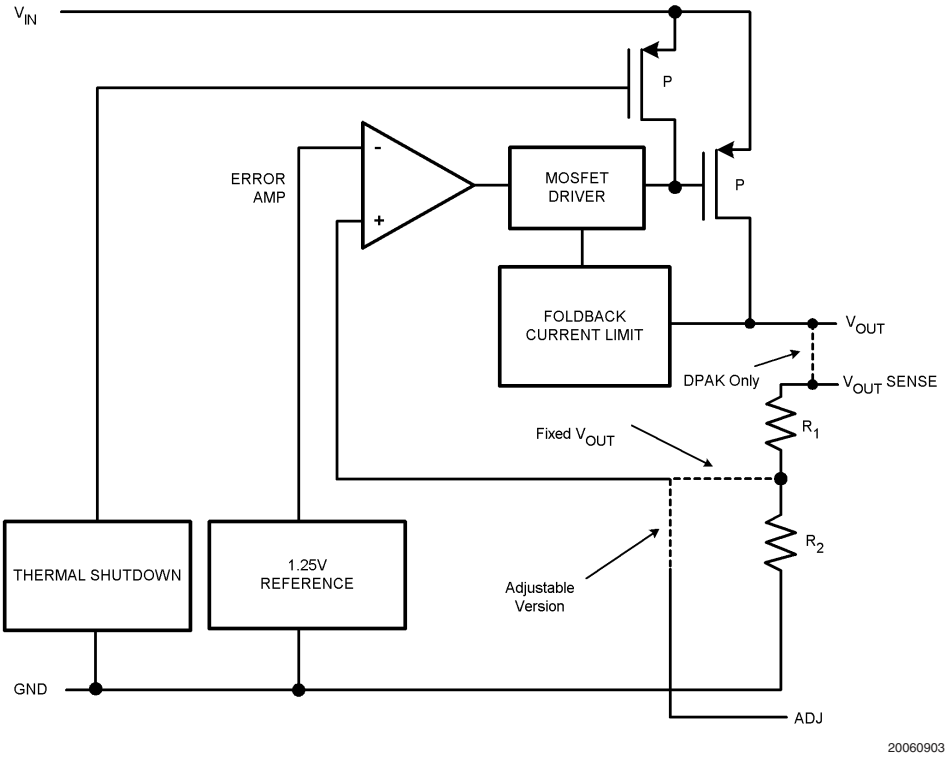


FIGURE 1. LP8340 Functional Block Diagram

EXTERNAL CAPACITOR

An Input capacitor of 1µF or greater is required between the LP8340 V_{IN} pin and ground. While 1µF will provide adequate bypassing of the V_{IN} supply larger values of input capacitor (i.e. 10µF) can provide improved bypassing of power supply noise.

Stable operation can be achieved with an output capacitor of 1µF or greater, either ceramic X7R dielectric or aluminum/tantalum electrolytic. While the minimum capacitor value is 1µF, the typical output capacitor values selected range from 1µF to 10µF. The larger values provide improved load-transient response, power supply rejection and stability.

OUTPUT VOLTAGE SETTING (ADJ VERSION ONLY)

The output voltage is set according to the amount of negative feedback (Note that the pass transistor inverts the feedback signal). This feedback is determined by R_1 and R_2 with the resulting output voltage represented by the following equation:

$$V_O = V_{REF}\left[\frac{R_1}{R_2} + 1\right]$$

Use the following equation to determine the values of R_1 and R_2 for a desired V_{OUT} (R_2 = 100Ω is recommended).

$$R_1 = R_2\left[\frac{V_O}{1.25V} - 1\right]$$

MINIMUM LOAD CURRENT

A minimum load of 100µA is required for regulation and stability over the entire operating temperature range. If actual load current fall below 100µA it is recommended that a resistor of value $R_L = V_O/100\mu A$ be placed between V_O and ground.

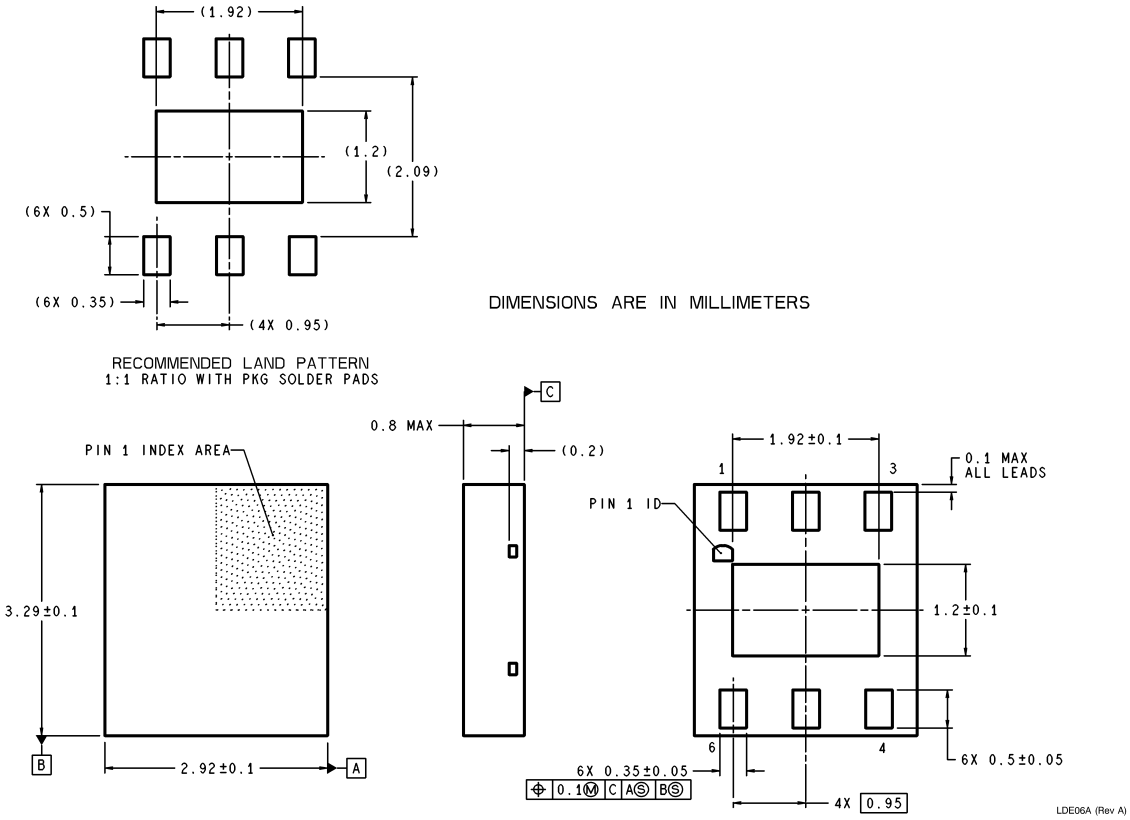
Applications Section (Continued)

START UP CONSIDERATIONS

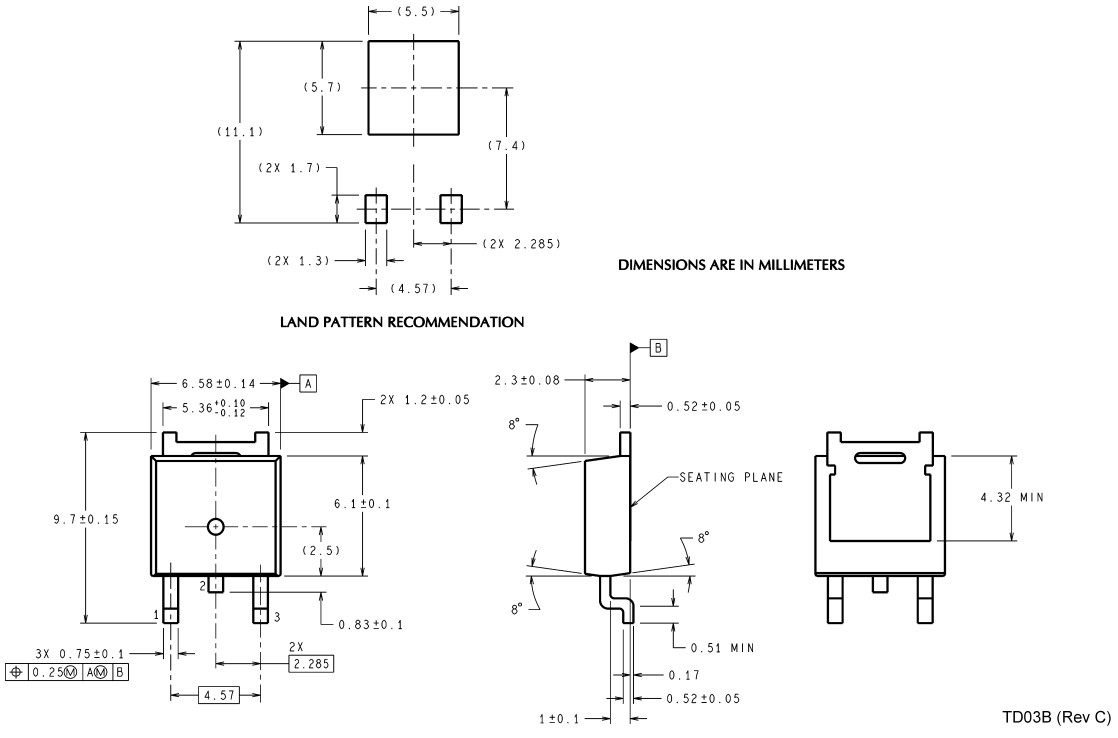
Under certain operating conditions, overshoot of V_{OUT} at start-up can occur. The observed overshoot is a function of rise time of V_{IN} waveform, C_{OUT}, start-up load current, and $V_{IN}-V_{OUT}$ differential. The relationship between these conditions is shown in the Typical Performance Characteristics curves (Minimum Input Voltage Rise Time). V_{IN} rise times above the curve result in <5% overshoot.

Customers are encouraged to check the suitability of LP8340 in their specific application.

Physical Dimensions inches (millimeters) unless otherwise noted



6-Pin LLP
NS Package Number LDE06A



3-Pin DPAK
NS Package Number TD03B

Notes

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