LP55281 12-Channel RGB/White-LED Drive With SPI, I²C Interface

1 Features

- Audio Synchronization for a Single Fun-Light LED
- Four PWM Controlled RGB LED Drivers
- High-Efficiency Boost DC-DC Converter
- SPI or I²C-Compatible Interface
- Two Addresses in I²C-Compatible Interface
- LED Connectivity Test Through the Serial Interface

2 Applications

- Cellular Phones
- PDAs, MP3 Players

3 Description

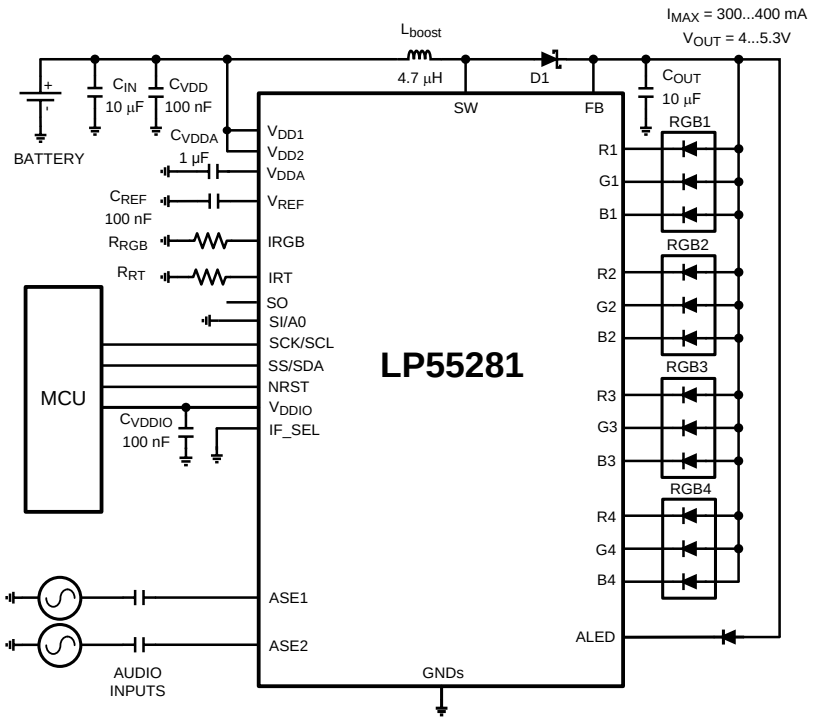
The LP55281 device is a quadruple RGB LED driver for handheld devices. It can drive 4 RGB LED sets and a single fun-light LED. The boost DC-DC converter drives high current loads with high efficiency. The RGB driver can drive individual color LEDs or RGB LEDs powered from boost output or external supply. Built-in audio synchronization feature allows user to synchronize the fun-light LED to audio inputs. The flexible SPI or I²C interface allows easy control of LP55281. A small YZR0036 or YPG0036 package, together with minimum number of external components, is a best fit for handheld devices. The LP55281 also has an LED test feature, which can be used, for example, in production for checking the LED connections.

Device Information(1)

PART NUMBER	PACKAGE	BODY SIZE (NOM)
LP55281	DSBGA (36)	2.982 mm × 2.982 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.

Typical Application



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4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision C (March 2013) to Revision D **Page**

- Added *Device Information* and *Pin Configuration and Functions* sections, *ESD Ratings* and *Thermal Information* tables, *Feature Description*, *Device Functional Modes*, *Application and Implementation*, *Power Supply Recommendations*, *Layout*, *Device and Documentation Support*, and *Mechanical, Packaging, and Orderable Information* sections; update title ... 1
- Added NRST pin connection to MCU on *Simplified Schematic* ... 1
- Changed $R_{\theta JA}$ for YPG package from "60°C/W" to "48.9°C/W"and for YZR package from "60°C/W" to "49.1°C/W" ... 6

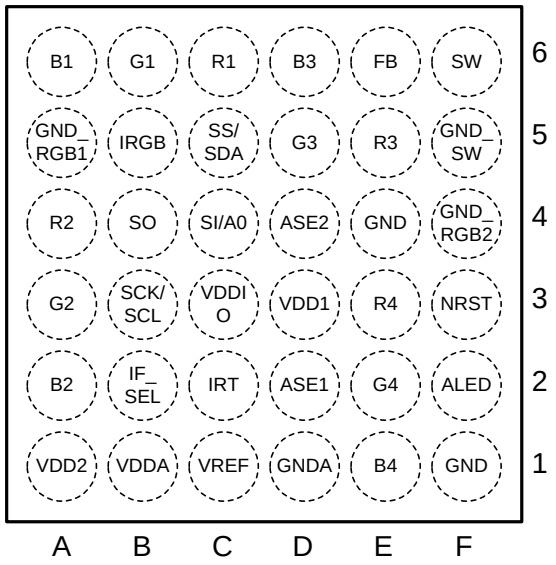
Changes from Revision B (March 2013) to Revision C **Page**

- Changed layout of National Semiconductor data sheet to TI format ... 1

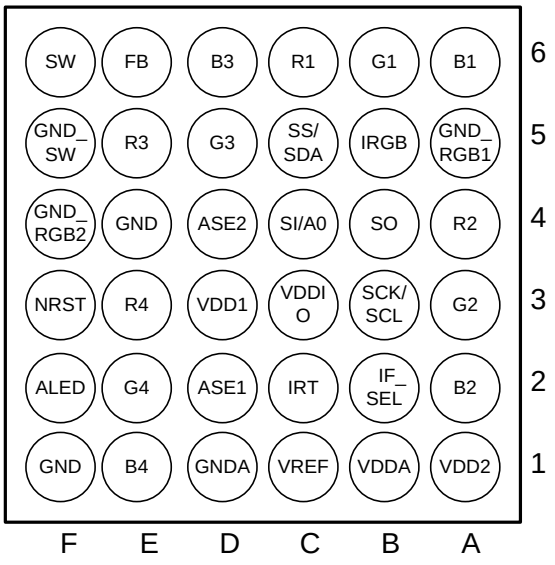
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5 Pin Configuration and Functions

YPG and YZR Packages
36-Pin DSBGA
Top View



YPG and YZR Packages
36-Pin DSBGA
Bottom View



Pin Functions

PIN		TYPE	DESCRIPTION
NUMBER	NAME		
1A	VDD2	Power	Supply voltage
1B	VDDA	Power	Internal LDO output
1C	VREF	Output	Reference voltage
1D	GNDA	Ground	Ground for analog circuitry
1E	B4	Output	Blue LED 4 output
1F	GND	Ground	Ground
2A	B2	Output	Blue LED 2 output
2B	IF_SEL	Logic Input	Interface (SPI or I^2C compatible) selection (IF_SEL = 1 for SPI)
2C	IRT	Input	Oscillator frequency resistor
2D	ASE1	Input	Audio synchronization input 1
2E	G4	Output	Green LED 4 output
2F	ALED	Output	Audio Synchronized LED oautput
3A	G2	Output	Green LED 2 output
3B	SCK/SCL	Logic Input	Clock (SPI/I^2C)
3C	VDDIO	Power	Supply voltage for input/output buffers and drivers
3D	VDD1	Power	Supply voltage
3E	R4	Output	Red LED 4 output
3F	NRST	Input	Asynchronous reset, active low
4A	R2	Output	Red LED 2 output
4B	SO	Logic Output	Serial data out (SPI)
4C	SI/A0	Logic Input	Serial input (SPI), address select (I^2C)
4D	ASE2	Input	Audio synchronization input 2
4E	GND	Ground	Ground
4F	GND_RGB2	Ground	Ground for RGB3-4 currents
5A	GND_RGB1	Ground	Ground for RGB1-2 currents

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Pin Functions (continued)

PIN		TYPE	DESCRIPTION
NUMBER	NAME		
5B	IRGB	Input	Bias current set resistor for RGB drivers
5C	SS/SDA	Logic Input/Output	Slave select (SPI), Serial data in/out (I^2C)
5D	G3	Output	Green LED 3 output
5E	R3	Output	Red LED 3 output
5F	GND_SW	Ground	Power switch ground
6A	B1	Output	Blue LED 1 output
6B	G1	Output	Green LED 1 output
6C	R1	Output	Red LED 1 output
6D	B3	Output	Blue LED 3 output
6E	FB	Input	Boost converter feedback
6F	SW	Output	Boost converter power switch

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6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)(2)(3)

	MIN	MAX	UNIT
V (SW, FB, R1-4, G1-4, B1-4, ALED)(4) (5)	–0.3	7.2	V
V_{VDD1}, V_{VDD2}, V_{VDDIO}, V_{VDDA}	–0.3	6	V
Voltage on ASE1-2, IRT, IRGB, VREF	–0.3 to V_{VDD1} + 0.3 V with 6 V maximum		
Voltage on logic pins	–0.3 to V_{VDDIO} + 0.3 V with 6 V maximum		
V (all other pins): voltage to GND	–0.3	6	
I (VREF)		10	µA
I (R1-4, G1-4, B1-4)		100	mA
Continuous power dissipation(6)	Internally limited		
Junction temperature, T_{J-MAX}		150	°C
Storage temperature, T_{stg}	–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltages are with respect to the potential at the GND pins.
(3) If Military/Aerospace specified devices are required, contact the Texas Instruments Sales Office/ Distributors for availability and specifications.
(4) Battery/Charger voltage must be above 6 V, and no more than 10% of the operational lifetime.
(5) Voltage tolerance of LP55281 above 6 V relies on fact that V_{VDD1} and V_{VDD2} (2.8 V) are available (ON) at all conditions. If V_{VDD1} and V_{VDD2} are not available (ON) at all conditions, Texas Instruments does not ensure any parameters or reliability for this device.
(6) Internal thermal shutdown circuitry protects the device from permanent damage. Thermal shutdown engages at T_J = 160°C (typical) and disengages at T_J = 140°C (typical)

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	±2000	V

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process..

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)(1)(2)

	MIN	NOM	MAX	UNIT
V (SW, FB, R1-4, G1-4, B1-4, ALED)	0		6	V
$V_{VDD1,2}$ with external LDO	2.7		5.5	V
$V_{VDD1,2}$ with internal LDO	3		5.5	V
V_{DDA}	2.7		2.9	V
V_{VDDIO}	1.65		V_{VDD1}	
Voltage on ASE1-2	0.1 V to VVDDA – 0.1 V			
Recommended load current	0		300	mA
Junction temperature, T_J	–30		125	°C
Ambient temperature, T_A (2)	–30		85	°C

(1) All voltages are with respect to the potential at the GND pins.
(2) In applications where high power dissipation and/or poor package thermal resistance is present, the maximum ambient temperature may have to be derated. Maximum ambient temperature (T_{A-MAX}) is dependent on the maximum operating junction temperature ($T_{J-MAX-OP}$ = 125°C), the maximum power dissipation of the device in the application (P_{D-MAX}), and the junction-to-ambient thermal resistance of the part/package in the application ($R_{\theta JA}$), as given by the following equation: $T_{A-MAX} = T_{J-MAX-OP} – (R_{\theta JA} \times P_{D-MAX})$.

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6.4 Thermal Information

THERMAL METRIC[1]		LP55281		UNIT
		YPG (DSGBA)	YZR (DSGBA)	
		36 PINS	36 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	48.9	49.1	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	0.2	0.2	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	10.6	10.8	°C/W
ψ_{JT}	Junction-to-top characterization parameter	0.1	0.1	°C/W
ψ_{JB}	Junction-to-board characterization parameter	10.4	10.6	°C/W

(1) For more information about traditional and new thermal metrics, see *Semiconductor and IC Package Thermal Metrics*.

6.5 Electrical Characteristics

Unless otherwise noted, specifications apply to *Functional Block Diagram* with: $V_{VDD1} = V_{VDD2} = 3.6$ V, $V_{VDDIO} = 2.8$ V, $C_{VDD} = C_{VDDIO} = 100$ nF, $C_{OUT} = C_{IN} = 10$ µF, $C_{VDDA} = 1$ µF, $C_{REF} = 100$ nF, L1 = 4.7 µH, $R_{RGB} = 8.2$ kΩ and $R_{RT} = 82$ kΩ, and limits are for $T_J = 25°C$.[1][2][3].

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
I_{VDD}	Standby supply current (V_{DD1} + V_{DD2} + leakage to SW, FB, RGB1-4, ALED)	NSTBY = L SCK = SS = SI = H NRST = L		1		µA
		NSTBY = L SCK = SS = SI = H NRST = L –30°C < T_A < 85°C			10	
	No-boost supply current (V_{DD1} + V_{DD2})	NSTBY = H, EN_BOOST = L SCK = SS = SI = H Audio synchronization and LEDs OFF		350		µA
	No-load supply current (V_{DD1} + V_{DD2})	NSTBY = H, EN_BOOST = H, SCK = SS = SI = H Audio synchronization and LEDs OFF Autoload OFF		0.6		mA
	Total RGB drivers quiescent current (V_{DD1} + V_{DD2})	EN_RGBx = H		250		µA
	ALED driver current (V_{DD1} + V_{DD2})	ALED[7:0] = FFh		180		µA
		ALED[7:0] = 00h		0		µA
	Audio synchronization current (V_{DD1} + V_{DD2})	Audio synchronization ON $V_{DD1,2}$ = 2.8 V		390		µA
		Audio synchronization ON $V_{DD1,2}$ = 3.6 V		700		µA
I_{DDIO}	V_{DDIO} standby supply current	NSTBY = L SCK = SS = SI = H –30°C < T_A < 85°C			1	µA
	V_{DDIO} supply current	1 MHz SCK frequency in SPI modeC_L = 50 pF at SO pin		20		µA
V_{DDA}	Output voltage of internal LDO for analog parts	See[4]	–3%	2.8	3%	V

(1) All voltages are with respect to the potential at the GND pins.
(2) Minimum (MIN) and maximum (MAX) limits are ensured by design, test or statistical analysis. Typical (TYP) numbers are not ensured, but do represent the most likely norm.
(3) Low-ESR surface-mount ceramic capacitors (MLCCs) used in setting electrical characteristics.
(4) VDDA output is not recommended for external use.

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Electrical Characteristics (continued)

Unless otherwise noted, specifications apply to *Functional Block Diagram* with: $V_{VDD1} = V_{VDD2} = 3.6$ V, $V_{VDDIO} = 2.8$ V, $C_{VDD} = C_{VDDIO} = 100$ nF, $C_{OUT} = C_{IN} = 10$ µF, $C_{VDDA} = 1$ µF, $C_{REF} = 100$ nF, L1 = 4.7 µH, $R_{RGB} = 8.2$ kΩ and $R_{RT} = 82$ kΩ, and limits are for $T_J = 25°C$.(1)(2) (3).

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
MAGNETIC BOOST DC-DC CONVERTER ELECTRICAL CHARACTERISTICS						
I_{LOAD}	Recommended load current	3 V ≤ V_{IN} V_{OUT} = 5 V	0		300	mA
		3 V ≤ V_{IN} V_{OUT} = 4 V	0		400	mA
V_{OUT}	Output voltage accuracy (FB pin)	3 V ≤ V_{IN} ≤ V_{OUT} – 0.5 V V_{OUT} = 5 V –30°C < T_A < 85°C	–5%		5%	
	Output voltage (FB pin)	1 mA ≤ I_{LOAD} ≤ 300 mA V_{IN} > V_{OUT} + $V_{Schottky}$(5)		V_{IN} – $V_{Schottky}$		V
RDS_{ON}	Switch ON resistance	$V_{DD1,2}$ = 3 V, I_{SW} = 0.5 A		0.4		Ω
		$V_{DD1,2}$ = 3 V, I_{SW} = 0.5 A –30°C < T_A < 85°C			0.8	
f_{Boost}	PWM mode switching frequency	RT = 82 kΩ freq_sel[2:0] = 1XX		2		MHz
	Frequency accuracy	2.7 V ≤ V_{DDA} ≤ 2.9 V RT = 82 kΩ ± 1%	–7%	±3%	7%	
		2.7 V ≤ V_{DDA} ≤ 2.9 V RT = 82 kΩ ± 1% –30°C < T_A < 85°C	–10%		10%	
t_{PULSE}	Switch pulse minimum width	no load		30		ns
$t_{START-UP}$	Start-up time	Boost start-up from STANDBY(6)		10		ms
I_{SW_MAX}	SW pin current limit		700	800	900	mA
		–30°C < T_A < 85°C	550		950	
RGB DRIVER ELECTRICAL CHARACTERISTICS (R1-4, G1-4, B1-4)						
$I_{leakage}$	R1-4, G1-4, B1-4 pin leakage current	5.5 V at measured pin		0.1		µA
		5.5 V at measured pin –30°C < T_A < 85°C			1	
I_{RGB}	Maximum recommended sink current	Limited with external resistor R_{RGB} –30°C < T_A < 85°C			40	mA
	Accuracy at 15 mA	R_{RGB} = 8.2 kΩ ± 1%		±5%		
	Current mirror ratio	See(6)		1 : 100		
	RGB1-4 current mismatch	I_{RGB} = 15 mA		±5%		
f_{PWM}	RGB switching frequency	Accuracy defined by internal oscillator, frequency value selectable		f_{PWM}		
AUDIO SYNCHRONIZATION INPUT ELECTRICAL CHARACTERISTICS						
Z_{IN}	Input Impedance of ASE1, ASE2	See(6)	10	15		kΩ
A_{IN}	ASE1, ASE2 audio input level range (peak-to-peak)	Min input level needs maximum gain; Max input level for minimum gain	0		1600	mV
ALED DRIVER ELECTRICAL CHARACTERISTICS						
$I_{leakage}$	Leakage current	V_{ALED} = 5.5 V		0.03		µA
		V_{ALED} = 5.5 V –30°C < T_A < 85°C			1	
I_{ALED}	ALED current tolerance	I_{ALED} set to 13.2 mA		13.2		mA
		I_{ALED} set to 13.2 mA –30°C < T_A < 85°C	11.9		14.5	mA
			–10%		10%	

(5) When V_{IN} rises above V_{OUT} + $V_{Schottky}$, V_{OUT} starts to follow the VIN voltage rise so that $V_{OUT} = V_{IN} – V_{Schottky}$.
(6) Data ensured by design.

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Electrical Characteristics (continued)

Unless otherwise noted, specifications apply to *Functional Block Diagram* with: $V_{VDD1} = V_{VDD2} = 3.6$ V, $V_{VDDIO} = 2.8$ V, $C_{VDD} = C_{VDDIO} = 100$ nF, $C_{OUT} = C_{IN} = 10$ µF, $C_{VDDA} = 1$ µF, $C_{REF} = 100$ nF, L1 = 4.7 µH, $R_{RGB} = 8.2$ kΩ and $R_{RT} = 82$ kΩ, and limits are for $T_J = 25°C$.(1)(2) (3).

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
LOGIC INTERFACE CHARACTERISTICS						
V_{IL}	Input low level	$-30°C < T_A < 85°C$			$0.2 \times V_{DDIO}$	V
V_{IH}	Input high level	$-30°C < T_A < 85°C$	$0.8 \times V_{DDIO}$			V
I_I	Logic input current	$-30°C < T_A < 85°C$	–1		1	µA
$f_{SCK/SCL}$	Clock frequency	I^2C, $-30°C < T_A < 85°C$			400	kHz
		$-30°C < T_A < 85°C$ SPI mode, $V_{DDIO} > 1.8$ V			13	MHz
		$-30°C < T_A < 85°C$ SPI mode, $1.65V \le V_{DDIO} < 1.8V$			5	MHz
LOGIC INPUT NRST						
V_{IL}	Input low level	$-30°C < T_A < 85°C$			0.5	V
V_{IH}	Input high level	$-30°C < T_A < 85°C$	1.2			V
I_I	Logic input current	$-30°C < T_A < 85°C$	–1		1	µA
t_{NRST}	Reset pulse width	$-30°C < T_A < 85°C$	10			µs
LOGIC OUTPUT SO						
V_{OL}	Output low level	$I_{SO} = 3$ mA $V_{DDIO} > 1.8$ V		0.3		V
		$I_{SO} = 3$ mA $V_{DDIO} > 1.8$ V $-30°C < T_A < 85°C$			0.5	
		$I_{SO} = 2$ mA, $1.65V \le V_{DDIO} < 1.8$ V		0.3		
		$I_{SO} = 2$ mA, $1.65V \le V_{DDIO} < 1.8$ V $-30°C < T_A < 85°C$			0.5	
V_{OH}	Output high level	$I_{SO} = -3$ mA, $V_{DDIO} > 1.8$ V		$V_{DDIO} - 0.3$		V
		$I_{SO} = -3$ mA, $V_{DDIO} > 1.8$ V $-30°C < T_A < 85°C$	$V_{DDIO} - 0.5$			
		$I_{SO} = -2$ mA, $1.65V \le V_{DDIO} < 1.8$ V		$V_{DDIO} - 0.3$		
		$I_{SO} = -2$ mA, $1.65V \le V_{DDIO} < 1.8$ V $-30°C < T_A < 85°C$	$V_{DDIO} - 0.5$			
I_L	Output leakage current	$V_{SO} = 2.8$ V, $-30°C < T_A < 85°C$			1	µA
LOGIC OUTPUT SDA						
V_{OL}	Output low level	$I_{SDA} = 3$ mA		0.3		V
		$I_{SDA} = 3$ mA, $-30°C < T_A < 85°C$			0.5	

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6.6 SPI Timing Requirements

V_{DD} = V_{DDIO} = 2.8 V(1)

		MIN	MAX	UNIT
1	Cycle time	70		ns
2	Enable lead time	35		ns
3	Enable lag time	35		ns
4	Clock low time	35		ns
5	Clock high time	35		ns
6	Data setup time	20		ns
7	Data hold time	0		ns
8	Data access time		20	ns
9	Disable time		10	ns
10	Data valid		20	ns
11	Data hold time	0		ns

(1) Data ensured by design.

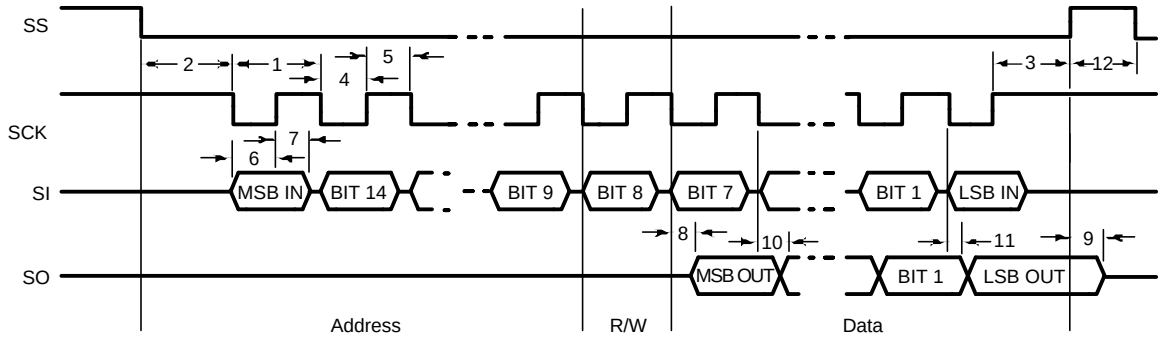


Figure 1. SPI Timing Diagram

6.7 I2C Timing Requirements

$V_{DD1,2}$ = 3 V to 4.5 V, V_{DDIO} = 1.65 V to $V_{DD1,2}$ (1)

		MIN	MAX	UNIT
1	Hold time (repeated) START condition	0.6		µs
2	Clock low time	1.3		µs
3	Clock high time	600		ns
4	Setup time for a repeated START Condition	600		ns
5	Data hold time	50		ns
6	Data setup time	100		ns
7	Rise time of SDA and SCL	20 + 0.1C_b	300	ns
8	Fall time of SDA and SCL	15 + 0.1C_b	300	ns
9	Set-up time for STOP condition	600		ns
10	Bus free time between a STOP and a START condition	1.3		µs
C_b	Capacitive load for each bus line	10	200	pF

(1) Data ensured by design.

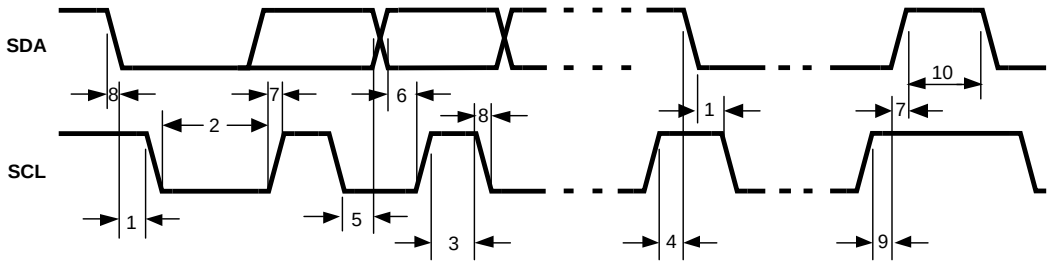


Figure 2. I2C Timing Diagram

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6.8 Boost Converter Typical Characteristics

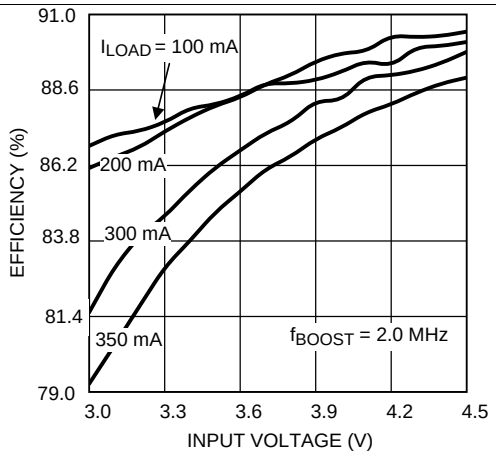


Figure 3. Boost Converter Efficiency

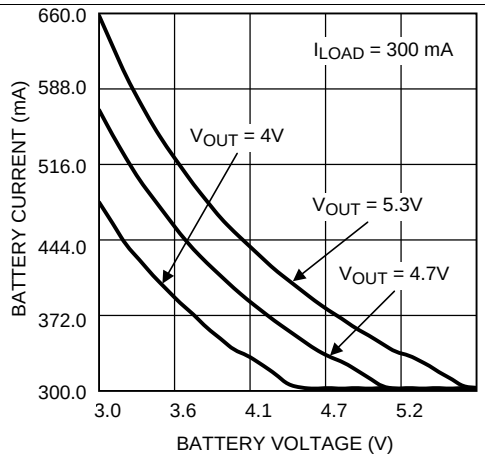


Figure 4. Battery Current vs Voltage

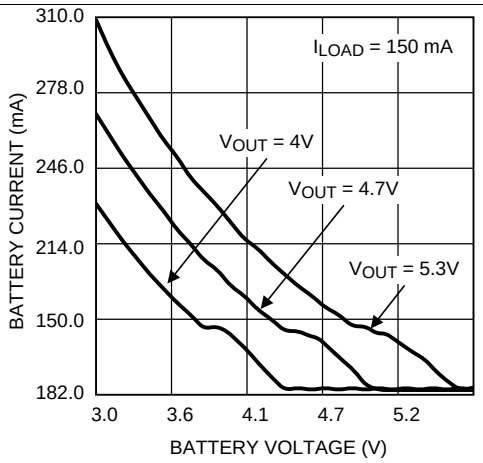


Figure 5. Battery Current vs Voltage

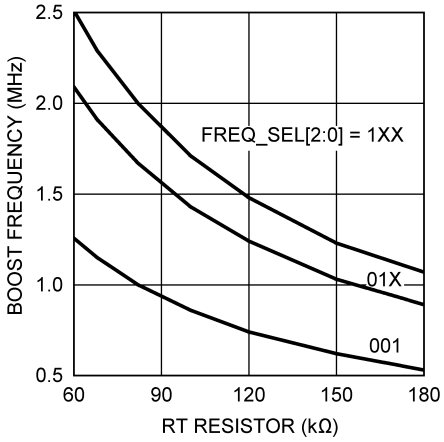


Figure 6. Boost Frequency vs RT Resistor

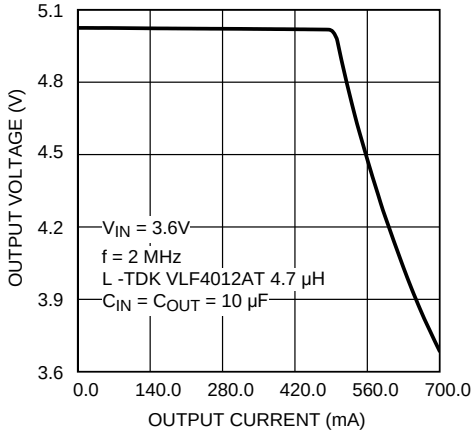


Figure 7. Output Voltage vs Load Current

6.9 RGB Driver Typical Characteristics

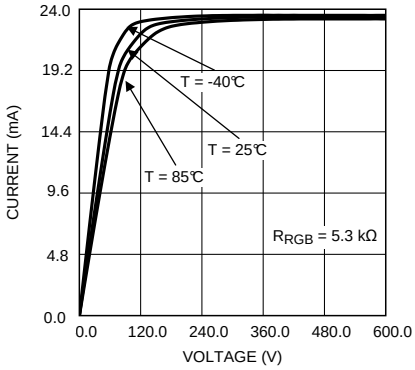


Figure 8. Output Current vs Pin Voltage (Current Sink Mode)

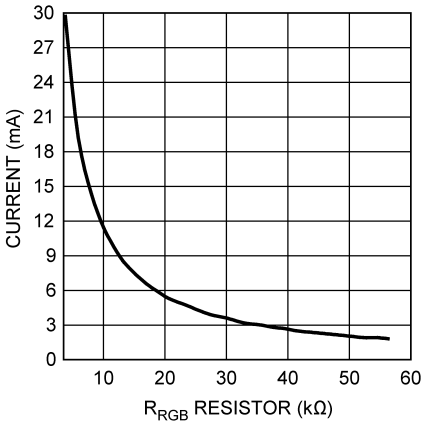


Figure 9. Output Current vs R_{RGB} (Current Sink Mode)

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7 Detailed Description

7.1 Overview

The LP55281 boost DC-DC converter generates a 4-V to 5.3-V supply voltage for the LEDs from single Li-Ion battery (3 V...4.5 V). The output voltage is controlled with an 8-bit register in 9 steps. The converter is a magnetic switching PWM mode DC-DC converter with a current limit. When timing resistor RT is 82 kΩ, the converter has three options for switching frequency: 1 MHz, 1.67 MHz, and 2 MHz (default). Timing resistor defines the internal oscillator frequency and thus directly affects boost frequency and all internally generated timing (RGB, ALED) of the circuit.

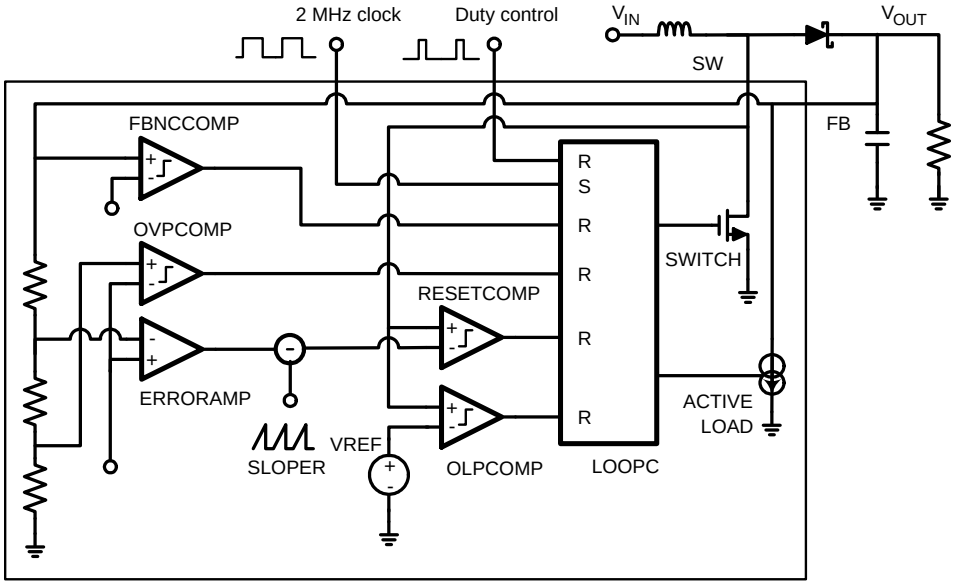
The LP55281 boost converter uses pulse-skipping elimination to stabilize the noise spectrum. Even with light load or no load a minimum length current pulse is fed to the inductor. An active load is used to remove the excess charge from the output capacitor at very light loads. At very light load and when input and output voltages are very close to each other, the pulse skipping is not completely eliminated. Output voltage must be at least 0.5 V higher than input voltage to avoid pulse skipping. Reducing the switching frequency also reduces the required voltage difference.

Active load can be disabled with the EN_AUTOLOAD bit. Disabling increases the efficiency at light loads, but the downside is that pulse skipping will occur. The boost converter must be stopped when there is no load to minimize the current consumption.

The topology of the magnetic boost converter is called current programmed mode (CPM) control, where the inductor current is measured and controlled with the feedback. The user can program the output voltage of the boost converter. The output voltage control changes the resistor divider in the feedback loop.

Figure 10 shows the boost topology with the protection circuitry. Four different protection schemes are implemented:

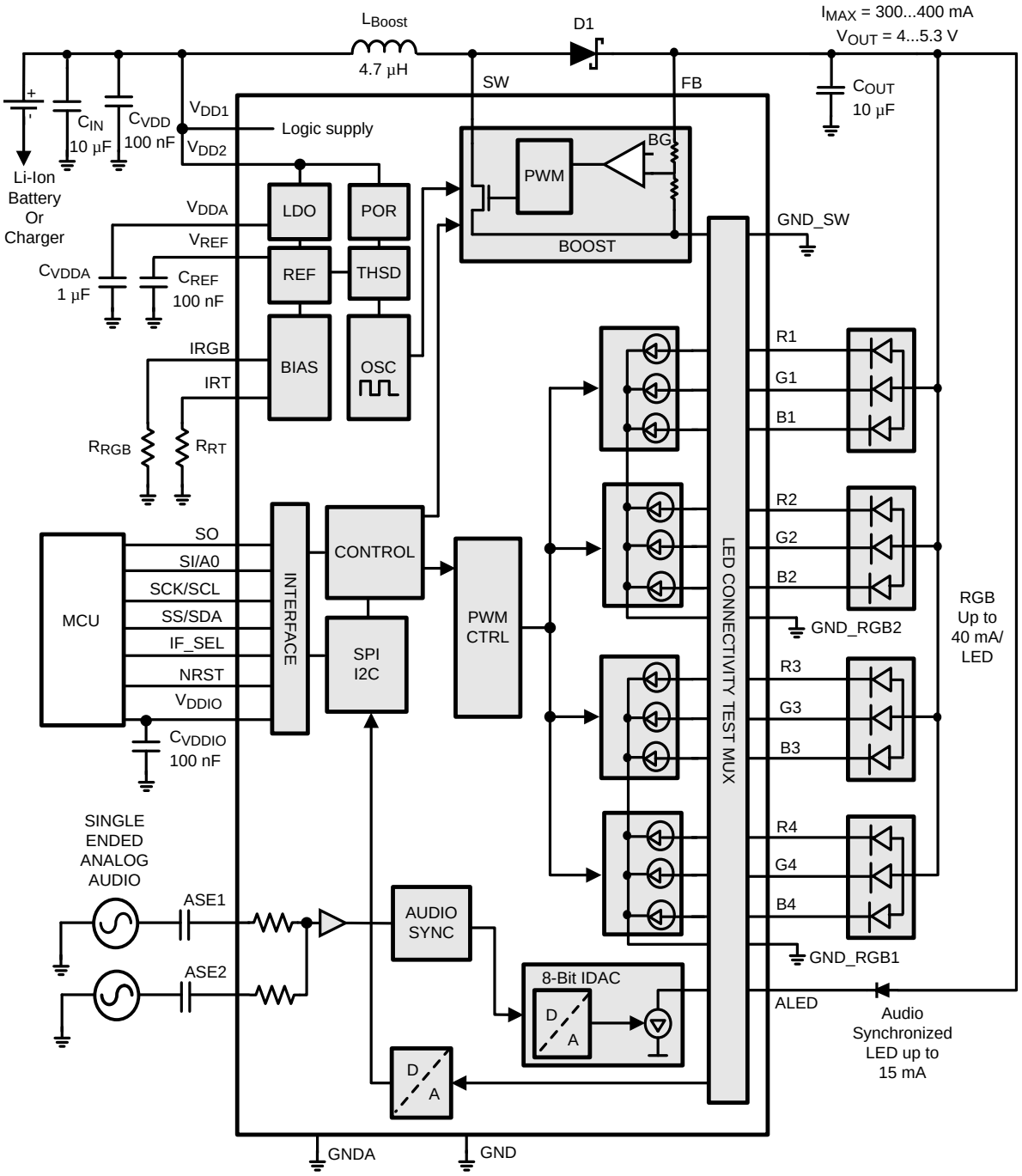
1. Overvoltage protection — limits the maximum output voltage
   - Keeps the output below breakdown voltage.
   - Prevents boost operation if battery voltage is much higher than desired output.
2. Overcurrent protection — limits the maximum inductor current
   - Voltage over switching NMOS is monitored; too high voltages turn the switch off.
3. Feedback break protection — prevents uncontrolled operation if FB pin gets disconnected.
4. Duty cycle limiting, done with digital control.



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Figure 10. Boost Converter Topology

7.2 Functional Block Diagram



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7.3 Feature Description

7.3.1 Magnetic Boost DC-DC Converter

7.3.1.1 Boost Standby Mode

User can stop the boost converter operation by writing the Enables register bit EN_BOOST low. When EN_BOOST is written high, the converter starts for 10 ms in PFM mode and then goes to PWM mode.

7.3.1.2 Boost Output Voltage Control

User can control the Boost output voltage by boost output 8-bit register.

BOOST OUTPUT [7:0] Register 0Fh		BOOST OUTPUT VOLTAGE (TYPICAL)
Bin	Hex	
0000 0000	00	4 V
0000 0001	01	4.25 V
0000 0011	03	4.4 V
0000 0111	07	4.55 V
0000 1111	0F	4.7 V
0001 1111	1F	4.85 V
0011 1111	**3F**	**5 V (default)**
0111 1111	7F	5.15 V
1111 1111	FF	5.3 V

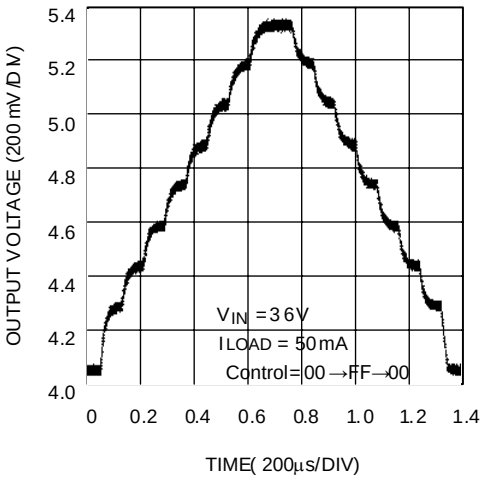


Figure 11. Boost Output Voltage Control

7.3.1.3 Boost Frequency Control

Register-frequency selections (address 10h). Register default value after reset is 07h.

FRQ_SEL[2:0]	FREQUENCY
1XX	2 MHz
01X	1.67 MHz
001	1 MHz

7.3.2 Functionality of RGB LED Outputs (R1-4, G1-4, B1-4)

The LP55281 device has 4 sets of RGB/color LED outputs. Each set has 3 outputs, which can be controlled individually with a 6-bit PWM control register. The pulsed current level for each LED output is set with a single external resistor R_{RGB} and a 2-bit coarse adjustment bit for each LED output (see Table 1 and Table 2).

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Table 1. LED Current Level Adjust

Rx_IPLS[7:6], Gx_IPLS[7:6], Bx_IPLS[7:6]	SINK CURRENT PULSE (I_{MAX} = 100 × 1.23 / R_{RGB}) – I_{PLS}
00	0.25 × I_{MAX}
01	0.50 × I_{MAX}
10	0.75 × I_{MAX}
11	1.00 × I_{MAX}

Table 2. LED PWM Control

Rx_PWM[5:0], Gx_PWM[5:0], Bx_PWM[5:0]	AVERAGE SINK CURRENT	PULSE RATIO (%)
000 000	0	0
000 001	1/63 × I_{PLS}	1.6
000 010	2/63 × I_{PLS}	3.2
...	...	...
111 110	62/63 × I_{PLS}	98.4
111 111	63/63 × I_{PLS}	100

Each RGB set must be enabled separately by setting EN_RGBx bit to 1. The device must be enabled (NSTBY = 1) before the RGB outputs can be activated.

When any of EN_RGBx bits are set to 1 and NSTBY = 1, the RGB driver takes a certain quiescent current from battery even if all PWM control bits are 0. The quiescent current is dependent on R_{RGB} resistor, and can be calculated from formula I_{R_RGB} = 1.23 V / R_{RGB}.

7.3.2.1 PWM Control Timing

PWM frequency can be selected from 3 predefined values: 10 kHz, 20 kHz, and 40 kHz. The frequency is selected with FPWM1 and FPWM0 bits, see Table 3.

Table 3. PWM Frequency

FPWM1	FPWM0	PWM FREQUENCY (f_{PWM})
0	0	9.92 kHz
0	1	19.84 kHz
1	0	39.68 kHz
1	1	39.68 kHz

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Each RGB set has equivalent internal PWM timing between R, G, and B: R has a fixed start time, G has a fixed mid-pulse time, and B has a fixed-pulse end time. PWM start time for each RGB set is different in order to minimize the instantaneous current loading due to the current sink switch on transition. See Figure 12 for details.

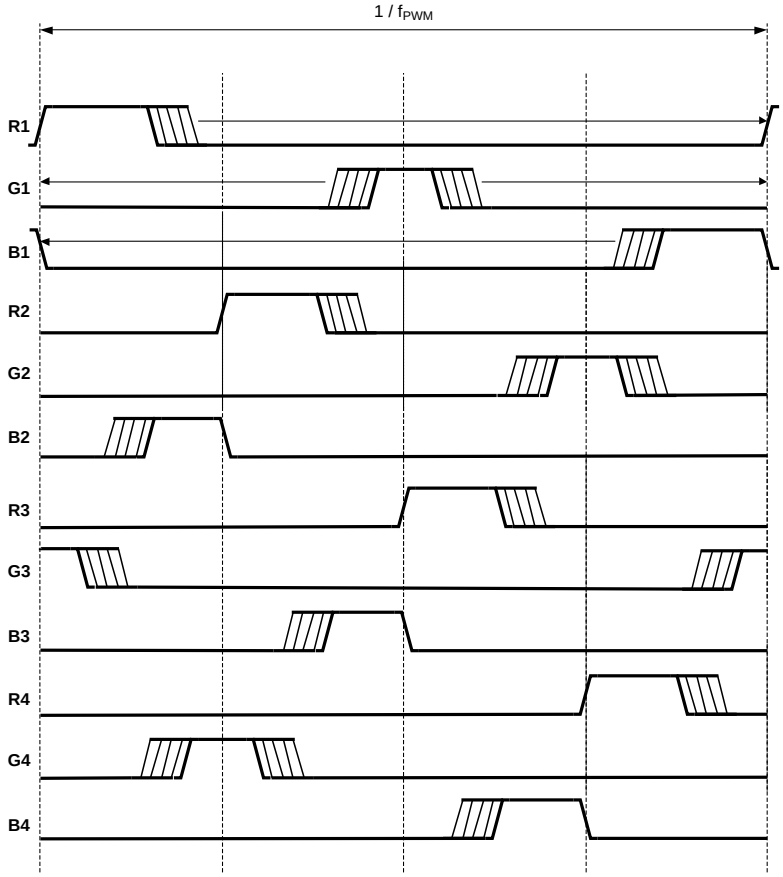


Figure 12. Timing Diagram

7.3.3 Audio Synchronization

The ALED output can be synchronized to incoming audio with an audio-synchronization feature. Audio synchronization synchronizes ALED based on the peak amplitude of the input signal. Programmable gain and automatic gain control function are also available for adjustment of input signal amplitude to light response. Control of ALED brightness refreshing frequency is done with four different frequency configurations. The digitized input signal has DC component that is removed by a digital DC-remover (–3 dB at 500 Hz). LP55281 has a 2-channel audio (stereo) input for audio synchronization, as shown in Figure 13. The inputs accept signals in the range of 0 V to 1.6 V peak-to-peak, and these signals are mixed into a single wave so that they can be filtered simultaneously.

LP55281 audio synchronization is mainly realized digitally, and it consists of the following signal path blocks (see Figure 13):

- Input buffer
- AD converter
- Automatic gain control (AGC) and manually programmable gain
- Peak detector

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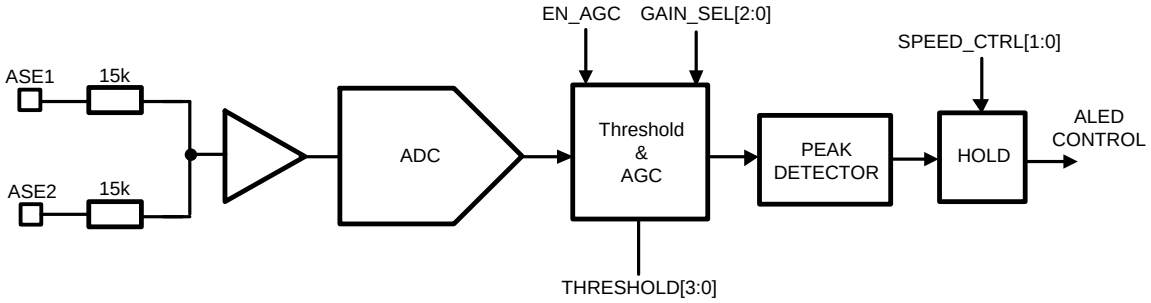


Figure 13. ALED Audio Synchronization

7.3.3.1 Control of Audio Synchronization

Table 4 describes the controls required for audio synchronization. ALED brightness control through serial interface is not available when audio synchronization is enabled.

Table 4. Audio Synchronization Control (Registers 0Dh And 0Eh)

NAME	BIT	DESCRIPTION
GAIN_SEL[2:0]	Register 0Dh Bits 7-5	Input signal gain control. Gain has a range from 0 dB to -46 dB. [000] = 0 dB, [001] = –6 dB, [010] = –12 dB, [011] = –18 dB, [100] = -24 dB, [101] = -31 dB, [110] = -37 dB, [111] = –46 dB
DC_FREQ	Register 0Dh Bit 4	Control of the high-pass filter's corner frequency: 0 = 80 Hz 1 = 510 Hz
EN_AGC	Register 0Dh Bits 3	Automatic gain control. Set EN_AGC = 1 to enable automatic control or 0 to disable. When EN_AGC is disabled, the audio input signal gain value is defined by GAIN_SEL.
EN_SYNC	Register 0Dh Bits 2	Audio synchronization enabled. Set EN_SYNC = 1 to enable audio synchronization or 0 to disable.
SPEED_CTRL[1:0]	Register 0Dh Bits 1-0	Control for refreshing frequency. Sets the typical refreshing rate for the ALED output [00] = FASTEST, [01] = 15 Hz, [10] = 7.6 Hz, [11] = 3.8 Hz
THRESHOLD[3:0]	Register 0Eh Bits 3-0	Control for the audio input threshold. Sets the typical threshold for the audio inputs signals. May be needed if there is noise on the audio lines.

Table 5. Audio Input Threshold Setting (Register 0Eh)

THRESHOLD[3:0]	THRESHOLD LEVEL (mV, typical)
0000	Disabled
0001	0.2
0010	0.4
...	...
1110	2.5
1111	2.7

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Table 6. Typical Gain Values vs Audio Input Amplitude

AUDIO INPUT AMPLITUDE mV_{P-P}	GAIN VALUE (dB)
0 to 10	0
0 to 20	–6
0 to 40	–12
1 to 85	–18
3 to 170	–24
5 to 400	–31
10 to 800	–37
20 to 1600	–46

7.3.3.2 ALED Driver

The LP55281 device has a single ALED driver. It is a constant current sink with an 8-bit control. ALED driver can be used as a DC current sink or an audio synchronized current sink. Note, that when the audio synchronization function is enabled, the 8-bit current control register has no effect.

ALED driver is enabled when audio synchronization is enabled (EN_SYNC = 1) or when ALED[7:0] control byte has other than 00h value.

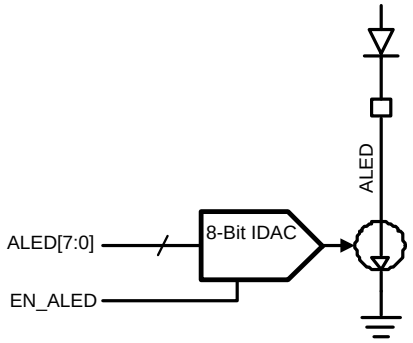


Figure 14. ALED Driver

7.3.3.2.1 Adjustment of ALED Driver

Adjustment of the ALED driver current (Register 0Ch) is described in Table 7.

Table 7. ALED Driver Current

ALED[7:0]	DRIVER CURRENT, mA (typical)
0000 0000	0
0000 0001	0.06
0000 0010	0.1
...	...
1111 1101	14.8
1111 1110	14.9
1111 1111	15

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With values other than those in Table 7, the current value can be calculated to be (15 mA / 255) × ALED[7:0], where ALED[7:0] is value in decimals.

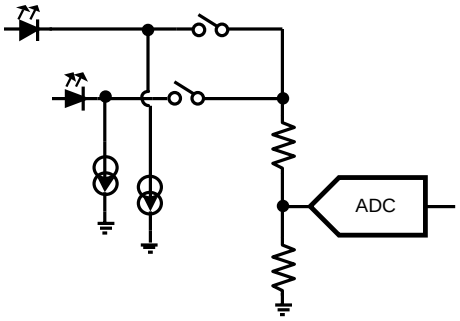


Figure 15. Principle of LED Connection to ADC

7.3.4 LED Test Interface

All LED pin voltages and boost output voltage in LP55281 can be measured and value can be read through the SPI/I^{2}C compatible interface. MUX_LED[3:0] bits in the LED test register (address 12h) are used to select one of the LED outputs or boost output for measurement. The selected output is connected to the internal ADC through a 55-kΩ resistor divider. The AD conversion is activated by setting the EN_LTEST bit to 1. The first conversion is ready after 128 µs from this. The result can be read from the ADC output register (address 13h). The device executes the AD conversions automatically once in every 128 µs period, as long as the EN_LTEST bit is 1.

User can set the preferred DC current level with the LED driver controls. The PWM of the RGB drivers must be set to 100% — otherwise random variation can appear on results. Note that the 55-kΩ resistor divider causes small additional current through the LED under measurement.

ADC result can be converted into a voltage value (of the selected pin) by multiplying the ADC result (in decimals) with 27.345 mV (value of LSB). The calculated voltage value is the voltage between the selected pin and ground. The internal LDO voltage is used as a reference voltage for the conversion. The accuracy of LDO is ± 3%, which is defining the overall accuracy. The non-linearity and offset figures are both better than 2LSB.

Table 8. LED Multiplexing (Register 12h)

MUX_LED[3:0]	CONNECTION
0000	R1
0001	G1
0010	B1
0011	R2
0100	G2
0101	B2
0110	R3
0111	G3
1000	B3
1001	R4
1010	G4
1011	B4
1100	ALED
1101	—
1110	
1111	Boost output

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7.3.4.1 LED Test Procedure

An example of LED test sequence is presented here. Note that user can use incremental write sequence on I^2C. The test sequence consists of the basic setup and measurement phases for all RGB LEDs and boost voltage.

Basic setup phase for the device:

1. Give reset to LP55281 (by power on, NRST pin or write any data to register 60h)
2. Set the preferred value for RED1 (write 3Fh, 7Fh, BFh or FFh to register 00h)
3. Set the preferred value for GREEN1 (write 3Fh, 7Fh, BFh or FFh to register 01h)
4. Set the preferred value for BLUE1 (write 3Fh, 7Fh, BFh or FFh to register 02h)
5. Set the preferred value for RED2 (write 3Fh, 7Fh, BFh or FFh to register 03h)
6. Set the preferred value for GREEN2 (write 3Fh, 7Fh, BFh or FFh to register 04h)
7. Set the preferred value for BLUE2 (write 3Fh, 7Fh, BFh or FFh to register 05h)
8. Set the preferred value for RED3 (write 3Fh, 7Fh, BFh or FFh to register 06h)
9. Set the preferred value for GREEN3 (write 3Fh, 7Fh, BFh or FFh to register 07h)
10. Set the preferred value for BLUE3 (write 3Fh, 7Fh, BFh or FFh to register 08h)
11. Set the preferred value for RED4 (write 3Fh, 7Fh, BFh or FFh to register 09h)
12. Set the preferred value for GREEN4 (write 3Fh, 7Fh, BFh or FFh to register 0Ah)
13. Set the preferred value for BLUE4 (write 3Fh, 7Fh, BFh or FFh to register 0Bh)
14. Set the preferred value for ALED (write 01h - FFh to register 0Ch)
15. Dummy write: 00h to register 0Dh (Only if the incremental write sequence is used)
16. Dummy write: 00h to register 0Eh (Only if the incremental write sequence is used)
17. Set preferred boost voltage (write 00h - FFh to register 0Fh)
18. Set preferred boost frequency (write 00h - 07h to register 10h, PWM frequency can be anything)
19. Enable boost and RGB drivers (write CFh to register 11h)
20. Wait 20 ms for the device and boost start-up

Measurement phase:

1. Enable LED test and select output (write 1xh to register 12h)
2. Wait for 128 µs
3. Read ADC output (read register 13h)
4. Go to step 1 of measurement phase and define next output to be measured as many times as needed
5. Disable LED test (write 00h to register 12h) or give reset to the device (see step 1 in basic setup phase)

7.3.4.2 LED Test Time Estimation

Assuming the maximum clock frequencies used in SPI or I^2C-compatible interfaces, Table 9 predicts the overall test sequence time for the test procedure shown above. This estimation gives the shortest time possible. Incremental write is assumed with I^2C. Reset and LED test disable are not included.

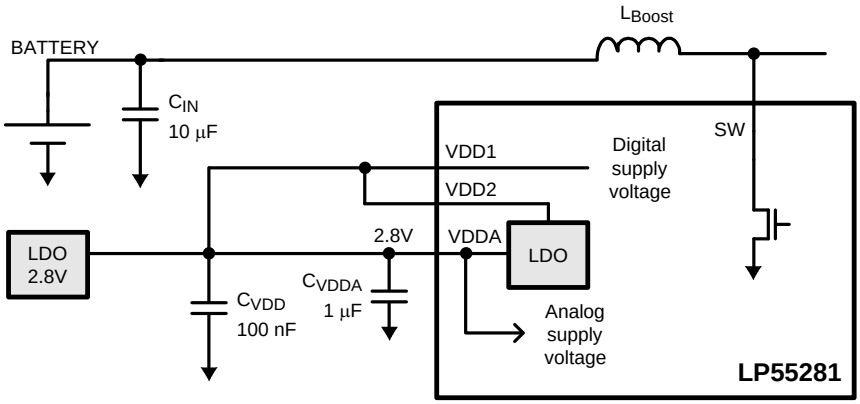
Table 9. LED Test Time

TEST PHASE	TIME (ms)	
	I2C	SPI
Setup	0.528	0.024
Boost start-up	20	20
14 measurements	4.137	1.831
Total time	24.7	21.9

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7.3.5 7-V Shielding

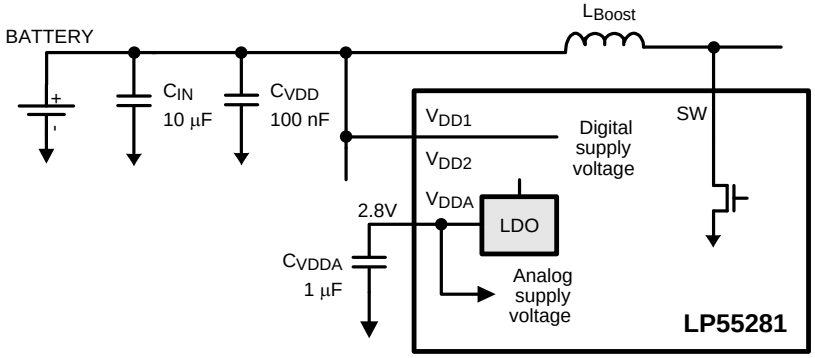
To shield the LP55281 device from high-input voltages (6 V to 7.2 V), the use of an external 2.8-V LDO is required. This 2.8-V voltage protects internally the device against high voltage condition. The recommended connection is shown in the picture below. Internally both logic and analog circuitry works at 2.8-V supply voltage. Both supply voltage pins should have separate filtering capacitors. TI recommends pulling down the external LDO voltage when it is disabled in order to minimize the leakage current of the LED outputs.



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Figure 16. LP55281 With 7-V Shielding

In cases where high voltage is not an issue, the alternative connection is shown below.



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Figure 17. LP55281 Without 7-V Shielding

7.4 Device Functional Modes

7.4.1 Modes Of Operation

RESET: In the RESET mode all the internal registers are reset to the default values and the device goes to STANDBY mode after reset. NSTBY control bit is low after reset by default. Reset is entered always if Reset Register is written, internal Power On Reset is active, or NRST pin is pulled down externally. The LP55281 can be reset by writing any data to the Reset Register (address 60H). Power On Reset (POR) will activate during the device startup or when the supply voltage V_{DD2} falls below 1.5 V. Once V_{DD2} rises above 1.5V, POR inactivates, and the device continues to the STANDBY mode.

STANDBY: The STANDBY mode is entered if the register bit NSTBY is LOW. This is the low power consumption mode, when all circuit functions are disabled. Registers can be written in this mode and the control bits are effective immediately after startup.

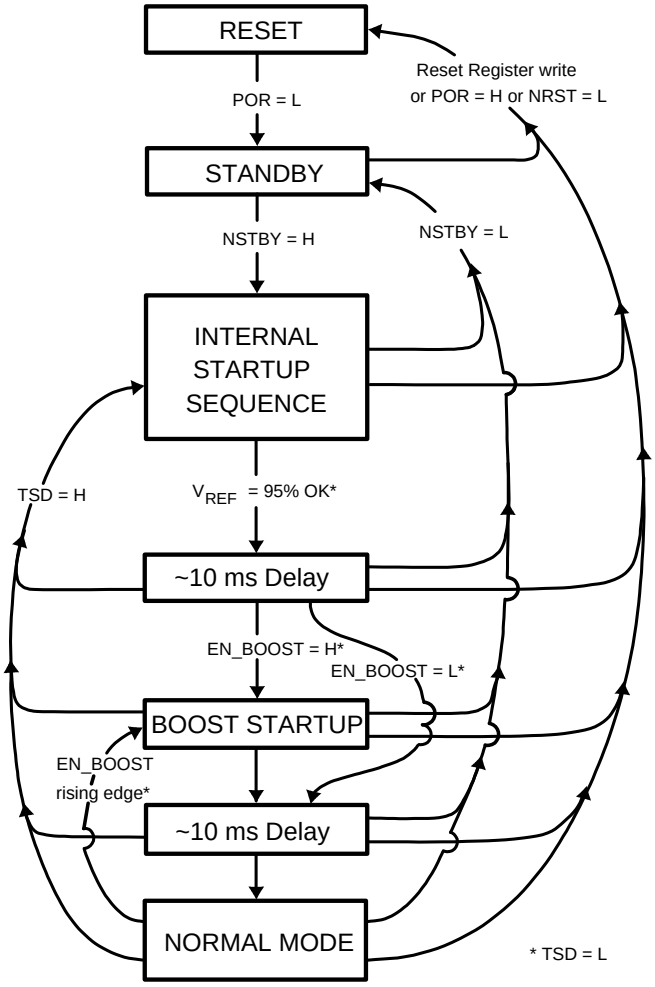
STARTUP: When NSTBY bit is written high, the INTERNAL STARTUP SEQUENCE powers up all the needed internal blocks (VREF, Oscillator, etc.). To ensure the correct oscillator initialization, a 10 ms delay is generated by the internal state-machine. If the device temperature rises too high, the Thermal Shutdown (TSD) disables the device operation and STARTUP mode is entered until no thermal shutdown is present.

BOOST STARTUP: Soft start for boost output is generated in the BOOST STARTUP mode. The boost output is raised in PWM mode during the 10 ms delay generated by the state-machine. The Boost startup is entered from Internal Startup Sequence if EN_BOOST is HIGH or from Normal mode when EN_BOOST is written HIGH. During the 10 ms Boost Startup time all LED outputs are switched off to ensure smooth startup.

NORMAL: During NORMAL mode the user controls the device using the Control Registers. The registers can be written in any sequence and any number of bits can be altered in a register in one write.

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Device Functional Modes (continued)



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7.5 Programming

The LP55281 supports two different interface modes:

- *SPI Interface* (4-wire, serial)
- *I²C Compatible Serial Bus Interface*

User can define the serial interface by IF_SEL pin. If IF_SEL = 0, I²C mode is selected.

7.5.1 SPI Interface

The LP55281 is compatible with SPI serial-bus specification and it operates as a slave. The transmission consists of 16-bit write and read cycles. One cycle consists of a 7 address bits, 1 read/write (RW) bit and 8 data bits. RW bit high state defines a write cycle and low a read cycle. SO output is normally in high-impedance state and it is active only when data is sent out during a read cycle. A pullup resistor may be needed in SO line if a floating logic signal can cause unintended current consumption in the input circuits where SO is connected. The Address and Data are transmitted MSB first. The slave select signal (SS) must be low during the cycle transmission. SS resets the interface when high and it has to be taken high between successive cycles. Data is clocked in on the rising edge of the clock signal (SCK), while data is clocked out on the falling edge of SCK.

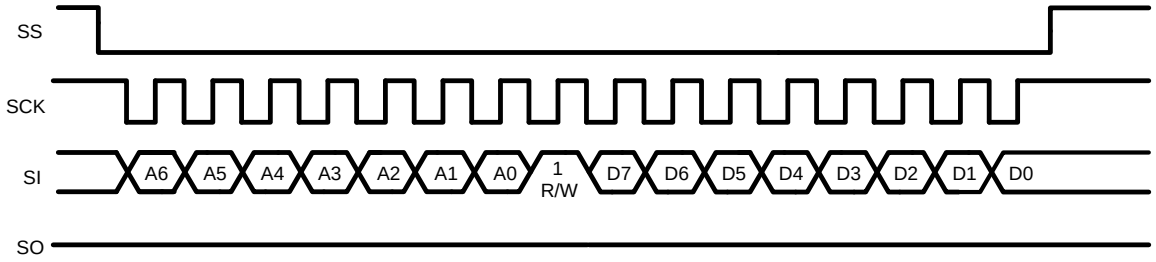


Figure 18. SPI Write Cycle

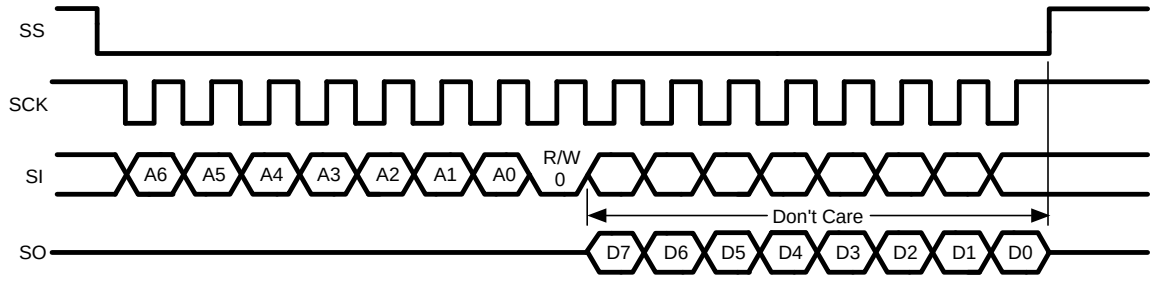


Figure 19. SPI Read Cycle

7.5.2 I²C Compatible Serial Bus Interface

7.5.2.1 Interface Bus Overview

The I²C compatible synchronous serial interface provides access to the programmable functions and registers on the device. This protocol uses a two-wire interface for bidirectional communications between the devices connected to the bus. The two interface lines are the serial data line (SDA) and the serial clock line (SCL). These lines should be connected to a positive supply, via a pullup resistor and remain HIGH even when the bus is idle.

For every device on the bus is assigned a unique address and it acts as a master or a slave, depending on whether it generates or receives the SCL. When LP55281 is connected in parallel with other I²C compatible devices, the LP55281 supply voltages V_{DD1}, V_{DD2} and V_{DDIO} must be active. Supplies are required to make sure that the LP55281 does not disturb the SDA and SCL lines.

Programming (continued)

7.5.2.2 Data Transactions

One data bit is transferred during each clock pulse. Data is sampled during the high state of the SCL. Consequently, throughout the clock's high period, the data should remain stable. Any changes on the SDA line during the high states of the SCL and in the middle of the transaction, aborts the current transaction. New data should be sent during the low SCL state. This protocol permits a single data line to transfer both command/control information and data using the synchronous serial clock.

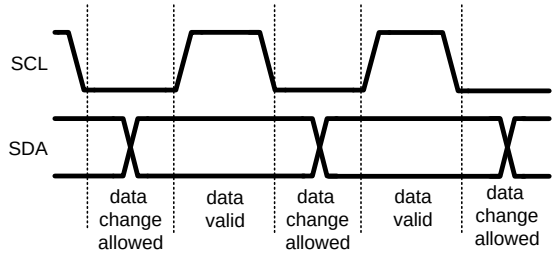


Figure 20. Data Validity

Each data transaction is composed of a start condition, a number of byte transfers (set by the software) and a stop condition to terminate the transaction. Every byte written to the SDA bus must be 8 bits long and is transferred with the most significant bit first. After each byte, an acknowledge signal must follow. The following sections provide further details of this process.

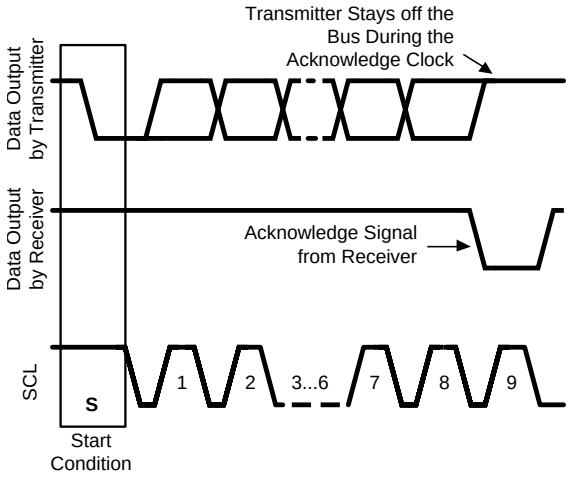


Figure 21. Acknowledge Signal

The Master device on the bus always generates the start and stop conditions (control codes). After a start condition is generated, the bus is considered busy and it retains this status until a certain time after a stop condition is generated. A high-to-low transition of the data line (SDA), while the clock (SCL) is high, indicates a Start Condition. A low-to-high transition of the SDA line, while the SCL is high, indicates a stop condition.

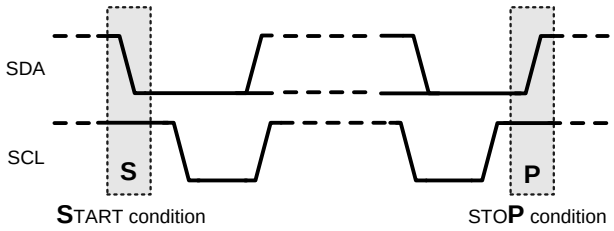


Figure 22. Start And Stop Conditions

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Programming (continued)

In addition to the first start condition, a repeated start condition can be generated in the middle of a transaction. This allows another device to be accessed or a register read cycle.

7.5.2.3 Acknowledge Cycle

The acknowledge cycle consists of two signals: the acknowledge clock pulse the master sends with each byte transferred, and the acknowledge signal sent by the receiving device.

The master generates the acknowledge clock pulse on the ninth clock pulse of the byte transfer. The transmitter releases the SDA line (permits it to go high) to allow the receiver to send the acknowledge signal. The receiver must pull down the SDA line during the acknowledge clock pulse and ensure that SDA remains low during the high period of the clock pulse, thus signaling the correct reception of the last data byte and its readiness to receive the next byte.

7.5.2.4 Acknowledge After Every Byte Rule

The master generates an acknowledge clock pulse after each byte transfer. The receiver sends an acknowledge signal after every byte received.

There is one exception to the*acknowledge after every byte* rule. When the master is the receiver, it must indicate to the transmitter an end of data by not-acknowledging (*negative acknowledge*) the last byte clocked out of the slave. This *negative acknowledge* still includes the acknowledge clock pulse (generated by the master), but the SDA line is not pulled down.

7.5.2.5 Addressing Transfer Formats

Each device on the bus has a unique slave address. The LP55281 operates as a slave device with 7-bit address. LP55281 I^2C address is pin selectable from two different choices. *The LP55281 address is 4Ch (SI/A0 = 0) or 4Dh (SI/A0 = 1) as selected with SI/A0 pin.* If eighth bit is used for programming, the 8^{th} bit is 1 for read and 0 for write.

Before any data is transmitted, the master transmits the address of the slave being addressed. The slave device should send an acknowledge signal on the SDA line, once it recognizes its address.

The slave address is the first seven bits after a start condition. The direction of the data transfer (R/W) depends on the bit sent after the slave address (the eighth bit).

When the slave address is sent, each device in the system compares this slave address with its own. If there is a match, the device considers itself addressed and sends an acknowledge signal. Depending upon the state of the R/W bit (1 for read, 0 for write), the device acts as a transmitter or a receiver.

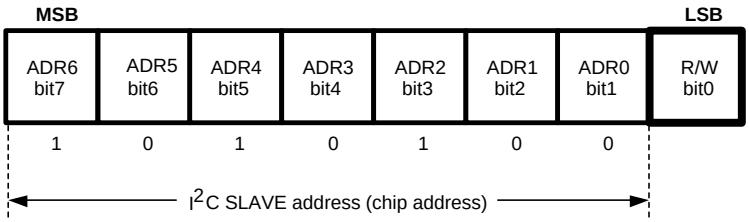


Figure 23. I^2C Device Address

Programming (continued)

7.5.2.6 Control Register Write Cycle

- Master device generates start condition
- Master device sends slave address (7 bits) and the data direction bit (r/w=0).
- Slave device sends acknowledge signal if the slave address is correct.
- Master sends control register address (8 bits).
- Slave sends acknowledge signal.
- Master sends data byte to be written to the addressed register.
- Slave sends acknowledge signal.
- If master will send further data bytes, the control register address will be incremented by one after acknowledge signal
- Write cycle ends when the master creates stop condition.

7.5.2.7 Control Register Read Cycle

- Master device generates a start condition.
- Master device sends slave address (7 bits) and the data direction bit (r/w=0).
- Slave device sends acknowledge signal if the slave address is correct.
- Master sends control register address (8 bits).
- Slave sends acknowledge signal.
- Master device generates repeated start condition.
- Master sends the slave address (7 bits) and the data direction bit (r/w=1).
- Slave sends acknowledge signal if the slave address is correct.
- Slave sends data byte from addressed register.
- If the master device sends acknowledge signal, the control register address will be incremented by one. Slave device sends data byte from addressed register.
- Read cycle ends when the master does not generate acknowledge signal after data byte and generates stop condition.

	ADDRESS MODE
Data Read	<Start Condition> <Slave Address><r/w = 0>[Ack] <Register Address>[Ack] <Repeated Start Condition> <Slave Address><r/w = 1>[Ack] [Register Data]<Ack or NAck> ...additional reads from subsequent register address possible <Stop Condition>
Data Write	<Start Condition> <Slave Address><r/w = 0>[Ack] <Register Address>[Ack] <Register Data>[Ack] ...additional writes to subsequent register address possible <Stop Condition>

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< > Data from master, [ ] data from slave

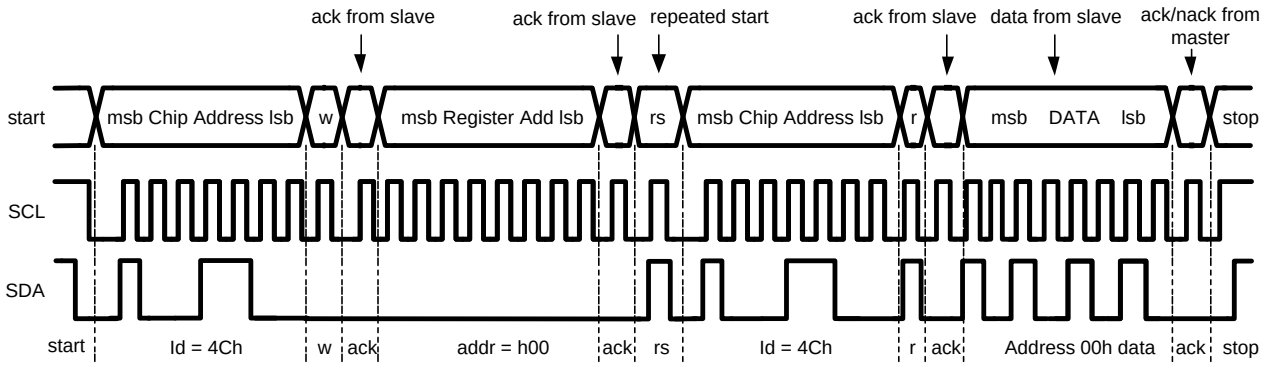


Figure 24. Register READ Format

When a READ function is to be accomplished, a WRITE function must precede the READ function, as shown in the Read Cycle waveform.

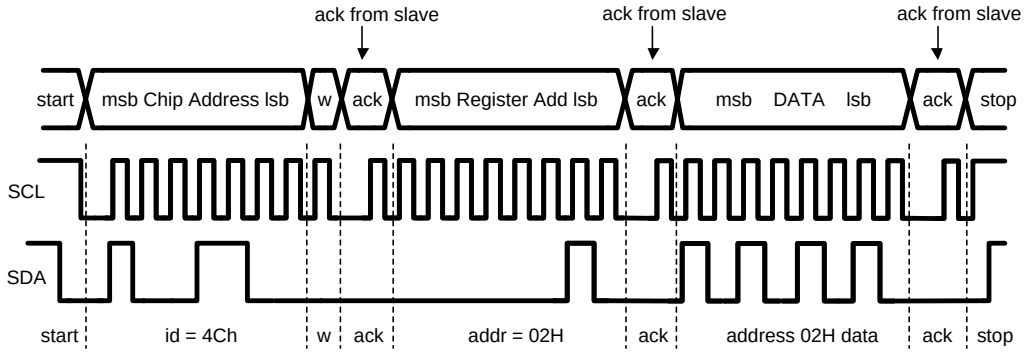


Figure 25. Register WRITE Format

- w = write (SDA = 0)
- r = read (SDA = 1)
- ack = acknowledge (SDA pulled down by either master or slave)
- rs = repeated start
- id = 7-bit device address

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7.6 Register Maps

Following table summarizes the registers and their default values

Address	Register	D7	D6	D5	D4	D3	D2	D1	D0
00h	RED1	R1 - IPLS[7:6]		R1_PWM[5:0]					
		0	0	0	0	0	0	0	0
01h	GREEN1	G1 - IPLS[7:6]		G1_PWM[5:0]					
		0	0	0	0	0	0	0	0
02h	BLUE1	B1 - IPLS[7:6]		B1_PWM[5:0]					
		0	0	0	0	0	0	0	0
03h	RED2	R2 - IPLS[7:6]		R2_PWM[5:0]					
		0	0	0	0	0	0	0	0
04h	GREEN2	G2 - IPLS[7:6]		G2_PWM[5:0]					
		0	0	0	0	0	0	0	0
05h	BLUE2	B2 - IPLS[7:6]		B2_PWM[5:0]					
		0	0	0	0	0	0	0	0
06h	RED3	R3 - IPLS[7:6]		R3_PWM[5:0]					
		0	0	0	0	0	0	0	0
07h	GREEN3	G3 - IPLS[7:6]		G3_PWM[5:0]					
		0	0	0	0	0	0	0	0
08h	BLUE3	B3 - IPLS[7:6]		B3_PWM[5:0]					
		0	0	0	0	0	0	0	0
09h	RED4	R4 - IPLS[7:6]		R4_PWM[5:0]					
		0	0	0	0	0	0	0	0
0Ah	GREEN4	G4 - IPLS[7:6]		G4_PWM[5:0]					
		0	0	0	0	0	0	0	0
0Bh	BLUE4	B4 - IPLS[7:6]		B4_PWM[5:0]					
		0	0	0	0	0	0	0	0
0Ch	ALED	ALED[7:0]							
		0	0	0	0	0	0	0	0
0Dh	Audio Sync CTRL1	GAIN_SEL[2:0]			DC_FREQ	EN_AGC	EN_SYNC	SPEED_CTRL[1:0]	
		0	0	0	0	0	0	1	1
0Eh	Audio Sync CTRL2					THRESHOLD[3:0]			
						0	0	0	0
0Fh	Boost Output	Boost[7:0]							
		0	0	1	1	1	1	1	1
10h	Frequency Selections			FPWM1	FPWM0		FRQ_SEL[2:0]		
				0	0		1	1	1
11h	Enables	NSTBY	EN_BOOST	EN_AUTOLOAD		EN_RGB4	EN_RGB3	EN_RGB2	EN_RGB1
		0	0	0		0	0	0	0
12h	LED Test				EN_LTEST	MUX_LED[3:0]			
					0	0	0	0	0
13h(1)	ADC Output	DATA[7:0]							
		0	0	0	0	0	0	0	0
		r/o	r/o	r/o	r/o	r/o	r/o	r/o	r/o
60h	Reset	Writing any data to Reset Register resets LP55281							

(1) r/o = read-only

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8 Application and Implementation

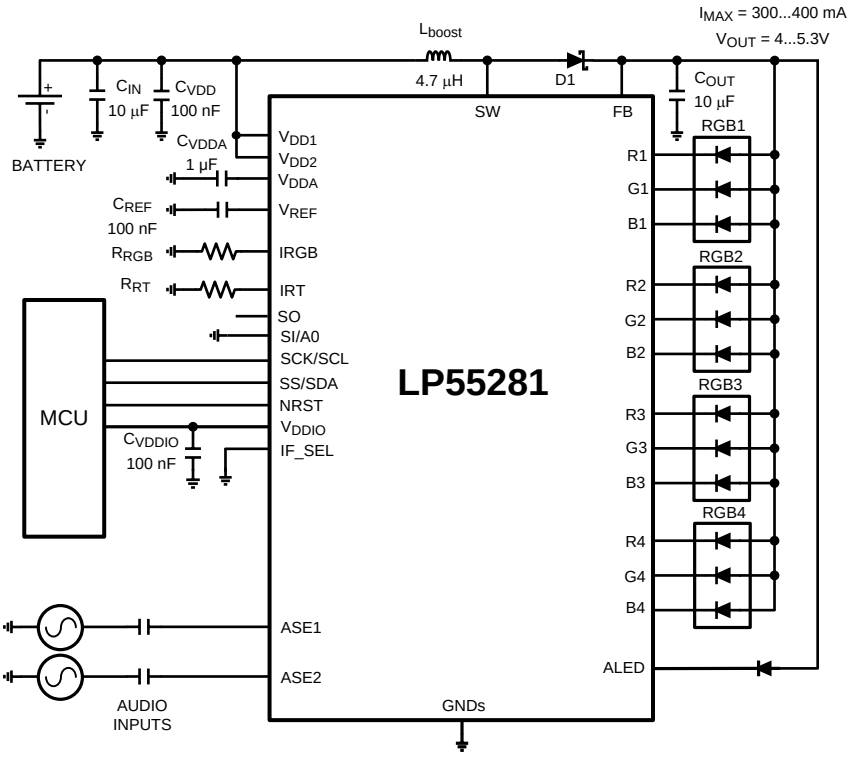
NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

8.1 Application Information

The LP55281 quadruple RGB driver with integrated boost converter provides a complete solution for driving up to 12 LEDs via either I^2C or SPI interface.

8.2 Typical Application



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Figure 26. LP55281 Typical Application

Typical Application (continued)

8.2.1 Design Requirements

For typical LED-driver applications, use the parameters listed in Table 10.

Table 10. Design Parameters

DESIGN PARAMETER	EXAMPLE VALUE
Input voltage	3 V
Output voltage	5 V
SW pin current limit	550 mA (minimum)
Efficiency	75%

8.2.2 Detailed Design Procedure

The output current can be approximated by using this formula: $I_{OUT} = (V_{IN} \times I_{SW_MAX} \times \text{efficiency}) / V_{OUT}$.

Example: 3 V × 550 mA × 0.75 / 5 V = 248 mA

8.2.2.1 Recommended External Components

8.2.2.1.1 Output Capacitor, C_{OUT}

The output capacitor C_{OUT} directly affects the magnitude of the output ripple voltage. In general, the higher the value of C_{OUT}, the lower the output ripple magnitude. Multilayer ceramic capacitors with low ESR are the best choice. At the lighter loads, the low ESR ceramics offer a much lower V_{OUT} ripple than the higher ESR tantalums of the same value. At the higher loads, the ceramics offer a slightly lower V_{OUT} ripple magnitude than the tantalums of the same value. However, the dv/dt of the V_{OUT} ripple with the ceramics is much lower than the tantalums under all load conditions. Capacitor voltage rating must be sufficient, TI recommends 10 V or greater.

Some ceramic capacitors, especially those in small packages, exhibit a strong capacitance reduction with the increased applied voltage. The capacitance value can fall to below half of the nominal capacitance. Output capacitance that is too low increase the noise, and it can make the boost converter unstable.

8.2.2.1.2 List Of Recommended External Components

PARAMETER		VALUE	UNIT	TYPE
C_{VDD1}	C between V_{DD1} and GND	100	nF	Ceramic, X7R/X5R
C_{VDD2}	C between V_{DD2} and GND	100	nF	Ceramic, X7R/X5R
C_{VDDIO}	C between V_{DDIO} and GND	100	nF	Ceramic, X7R/X5R
C_{VDDA}	C between V_{DDA} and GND	1	µF	Ceramic, X7R/X5R
C_{OUT}	C between FB and GND	10	µF	Ceramic, X7R/X5R
C_{IN}	C between battery voltage and GND	10	µF	Ceramic, X7R/X5R
L_{BOOST}	L between SW and VBAT at 2 MHz	4.7	µH	Shielded, low ESR, I_{SAT} 1A
C_{VREF}	C between VREF and GND	100	nF	Ceramic, X7R
C_{VDDIO}	C between V_{DDIO} and GND	100	nF	Ceramic, X7R
R_{RGB}	R between IRGB and GND	8.2	kΩ	±1%
R_{RT}	R between IRT and GND	82	kΩ	±1%
D_1	Rectifying Diode (V_f at maxload)	0.3	V	Schottky diode
C_{ASE}	C between Audio input and ASEx	100	nF	Ceramic, X7R/X5R
LEDs		User defined		

8.2.2.1.3 Input Capacitor, C_{IN}

The input capacitor C_{IN} directly affects the magnitude of the input ripple voltage and to a lesser degree the V_{OUT} ripple. A higher value C_{IN} gives a lower V_{IN} ripple. Capacitor voltage rating must be sufficient, TI recommends 10 V or greater.

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8.2.2.1.4 Output Diode, D_1

A Schottky diode must be used for the output diode. To maintain high efficiency the average current rating of the Schottky diode must be larger than the peak inductor current (1 A). Schottky diodes with a low forward drop and fast switching speeds are ideal for increasing efficiency in portable applications. Choose a reverse breakdown of the Schottky diode larger than the output voltage. Do not use ordinary rectifier diodes, since slow switching speeds and long recovery times cause the efficiency and the load regulation to suffer.

8.2.2.1.5 Inductor, L

The high switching frequency of the LP55281 device enables the use of the small surface mount inductor. A 4.7-µH shielded inductor is suggested for 2-MHz operation, use 10 µH at 1 MHz. The inductor should have a saturation current rating higher than the peak current it will experience during circuit operation (approximately 1 A). Less than 300-mΩ ESR is suggested for high efficiency. Open core inductors cause flux linkage with circuit components and interfere with the normal operation of the circuit. This should be avoided. For high efficiency, choose an inductor with a high frequency core material such as ferrite to reduce the core losses. To minimize radiated noise, use a toroid, pot core or shielded core inductor. TI recommends inductors LPS3015 and LPS4012 from Coilcraft and VLF4012 from TDK.

8.2.3 Application Curves

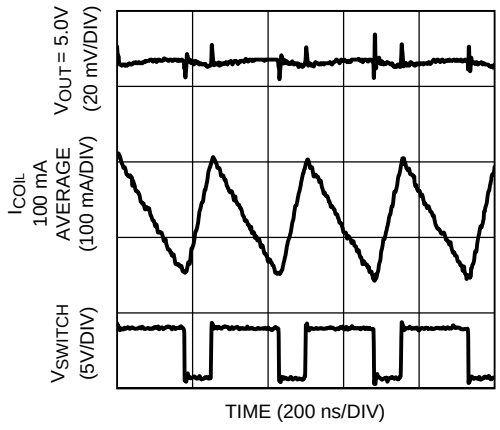


Figure 27. Boost Typical Waveforms With 100 mA Load

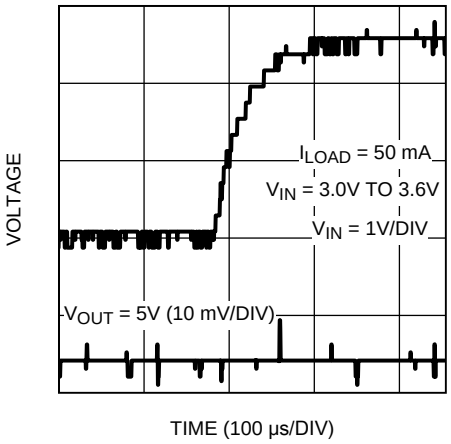


Figure 28. Boost Line Regulation

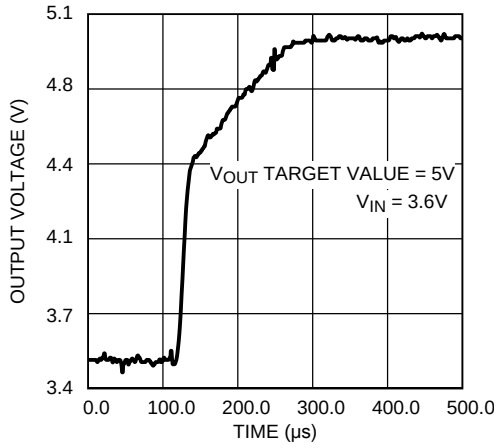
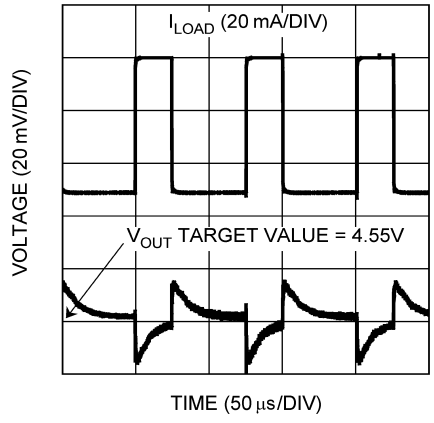


Figure 29. Boost Start-up With No Load



50 - 100 mA

Figure 30. Boost Load Regulation

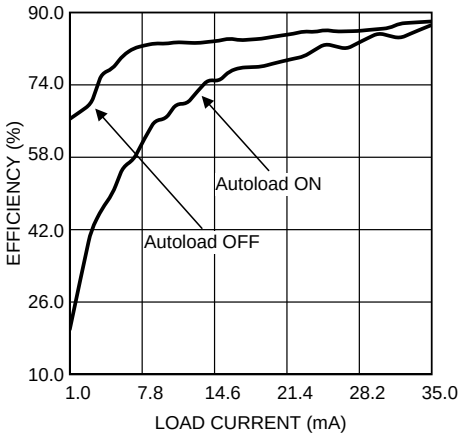


Figure 31. Efficiency at Low Load vs Autoload

8.3 Initialization Set Up Example

The following table gives an example initialization sequence to illustrate the various LED and Boost configuration options. Not every feature of the LP55281 is configured in this example.

Table 11. Initialization Example

ADDRESS	DATA	REGISTER	COMMENT
60h	00h	RESET	Execute software reset to initialize LP55281
00h	3Fh	RED 1	IPLS = 0 (25% IRGB), PWM = 100%
01h	5Fh	GREEN1	IPLS = 1 (50% IRGB), PWM = 50%
02h	90h	BLUE1	IPLS = 2 (75% IRGB), PWM = 25.4%
03h	C8h	RED 2	IPLS = 3 (100% IRGB), PWM = 12.7%
04h	1Fh	GREEN2	IPLS = 0 (25% IRGB), PWM = 50%
05h	10h	BLUE2	IPLS = 0 (25% IRGB), PWM = 25.4%
06h	07h	RED 3	IPLS = 0 (25% IRGB), PWM = 11.1%
07h	03h	GREEN3	IPLS = 0 (25% IRGB), PWM = 4.8%
08h	01h	BLUE3	IPLS = 0 (25% IRGB), PWM = 1.6%
09h	0h	RED 4	IPLS = 0 (25% IRGB), PWM = 0%
0Ah	0h	GREEN4	IPLS = 0 (25% IRGB), PWM = 0%
0Bh	0h	BLUE4	IPLS = 0 (25% IRGB), PWM = 0%
0Fh	0Fh	Boost Output	Boost output voltage set to 4.7V
10h	07h	Frequency Selections	PWM frequency (FPWM[1:0] = 0, 9.92 kHz), Boost SW frequency = 2 MHz
11h	CFh	Enables	NSTBY, EN_BOOST, EN_RGB4, EN_RGB3, EN_RGB2, EN_RGB1 = 1 (exit standby state, enable boost and rgb drivers)

9 Power Supply Recommendations

The LP55281 is designed to operate from an input supply range of 2.7 V to 5.5 V. This input supply must be well regulated and able to provide the peak current required by the LED configuration without voltage drop under load transients (enable on/off). The resistance of the input supply rail should be low enough such that the input current transient does not cause the LP55281 supply voltage to droop more than 5%. Additional bulk decoupling located close to the input capacitor (CIN) may be required to minimize the impact of the input supply rail resistance.

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10 Layout

10.1 Layout Guidelines

The inductive boost converter of the LP55281 regulates a switched voltage at the SW pin, and a step current (up to ICL) through the Schottky diode and output capacitor each switching cycle. The switching voltage can create interference into nearby nodes due to electric field coupling (I = CdV/dt). The large step current through the diode and the output capacitor can cause a large voltage spike at the SW pin and the OUT pin due to parasitic inductance in the step current conducting path (V = Ldi/dt). Board layout guidelines are geared towards minimizing this electric field coupling and conducted noise.

The following list details the main (layout sensitive) areas of the LP55281 device's inductive boost converter in order of decreasing importance:

- Output Capacitor
  - Schottky cathode to COUT+
  - COUT– to GND
- Schottky Diode
  - SW pin to Schottky anode
  - Schottky Cathode to COUT+
- Inductor
  - SW Node PCB capacitance to other traces
- Input Capacitor
  - CIN+ to IN pin

10.1.1 Boost Output Capacitor Placement

Because the output capacitor is in the path of the inductor current discharge path it detects a high-current step from 0 to IPEAK each time the switch turns off and the Schottky diode turns on. Any parasitic inductance (LP_) along this series path from the cathode of the diode through COUT and back into the GND pin of the LP55281 device GND pin contributes to voltage spikes (VSPIKE = LP_ × di/dt) at SW and FB. These spikes can potentially over-voltage the SW pin, or feed through to GND. To avoid this, COUT+ must be connected as close as possible to the cathode of the Schottky diode, and COUT− must be connected as close the the GND pin of the device as possible. The best placement for COUT is on the same layer as the LP55281 in order to avoid any vias that can add excessive series inductance.

10.1.2 Schottky Diode Placement

In the boost circuit of the LP55281 device the Schottky diode is in the path of the inductor current discharge. As a result the Schottky diode sees a high-current step from 0 to IPEAK each time the switch turns off and the diode turns on. Any parasitic inductance (LP) in series with the diode causes a voltage spike (VSPIKE = LP × di/dt) at SW and OUT. This can potentially over-voltage the SW pin, or feed through to VOUT and through the output capacitor and into GND. Connecting the anode of the diode as close as possible to the SW pin and the cathode of the diode as close as possible to COUT and reduces the parasitic inductance and minimize these voltage spikes.

10.1.3 Inductor Placement

The node where the inductor connects to the LP55281 device's SW pin has 2 concerns. First, the switched voltage (0 to VOUT + VF_SCHOTTKY) appears on this node every switching cycle. This switched voltage can be capacitively coupled into nearby nodes. Second, there is a relatively large current (input current) on the traces connecting the input supply to the inductor and connecting the inductor to the SW bump. Any resistance in this path can cause voltage drops that can negatively affect efficiency and reduce the input operating voltage range. To reduce the capacitive coupling of the signal on SW into nearby traces, the SW bump-to-inductor connection must be minimized in area. This limits the PCB capacitance from SW to other traces. Additionally, high impedance nodes that are more susceptible to electric field coupling need to be routed away from SW and not directly adjacent or beneath. This is especially true for sensitive analog signals (ASE1, ASE2, FB, IRT, IRGB, VREF). A GND plane placed directly below SW dramatically reduces the capacitance from SW into nearby traces. Lastly, limit the trace resistance of the VIN to inductor connection and from the inductor to SW connection, by use of short, wide traces.

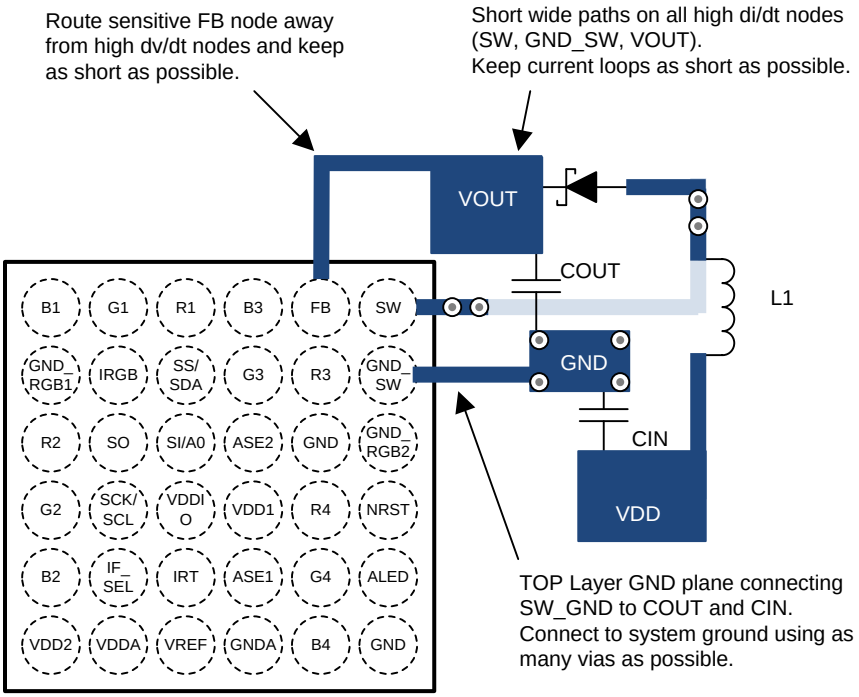
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Layout Guidelines (continued)

10.1.4 Boost Input Capacitor Placement

Close placement of the input capacitor to the IN pin and to the GND pin is critical because any series inductance between IN and CIN+ or CIN− and GND can create voltage spikes that could appear on the VIN supply line and in the GND plane. Close placement of the input bypass capacitor at the input side of the inductor is also critical.

10.2 Layout Example



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Figure 32. LP55281 Layout

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11 Device and Documentation Support

11.1 Device Support

11.1.1 Third-Party Products Disclaimer

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11.2 Related Documentation

For additional information, see the following:

- *AN-1112 DSBGA Wafer Level Chip Scale Package*
- *AN-1412 Micro SMDxt Wafer Level Chip Scale Package*

11.3 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. In the upper right corner, click on *Alert me* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

11.4 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

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Design Support ***TI's Design Support*** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

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11.6 Electrostatic Discharge Caution



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

11.7 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

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PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
LP55281RL/NOPB	ACTIVE	DSBGA	YPG	36	250	Green (RoHS & no Sb/Br)	SNAG	Level-1-260C-UNLIM	-30 to 85	D61B	Samples
LP55281RLX/NOPB	ACTIVE	DSBGA	YPG	36	1000	Green (RoHS & no Sb/Br)	SNAG	Level-1-260C-UNLIM	-30 to 85	D61B	Samples
LP55281TL/NOPB	ACTIVE	DSBGA	YZR	36	250	Green (RoHS & no Sb/Br)	SNAGCU	Level-1-260C-UNLIM	-30 to 85	D56B	Samples
LP55281TLX/NOPB	ACTIVE	DSBGA	YZR	36	1000	Green (RoHS & no Sb/Br)	SNAGCU	Level-1-260C-UNLIM	-30 to 85	D56B	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

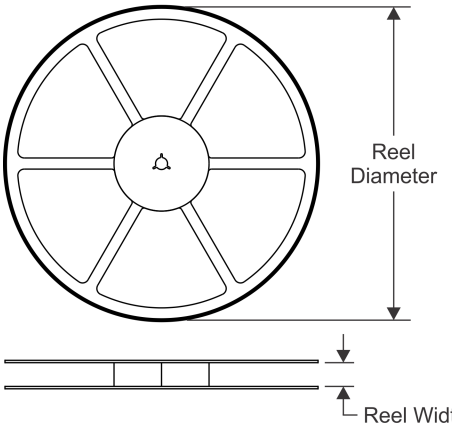
(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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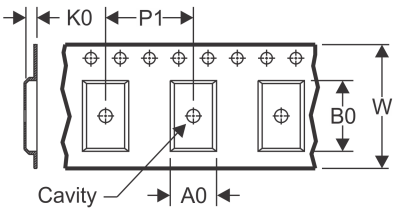
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TAPE AND REEL INFORMATION

REEL DIMENSIONS

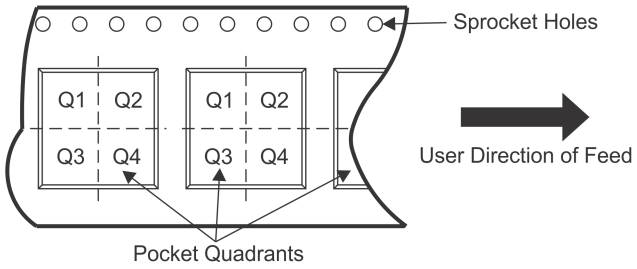


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

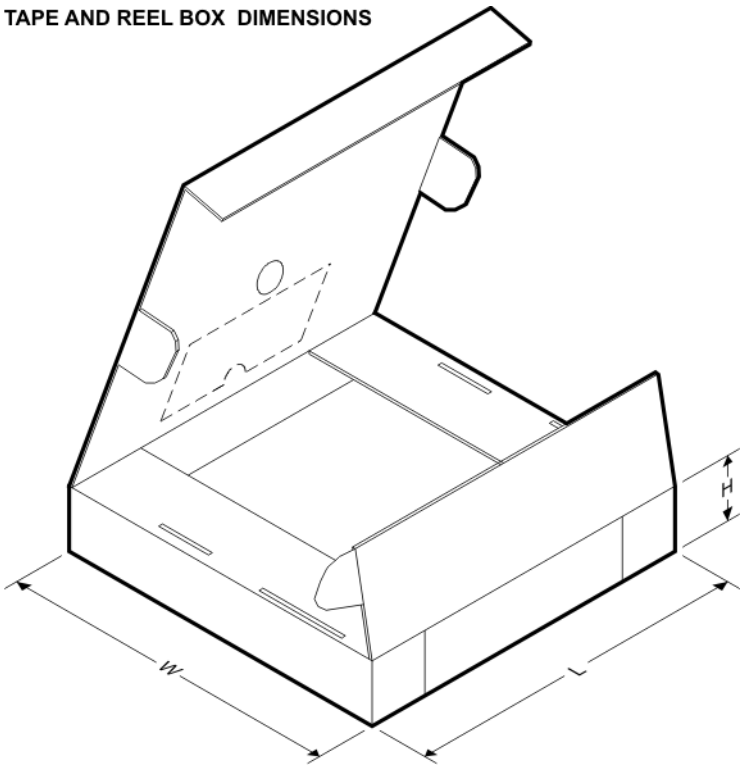
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
LP55281RL/NOPB	DSBGA	YPG	36	250	178.0	12.4	3.21	3.21	0.76	8.0	12.0	Q1
LP55281RLX/NOPB	DSBGA	YPG	36	1000	178.0	12.4	3.21	3.21	0.76	8.0	12.0	Q1
LP55281TL/NOPB	DSBGA	YZR	36	250	178.0	12.4	3.21	3.21	0.76	8.0	12.0	Q1
LP55281TLX/NOPB	DSBGA	YZR	36	1000	178.0	12.4	3.21	3.21	0.76	8.0	12.0	Q1

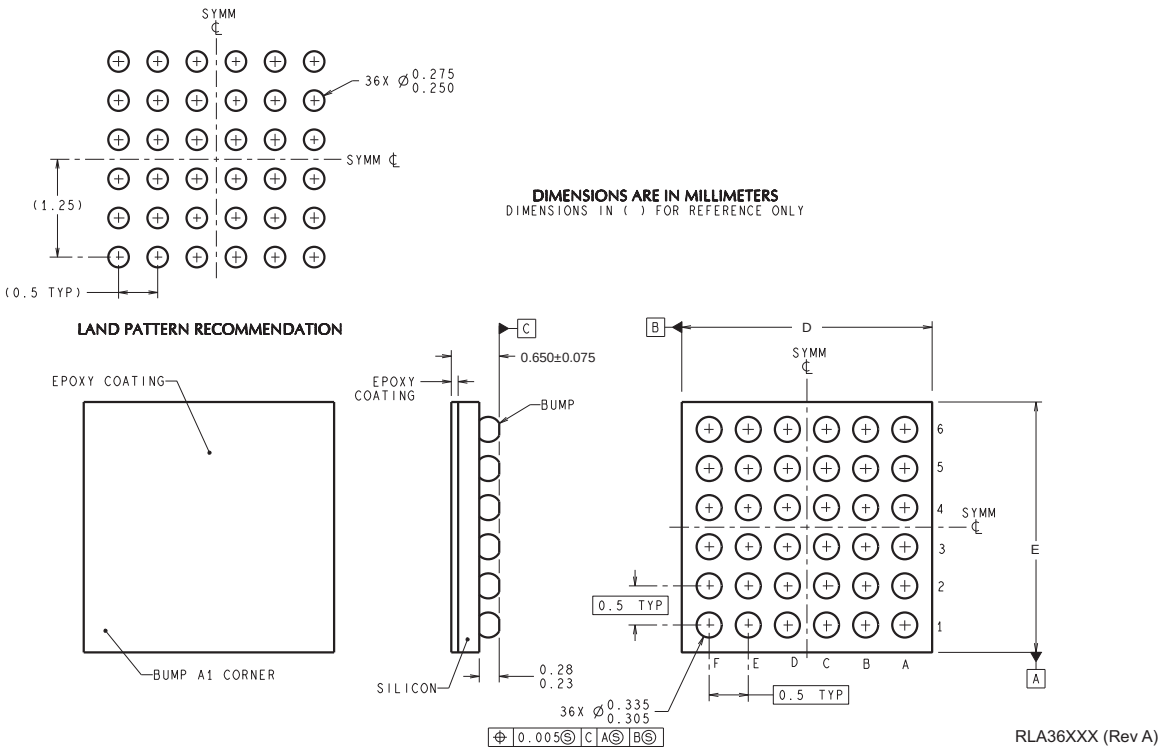
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
LP55281RL/NOPB	DSBGA	YPG	36	250	210.0	185.0	35.0
LP55281RLX/NOPB	DSBGA	YPG	36	1000	210.0	185.0	35.0
LP55281TL/NOPB	DSBGA	YZR	36	250	210.0	185.0	35.0
LP55281TLX/NOPB	DSBGA	YZR	36	1000	210.0	185.0	35.0

YPG0036



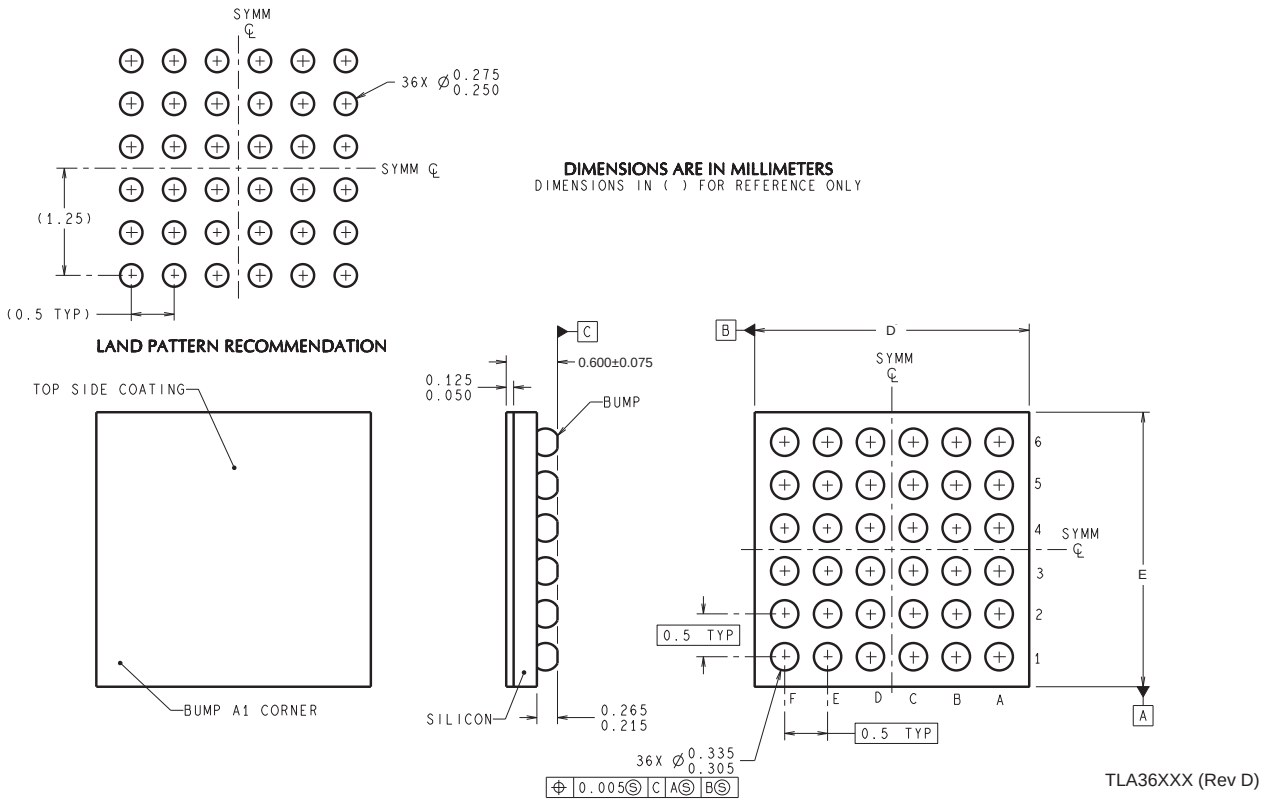
D: Max = 3.013 mm, Min =2.952 mm

E: Max = 3.013 mm, Min =2.952 mm

4214895/A 12/12

NOTES: A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.
B. This drawing is subject to change without notice.

YZR0036



D: Max = 3.013 mm, Min =2.952 mm

E: Max = 3.013 mm, Min =2.952 mm

4215058/A 12/12

NOTES: A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.
B. This drawing is subject to change without notice.

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