Micropower DSBGA 150-mA Ultra Low-Dropout CMOS Voltage Regulator With Sleep MODE

Check for Samples: LP3987

FEATURES

- **Miniature 5-I/O DSBGA Package**
- **Stable With Ceramic and High-Quality Tantalum Output Capacitors**
- **Logic Controlled Enable**
- **Thermal Shutdown and Short-Circuit Current Limit**

APPLICATIONS

- **CDMA Cellular Handsets**
- **Wideband CDMA Cellular Handsets**
- **GSM Cellular Handsets**
- **Portable Information Appliances**
- **µP/DSP Power Supplies**
- **Digital Cameras**
- **SRAM Backup**

KEY SPECIFICATIONS

- **2.7 to 6.0V Input Range**
- **150 mA Output Current**
- **1µA Quiescent Current on Shutdown**
- **100 mV Maximum Dropout with 150 mA Load**
- **50dB PSRR at 10KHz**
- **Sleep MODE Features**
- **Over Temperature & Over Current Protection**
- **−40°C to +125°C Junction Temperature Range for Operation**

DESCRIPTION

The LP3987 is a 150mA fixed output voltage regulator with very low dropout voltage designed specially to meet requirements of battery-powered applications. The additional sleep MODE feature will reduce current consumption during standby operation to prolong the usage of battery.

Dropout Voltage: 100mV maximum dropout with 150mA load.

Shutdown: Less than 1µA quiescent current.

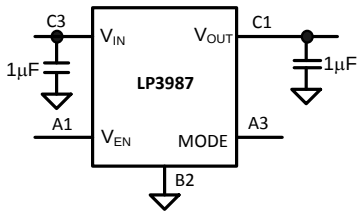
Sleep Mode: Typically 14µA quiescent current during sleep MODE to reduce battery consumption.

Enhanced Stability: The LP3987 is stable with minimum 1µF±20% low ESR ceramic output capacitor as low as 5mΩ and high quality tantalum capacitors.

The LP3987 is available in a thin 5 Bump DSBGA package. Performance is specified for −40°C to 125°C.

This device is available with output voltage options of 2.5V, 2.6V, 2.8V, 2.85V, and 3.0V. For other voltage options, please contact Texas Instruments.

Typical Application Circuit



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

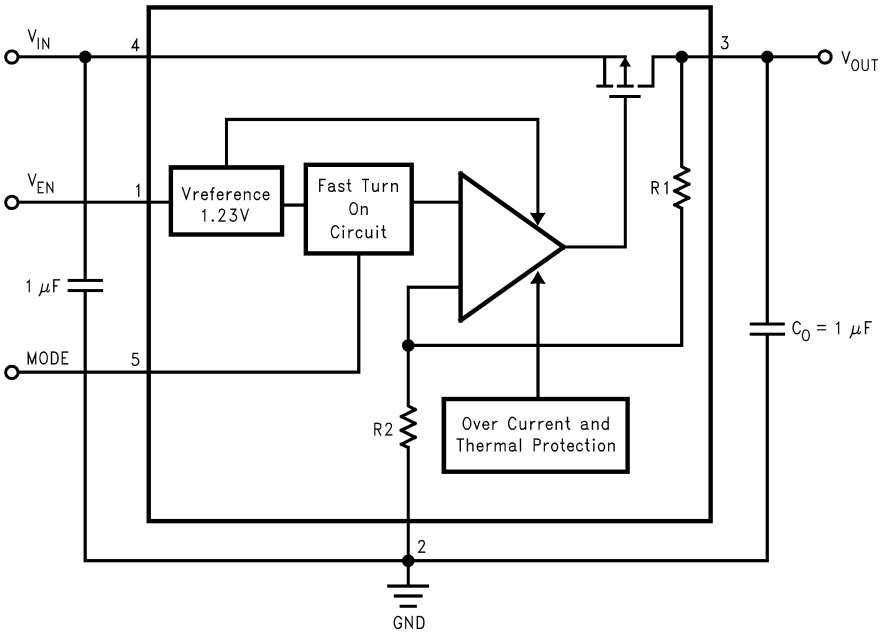
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PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of the Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

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Block Diagram

Figure 1. LP3987



Connection Diagram

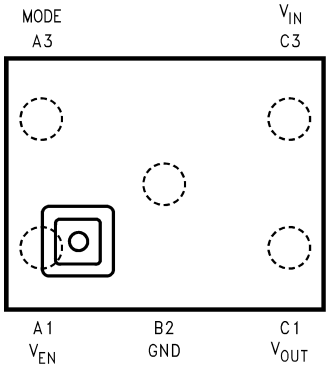


Figure 2. Top View
5 I/O DSBGA Package
See Package Number YZR0005ADA

PIN DESCRIPTIONS

Name	Pin(1)	Function
V_{EN}	A1	Enable Input Logic, Enable High
GND	B2	Common Ground
V_{OUT}	C1	Output voltage of the LDO
V_{IN}	C3	Input voltage of the LDO
MODE	A3	Power Mode Control, Active = 1, Sleep Mode = 0

(1) The pin numbering scheme for the DSBGA package was revised in April, 2002 to conform to JEDEC standard. Only the pin numbers were revised. No changes to the physical location of the inputs/outputs were made. For reference purposes, the obsolete numbering scheme had VEN as pin 1, GND as pin 2, VOUT as pin 3, VIN as pin 4, and MODE as pin 5.

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ORDERING INFORMATION(1)(2)

DSBGA Package			
Output Voltage	**Grade**	**LP3987 Supplied as 250 Units Tape and Reel**	**LP3987 Supplied as 3000 Units Tape and Reel**
2.5V	STD	LP3987ITL-2.5	LP3987ITLX-2.5
2.6V		LP3987ITL-2.6	LP3987ITLX-2.6
2.8V		LP3987ITL-2.8	LP3987ITLX-2.8
2.85V		LP3987ITL-2.85	LP3987ITLX-2.5
3.0V		LP3987ITL-3.0	LP3987ITLX-3.0

(1) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI web site at www.ti.com.
(2) Package drawings, thermal data, and symbolization are available at www.ti.com/packaging.

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

Absolute Maximum Ratings (1) (2)(3)

V_{IN}		−0.3 to 6.5V
V_{EN}, V_{MODE}		−0.3 to 6.5V
V_{OUT}		−0.3V to(V_{IN}+ 0.3V) ≤ 6.5
Storage Temperature		−65°C to +150°C
ESD (4)	Human Body Model	2KV
	Machine Model	200V
Maximum Power Dissipation (5)	θ_{JA} (DSBGA small bump)	255°C/W

(1) Stresses beyond those listed under absolute maximum ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under recommended operating conditions is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltages are with respect to the potential at the GND pin.
(3) If Military/Aerospace specified devices are required, please contact theTI Sales Office/Distributors for availability and specifications.
(4) The human body model is 100pF discharged through 1.5kΩ.
(5) The Absolute Maximum power dissipation depends on the ambient temperature and can be calculated using the formula:$P_D = (T_J - T_A)/\theta_{JA}$,Where T_J is the junction temperature, T_A is the ambient temperature, and θ_{JA} is the junction-to-ambient thermal resistance. For instant, if V_{IN} in target application is 4.2V and worse case current consumption is 90mA. Therefore $P_{MAX_DISSIPATION}$ = (4.2-2.7)*0.09 =135mW. With $P_{MAX_DISSIPATION}$ is 135mW, T_{Jmax} is 125°C and worse case ambient temperature (TA) in target application is 85°C, θ_{JA} = (125-85)/0.135 = 296°C/W.

Operating Ratings (1) (2)

V_{IN}	V_{OUT}+ 200mV to 6V
V_{EN}, V_{MODE}	0 to 6.0V
Junction Temperature	−40°C to +125°C
Maximum Power Dissipation (3)	392mW at 25°C

(1) Stresses beyond those listed under absolute maximum ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under recommended operating conditions is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltages are with respect to the potential at the GND pin.
(3) The Absolute Maximum power dissipation depends on the ambient temperature and can be calculated using the formula:$P_D = (T_J - T_A)/\theta_{JA}$,Where T_J is the junction temperature, T_A is the ambient temperature, and θ_{JA} is the junction-to-ambient thermal resistance. For instant, if V_{IN} in target application is 4.2V and worse case current consumption is 90mA. Therefore $P_{MAX_DISSIPATION}$ = (4.2-2.7)*0.09 =135mW. With $P_{MAX_DISSIPATION}$ is 135mW, T_{Jmax} is 125°C and worse case ambient temperature (TA) in target application is 85°C, θ_{JA} = (125-85)/0.135 = 296°C/W.

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Electrical Characteristics

Unless otherwise specified: V_{EN} = 1.8V, MODE = 1.8V, V_{IN} = $V_{OUT(nom)}$ + 0.5V, C_{IN} = 1 µF, I_{OUT} = 1mA, C_{OUT} = 1 µF. Typical values and limits appearing in standard typeface are for T_J = 25°C. Limits appearing in **boldface type** apply over the entire junction temperature range for operation, −40°C to +125°C. (1) (2)

Parameter		Test Conditions	Typ	Limit		Unit
				Min	Max	
ΔV_{OUT}	Output Voltage Tolerance	I_{OUT} = 1mA, 25°C		-2	2	% of $V_{OUT(nom)}$
		I_{OUT} = 1mA		**−3**	**3**	
	Line Regulation Error	V_{IN} = ($V_{OUT(nom)}$ + 0.5V) to 6.0V, I_{OUT} = 1 mA		**−0.1**	**0.1**	%/V
	Load Regulation Error	I_{OUT} = 1mA to 150 mA		0.0004	**0.002**	%/mA
	Dropout Voltage (3)	I_{OUT} = 1mA	0.4		**2**	mV
		I_{OUT} = 150mA	60		**100**	
$\Delta V_{OUT(SLEEP)}$	Output Voltage difference at MODE = 0V	MODE = 0V, (4)		**-150**	**+100**	mV
Transient Response	Line Transient Response (5)	MODE = 1.8V, I_{LOAD} = 100mA, T_{RISE} = T_{FALL} = 10µS, V_{IN} = 600mV $_{P-P}$ AC Square wave, (6)	21			mVpp
	Load Transient Response (5)	MODE = 1.8V, C_{OUT} = 4.7µF, T_{RISE} = T_{FALL} = 100nS, V_{IN} = 3.1V, 3.6V, 4.2V, (7) (8)	100			mVpk
PSRR	Power Supply Rejection Ratio (5)	V_{IN} = $V_{OUT(nom)}$ + 1V, MODE = 1.8V, f = <10 kHz, I_{OUT} = 1mA	50			dB
		V_{IN} = $V_{OUT(nom)}$ + 1V, MODE = 0V, f = <10 kHz, I_{OUT} = 1mA	10			
$I_{Q(ON)}$	Quiescent Current	MODE = 1.8V, I_{OUT} = 0mA, V_{IN} = 4.2V	85		**120**	µA
		MODE = 1.8V, I_{OUT} = 150mA, V_{IN} = 4.2V	160		**200**	
$I_{Q(OFF)}$	Quiescent Current	ENABLE = 0V, V_{IN} = 4.2V	1		**3**	µA
$I_{Q(SLEEP)}$	Current in Standby Mode	MODE = 0V, I_{OUT} = 50µA, V_{IN} = 4.2V	14		**21**	µA
I_{SC}	Short Circuit Current Limit (5)	Output Grounded	600			mA
$I_{SC(SLEEP)}$	Short Circuit Current in Sleep MODE	Output Grounded	28		**43**	mA
$I_{OUT(ON)}$	Maximum Output Current at MODE = 1.8V	MODE = 1.8V		**150**		mA
$I_{OUT(SLEEP)}$	Maximum Output Current at MODE = 0V	MODE = 0V		**3**		mA
e_n	Output Noise Voltage (5)	BW = 10 Hz to 100 kHz, C_{OUT} = 1µF	70			µVrms
$T_{SHUTDOWN}$	Shutdown Temperature (5)	Sleep MODE = 1.8V	155			°C
Logic Control Characteristics						
I_{EN}	Maximum Input Current at EN	V_{EN} = 0 and V_{IN}= 6.0V	0.015			µA
V_{IL}	Logic Low Input Threshold	V_{IN} = 3.05 to 6V		**0.5**		V
V_{IH}	Logic High Input Threshold	V_{IN} = 3.05 to 6V			**1.2**	V

(1) Min and Max Limits are verified by design, test, or statistical analysis. Typical (Typ.) numbers are not verified, but do represent the most likely norm.
(2) The nominal output voltage, which is labeled $V_{OUT(nom)}$, is the output voltage measured with the input 0.5V above $V_{OUT(nom)}$ and a 1mA load.
(3) Dropout voltage is defined as the input to output voltage differential at which the output voltage falls to 100mV below the nominal output voltage. V_{IN} less than minimum operating voltage may be used for test purposes.
(4) On/Sleep Mode voltage tolerance and current capability requirement. See Figure 3.
(5) This electrical specification is specified by design.
(6) Line Transient response requirement. See Figure 4.
(7) Load Transient response requirement. See Figure 5.
(8) During transient recovery, output voltage should not be oscillating.

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Electrical Characteristics (continued)

Unless otherwise specified: V_{EN} = 1.8V, MODE = 1.8V, V_{IN} = $V_{OUT(nom)}$ + 0.5V, C_{IN} = 1 µF, I_{OUT} = 1mA, C_{OUT} = 1 µF. Typical values and limits appearing in standard typeface are for T_J = 25°C. Limits appearing in **boldface type** apply over the entire junction temperature range for operation, −40°C to +125°C. (1) (2)

Parameter		Test Conditions	Typ	Limit		Unit
				Min	Max	
V_{MODE_L}	Logic Low Input Threshold	V_{IN} = 3.05 to 6V		**0.5**		V
V_{MODE_H}	Logic High Input Threshold	V_{IN} = 3.05 to 6V			**1.2**	V
I_{MODE}	Maximum Input Current at V_{MODE}	V_{MODE} = 0 and V_{IN} = 6.0V	0.015			µA
Timing Characteristics						
T_{ON}	Turn on Time (On Mode)(5) (9)	MODE = 1.8V, C_{OUT} = 4.7µF	170		**250**	µs
T_{SLEEP}	Turn on Time (Sleep Mode)(5)(10)	MODE = 0V, C_{OUT} = 4.7µF	0.5		**5**	ms
T_{MODE}	Sleep to On Mode Settle Time(5)(11)	C_{OUT} = 4.7µF, Enable = 1.8V	200		**300**	µs

(9) T_{ON} is measured from rising edge of Enable with MODE = 1.8V to when V_{OUT} reaches 95% of final value.
(10) T_{SLEEP} is measured from rising edge of Enable with MODE = 0V to when V_{OUT} reaches 95% of final value.
(11) T_{MODE} is measured from rising edge of MODE with ENABLE = 1.8V to time before full current capability.

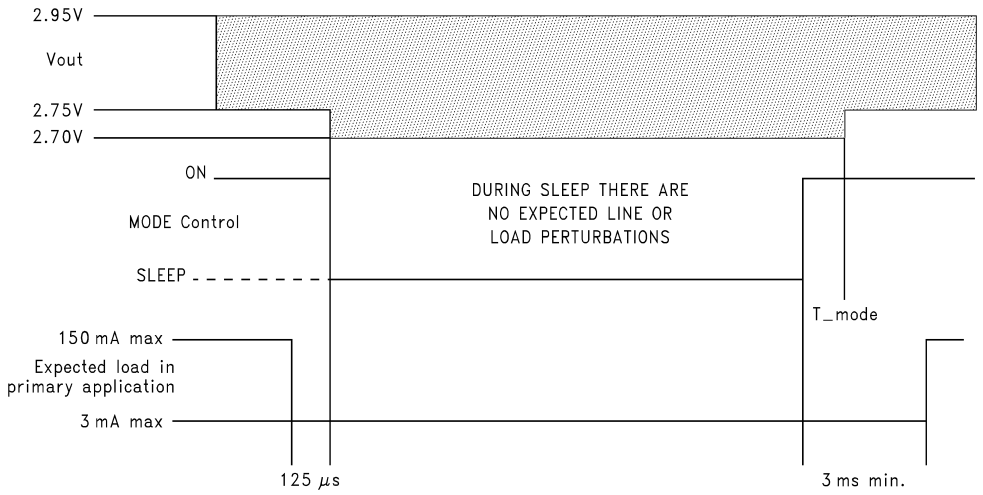


Figure 3.

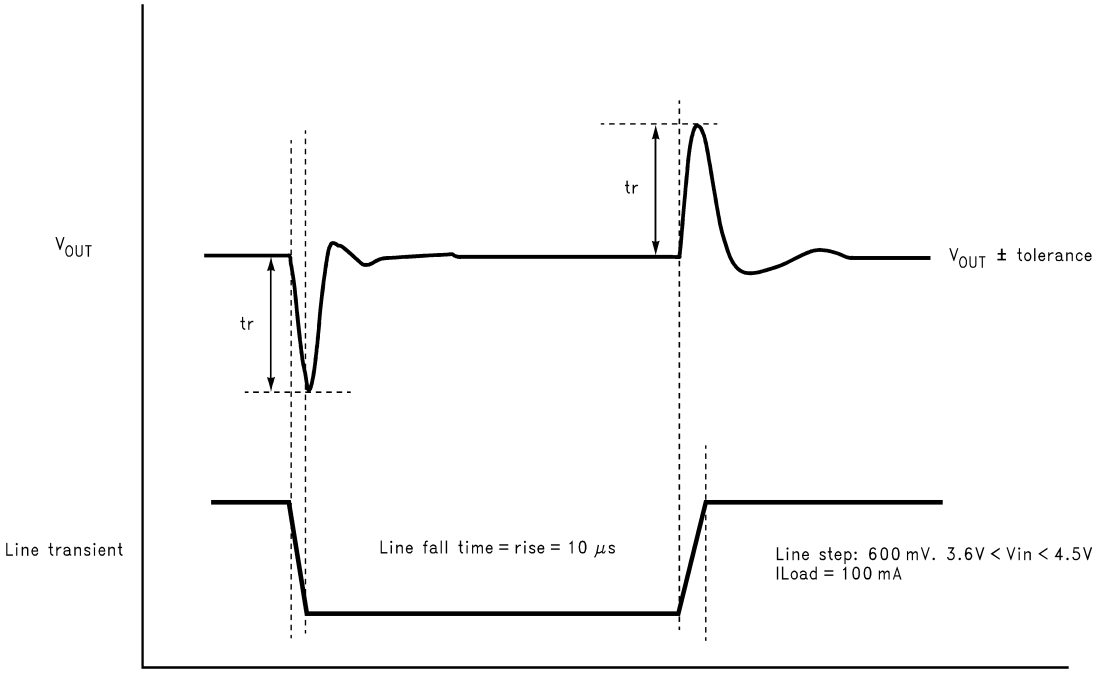


Figure 4.

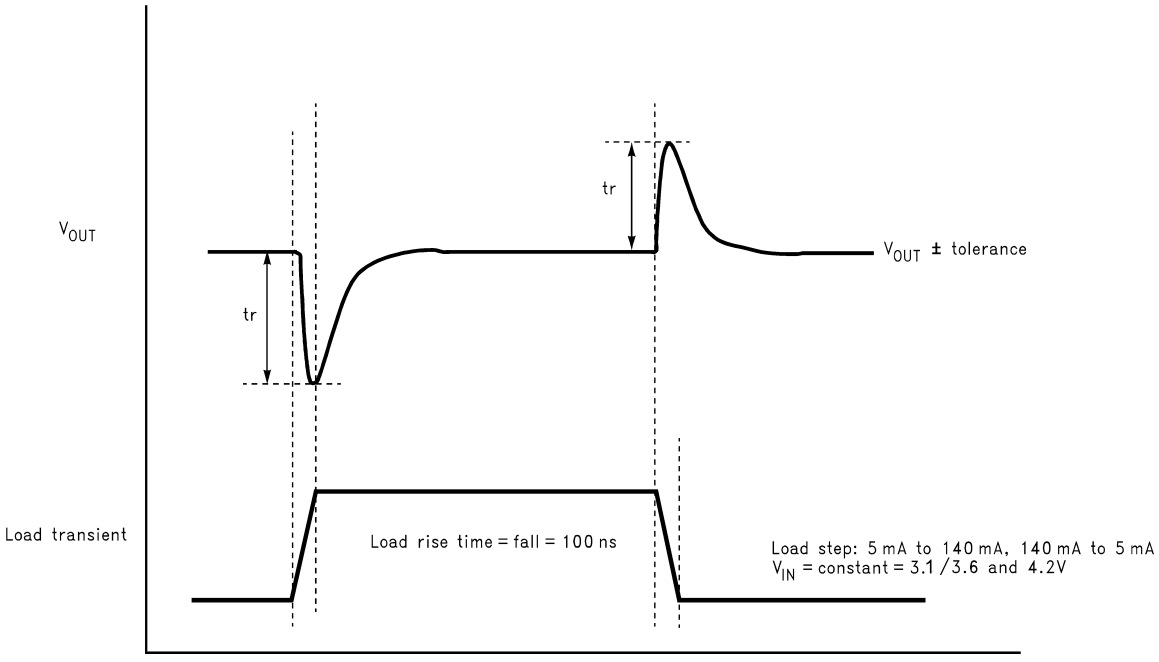


Figure 5.

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Typical Performance Characteristics

Unless otherwise specified, $C_{IN} = C_{OUT} = 1$ µF Ceramic, $V_{IN} = V_{OUT(nom)} + 0.5V$, $T_A = 25°C$, Enable pin is tied to V_{IN}, MODE = 1.8V.

Ground Current at T_A = 25°C

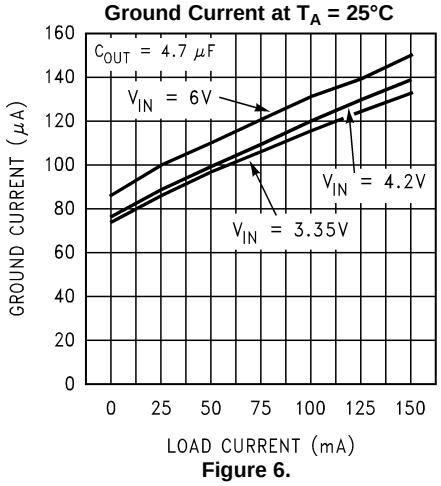


Figure 6.

Ground Current at T_A = 40°C

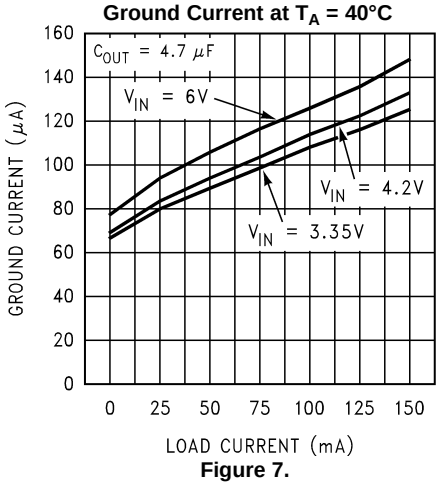


Figure 7.

Ground Current at T_A = 85°C

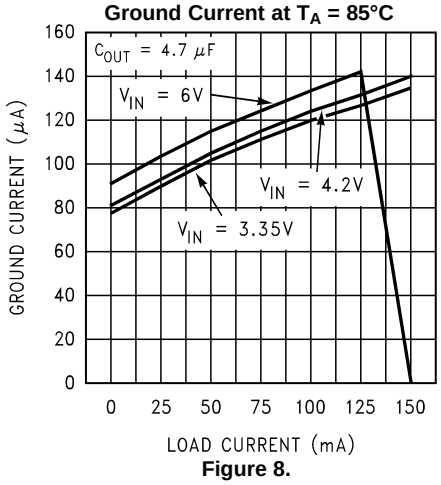


Figure 8.

Dropout Voltage vs Load Current

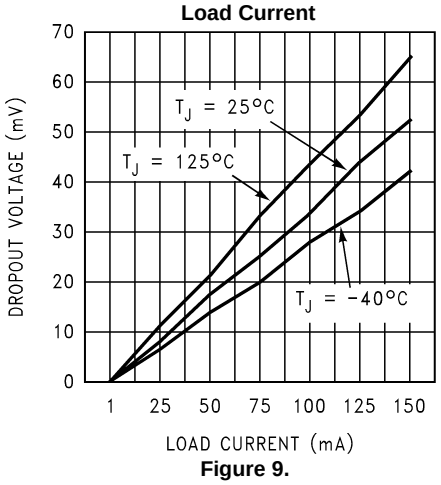


Figure 9.

Ripple Rejection ($C_{IN} = C_{OUT} = 1µF$, $I_L = 1mA$)

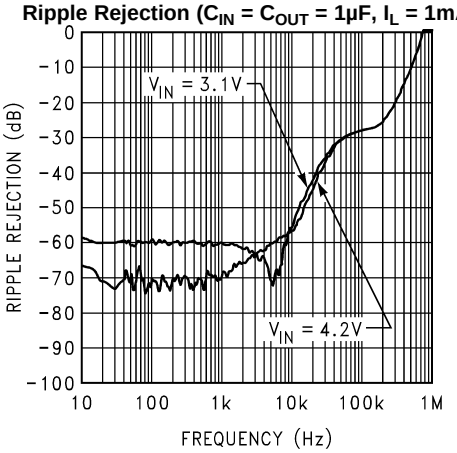


Figure 10.

Ripple Rejection ($V_{IN} = V_{OUT(nom)} + 1V$, $C_{IN} = C_{OUT} = 1µF$, $I_L = 1mA$)

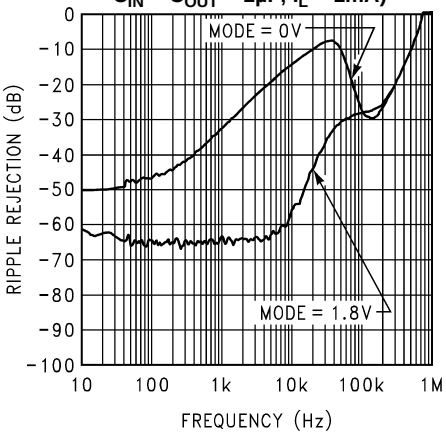


Figure 11.

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Typical Performance Characteristics (continued)

Unless otherwise specified, $C_{IN} = C_{OUT} = 1$ µF Ceramic, $V_{IN} = V_{OUT(nom)} + 0.5V$, $T_A = 25°C$, Enable pin is tied to V_{IN}, MODE = 1.8V.

T_{SLEEP} at MODE = 0V, C_{OUT} = 1µF, I_L = 1mA

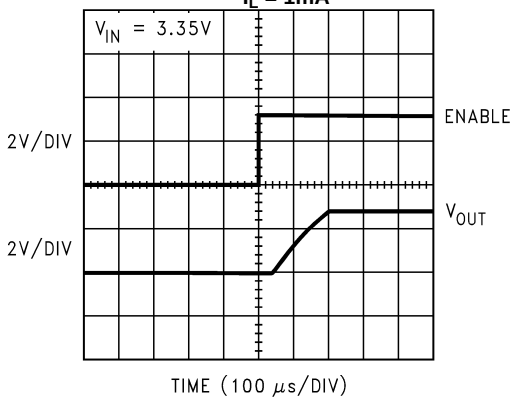


Figure 12.

T_{SLEEP} at MODE = 0V, C_{OUT} = 1µF, I_L = 1mA

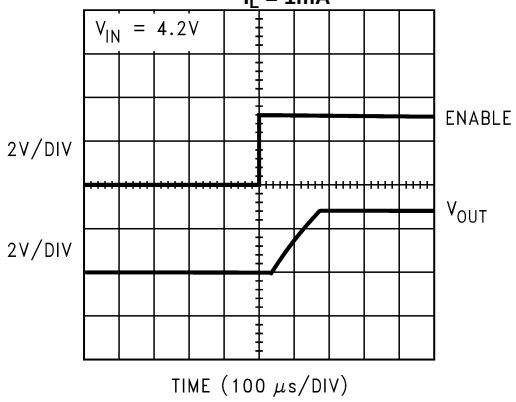


Figure 13.

T_{ON} at MODE = 1.8V, C_{OUT} = 1µF, I_L = 150mA

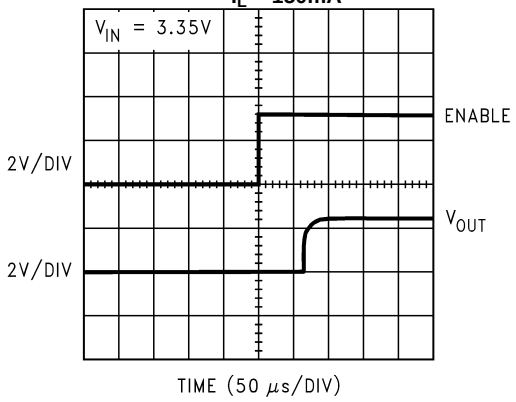


Figure 14.

T_{ON} at MODE = 1.8V, C_{OUT} = 1µF, I_L = 150mA

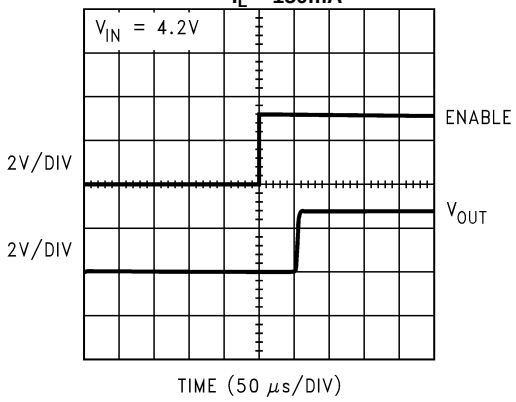


Figure 15.

T_{SLEEP} at MODE = 0V, C_{OUT} = 4.7µF, I_L = 1mA

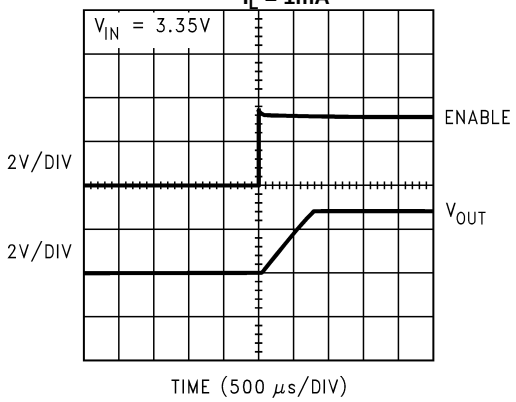


Figure 16.

T_{SLEEP} at MODE = 0V, C_{OUT} = 4.7µF, I_L = 1mA

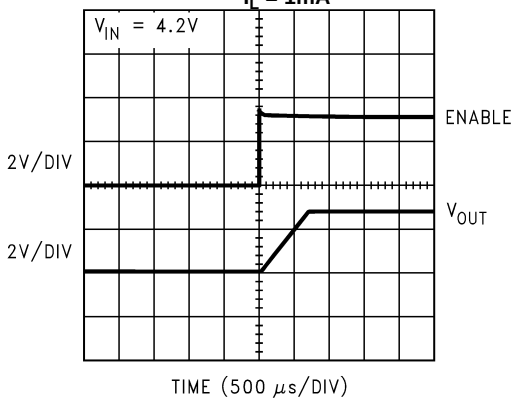


Figure 17.

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Typical Performance Characteristics (continued)

Unless otherwise specified, $C_{IN} = C_{OUT} = 1$ µF Ceramic, $V_{IN} = V_{OUT(nom)} + 0.5V$, $T_A = 25°C$, Enable pin is tied to V_{IN}, MODE = 1.8V.

T_{ON} at MODE = 1.8V, C_{OUT} = 4.7µF, I_L = 150mA

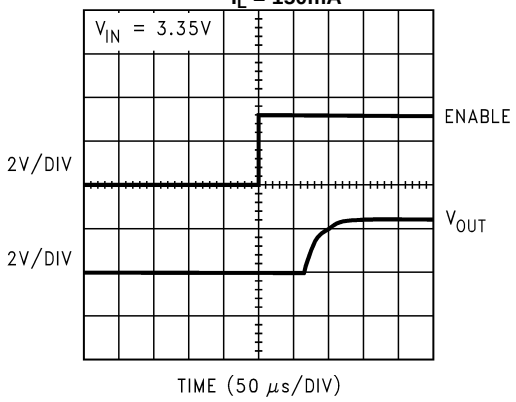


Figure 18.

T_{ON} at MODE = 1.8V, C_{OUT} = 4.7µF, I_L = 150mA

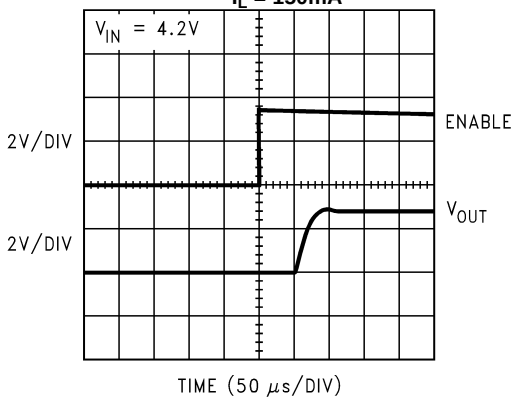


Figure 19.

T_{MODE} Measurement at V_{IN} = 3.05V

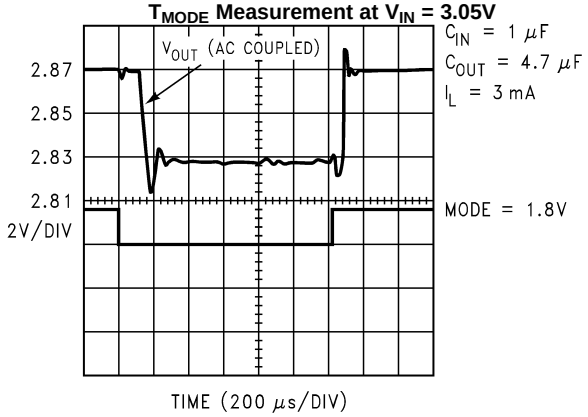


Figure 20.

T_{MODE} Measurement at V_{IN} = 3.6V

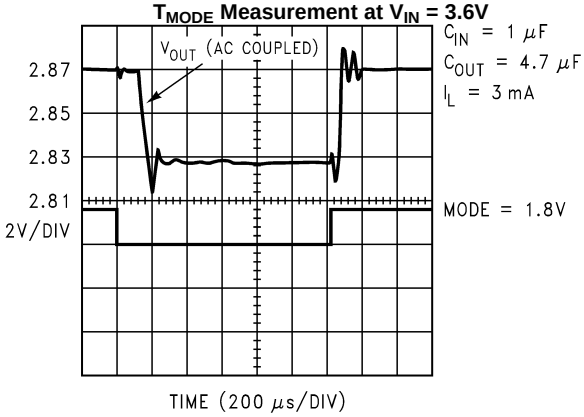


Figure 21.

T_{MODE} Measurement at V_{IN} = 4.2V

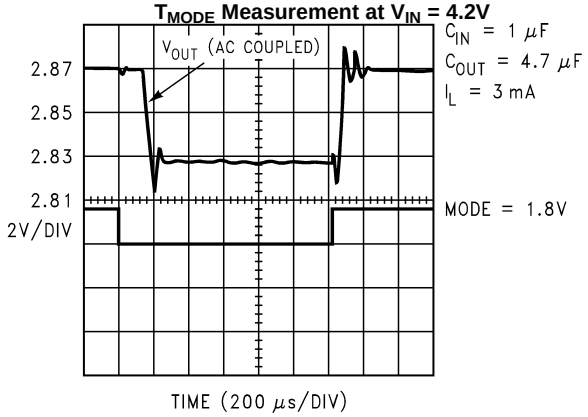


Figure 22.

Output Short Circuit Current

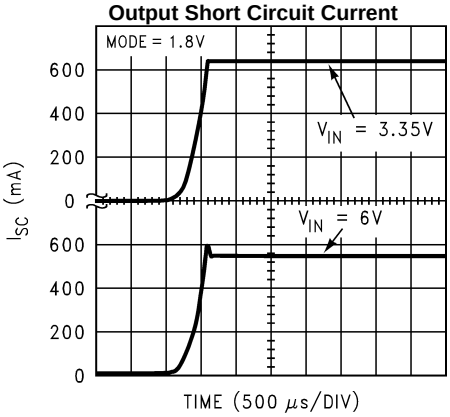


Figure 23.

Typical Performance Characteristics (continued)

Unless otherwise specified, $C_{IN} = C_{OUT} = 1$ µF Ceramic, $V_{IN} = V_{OUT(nom)} + 0.5V$, $T_A = 25°C$, Enable pin is tied to V_{IN}, MODE = 1.8V.

Output Short Circuit Current

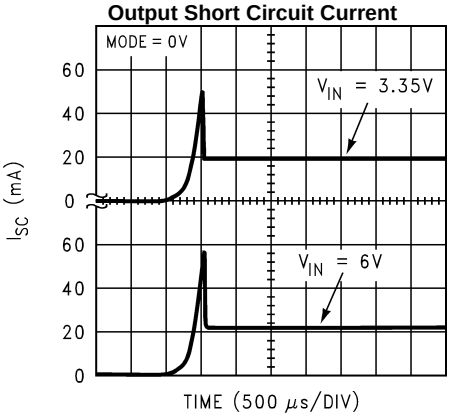


Figure 24.

Load Transient Response at V_{IN} = 3.1V

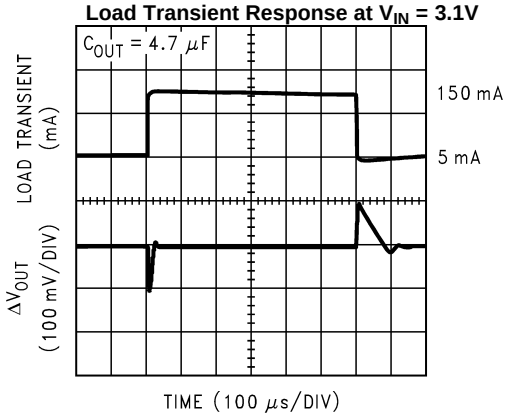


Figure 25.

Load Transient Response at V_{IN} = 3.35V

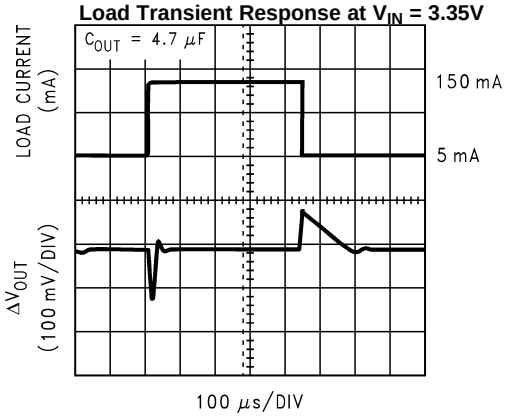


Figure 26.

Load Transient Response at V_{IN} = 3.6V

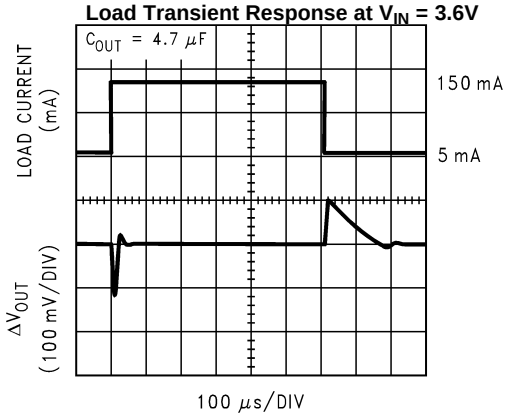


Figure 27.

Load Transient Response at V_{IN} = 4.2V

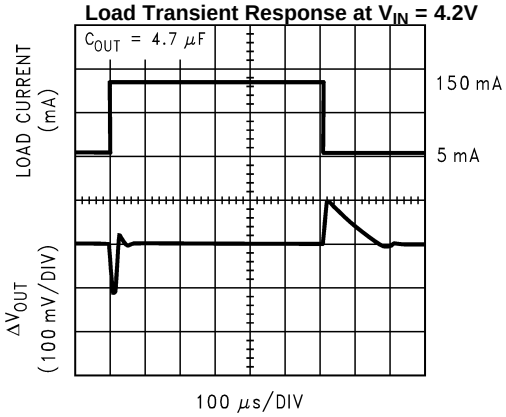


Figure 28.

Load Transient Response at V_{IN} = 3.1V, C_{OUT} = 1µF

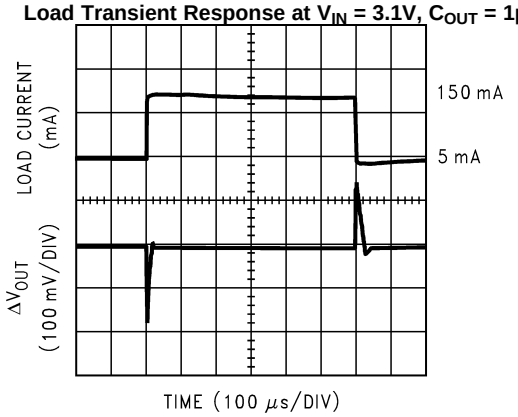


Figure 29.

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Typical Performance Characteristics (continued)

Unless otherwise specified, C_{IN} = C_{OUT} = 1 µF Ceramic, V_{IN} = $V_{OUT(nom)}$ + 0.5V, T_A = 25°C, Enable pin is tied to V_{IN}, MODE = 1.8V.

Load Transient Response at V_{IN} = 3.35V, C_{OUT} = 1µF

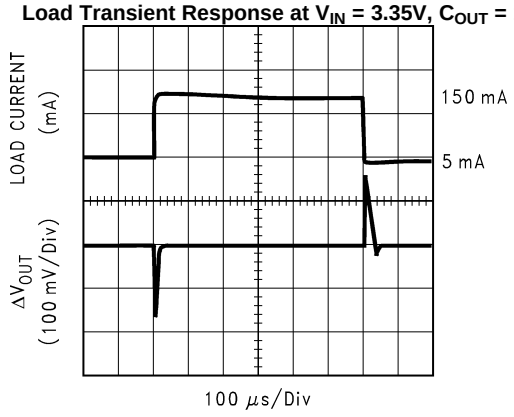


Figure 30.

Load Transient Response at V_{IN} = 4.2V, C_{OUT} = 1µF

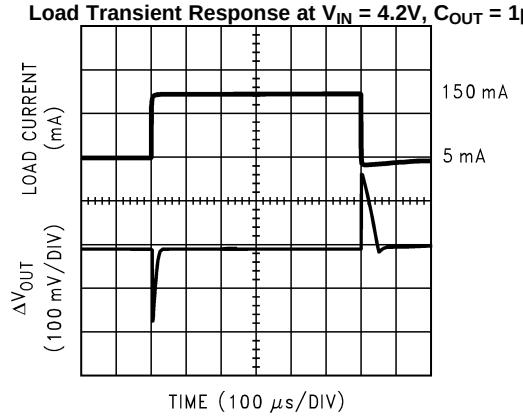


Figure 31.

Load Transient Response at V_{IN} = 3.6V, C_{OUT} = 1µF

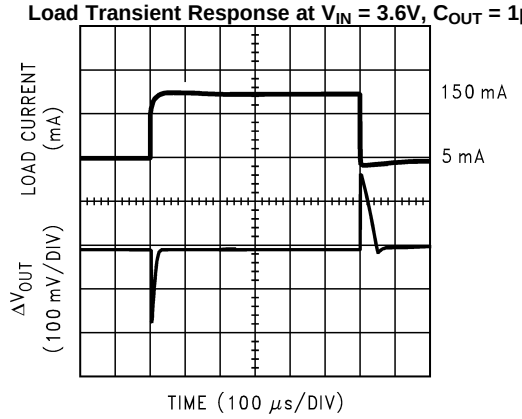


Figure 32.

Output Voltage Change vs Temperature

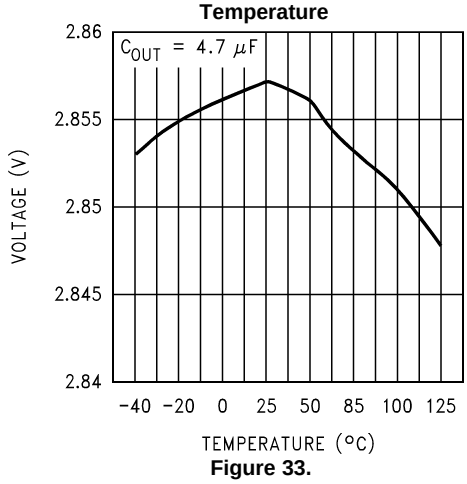


Figure 33.

Line Transient Response

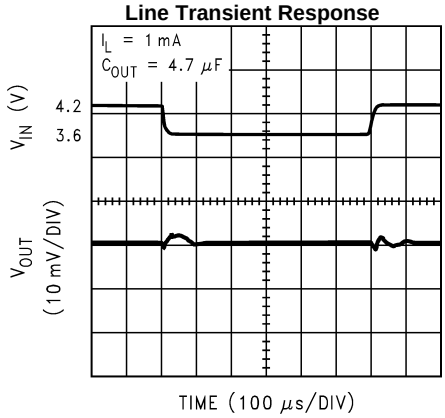


Figure 34.

Line Transient Response

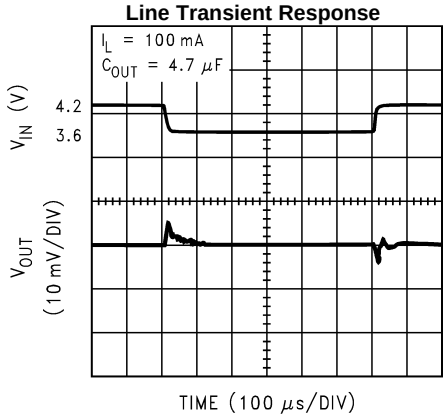


Figure 35.

Typical Performance Characteristics (continued)

Unless otherwise specified, $C_{IN} = C_{OUT} = 1$ µF Ceramic, $V_{IN} = V_{OUT(nom)} + 0.5V$, $T_A = 25°C$, Enable pin is tied to V_{IN}, MODE = 1.8V.

Line Transient Response

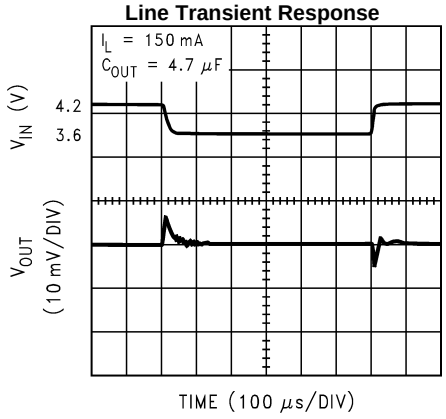


Figure 36.

Line Transient Response

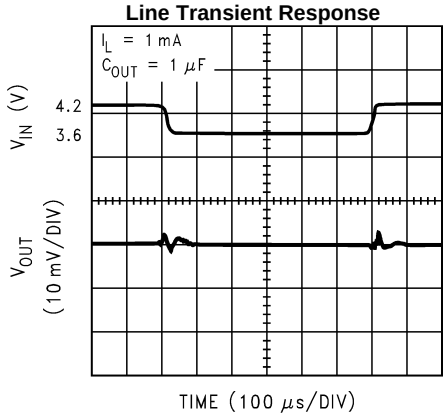


Figure 37.

Line Transient Response

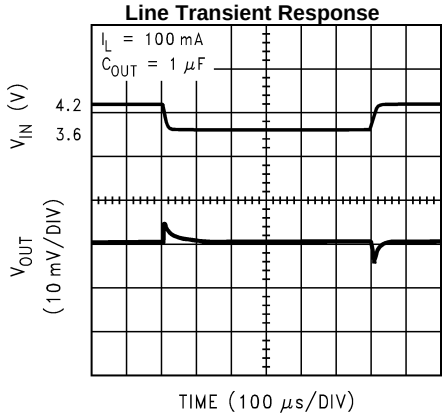


Figure 38.

Line Transient Response

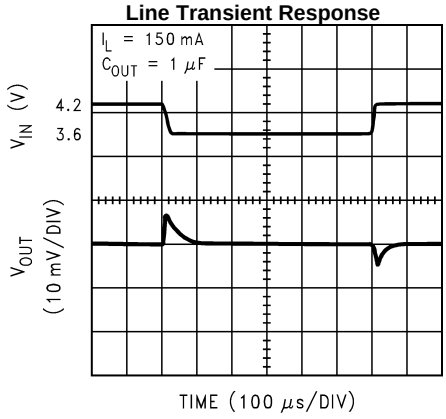


Figure 39.

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APPLICATION HINTS

EXTERNAL CAPACITORS

Like any low-dropout regulator, the LP3987 requires external capacitors for regulator stability. The LP3987 is specifically designed for portable applications requiring minimum board space and smallest components. These capacitors must be correctly selected for good performance.

INPUT CAPACITOR

An input capacitance of ≅ 1µF is required between the LP3987 input pin and ground (the amount of the capacitance may be increased without limit).

This capacitor must be located a distance of not more than 1cm from the input pin and returned to a clean analog ground. Any good quality ceramic, tantalum, or film capacitor may be used at the input.

Important: Tantalum capacitors can suffer catastrophic failures due to surge current when connected to a low-impedance source of power (like a battery or a very large capacitor). If a tantalum capacitor is used at the input, it must be specified by the manufacturer to have a surge current rating sufficient for the application.

There are no requirements for the ESR on the input capacitor, but tolerance and temperature coefficient must be considered when selecting the capacitor to ensure the capacitance will be ≅ 1µF over the entire operating temperature range.

OUTPUT CAPACITOR

The LP3987 is designed specifically to work with very small ceramic output capacitors. A ceramic capacitor (dielectric types Z5U, Y5V or X7R) in 1 to 4.7 µF range with 5mΩ to 500mΩ ESR range is suitable in the LP3987 application circuit.

It may also be possible to use tantalum or film capacitors at the output, but these are not as attractive for reasons of size and cost (see next section Capacitor Characteristics).

The output capacitor must meet the requirement for minimum amount of capacitance and also have an ESR (Equivalent Series Resistance) value which is within a stable range (5 mΩ to 500 mΩ).

NO-LOAD STABILITY

The LP3987 will remain stable and in regulation with no external load. This is specially important in CMOS RAM keep-alive applications.

CAPACITOR CHARACTERISTICS

The LP3987 is designed to work with ceramic capacitors on the output to take advantage of the benefits they offer: for capacitance values in the range of 1µF to 4.7µF range, ceramic capacitors are the smallest, least expensive and have the lowest ESR values (which makes them best for eliminating high frequency noise). The ESR of a typical 1µF ceramic capacitor is in the range of 20 mΩ to 40 mΩ, which easily meets the ESR requirement for stability by the LP3987. The ceramic capacitor's capacitance can vary with temperature. Most large value ceramic capacitors (≅ 2.2µF) are manufactured with Z5U or Y5V temperature characteristics, which results in the capacitance dropping by more than 50% as the temperature goes from 25°C to 85°C.

A better choice for temperature coefficient in a ceramic capacitor is X7R, which holds the capacitance within ±15%. Tantalum capacitors are less desirable than ceramic for use as output capacitors because they are more expensive when comparing equivalent capacitance and voltage ratings in the 1µF to 4.7µF range.

Another important consideration is that tantalum capacitors have higher ESR values than equivalent size ceramics. This means that while it may be possible to find a tantalum capacitor with an ESR value within the stable range, it would have to be larger in capacitance (which means bigger and more costly) than a ceramic capacitor with the same ESR value. It should also be noted that the ESR of a typical tantalum will increase about 2:1 as the temperature goes from 25°C down to −40°C, so some guard band must be allowed.

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ON/OFF INPUT OPERATION

The LP3987 is turned off by pulling the V_{EN} pin low, and turned on by pulling it high. If this feature is not used, the V_{EN} pin should be tied to V_{IN} to keep the regulator output on at all time. To assure proper operation, the signal source used to drive the V_{EN} input must be able to swing above and below the specified turn-on/off voltage thresholds listed in the Electrical Characteristics section under V_{IL} and V_{IH}.

MODE OPERATION

The LP3987 enters sleep mode by pulling MODE = 0V externally to reduce current during standby operation. During sleep mode, LP3987 consumes only 14µA of quiescent current and supplies up to 3mA of current. The device returns to active mode by pulling MODE = 1.8V. If this function is not used, the MODE pin should be tied to V_{IN}.

THERMAL PROTECTION

The LP3987 has internal thermal protection circuitry to disable the internal pass transistor if the junction temperature exceeds 125°C to allow the device to cool down. The pass transistor will turn on when temperature falls below the maximum operating junction temperature of 125°C. This feature is designed to protect the device in the event of fault conditions. For normal operation, it is suggested to limit the device junction temperature to less than 125°C.

DSBGA MOUNTING

The DSBGA package requires specific mounting techniques which are detailed in Texas Instruments AN-1112 Application Report (SNOA401). Referring to the section *PCB Layout*, note that the pad style which must be used with the 5 pin package is NSMD (non-solder mask defined) type.

For best results during assembly, alignment ordinals on the PC board may be used to facilitate placement of the DSBGA device.

DSBGA LIGHT SENSITIVITY

Exposing the DSBGA device to direct sunlight will cause misoperation of the device. Light sources such as Halogen lamps can effect electrical performance if brought near to the device. The wavelengths which have most detrimental effect are reds and infra-reds, which means that the fluorescent lighting used inside most buildings has very little effect on performance. A DSBGA test board was brought to within 1cm of a fluorescent desk lamp and the effect on the regulated output voltage was negligible, showing a deviation of less than 0.1% from nominal.

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REVISION HISTORY

Changes from Revision F (May 2013) to Revision G	Page
• Changed layout of National Data Sheet to TI format	14

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PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)	Op Temp (°C)	Top-Side Markings (4)	Samples
LP3987ITL-2.5/NOPB	ACTIVE	DSBGA	YZR	5	250	Green (RoHS & no Sb/Br)	SNAGCU	Level-1-260C-UNLIM		7	Samples
LP3987ITL-2.6/NOPB	ACTIVE	DSBGA	YZR	5	250	Green (RoHS & no Sb/Br)	SNAGCU	Level-1-260C-UNLIM	-40 to 125	7	Samples
LP3987ITL-2.8/NOPB	ACTIVE	DSBGA	YZR	5	250	Green (RoHS & no Sb/Br)	SNAGCU	Level-1-260C-UNLIM	-40 to 125	7	Samples
LP3987ITL-2.85/NOPB	ACTIVE	DSBGA	YZR	5	250	Green (RoHS & no Sb/Br)	SNAGCU	Level-1-260C-UNLIM	-40 to 125	7	Samples
LP3987ITL-3.0/NOPB	ACTIVE	DSBGA	YZR	5	250	Green (RoHS & no Sb/Br)	SNAGCU	Level-1-260C-UNLIM		7	Samples
LP3987ITLX-2.5/NOPB	ACTIVE	DSBGA	YZR	5	3000	Green (RoHS & no Sb/Br)	SNAGCU	Level-1-260C-UNLIM		7	Samples
LP3987ITLX-2.6/NOPB	ACTIVE	DSBGA	YZR	5	3000	Green (RoHS & no Sb/Br)	SNAGCU	Level-1-260C-UNLIM	-40 to 125	7	Samples
LP3987ITLX-2.8/NOPB	ACTIVE	DSBGA	YZR	5	3000	Green (RoHS & no Sb/Br)	SNAGCU	Level-1-260C-UNLIM	-40 to 125	7	Samples
LP3987ITLX-2.85/NOPB	ACTIVE	DSBGA	YZR	5	3000	Green (RoHS & no Sb/Br)	SNAGCU	Level-1-260C-UNLIM	-40 to 125	7	Samples
LP3987ITLX-3.0/NOPB	ACTIVE	DSBGA	YZR	5	3000	Green (RoHS & no Sb/Br)	SNAGCU	Level-1-260C-UNLIM		7	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

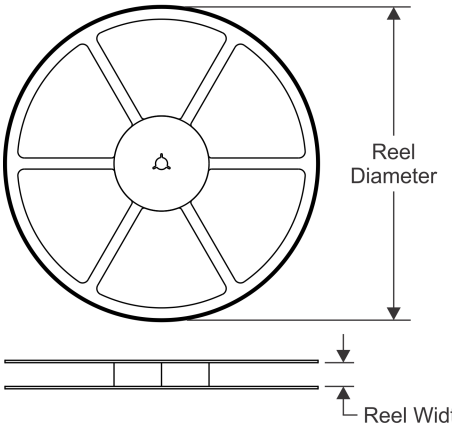
(4) Multiple Top-Side Markings will be inside parentheses. Only one Top-Side Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Top-Side Marking for that device.

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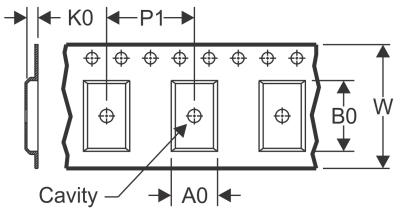
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TAPE AND REEL INFORMATION

REEL DIMENSIONS

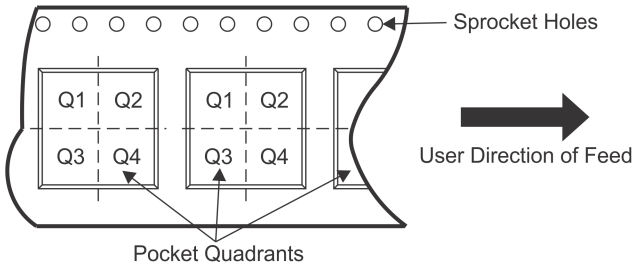


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

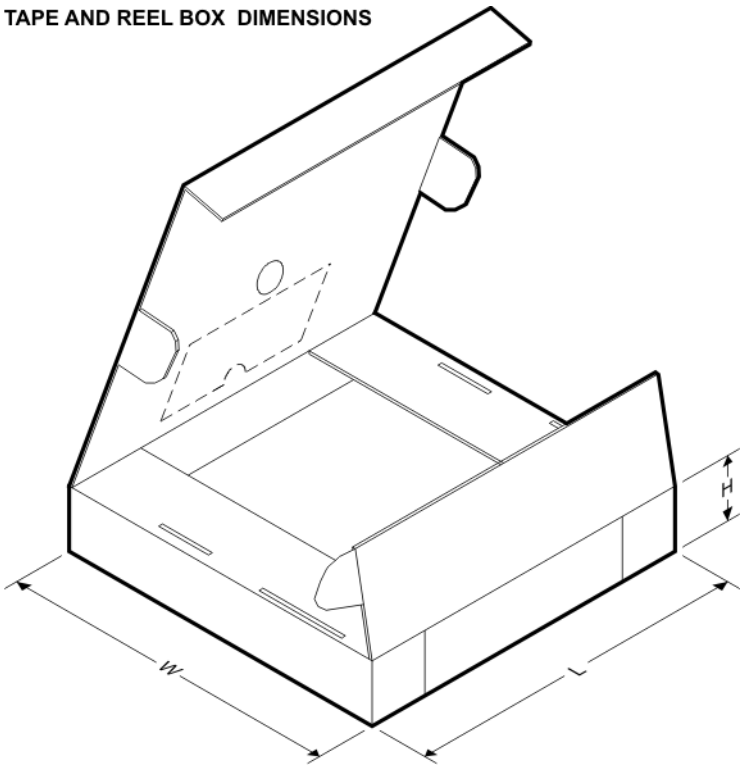
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
LP3987ITL-2.5/NOPB	DSBGA	YZR	5	250	178.0	8.4	1.09	1.55	0.76	4.0	8.0	Q1
LP3987ITL-2.6/NOPB	DSBGA	YZR	5	250	178.0	8.4	1.09	1.55	0.76	4.0	8.0	Q1
LP3987ITL-2.8/NOPB	DSBGA	YZR	5	250	178.0	8.4	1.09	1.55	0.76	4.0	8.0	Q1
LP3987ITL-2.85/NOPB	DSBGA	YZR	5	250	178.0	8.4	1.09	1.55	0.76	4.0	8.0	Q1
LP3987ITL-3.0/NOPB	DSBGA	YZR	5	250	178.0	8.4	1.09	1.55	0.76	4.0	8.0	Q1
LP3987ITLX-2.5/NOPB	DSBGA	YZR	5	3000	178.0	8.4	1.09	1.55	0.76	4.0	8.0	Q1
LP3987ITLX-2.6/NOPB	DSBGA	YZR	5	3000	178.0	8.4	1.09	1.55	0.76	4.0	8.0	Q1
LP3987ITLX-2.8/NOPB	DSBGA	YZR	5	3000	178.0	8.4	1.09	1.55	0.76	4.0	8.0	Q1
LP3987ITLX-2.85/NOPB	DSBGA	YZR	5	3000	178.0	8.4	1.09	1.55	0.76	4.0	8.0	Q1
LP3987ITLX-3.0/NOPB	DSBGA	YZR	5	3000	178.0	8.4	1.09	1.55	0.76	4.0	8.0	Q1

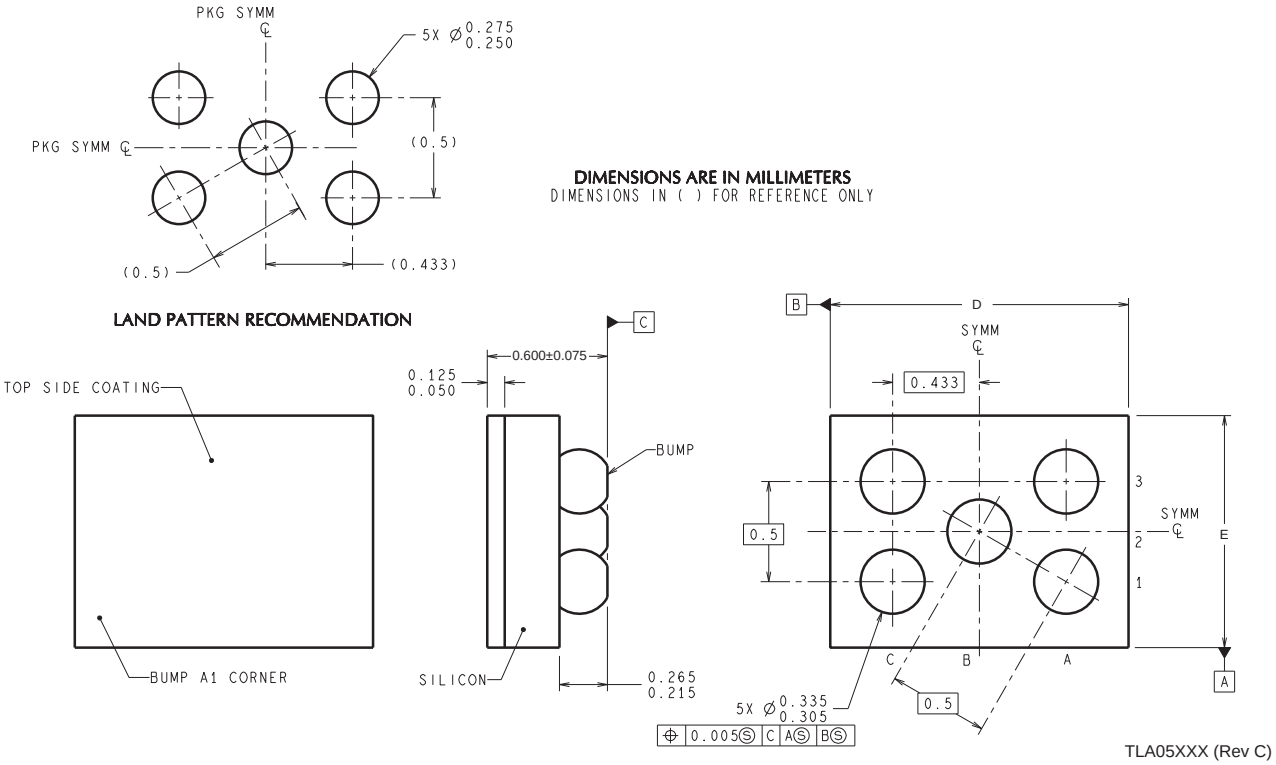
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
LP3987ITL-2.5/NOPB	DSBGA	YZR	5	250	210.0	185.0	35.0
LP3987ITL-2.6/NOPB	DSBGA	YZR	5	250	210.0	185.0	35.0
LP3987ITL-2.8/NOPB	DSBGA	YZR	5	250	210.0	185.0	35.0
LP3987ITL-2.85/NOPB	DSBGA	YZR	5	250	210.0	185.0	35.0
LP3987ITL-3.0/NOPB	DSBGA	YZR	5	250	210.0	185.0	35.0
LP3987ITLX-2.5/NOPB	DSBGA	YZR	5	3000	210.0	185.0	35.0
LP3987ITLX-2.6/NOPB	DSBGA	YZR	5	3000	210.0	185.0	35.0
LP3987ITLX-2.8/NOPB	DSBGA	YZR	5	3000	210.0	185.0	35.0
LP3987ITLX-2.85/NOPB	DSBGA	YZR	5	3000	210.0	185.0	35.0
LP3987ITLX-3.0/NOPB	DSBGA	YZR	5	3000	210.0	185.0	35.0

YZR0005



D: Max = 1.502 mm, Min =1.441 mm

E: Max = 1.045 mm, Min =0.984 mm

4215043/A 12/12

NOTES: A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.
B. This drawing is subject to change without notice.

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