National Semiconductor

June 2006

LP38859
3A Fast-Response High-Accuracy LDO Linear Regulator with Soft-Start

General Description

The LP38859 is a high current, fast response regulator which can maintain output voltage regulation with extremely low input to output voltage drop. Fabricated on a CMOS process, the device operates from two input voltages: V_{BIAS} provides voltage to drive the gate of the N-MOS power transistor, while V_{IN} is the input voltage which supplies power to the load. The use of an external bias rail allows the part to operate from ultra low V_{IN} voltages. Unlike bipolar regulators, the CMOS architecture consumes extremely low quiescent current at any output load current. The use of an N-MOS power transistor results in wide bandwidth, yet minimum external capacitance is required to maintain loop stability.

The fast transient response of this device makes it suitable for use in powering DSP, Microcontroller Core voltages and Switch Mode Power Supply post regulators. The LP38859 is available in TO-220 and TO-263 5-Lead packages.

Dropout Voltage: 240 mV (typical) at 3A load current.

Low Ground Pin Current: 14 mA (typical) at 3A load current.

Soft-Start: Programmable Soft-Start time.

Precision Output Voltage: ±1.0% for T_J = 25˚C and ±2.0% for 0˚C ≤ T_J ≤ +125˚C, across all line and load conditions

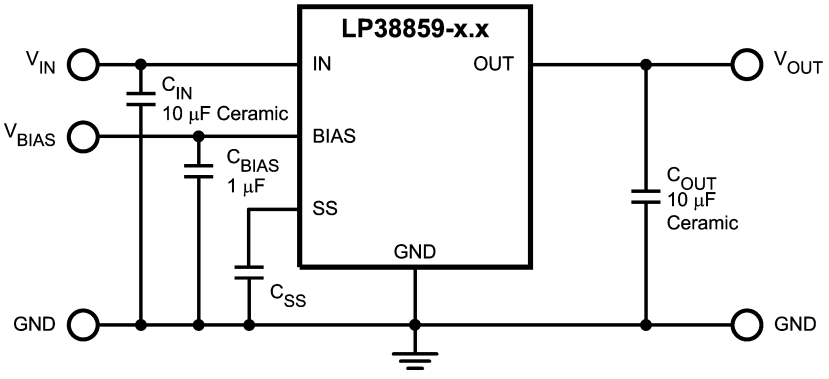
Features

- Standard V_{OUT} values of 0.8V and 1.2V
- Stable with 10µF Ceramic capacitors
- Dropout voltage of 240 mV (typical) at 3A load current
- Precision Output Voltage across all line and load conditions:
  — ±1.0% V_{OUT} for T_J = 25˚C
  — ±2.0% V_{OUT} for 0˚C ≤ T_J ≤ +125˚C
  — ±3.0% V_{OUT} for -40˚C ≤ T_J ≤ +125˚C
- Over-Temperature and Over-Current protection
- Available in 5 lead TO-220 and TO-263 packages
- Custom V_{OUT} values between 0.8V and 1.2V are available
- –40˚C to +125˚C Operating Temperature Range

Applications

- ASIC Power Supplies In:
  - Desktops, Notebooks, and Graphics Cards, Servers
  - Gaming Set Top Boxes, Printers and Copiers
- Server Core and I/O Supplies
- DSP and FPGA Power Supplies
- SMPS Post-Regulator

Typical Application Circuit



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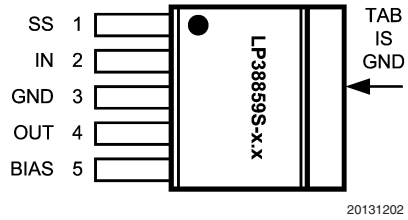
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Ordering Information

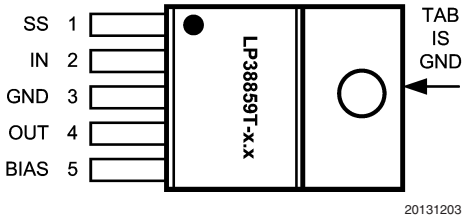
V_{OUT} *	Order Number	Package Type	Package Drawing	Supplied As
0.8V	LP38859S-0.8	TO263-5	TS5B	Rail of 45
	LP38859SX-0.8	TO263-5	TS5B	Tape and Reel of 500
	LP38859T-0.8	TO220-5	T05D	Rail of 45
1.2V	LP38859S-1.2	TO263-5	TS5B	Rail of 45
	LP38859SX-1.2	TO263-5	TS5B	Tape and Reel of 500
	LP38859T-1.2	TO220-5	T05D	Rail of 45

* For custom V_{OUT} values between 0.8V and 1.2V please contact the National Semiconductor Sales Office.

Connection Diagrams



TO263–5, Top View



TO220–5, Top View

Pin Descriptions

TO220–5 and TO263–5 Packages

Pin #	Pin Symbol	Pin Description
1	SS	Soft-Start capacitor connection. Used to slow the rise time of V_{OUT} at turn-on.
2	IN	The unregulated voltage input pin.
3	GND	Ground
4	OUT	The regulated output voltage pin.
5	BIAS	The supply for the internal control and reference circuitry.
TAB	TAB	The TAB is a thermal connection that is physically attached to the backside of the die, and used as a thermal heat-sink connection. See the Application Information section for details.

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

Storage Temperature Range	−65˚C to +150˚C
Lead Temperature	
Soldering, 5 seconds	260˚C
ESD Rating	
Human Body Model (Note 2)	±2 kV
Power Dissipation (Note 3)	Internally Limited
V_{IN} Supply Voltage (Survival)	−0.3V to +6.0V
V_{BIAS} Supply Voltage (Survival)	−0.3V to +6.0V
V_{SS} SoftStart Voltage (Survival)	−0.3V to +6.0V
V_{OUT} Voltage (Survival)	−0.3V to +6.0V
I_{OUT} Current (Survival)	Internally Limited
Junction Temperature	−40˚C to +150˚C

Operating Ratings (Note 1)

V_{IN} Supply Voltage	$(V_{OUT} + V_{DO})$ to V_{BIAS}
V_{BIAS} Supply Voltage	3.0V to 5.5V
I_{OUT}	0 mA to 3.0A
Junction Temperature Range(Note 3)	−40˚C to +125˚C

Electrical Characteristics

Unless otherwise specified: $V_{IN} = V_{OUT(NOM)} + 1V$, $V_{BIAS} = 3.0V$, $I_{OUT} = 10$ mA, $C_{IN} = C_{OUT} = 10$ µF, $C_{BIAS} = 1$ µF, C_{SS} = open. Limits in standard type are for $T_J = 25$˚C only; limits in **boldface type** apply over the junction temperature (T_J) range of -40˚C to +125˚C. Minimum and Maximum limits are guaranteed through test, design, or statistical correlation. Typical values represent the most likely parametric norm at $T_J = 25$˚C, and are provided for reference purposes only.

Symbol	Parameter	Conditions	MIN	TYP	MAX	Units
V_{OUT}	V_{OUT} Accuracy	$V_{OUT(NOM)} + 1V \le V_{IN} \le V_{BIAS}$, $3.0V \le V_{BIAS} \le 5.5V$, $10\text{ mA} \le I_{OUT} \le 3A$	-1.0 **-3.0**	0.0	1.0 **3.0**	%
		$V_{OUT(NOM)} + 1V \le V_{IN} \le V_{BIAS}$, $3.0V \le V_{BIAS} \le 5.5V$, $10\text{ mA} \le I_{OUT} \le 3.0A$, $0˚C \le T_J \le +125˚C$	-2.0	0.0	2.0	
$\Delta V_{OUT}/\Delta V_{IN}$	Line Regulation, V_{IN} (Note 4)	$V_{OUT(NOM)} + 1V \le V_{IN} \le V_{BIAS}$	-	0.04	-	%/V
$\Delta V_{OUT}/\Delta V_{BIAS}$	Line Regulation, V_{BIAS} (Note 4)	$3.0V \le V_{BIAS} \le 5.5V$	-	0.10	-	%/V
$\Delta V_{OUT}/\Delta I_{OUT}$	Output Voltage Load Regulation (Note 5)	$10\text{ mA} \le I_{OUT} \le 3.0A$	-	0.2	-	%/A
V_{DO}	Dropout Voltage (Note 6)	$I_{OUT} = 3.0A$	-	240	300 **450**	mV
$I_{GND(IN)}$	Quiescent Current Drawn from V_{IN} Supply	LP38859-0.8 $10\text{ mA} \le I_{OUT} \le 3.0A$	-	7.0	8.5 **9.0**	mA
		LP38859-1.2 $10\text{ mA} \le I_{OUT} \le 3.0A$		11	12 **15**	
$I_{GND(BIAS)}$	Quiescent Current Drawn from V_{BIAS} Supply	$10\text{ mA} \le I_{OUT} \le 3.0A$	-	3.0	3.8 **4.5**	mA
UVLO	Under-Voltage Lock-Out Threshold	V_{BIAS} rising until device is functional	2.20 **2.00**	2.45	2.70 **2.90**	V
$UVLO_{(HYS)}$	Under-Voltage Lock-Out Hysteresis	V_{BIAS} falling from UVLO threshold until device is non-functional	60 **50**	150	300 **350**	mV
I_{SC}	Output Short-Circuit Current	$V_{IN} = V_{OUT(NOM)} + 1V$, $V_{BIAS} = 3.0V$, $V_{OUT} = 0.0V$	-	6.2	-	A
Soft-Start						
r_{SS}	Soft-Start internal resistance	LP38859-0.8	11.0	13.5	16.0	kΩ
		LP38859-1.2	13.5	16.0	18.5	
t_{SS}	Soft-Start time $t_{SS} = C_{SS} \times r_{SS} \times 5$	LP38859-0.8, $C_{SS} = 10$ nF	-	675	-	µs
		LP38859-1.2, $C_{SS} = 10$ nF	-	800	-	

Electrical Characteristics Unless otherwise specified: $V_{IN} = V_{OUT(NOM)} + 1V$, $V_{BIAS} = 3.0V$, $I_{OUT} = 10$ mA, $C_{IN} = C_{OUT} = 10$ µF, $C_{BIAS} = 1$ µF, C_{SS} = open. Limits in standard type are for $T_J = 25^{\circ}C$ only; limits in **boldface type** apply over the junction temperature (T_J) range of -40˚C to +125˚C. Minimum and Maximum limits are guaranteed through test, design, or statistical correlation. Typical values represent the most likely parametric norm at $T_J = 25^{\circ}C$, and are provided for reference purposes only. (Continued)

Symbol	Parameter	Conditions	MIN	TYP	MAX	Units
AC Parameters						
PSRR (V_{IN})	Ripple Rejection for V_{IN} Input Voltage	$V_{IN} = V_{OUT(NOM)} + 1V$, f = 120 Hz	-	80	-	dB
		$V_{IN} = V_{OUT(NOM)} + 1V$, f = 1 kHz	-	65	-	
PSRR (V_{BIAS})	Ripple Rejection for V_{BIAS} Voltage	$V_{BIAS} = V_{OUT(NOM)} + 3V$, f = 120 Hz	-	58	-	
		$V_{BIAS} = V_{OUT(NOM)} + 3V$, f = 1 kHz	-	58	-	
e_n	Output Noise Density	f = 120 Hz	-	1	-	µV/√Hz
	Output Noise Voltage V_{OUT} = 1.8V	BW = 10 Hz – 100 kHz	-	150	-	µV (rms)
		BW = 300 Hz – 300 kHz	-	90	-	
Thermal Parameters						
T_{SD}	Thermal Shutdown Junction Temperature		-	160	-	˚C
$T_{SD(HYS)}$	Thermal Shutdown Hysteresis		-	10	-	
θ_{J-A}	Thermal Resistance, Junction to Ambient(Note 3)	TO220-5	-	60	-	˚C/W
		TO263-5	-	60	-	
θ_{J-C}	Thermal Resistance, Junction to Case(Note 3)	TO220-5	-	3	-	
		TO263-5	-	3	-	

Note 1: Note 1: Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Operating Ratings indicate conditions for which the device is intended to be functional, but does not guarantee specific performance limits. For guaranteed specifications and conditions, see the Electrical Characteristics.

Note 2: The human body model is a 100 pF capacitor discharged through a 1.5k resistor into each pin. Test method is per JESD22-A114. The HBM rating for device pin 1 (SS) is ±1.5 kV.

Note 3: Device power dissipation must be de-rated based on device power dissipation (P_D), ambient temperature (T_A), and package junction to ambient thermal resistance (θ_{JA}). Additional heat-sinking may be required to ensure that the device junction temperature (T_J) does not exceed the maximum operating rating. See the Application Information section for details.

Note 4: Output voltage line regulation is defined as the change in output voltage from nominal value resulting from a change in input voltage.

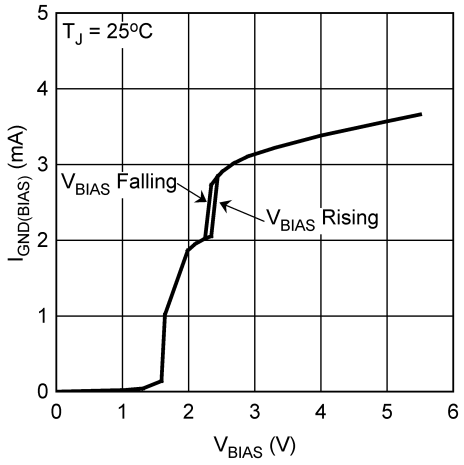
Note 5: Output voltage load regulation is defined as the change in output voltage from nominal value as the load current increases from no load to full load.

Note 6: Dropout voltage is defined the as input to output voltage differential ($V_{IN} - V_{OUT}$) where the input voltage is low enough to cause the output voltage to drop no more than 2% from the nominal value.

Typical Performance Characteristics

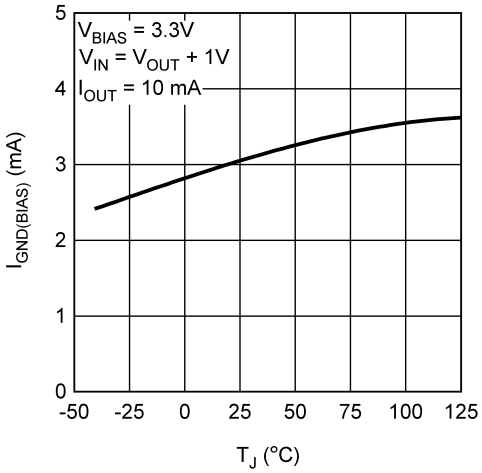
Unless otherwise specified: T_J = 25˚C, V_{IN} = $V_{OUT(NOM)}$ + 1V, V_{BIAS} = 3.0V, I_{OUT} = 10 mA, C_{IN} = C_{OUT} = 10 µF Ceramic, C_{BIAS} = 1 µF Ceramic, C_{SS} = open.

V_{BIAS} Ground Pin Current ($I_{GND(BIAS)}$) vs V_{BIAS}



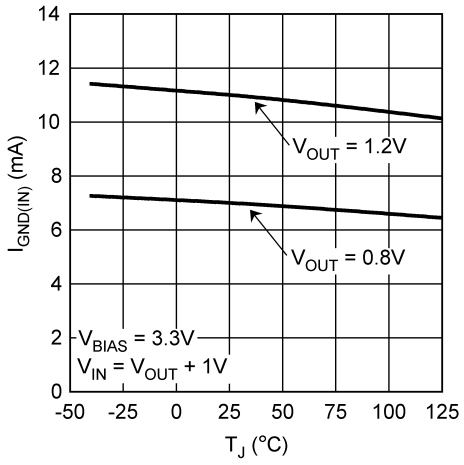
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V_{BIAS} Ground Pin Current ($I_{GND(BIAS)}$) vs Temperature



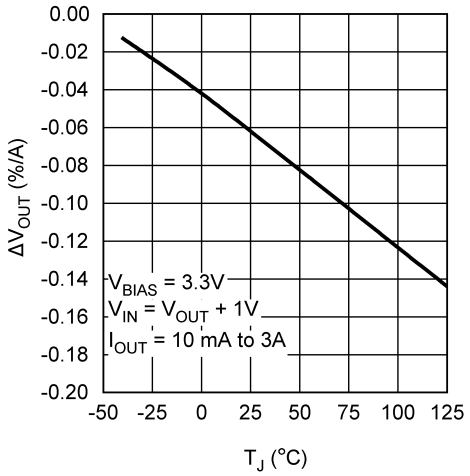
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V_{IN} Ground Pin Current vs Temperature



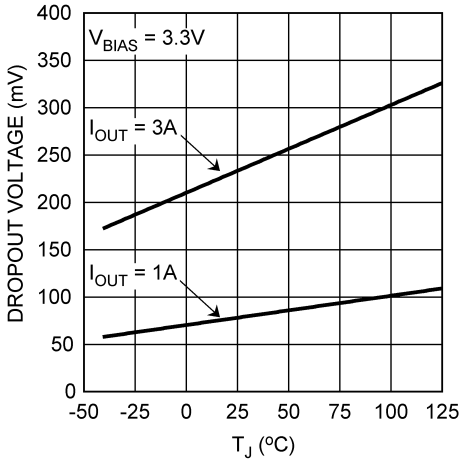
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Load Regulation vs Temperature



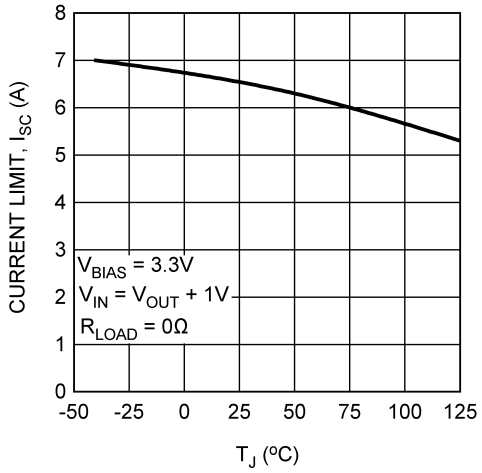
20131263

Dropout Voltage (V_{DO}) vs Temperature



20131265

Output Current Limit (I_{SC}) vs Temperature

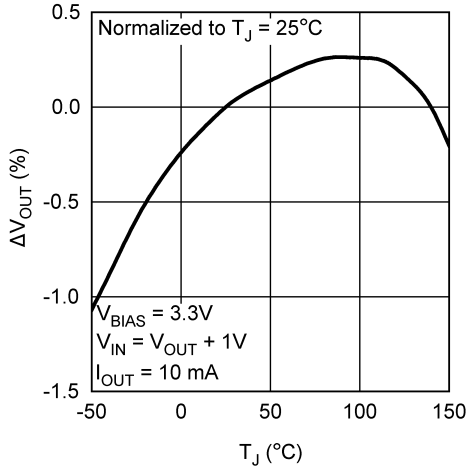


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Typical Performance Characteristics

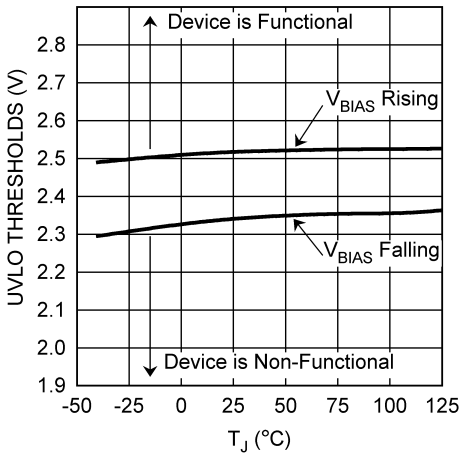
Unless otherwise specified: T_J = 25˚C, V_{IN} = $V_{OUT(NOM)}$ + 1V, V_{BIAS} = 3.0V, I_{OUT} = 10 mA, C_{IN} = C_{OUT} = 10 µF Ceramic, C_{BIAS} = 1 µF Ceramic, C_{SS} = open. (Continued)

V_{OUT} vs Temperature



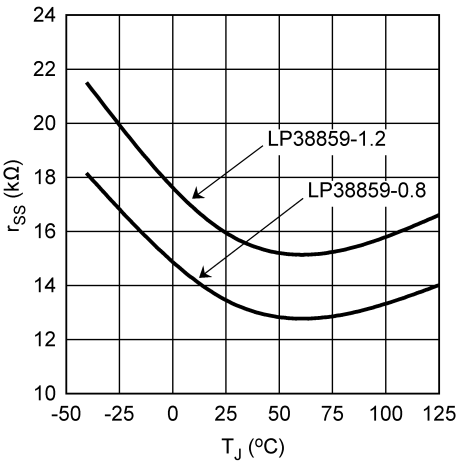
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UVLO Thresholds vs Temperature



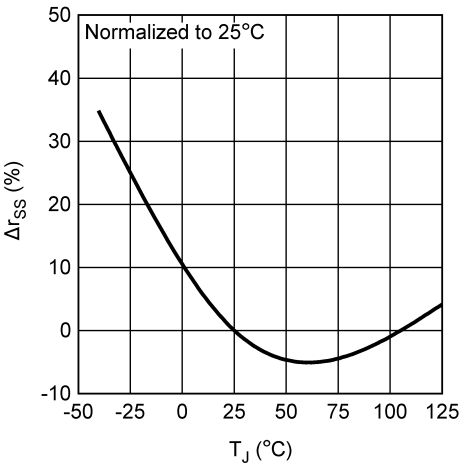
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Soft-Start Resistor (r_{SS}) vs Temperature



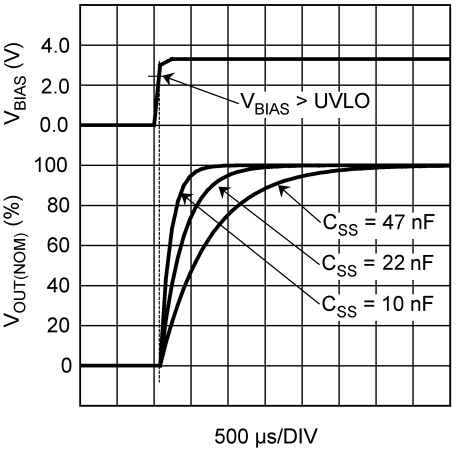
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Soft-Start r_{SS} Variation vs Temperature



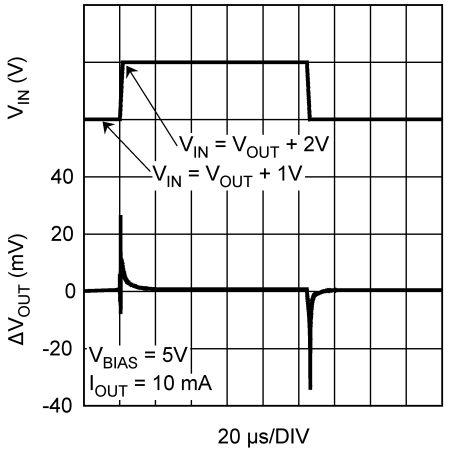
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V_{OUT} vs C_{SS}, 10 nF to 47 nF



20131276

V_{IN} Line Transient Response

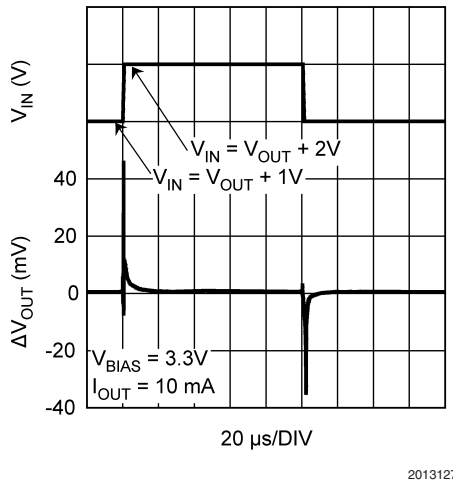


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Typical Performance Characteristics

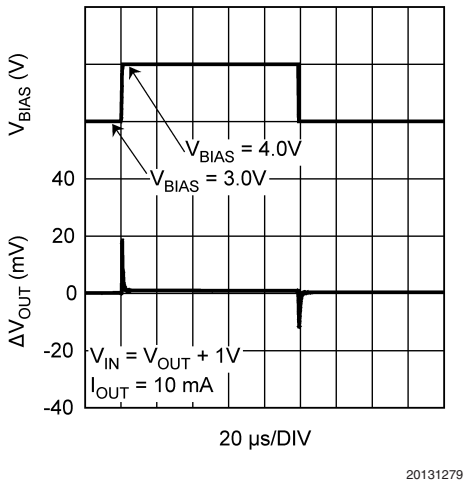
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V_{IN} Line Transient Response



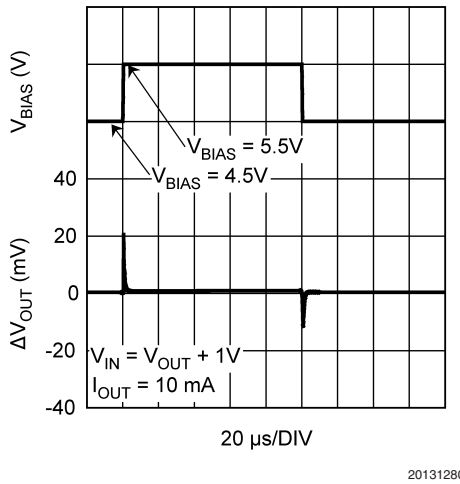
20131278

V_{BIAS} Line Transient Response



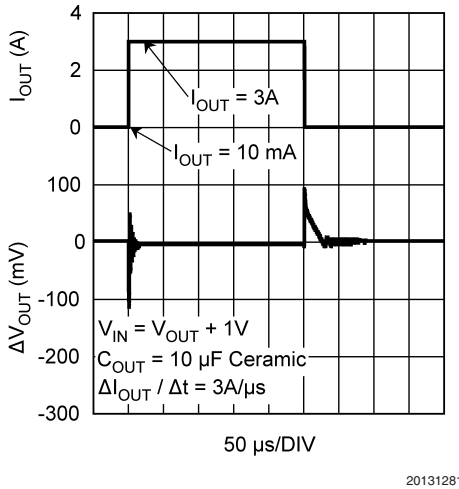
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V_{BIAS} Line Transient Response



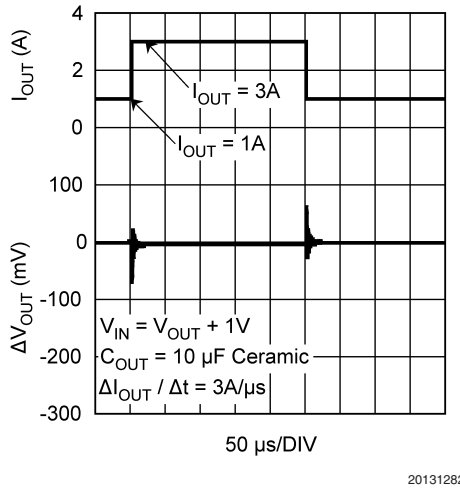
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Load Transient Response, C_{OUT} = 10 µF Ceramic



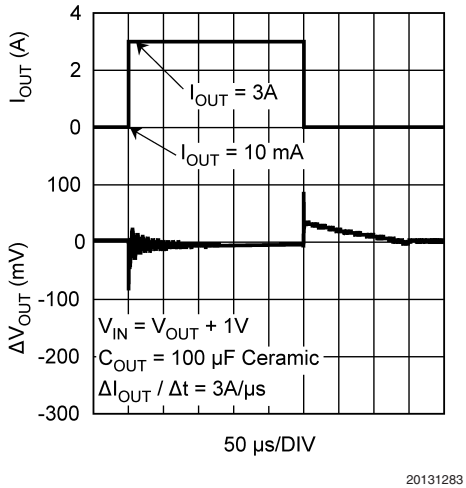
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Load Transient Response, C_{OUT} = 10 µF Ceramic



20131282

Load Transient Response, C_{OUT} = 100 µF Ceramic

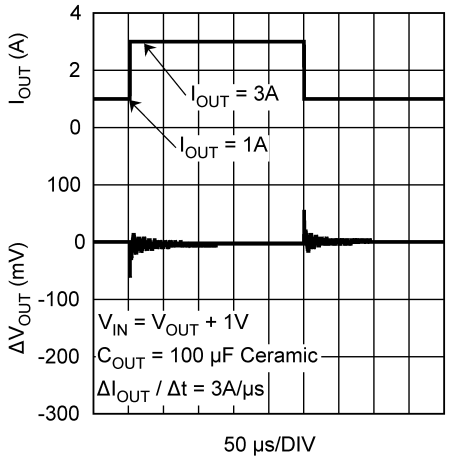


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Typical Performance Characteristics

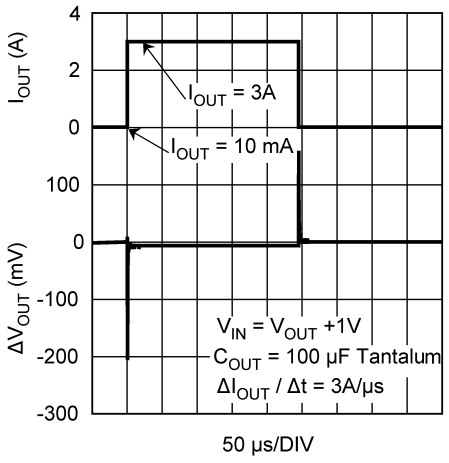
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Load Transient Response, C_{OUT} = 100 µF Ceramic



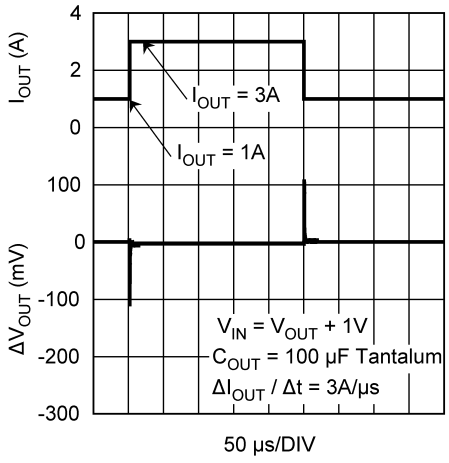
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Load Transient Response, C_{OUT} = 100 µF Tantalum



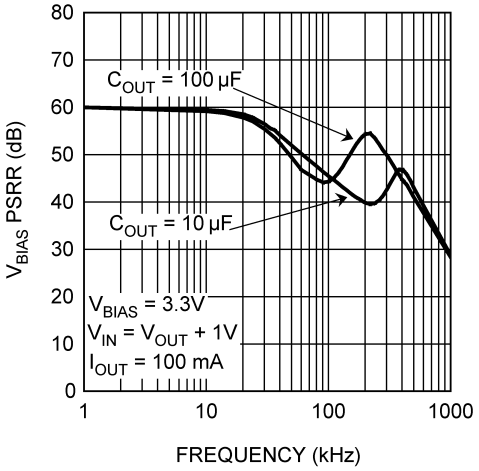
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Load Transient Response, C_{OUT} = 100 µF Tantalum



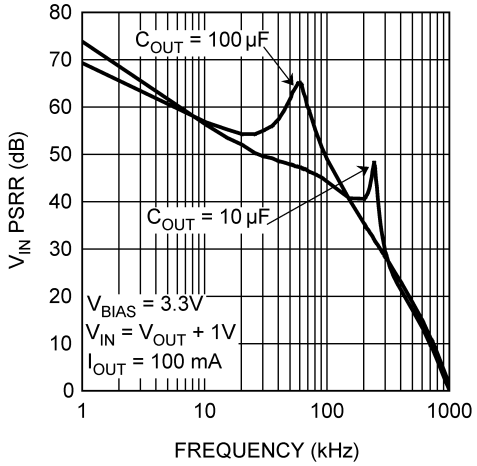
20131286

V_{BIAS} PSRR



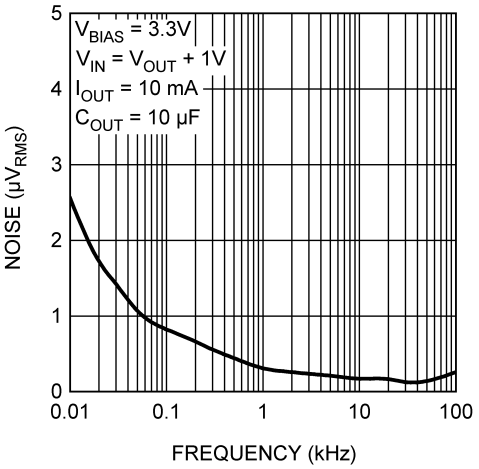
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V_{IN} PSRR



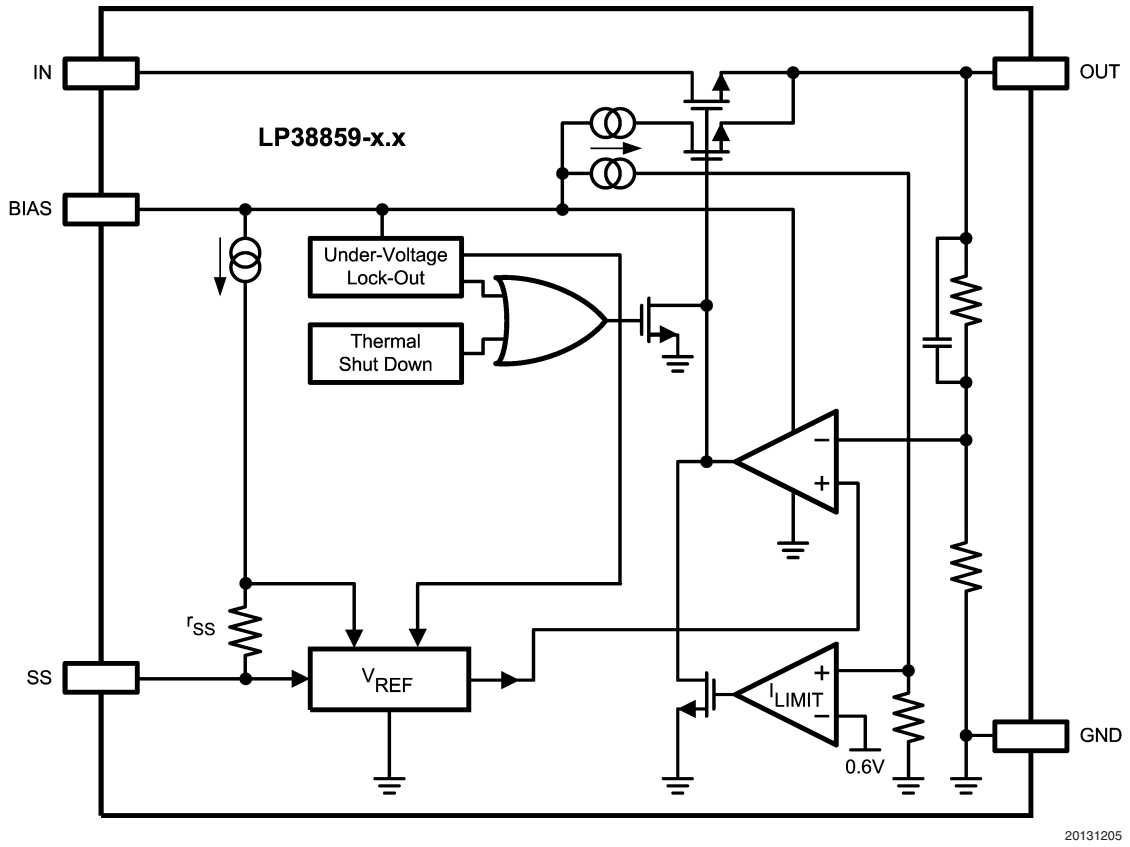
20131271

Output Noise



20131269

Block Diagram



Application Information

EXTERNAL CAPACITORS

To assure regulator stability, input and output capacitors are required as shown in the Typical Application Circuit.

Output Capacitor

A minimum output capacitance of 10 µF, ceramic, is required for stability. The amount of output capacitance can be increased without limit. The output capacitor must be located less than 1 cm from the output pin of the IC and returned to the device ground pin with a clean analog ground.

Only high quality ceramic types such as X5R or X7R should be used, as the Z5U and Y5F types do not provide sufficient capacitance over temperature.

Tantalum capacitors will also provide stable operation across the entire operating temperature range. However, the effects of ESR may provide variations in the output voltage during fast load transients. Using the minimum recommended 10 µF ceramic capacitor at the output will allow unlimited capacitance, Tantalum and/or Aluminum, to be added in parallel.

Input Capacitor

The input capacitor must be at least 10 µF, but can be increased without limit. It's purpose is to provide a low source impedance for the regulator input. A ceramic capacitor, X5R or X7R, is recommended.

Tantalum capacitors may also be used at the input pin. There is no specific ESR limitation on the input capacitor (the lower, the better).

Aluminum electrolytic capacitors can be used, but are not recommended as their ESR increases very quickly at cold temperatures. They are not recommended for any application where the ambient temperature falls below 0˚C.

Bias Capacitor

The capacitor on the bias pin must be at least 1 µF, and can be any good quality capacitor (ceramic is recommended).

INPUT VOLTAGE

The input voltage (V_{IN}) is the high current external voltage rail that will be regulated down to a lower voltage, which is applied to the load. The input voltage must be at least V_{OUT} + V_{DO}, and no higher than whatever values is used for V_{BIAS}.

BIAS VOLTAGE

The bias voltage (V_{BIAS}) is a low current external voltage rail required to bias the control circuitry and provide gate drive for the N-FET pass transistor. The bias voltage must be in the range of 3.0V to 5.5V to ensure proper operation of the device.

UNDER VOLTAGE LOCKOUT

The bias voltage is monitored by a circuit which prevents the device from functioning when the bias voltage is below the Under-Voltage Lock-Out (UVLO) threshold of approximately 2.45V.

As the bias voltage rises above the UVLO threshold the device control circuitry becomes active. There is approximately 150 mV of hysteresis built into the UVLO threshold to provide noise immunity.

When the bias voltage is between the UVLO threshold and the Minimum Operating Rating value of 3.0V the device will be functional, but the operating parameters will not be within the guaranteed limits.

SUPPLY SEQUENCING

There is no requirement for the order that V_{IN} or V_{BIAS} are applied or removed.

One practical limitation is that the Soft-Start circuit starts charging C_{SS} when V_{BIAS} rises above the UVLO threshold. If the application of V_{IN} is delayed beyond this point the benefits of Soft-Start will be compromised.

In any case, the output voltage cannot be guaranteed until both V_{IN} and V_{BIAS} are within the range of guaranteed operating values.

If used in a dual-supply system where the regulator output load is returned to a negative supply, the output pin must be diode clamped to ground. A Schottky diode is recommended for this diode clamp.

REVERSE VOLTAGE

A reverse voltage condition will exist when the voltage at the output pin is higher than the voltage at the input pin. Typically this will happen when V_{IN} is abruptly taken low and C_{OUT} continues to hold a sufficient charge such that the input to output voltage becomes reversed.

The NMOS pass element, by design, contains no body diode. This means that, as long as the gate of the pass element is not driven, there will not be any reverse current flow through the pass element during a reverse voltage event. The gate of the pass element is not driven when V_{BIAS} is below the UVLO threshold.

When V_{BIAS} is above the UVLO threshold the control circuitry is active and will attempt to regulate the output voltage. Since the input voltage is less than the output voltage the control circuit will drive the gate of the pass element to the full V_{BIAS} potential when the output voltage begins to fall. In this condition, reverse current will flow from the output pin to the input pin , limited only by the $R_{DS(ON)}$ of the pass element and the output to input voltage differential. This condition is outside the guaranteed operating range and should be avoided.

SOFT-START

The LP38859 incorporates a Soft-Start function that reduces the start-up current surge into the output capacitor (C_{OUT}) by allowing V_{OUT} to rise slowly to the final value. This is accomplished by controlling V_{REF} at the SS pin. The soft-start timing capacitor (C_{SS}) is internally held to ground until V_{BIAS} rises above the Under-Voltage Lock-Out threshold (ULVO).

V_{REF} will rise at an RC rate defined by the internal resistance of the SS pin (r_{SS}), and the external capacitor connected to the SS pin. This allows the output voltage to rise in a controlled manner until steady-state regulation is achieved. Typically, five time constants are recommended to assure that the output voltage is sufficiently close to the final steady-state value. During the soft-start time the output current can rise to the built-in current limit.

$$\text{Soft-Start Time} = C_{SS} \times r_{SS} \times 5 \quad (1)$$

Application Information (Continued)

Since the V_{OUT} rise will be exponential, not linear, the in-rush current will peak during the first time constant (τ), and V_{OUT} will require four additional time constants (4τ) to reach the final value (5τ) .

After achieving normal operation, should V_{BIAS} fall below the ULVO threshold the device output will be disabled and the Soft-Start capacitor (C_{SS}) discharge circuit will become active. The C_{SS} discharge circuit will remain active until V_{BIAS} falls to 500 mV (typical). When V_{BIAS} falls below 500 mV (typical), the C_{SS} discharge circuit will cease to function due to a lack of sufficient biasing to the control circuitry.

Since V_{REF} appears on the SS pin, any leakage through C_{SS} will cause V_{REF} to fall, and thus affect V_{OUT}. A leakage of 50 nA (about 10 MΩ) through C_{SS} will cause V_{OUT} to be approximately 0.1% lower than nominal, while a leakage of 500 nA (about 1 MΩ) will cause V_{OUT} to be approximately 1% lower than nominal. Typical ceramic capacitors will have a factor of 10X difference in leakage between 25˚C and 85˚C, so the maximum ambient temperature must be included in the capacitor selection process.

Typical C_{SS} values will be in the range of 1 nF to 100 nF, providing typical Soft-Start times in the range of 70 µs to 7 ms (5τ). Values less than 1 nF can be used, but the Soft-Start effect will be minimal. Values larger than 100 nF will provide soft-start, but may not be fully discharged if V_{BIAS} falls from the UVLVO threshold to less than 500 mV in less than 100 µs.

Figure 1 shows the relationship between the C_{OUT} value and a typical C_{SS} value.

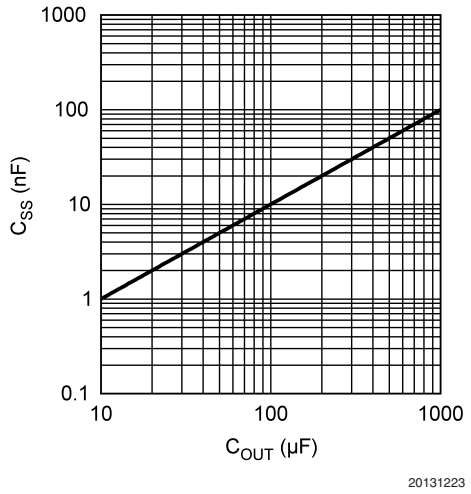


FIGURE 1. Typical C_{SS} vs C_{OUT} Values

The C_{SS} capacitor must be connected to a clean ground path back to the device ground pin. No components, other than C_{SS}, should be connected to the SS pin, as there could be adverse effects to V_{OUT}.

If the Soft-Start function is not needed the SS pin should be left open, although some minimal capacitance value is always recommended.

POWER DISSIPATION AND HEAT-SINKING

Additional copper area for heat-sinking may be required depending on the maximum device dissipation (P_D) and the maximum anticipated ambient temperature (T_A) for the device. Under all possible conditions, the junction temperature must be within the range specified under operating conditions.

The total power dissipation of the device is the sum of three different points of dissipation in the device.

The first part is the power that is dissipated in the NMOS pass element, and can be determined with the formula:

$$P_{D(PASS)} = (V_{IN} - V_{OUT}) \times I_{OUT} \quad (2)$$

The second part is the power that is dissipated in the bias and control circuitry, and can be determined with the formula:

$$P_{D(BIAS)} = V_{BIAS} \times I_{GND(BIAS)} \quad (3)$$

where $I_{GND(BIAS)}$ is the portion of the operating ground current of the device that is related to V_{BIAS}.

The third part is the power that is dissipated in portions of the output stage circuitry, and can be determined with the formula:

$$P_{D(IN)} = V_{IN} \times I_{GND(IN)} \quad (4)$$

where $I_{GND(IN)}$ is the portion of the operating ground current of the device that is related to V_{IN}.

The total power dissipation is then:

$$P_D = P_{D(PASS)} + P_{D(BIAS)} + P_{D(IN)} \quad (5)$$

The maximum allowable junction temperature rise (ΔT_J) depends on the maximum anticipated ambient temperature (T_A) for the application, and the maximum allowable operating junction temperature ($T_{J(MAX)}$) .

$$\Delta T_J = T_{J(MAX)} - T_{A(MAX)} \quad (6)$$

The maximum allowable value for junction to ambient Thermal Resistance, θ_{JA}, can be calculated using the formula:

$$\theta_{JA} \leq \frac{\Delta T_J}{P_D} \quad (7)$$

Heat-Sinking The TO-220 Package

The TO220-5 package has a θ_{JA} rating of 60˚C/W and a θ_{JC} rating of 3˚C/W. These ratings are for the package only, no additional heat-sinking, and with no airflow. If the needed θ_{JA}, as calculated above, is greater than or equal to 60˚C/W then no additional heat-sinking is required since the package can safely dissipate the heat and not exceed the operating $T_{J(MAX)}$. If the needed θ_{JA} is less than 60˚C/W then additional heat-sinking is needed.

The thermal resistance of a TO-220 package can be reduced by attaching it to a heat sink or a copper plane on a PC board. If a copper plane is to be used, the values of θ_{JA} will be same as shown in next section for TO-263 package.

The heat-sink to be used in the application should have a heat-sink to ambient thermal resistance, θ_{HA}:

Application Information (Continued)

$$\theta_{HA} \leq \theta_{JA} - (\theta_{CH} + \theta_{JC}) \quad (8)$$

where θ_{JA} is the required total thermal resistance from the junction to the ambient air, θ_{CH} is the thermal resistance from the case to the surface of the heart-sink, and θ_{JC} is the thermal resistance from the junction to the surface of the case.

For this equation, θ_{JC} is about 3˚C/W for a TO-220 package. The value for θ_{CH} depends on method of attachment, insulator, etc. θ_{CH} varies between 1.5˚C/W to 2.5˚C/W. Consult the heat-sink manufacturer datasheet for details and recommendations.

Heat-Sinking The TO-263 Package

The TO-263 package has a θ_{JA} rating of 60˚C/W, and a θ_{JC} rating of 3˚C/W. These ratings are for the package only, no additional heat-sinking, and with no airflow.

The TO-263 package uses the copper plane on the PCB as a heat-sink. The tab of this package is soldered to the copper plane for heat sinking. shows a curve for the θ_{JA} of TO-263 package for different copper area sizes, using a typical PCB with 1 ounce copper and no solder mask over the copper area for heat-sinking.

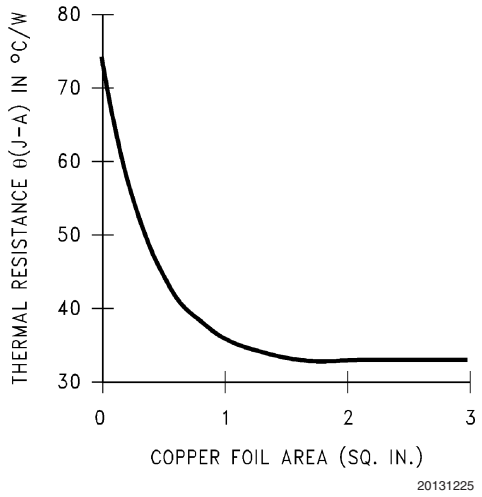


FIGURE 2. θ_{JA} vs Copper (1 Ounce) Area for the TO-263 package

Figure 2 shows that increasing the copper area beyond 1 square inch produces very little improvement. The minimum value for θ_{JA} for the TO-263 package mounted to a PCB is 32˚C/W.

Figure 3 shows the maximum allowable power dissipation for TO-263 packages for different ambient temperatures, assuming θ_{JA} is 35˚C/W and the maximum junction temperature is 125˚C.

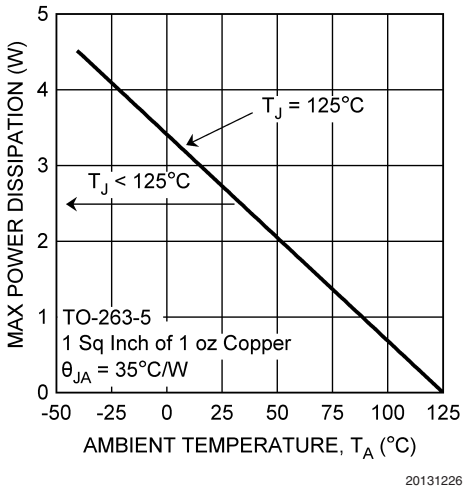
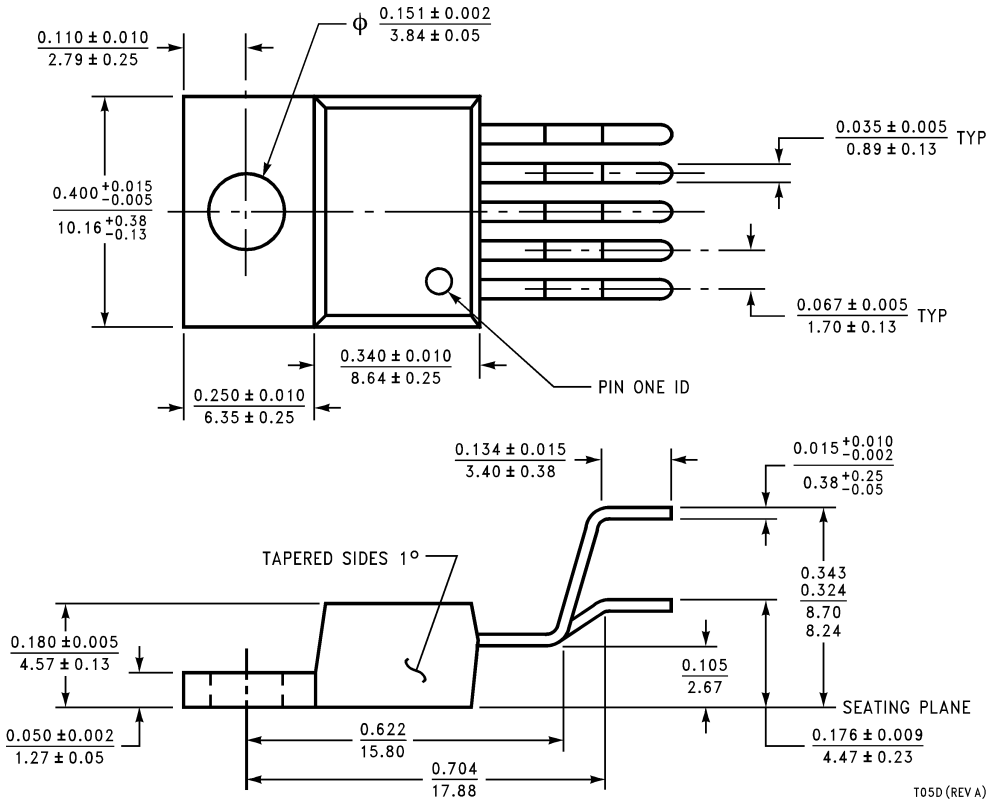
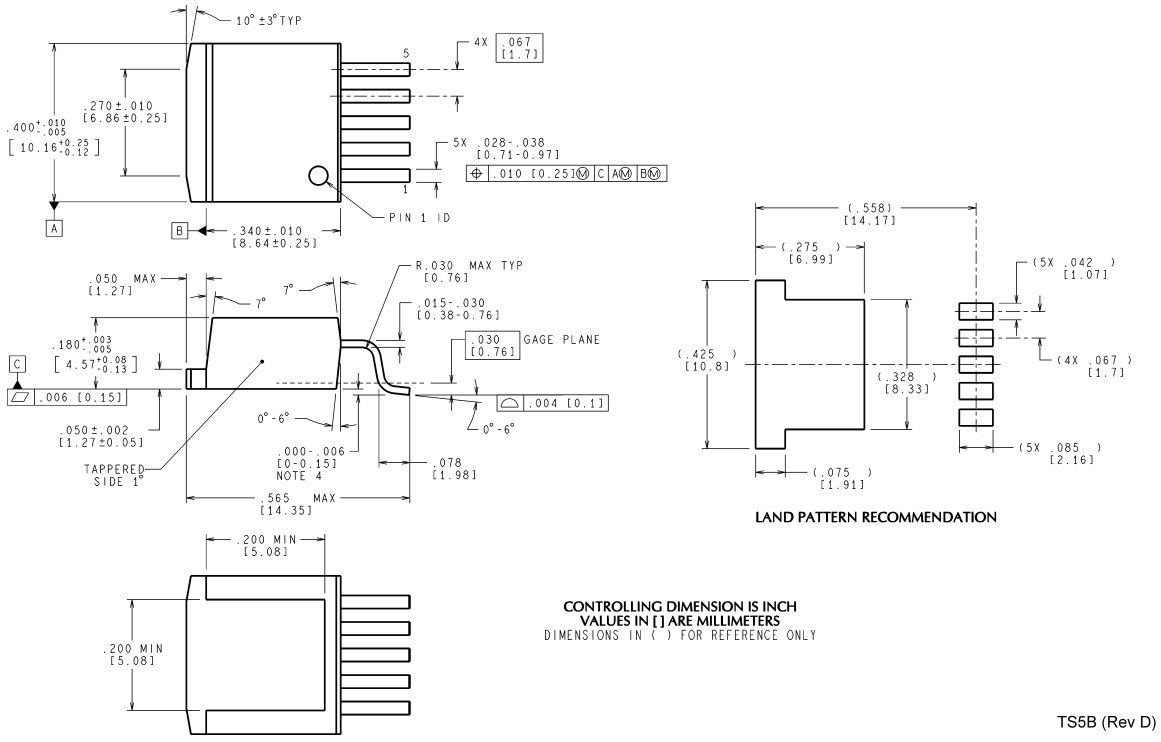


FIGURE 3. Maximum power dissipation vs ambient temperature for the TO-263 package

Physical Dimensions inches (millimeters) unless otherwise noted



TO-220 5-Lead, Stagger Bend Package (TO220-5)
NS Package Number TO5D



TO-263 5-Lead, Molded, Surface Mount Package (TO263-5)
NS Package Number TS5B

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