TEXAS INSTRUMENTS

LP38691-ADJ, LP38693-ADJ, LP38691-ADJ-Q1, LP38693-ADJ-Q1

SNVS324K – JANUARY 2005 – REVISED JANUARY 2016

LP3869x-ADJ/Q1 500-mA Low-Dropout CMOS Linear Regulators Stable With Ceramic Output Capacitors

1 Features

- Wide Input Voltage Range: 2.7 V to 10 V
- All WSON Options are Available as AEC-Q100 Grade 1
- Output Voltage Range: 1.25 V to 9 V
- 2% Adjust (ADJ) Pin Voltage Accuracy (25°C)
- Low Dropout Voltage: 250 mV at 500 mA (Typical, 5-V Out)
- Precision (Trimmed) Bandgap Reference
- Ensured Specs for –40°C to +125°C
- 1-µA Off-State Quiescent Current
- Thermal Overload Protection
- Foldback Current Limiting
- Ground (GND) Pin Current: 55 µA (Typical) at Full Load
- Enable (EN) Pin (LP38693-ADJ)

2 Applications

- Hard Disk Drives
- Notebook Computers
- Battery-Powered Devices
- Portable Instrumentation

3 Description

The LP3869x-ADJ low-dropout CMOS linear regulators provide 2% precision reference voltage, extremely low dropout voltage (250 mV at 500-mA load current, V_{OUT} = 5 V), and excellent AC performance using ultra-low equivalent series resistance (ESR) ceramic output capacitors.

The low thermal resistance of the WSON and SOT-223 packages allow use of the full operating current even in high ambient temperature environments.

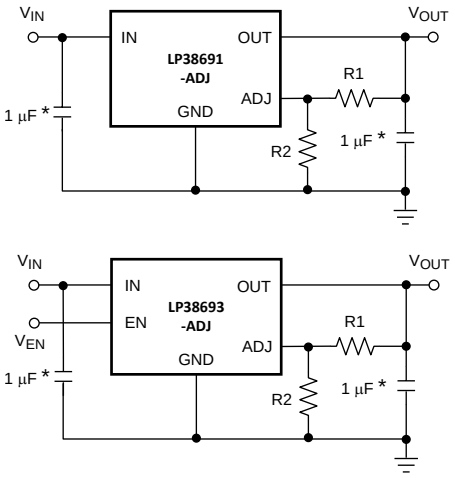
The use of a PMOS power transistor means that no DC base drive current is required to bias it, thus allowing the GND-pin current to remain below 100 µA regardless of load current, input voltage, or operating temperature.

Device Information(1)

PART NUMBER	PACKAGE	BODY SIZE (NOM)
LP38691-ADJ	WSON (6)	3.00 mm × 3.00 mm
LP38693-ADJ	SOT-223 (5)	6.50 mm × 3.56 mm
	WSON (6)	3.00 mm × 3.00 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.

Typical Application Circuits



$V_{OUT} = V_{ADJ} \times (1 + R1/R2)$

* Minimum value required for stability

An IMPORTANT NOTICE at the end of this data sheet addresses availability, warranty, changes, use in safety-critical applications, intellectual property matters and other important disclaimers. PRODUCTION DATA.

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4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision J (October 2015) to Revision K	Page
• Added Caution note to *Foldback Current Limiting* subsection	12

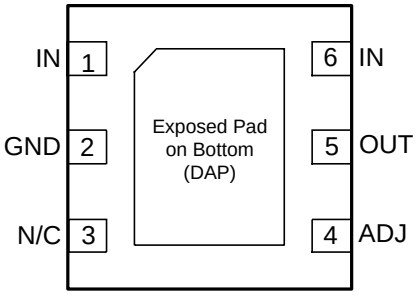
Changes from Revision I (April 2013) to Revision J	Page
• Added *Device Information* and *Pin Configuration and Functions* sections, *ESD Ratings* table, update *Thermal Values; add Feature Description*, *Device Functional Modes*, *Application and Implementation*, *Power Supply Recommendations*, *Layout*, *Device and Documentation Support*, and *Mechanical, Packaging, and Orderable Information* sections; update Vin, Vout and Ven pin names to IN, OUT, and EN in text and graphics; modified wording of *Description* to eliminate redundancy; added top nav icon for reference design.	1

Changes from Revision H (April 2013) to Revision I	Page
• Changed layout of National Data Sheet to TI format	15
• Changed layout of National Data Sheet to TI format	19

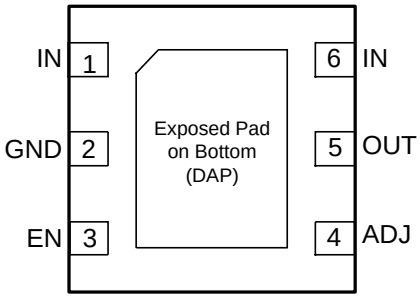
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5 Pin Configuration and Functions

NGG Package
6-Pin WSON With Exposed Thermal Pad
LP38691-ADJ Top View

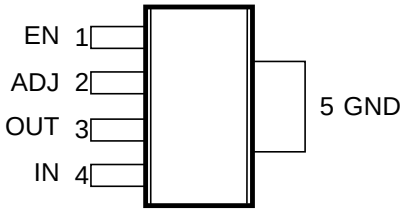


NGG Package
6-Pin WSON With Exposed Thermal Pad
LP38693-ADJ Top View



NC - No internal connection

NDC Package
5-Pin SOT-223
LP38693-ADJ Top View



Pin Functions

PIN				I/O	DESCRIPTION
	LP38691-ADJ	LP38693-ADJ			
NAME	WSON	WSON	SOT-223		
DAP	√	√	—	—	WSON Only - The DAP (exposed pad) functions as a thermal connection when soldered to a copper plane. See *WSON Mounting* section for more information.
EN	—	3	1	I	The EN pin allows the part to be turned to an ON or OFF state by pulling this pin high or low.
GND	2	2	5	—	Circuit ground for the regulator. For the SOT-223 package this is thermally connected to the die and functions as a heat sink when the soldered down to a large copper plane.
IN	1, 6	1, 6	4	I	This is the input supply voltage to the regulator. For WSON devices, both IN pins must be tied together for full current operation (250 mA maximum per pin).
N/C	3	—	—	—	No internal connection.
ADJ	4	4	2	O	The ADJ pin is used to set the regulated output voltage by connecting it to the external resistors R1 and R2 (see *Typical Application Circuits*).
OUT	5	5	3	I	Regulated output voltage.

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6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)(2)

	MIN	MAX	UNIT
$V_{(MAX)}$ All pins (with respect to GND)	–0.3	12	V
I_{OUT}(3)	Internally limited		V
Power dissipation(4)	Internally limited		V
Junction temperature	–40	150	°C
Storage temperature, T_{stg}	−65	150	

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) If Military/Aerospace specified devices are required, contact the Texas Instruments Sales Office/ Distributors for availability and specifications.
(3) If used in a dual-supply system where the regulator load is returned to a negative supply, the OUT pin must be diode clamped to ground.
(4) At elevated temperatures, device power dissipation must be derated based on package thermal resistance and heatsink values (if a heatsink is used). When using the WSON package, refer to *Leadless Leadframe Package (LLP)* (SNOA401) and the *WSON Mounting* section in this data sheet. If power dissipation causes the junction temperature to exceed specified limits, the device will go into thermal shutdown.

6.2 ESD Ratings: LP38691-ADJ, LP38693-ADJ

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	±2000	V

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.

6.3 ESD Ratings: LP38691-ADJ-Q1, LP38693-ADJ-Q1

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per AEC Q100-002(1)	2000	V

(1) AEC Q100-002 indicates that HBM stressing shall be in accordance with the ANSI/ESDA/JEDEC JS-001 specification.

6.4 Recommended Operating Conditions

	MIN	NOM	MAX	UNIT
V_{IN} supply voltage	2.7		10	V
Operating junction temperature	−40		125	°C

6.5 Thermal Information

THERMAL METRIC(1)		LP3869x-ADJ WSON 6 PINS	LP38693-ADJ SOT-223 5 PINS	UNIT
$R_{\theta JA}$(2)	Junction-to-ambient thermal resistance, High-K	50.6	68.5(3)	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	44.4	52.2	
$R_{\theta JB}$	Junction-to-board thermal resistance	24.9	13.0	
ψ_{JT}	Junction-to-top characterization parameter	0.4	5.5	
ψ_{JB}	Junction-to-board characterization parameter	25.1	12.8	
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	5.4	n/a	

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report, SPRA953.
(2) Thermal resistance value $R_{\theta JA}$ is based on the EIA/JEDEC High-K printed circuit board defined by: JESD51-7 - *High Effective Thermal Conductivity Test Board for Leaded Surface Mount Packages.*
(3) The PCB for the WSON (NGN) package $R_{\theta JA}$ includes thermal vias under the exposed thermal pad per EIA/JEDEC JESD51-5.

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6.6 Electrical Characteristics

Unless otherwise specified, limits apply for T_J = 25°C, V_{IN} = V_{OUT} + 1 V, C_{IN} = C_{OUT} = 10 µF, I_{LOAD} = 10 mA. Minimum and maximum limits are specified through testing, statistical correlation, or design.

PARAMETER		TEST CONDITIONS		MIN	TYP(1)	MAX	UNIT
V_{ADJ}	ADJ pin voltage	V_{IN} = 2.7 V		1.225	1.25	1.275	V
		3.2 V ≤ V_{IN} ≤ 10 V, 100 µA < I_L < 0.5 A			1.25		
		3.2 V ≤ V_{IN} ≤ 10 V, 100 µA < I_L < 0.5 A Full operating temperature range		1.2		1.3	
$\Delta V_{OUT}/\Delta V_{IN}$	Output voltage line regulation(2)	V_{OUT} + 0.5 V ≤ V_{IN} ≤ 10 V I_L = 25 mA			0.03		%/V
		V_{OUT} + 0.5 V ≤ V_{IN} ≤ 10 V I_L = 25 mA Full operating temperature range				0.1	
$\Delta V_{OUT}/\Delta I_L$	Output voltage load regulation(3)	1 mA < I_L < 0.5 A V_{IN} = V_{OUT} + 1 V			1.8		%/A
		1 mA < I_L < 0.5 A V_{IN} = V_{OUT} + 1 V Full operating temperature range				5	
V_{DO}	Dropout voltage(4)	(V_{OUT} = 2.5 V)	I_L = 0.1 A		80		mV
			I_L = 0.5 A		430		
		(V_{OUT} = 2.5 V) Full operating temperature range	I_L = 0.1 A			145	
			I_L = 0.5 A			725	
		(V_{OUT} = 3.3 V)	I_L = 0.1 A		65		
			I_L = 0.5 A		330		
		(V_{OUT} = 3.3 V) Full operating temperature range	I_L = 0.1 A			110	
			I_L = 0.5 A			550	
		(V_{OUT} = 5 V)	I_L = 0.1 A		45		
			I_L = 0.5 A		250		
		(V_{OUT} = 5 V) Full operating temperature range	I_L = 0.1 A			100	
			I_L = 0.5 A			450	
I_Q	Quiescent current	V_{IN} ≤ 10 V, I_L =100 µA – 0.5 A			55		µA
		V_{IN} ≤ 10 V, I_L =100 µA – 0.5 A Full operating temperature range				100	
		V_{EN} ≤ 0.4 V, (LP38693 Only)			0.001	1	
$I_{L(MIN)}$	Minimum load current	V_{IN} – V_{OUT} ≤ 4 V Full operating temperature range				100	
I_{FB}	Foldback current limit	V_{IN} – V_{OUT} > 5 V			350		mA
		V_{IN} – V_{OUT} < 4 V			850		
PSRR	Ripple rejection	V_{IN} = V_{OUT} + 2 V(DC), with 1 V(p-p) / 120-Hz Ripple			55		dB
T_{SD}	Thermal shutdown activation (junction temp)				160		°C
T_{SD} (HYST)	Thermal shutdown hysteresis (junction temp)				10		
I_{ADJ}	ADJ input leakage current	V_{ADJ} = 0 V to 1.5 V, V_{IN} = 10 V		–100	0.01	100	nA
e_n	Output noise	BW = 10 Hz to 10 kHz V_{OUT} = 3.3 V			0.7		µV/√Hz
V_{OUT} (LEAK)	Output leakage current	V_{OUT} = $V_{OUT(NOM)}$ + 1 V at 10 V_{IN}			0.5	2	µA

(1) Typical numbers represent the most likely parametric norm for 25°C operation.
(2) Output voltage line regulation is defined as the change in output voltage from nominal value resulting from a change in input voltage.
(3) Output voltage load regulation is defined as the change in output voltage from nominal value as the load current increases from 1 mA to full load.
(4) Dropout voltage is defined as the minimum input to output differential required to maintain the output within 100 mV of nominal value.

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Electrical Characteristics (continued)

Unless otherwise specified, limits apply for T_J = 25°C, V_{IN} = V_{OUT} + 1 V, C_{IN} = C_{OUT} = 10 µF, I_{LOAD} = 10 mA. Minimum and maximum limits are specified through testing, statistical correlation, or design.

PARAMETER		TEST CONDITIONS	MIN	TYP(1)	MAX	UNIT
V_{EN}	Enable voltage (LP38693 Only)	Output = OFF state Full operating temperature range			0.4	V
		Output = ON state, V_{IN} = 4 V Full operating temperature range	1.8			
		Output = ON state, V_{IN} = 6 V Full operating temperature range	3			
		Output = ON state, V_{IN} = 10 V Full operating temperature range	4			
I_{EN}	EN pin leakage (LP38693 only)	V_{EN} = 0 V or 10 V, V_{IN} = 10 V	–1	0.001	1	µA

6.7 Typical Characteristics

Unless otherwise specified: T_J = 25°C, C_{IN} = C_{OUT} = 10 µF, EN pin is tied to IN (LP38693-ADJ only), V_{OUT} = 1.25 V, V_{IN} = V_{OUT} 1 V, I_{LOAD} = 10 mA.

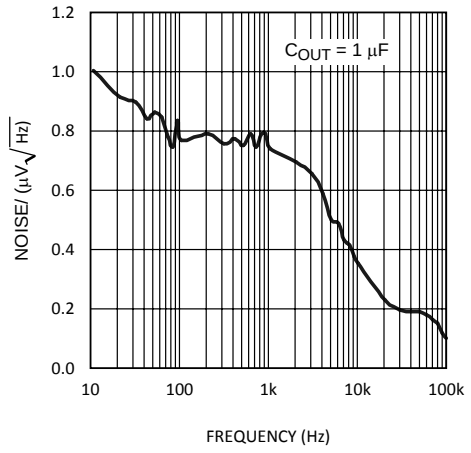


Figure 1. Noise vs Frequency

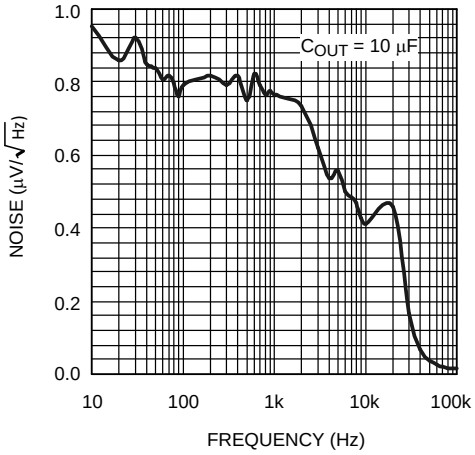


Figure 2. Noise vs Frequency

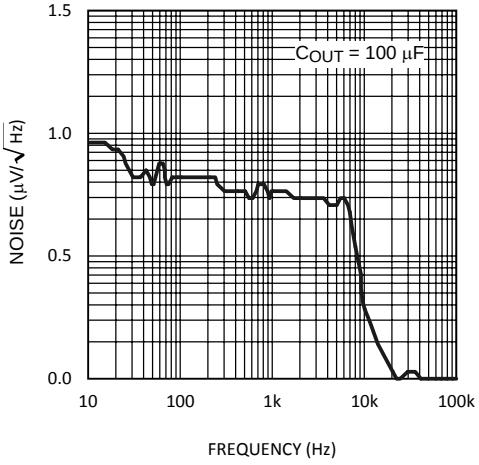


Figure 3. Noise vs Frequency

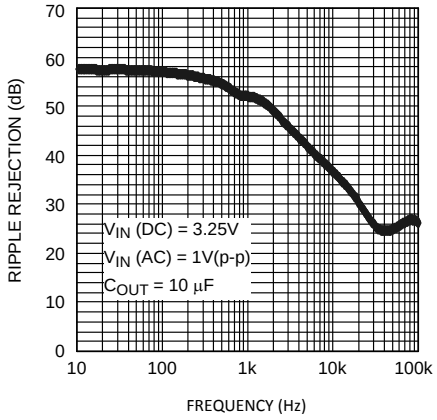


Figure 4. Ripple Rejection

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Typical Characteristics (continued)

Unless otherwise specified: T_J = 25°C, C_{IN} = C_{OUT} = 10 µF, EN pin is tied to IN (LP38693-ADJ only), V_{OUT} = 1.25 V, V_{IN} = V_{OUT} 1 V, I_{LOAD} = 10 mA.

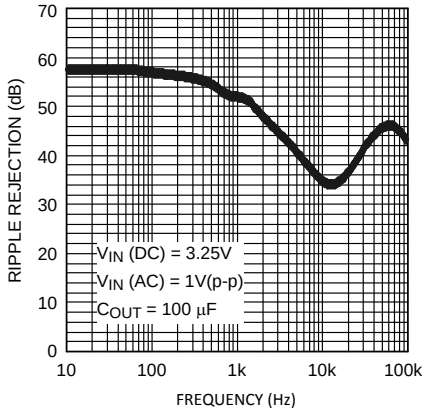


Figure 5. Ripple Rejection

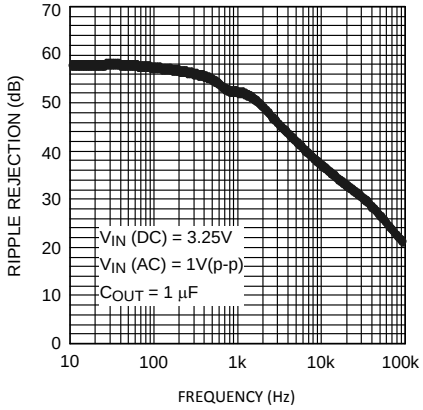


Figure 6. Ripple Rejection

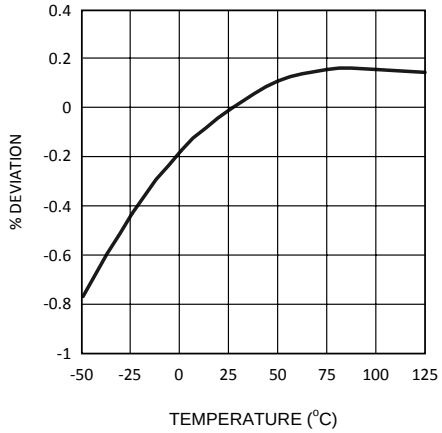


Figure 7. V_{REF} vs Temperature

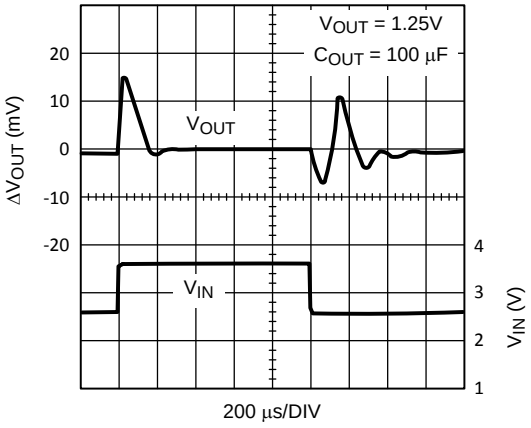


Figure 8. Line Transient Response

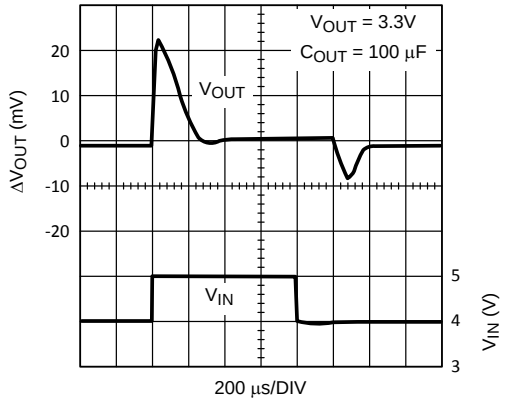


Figure 9. Line Transient Response

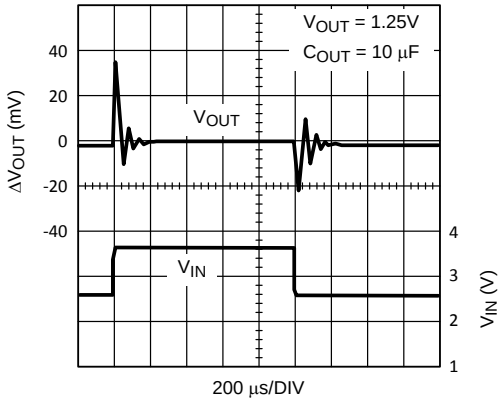


Figure 10. Line Transient Response

Typical Characteristics (continued)

Unless otherwise specified: T_J = 25°C, C_{IN} = C_{OUT} = 10 µF, EN pin is tied to IN (LP38693-ADJ only), V_{OUT} = 1.25 V, V_{IN} = V_{OUT} 1 V, I_{LOAD} = 10 mA.

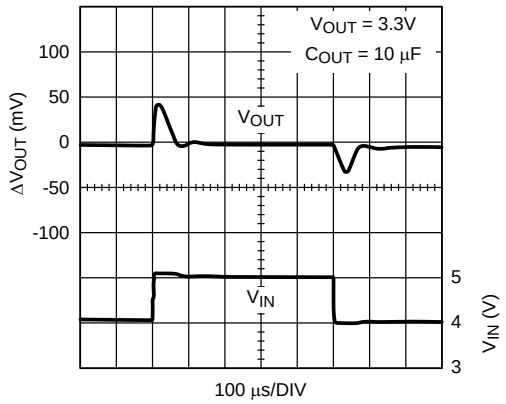


Figure 11. Line Transient Response

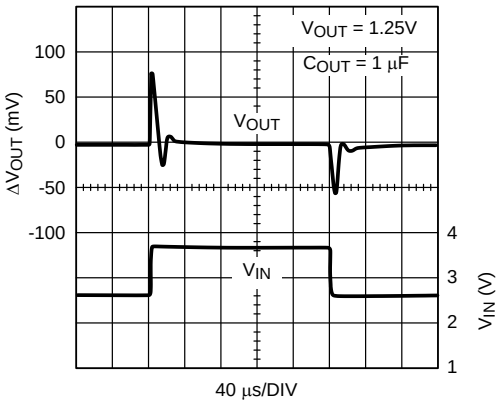


Figure 12. Line Transient Response

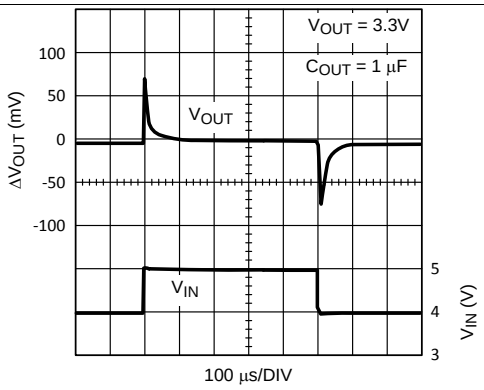


Figure 13. Line Transient Response

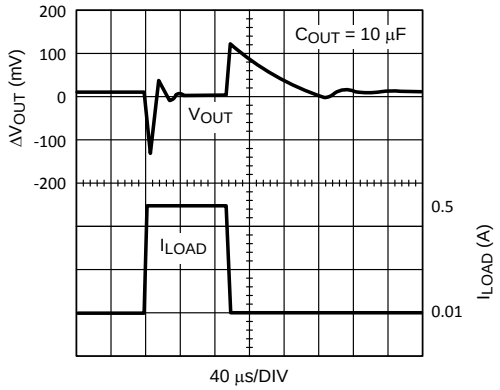


Figure 14. Load Transient Response

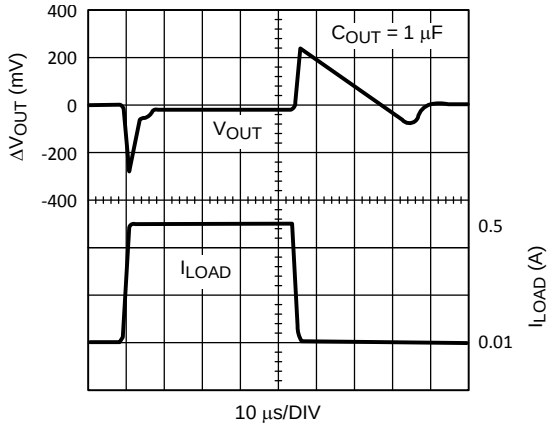


Figure 15. Load Transient Response

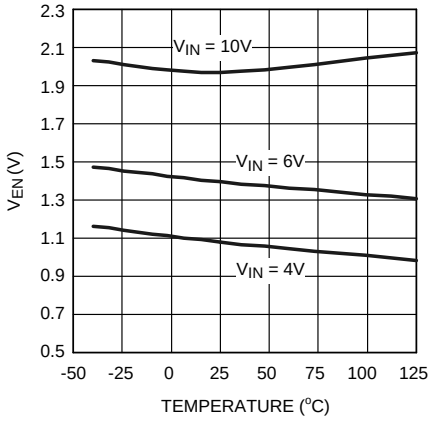


Figure 16. EN Voltage vs Temperature

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Typical Characteristics (continued)

Unless otherwise specified: T_J = 25°C, C_{IN} = C_{OUT} = 10 µF, EN pin is tied to IN (LP38693-ADJ only), V_{OUT} = 1.25 V, V_{IN} = V_{OUT} 1 V, I_{LOAD} = 10 mA.

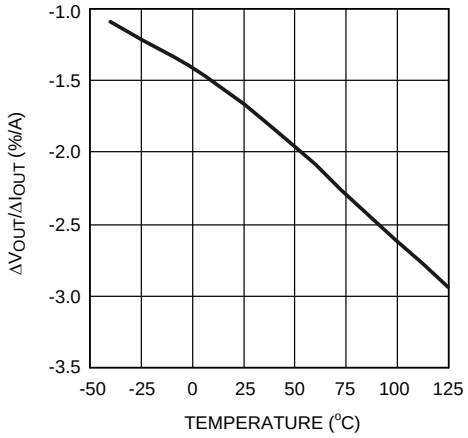


Figure 17. Load Regulation vs Temperature

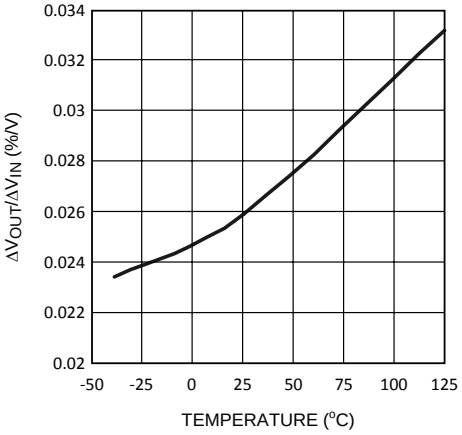
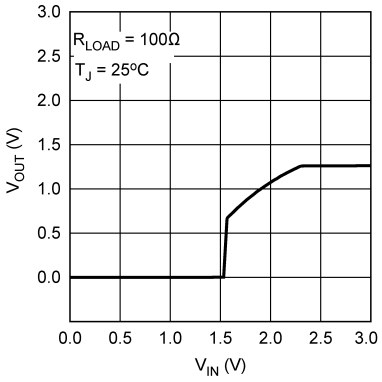
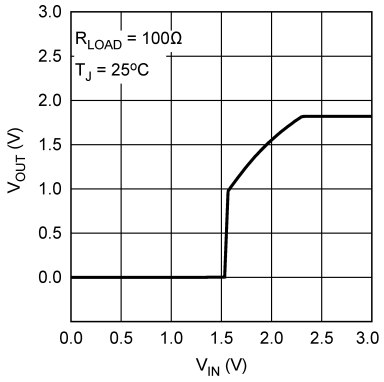


Figure 18. Line Regulation vs Temperature



V_{OUT} = 1.25 V

Figure 19. V_{OUT} vs V_{IN}



V_{OUT} = 1.8 V

Figure 20. V_{OUT} vs V_{IN}

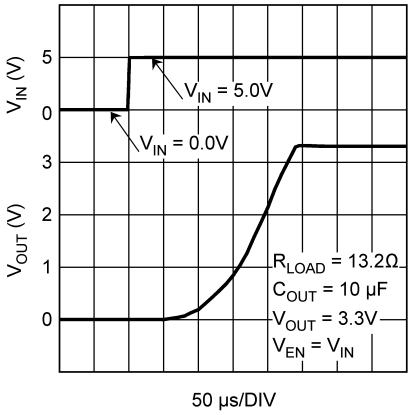


Figure 21. V_{OUT} vs. V_{IN}, Power-up

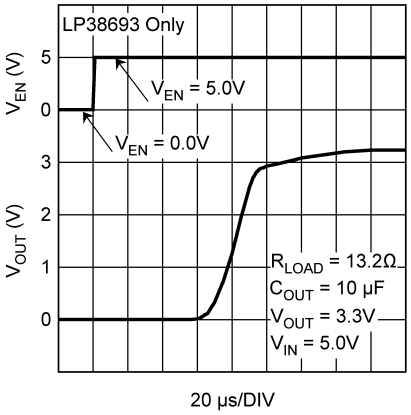


Figure 22. V_{OUT} vs. V_{EN}, On (LP38693-ADJ only)

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Typical Characteristics (continued)

Unless otherwise specified: T_J = 25°C, C_{IN} = C_{OUT} = 10 µF, EN pin is tied to IN (LP38693-ADJ only), V_{OUT} = 1.25 V, V_{IN} = V_{OUT} 1 V, I_{LOAD} = 10 mA.

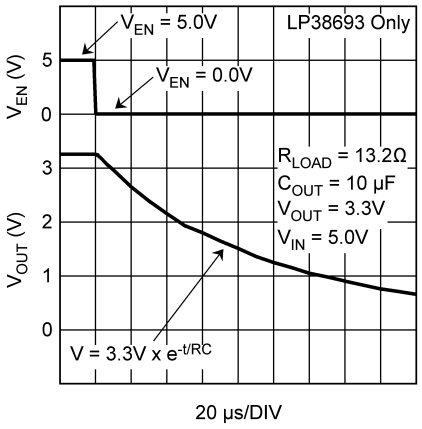


Figure 23. V_{OUT} vs. V_{EN}, Off (LP38693-ADJ only)

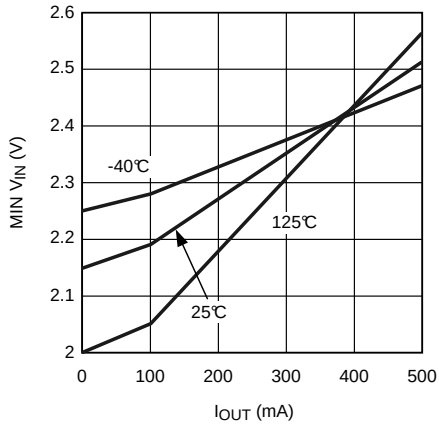
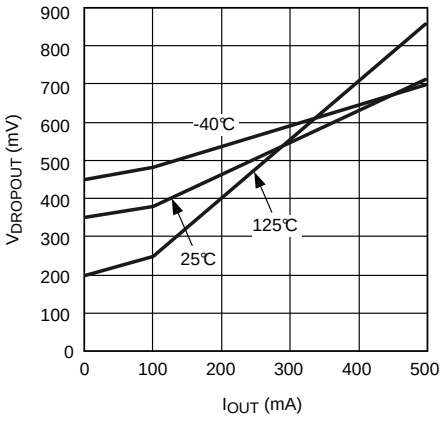


Figure 24. MIN V_{OUT} vs. I_{OUT}



V_{OUT} = 1.8 V

Figure 25. Dropout Voltage vs. I_{OUT}

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7 Detailed Description

7.1 Overview

The LP3869x-ADJ devices are designed to meet the requirements of portable, battery-powered digital systems providing an accurate output voltage with fast start-up. When disabled via a low logic signal at the enable pin (EN), the power consumption is reduced to virtually zero (LP38693-ADJ only).

These LP3869x-ADJ devices perform well with a single 1-µF input capacitor and a single 1-µF ceramic output capacitor.

7.2 Functional Block Diagrams

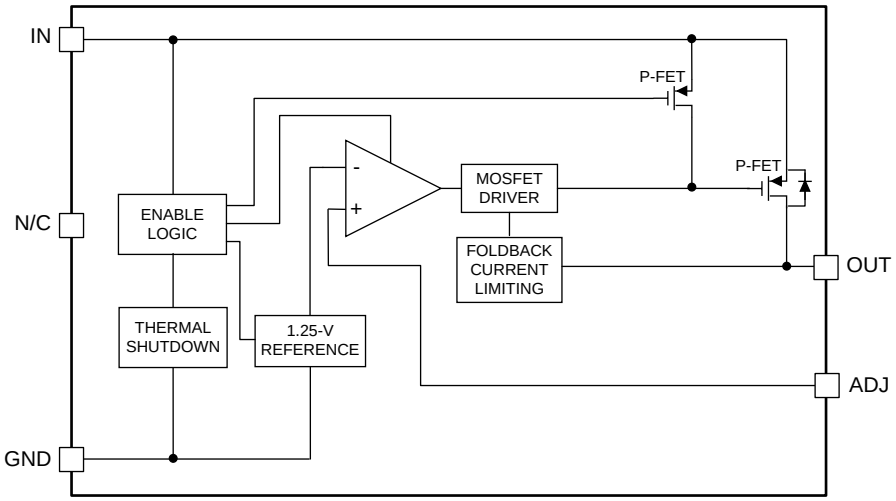


Figure 26. LP38691 Functional Diagram (WSON)

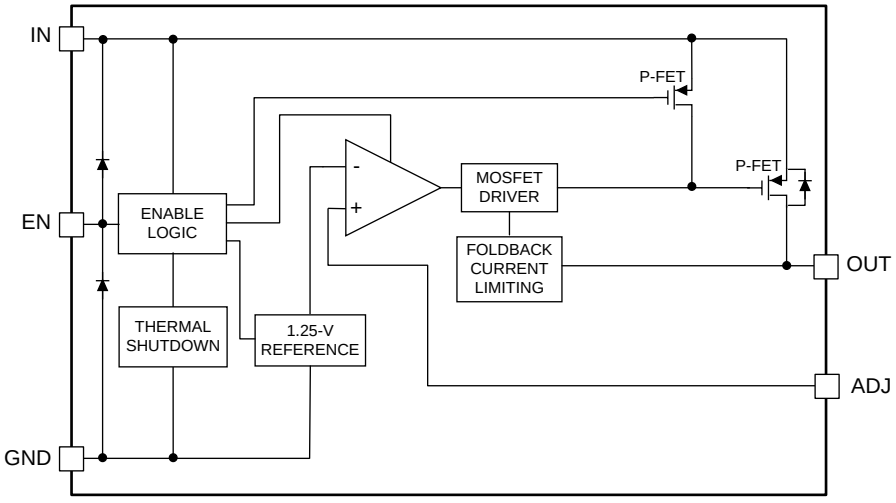


Figure 27. LP38693 Functional Diagram (SOT-223, WSON)

7.3 Feature Description

7.3.1 Enable (EN)

The LP38693-ADJ has an enable pin (EN) which allows an external control signal to turn the regulator output to either an ON or OFF state. The Enable on/off threshold has no hysteresis. The voltage signal must rise and fall cleanly, and promptly, through the on and off voltage thresholds. The EN pin voltage must be higher than the $V_{EN(MIN)}$ threshold to ensure that the device is fully enabled under all operating conditions. The EN pin voltage must be lower than the $V_{EN(MAX)}$ threshold to ensure that the device is fully disabled. The EN pin has no internal pullup or pulldown to establish a default condition and, as a result, this pin must be terminated either actively or passively. If the EN pin is driven from a source that actively pulls high and low, the drive voltage should not be allowed to go below ground potential or higher than V_{IN}. If the application does not require the enable function, the EN pin should be connected directly to the IN pin.

7.3.2 Thermal Overload Protection (T_{SD})

Thermal shutdown disables the output when the junction temperature rises to approximately 160°C which allows the device to cool. When the junction temperature cools to approximately 150°C, the output circuitry enables.

Based on power dissipation, thermal resistance, and ambient temperature, the thermal protection circuit may cycle on and off. This thermal cycling limits the dissipation of the regulator and protects it from damage as a result of overheating. The T_{SD} circuitry of the LP38693 has been designed to protect against temporary thermal overload conditions.

The T_{SD} circuitry was not intended to replace proper heat-sinking. Continuously running the LP38693 device into thermal shutdown degrades device reliability.

7.3.3 Foldback Current Limiting

Foldback current limiting is built into the LP3869x-ADJ devices which reduces the amount of output current the part can deliver as the output voltage is reduced. The amount of load current is dependent on the differential voltage between the V_{IN} and V_{OUT}. Typically, when this differential voltage exceeds 5 V, the load current will limit at about 350 mA. When the $V_{IN} - V_{OUT}$ differential is reduced below 4 V, load current is limited to about 850 mA.

CAUTION

When toggling the LP38693 Enable (EN) after the input voltage (V_{IN}) is applied, the foldback current limit circuitry is functional the first time that the EN pin is taken high. The foldback current limit circuitry is non-functional the second, and subsequent, times that the EN pin is taken high. Depending on the input and output capacitance values the input inrush current may be higher than expected which can cause the input voltage to droop.

If the EN pin is connected to the IN pin, the foldback current limit circuitry is functional when V_{IN} is applied if V_{IN} starts from less than 0.4 V.

7.4 Device Functional Modes

7.4.1 Enable (EN)

The LP38693-ADJ may be switched to the ON or OFF state by logic input at the EN pin. A logic-high voltage on the EN pin turns the device to the ON state. A logic-low voltage on the EN pin turns the device to the OFF state. If the application does not require the shutdown feature, the EN pin must be tied to V_{IN} to keep the regulator output permanently in the ON state when power is applied.

To ensure proper operation, the signal source used to drive the EN input must be able to swing above and below the specified turnon or turnoff voltage thresholds listed in the *Electrical Characteristics* section under V_{EN}.

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8 Application and Implementation

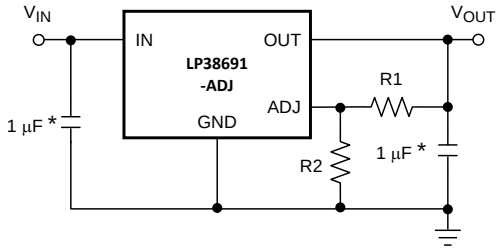
NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

8.1 Application Information

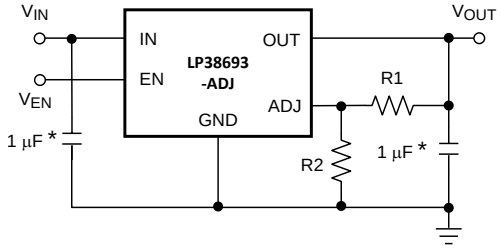
The LP3869x-ADJ can provide 500 mA output current with 2.7 V to 10 V input. Adjustable output voltage in the range of 1.25 V to 9 V. LP3869x-ADJ is stable with a 1-µF ceramic output capacitor. Typical output noise is 0.7 μV_{RMS} at frequencies from 10 Hz to 10 kHz. Typical PSSR is 55 dB at 1 kHz.

8.2 Typical Applications



* Minimum value required for stability

Figure 28. LP38691-ADJ Typical Application



* Minimum value required for stability

Figure 29. LP38693-ADJ Typical Application

8.2.1 Design Requirements

For typical LDO CMOS linear regulators , use the parameters listed in Table 1.

Table 1. Design Parameters

DESIGN PARAMETERS	EXAMPLE VALUE
Input voltage range	2.7 V to 10 V
Output range	Adjustable
Output current	500 mA (maximum)
Output capacitor range	1 µF

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8.2.2 Detailed Design Procedure

8.2.2.1 Setting the Output Voltage

The output voltage is set using the external resistors R1 and R2 (see *Typical Applications* . The output voltage will be given by Equation 1:

$$V_{OUT} = V_{ADJ} \times (1 + (R1 / R2)) \quad (1)$$

Because the part has a minimum load current requirement of 100 µA, it is recommended that R2 always be 12 kΩ or less to provide adequate loading. Even if a minimum load is always provided by other means, it is not recommended that very high value resistors be used for R1 and R2 because it can make the ADJ node susceptible to noise pickup. A maximum Ohmic value of 100 kΩ is recommended for R2 to prevent this from occurring.

8.2.2.2 External Capacitors

In common with most regulators, the LP3869x-ADJ devices require an external capacitors for regulator stability. The devices are specifically designed for portable applications requiring minimum board space and smallest components. These capacitors must be correctly selected for good performance.

8.2.2.3 Input Capacitor

An input capacitor of at least 1 µF is required (ceramic recommended). The capacitor must be located not more than one centimeter from the input pin and returned to a clean analog ground.

8.2.2.4 Output Capacitor

An output capacitor is required for loop stability. It must be located less than 1 centimeter from the device and connected directly to the output and ground pins using traces which have no other currents flowing through them.

The minimum amount of output capacitance that can be used for stable operation is 1 µF. Ceramic capacitors are recommended; the LP3869x-ADJ devices were designed for use with ultra-low equivalent series resistance (ESR) capacitors. The LP3869x-ADJ is stable with any output capacitor ESR between 5 mΩ to 500 mΩ.

8.2.2.5 Capacitor Characteristics

It is important that capacitance tolerance and variation with temperature be taken into consideration when selecting a capacitor so that the minimum required amount of capacitance is provided over the full operating temperature range.

8.2.2.5.1 Ceramic Capacitors

For values of capacitance in the 10- to 100-µF range, ceramics are usually larger and more costly than tantalums but give superior AC performance for bypassing high frequency noise because of very low ESR (typically less than 10 mΩ). However, some dielectric types do not have good capacitance characteristics as a function of voltage and temperature.

The LP3869x-ADJ is designed to work with ceramic capacitors on the output to take advantage of the benefits they offer. For capacitance values in the range of 0.47 µF to 4.7 µF, ceramic capacitors are the smallest, least expensive and have the lowest ESR values, thus making them best for eliminating high frequency noise. The ESR of a typical 1-µF ceramic capacitor is in the range of 20 mΩ to 40 mΩ, which easily meets the ESR requirement for stability for the LP3869x.

Z5U and Y5V dielectric ceramics have capacitance that drops severely with applied voltage. A typical Z5U or Y5V capacitor can lose 60% of its rated capacitance with half of the rated voltage applied to it. The Z5U and Y5V also exhibit a severe temperature effect, losing more than 50% of nominal capacitance at high and low limits of the temperature range.

X7R and X5R dielectric ceramic capacitors are strongly recommended if ceramics are used, as they typically maintain a capacitance range within ±20% of nominal over full operating ratings of temperature and voltage. Of course, they are typically larger and more costly than Z5U/Y5U types for a given voltage and capacitance.

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8.2.2.5.2 Tantalum Capacitors

Solid tantalum capacitors have good temperature stability: a high-quality tantalum capacitor typically shows a capacitance value that varies less than 10-15% across the full temperature range of -40°C to 125°C. ESR will vary only about 2× going from the high to low temperature limits.

The increasing ESR at lower temperatures can cause oscillations when marginal quality capacitors are used (if the ESR of the capacitor is near the upper limit of the stability range at room temperature).

8.2.2.6 RFI/EMI Susceptibility

Radio frequency interference (RFI) and electromagnetic interference (EMI) can degrade the performance of any integrated circuit because of the small dimensions of the geometries inside the device. In applications where circuit sources are present which generate signals with significant high frequency energy content (> 1 MHz), care must be taken to ensure that this does not affect the device regulator.

If RFI/EMI noise is present on the input side of the regulator (such as applications where the input source comes from the output of a switching regulator), good ceramic bypass capacitors must be used at the input pin of the device.

If a load is connected to the device output which switches at high speed (such as a clock), the high-frequency current pulses required by the load must be supplied by the capacitors on the device output. Because the bandwidth of the regulator loop is less than 100 kHz, the control circuitry cannot respond to load changes above that frequency. This means the effective output impedance of the device at frequencies above 100 kHz is determined only by the output capacitors.

In applications where the load is switching at high speed, the output of the device may need RF isolation from the load. It is recommended that some inductance be placed between the output capacitor and the load, and good RF bypass capacitors be placed directly across the load.

PCB layout is also critical in high noise environments, because RFI/EMI is easily radiated directly into PC traces. Noisy circuitry should be isolated from *clean* circuits where possible, and grounded through a separate path. At MHz frequencies, ground planes begin to look inductive and RFI/ EMI can cause ground bounce across the ground plane. In multi-layer PCB applications, care should be taken in layout so that noisy power and ground planes do not radiate directly into adjacent layers which carry analog power and ground.

8.2.2.7 Output Noise

Noise is specified in two ways:

- Spot Noise or Output Noise Density is the RMS sum of all noise sources, measured at the regulator output, at a specific frequency (measured with a 1-Hz bandwidth). This type of noise is usually plotted on a curve as a function of frequency.
- Total Output Noise or Broad-Band Noise is the RMS sum of spot noise over a specified bandwidth, usually several decades of frequencies.

Attention should be paid to the units of measurement. Spot noise is measured in units $\mu V\sqrt{Hz}$ or $nV\sqrt{Hz}$, and total output noise is measured in μV_{RMS}.

The primary source of noise in low-dropout regulators is the internal reference. Noise can be reduced in two ways: by increasing the transistor area or by increasing the current drawn by the internal reference. Increasing the area will decrease the chance of fitting the die into a smaller package. Increasing the current drawn by the internal reference increases the total supply current (GND pin current).

8.2.2.8 Power Dissipation

Knowing the device power dissipation and proper sizing of the thermal plane connected to the tab or pad is critical to ensuring reliable operation. Device power dissipation depends on input voltage, output voltage, and load conditions and can be calculated with Equation 2.

$$P_{D(MAX)} = (V_{IN(MAX)} - V_{OUT}) \times I_{OUT(MAX)} \quad (2)$$

Power dissipation can be minimized, and greater efficiency can be achieved, by using the lowest available voltage drop option that would still be greater than the dropout voltage (V_{DO}). However, keep in mind that higher voltage drops result in better dynamic (that is, PSRR and transient) performance.

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On the WSON (DRV) package, the primary conduction path for heat is through the exposed power pad to the PCB. To ensure the device does not overheat, connect the exposed pad, through thermal vias, to an internal ground plane with an appropriate amount of copper PCB area .

On the VSSOP (DGK) and SOT-223 (NDC) packages, the primary conduction path for heat is through the pins to the PCB.

The maximum allowable junction temperature ($T_{J(MAX)}$) determines maximum power dissipation allowed ($P_{D(MAX)}$) for the device package.

Power dissipation and junction temperature are most often related by the junction-to-ambient thermal resistance ($R_{\theta JA}$) of the combined PCB and device package and the temperature of the ambient air (T_A), according to Equation 3 or Equation 4:

$$T_{J(MAX)} = T_{A(MAX)} + (R_{\theta JA} \times P_{D(MAX)}) \quad (3)$$

$$P_{D(MAX)} = (T_{J(MAX)} - T_{A(MAX)}) / R_{\theta JA} \quad (4)$$

Unfortunately, this $R_{\theta JA}$ is highly dependent on the heat-spreading capability of the particular PCB design, and therefore varies according to the total copper area, copper weight, and location of the planes. The $R_{\theta JA}$ recorded in *Thermal Information* is determined by the specific EIA/JEDEC JESD51-7 standard for PCB and copper-spreading area, and is to be used only as a relative measure of package thermal performance. For a well-designed thermal layout, $R_{\theta JA}$ is actually the sum of the package junction-to-case (bottom) thermal resistance ($R_{\theta JCbot}$) plus the thermal resistance contribution by the PCB copper area acting as a heat sink.

8.2.2.9 Estimating Junction Temperature

The EIA/JEDEC standard recommends the use of psi (Ψ) thermal characteristics to estimate the junction temperatures of surface mount devices on a typical PCB board application. These characteristics are not true thermal resistance values, but rather package specific thermal characteristics that offer practical and relative means of estimating junction temperatures. These psi metrics are determined to be significantly independent of copper-spreading area. The key thermal characteristics (Ψ_{JT} and Ψ_{JB}) are given in *Thermal Information* and are used in accordance with Equation 5 or Equation 6.

$$T_{J(MAX)} = T_{TOP} + (\Psi_{JT} \times P_{D(MAX)})$$

where

- $P_{D(MAX)}$ is explained in Equation 2.
- T_{TOP} is the temperature measured at the center-top of the device package. (5)

$$T_{J(MAX)} = T_{BOARD} + (\Psi_{JB} \times P_{D(MAX)})$$

where

- $P_{D(MAX)}$ is explained in Equation 2.
- T_{BOARD} is the PCB surface temperature measured 1-mm from the device package and centered on the package edge. (6)

For more information about the thermal characteristics Ψ_{JT} and Ψ_{JB}, see the TI Application Report *Semiconductor and IC Package Thermal Metrics* (SPRA953), available for download at www.ti.com.

For more information about measuring T_{TOP} and T_{BOARD}, see the TI Application Report *Using New Thermal Metrics* (SBVA025), available for download at www.ti.com.

For more information about the EIA/JEDEC JESD51 PCB used for validating $R_{\theta JA}$, see the TI Application Report *Thermal Characteristics of Linear and Logic Packages Using JEDEC PCB Designs* (SZZA017), available for download at www.ti.com.

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8.2.2.10 Reverse Voltage

A reverse voltage condition will exist when the voltage at the OUT pin is higher than the voltage at the IN pin. Typically this will happen when V_{IN} is abruptly taken low and C_{OUT} continues to hold a sufficient charge such that the input to output voltage becomes reversed. A less common condition is when an alternate voltage source is connected to the output.

There are two possible paths for current to flow from the OUT pin back to IN during a reverse voltage condition.

1. While V_{IN} is high enough to keep the control circuity alive, and the EN pin (LP38693-ADJ only) is above the $V_{EN(ON)}$ threshold, the control circuitry will attempt to regulate the output voltage. If the input voltage is less than the programmed output voltage, the control circuit will drive the gate of the pass element to the full ON condition. In this condition, reverse current will flow from the OUT to the IN pin, limited only by the $R_{DS(ON)}$ of the pass element and the output to input voltage differential. Discharging an output capacitor up to 1000 µF in this manner will not damage the device as the current will rapidly decay. However, continuous reverse current should be avoided. When the EN pin is low, this condition will be prevented.
2. The internal PFET pass element has an inherent parasitic diode. During normal operation, the input voltage is higher than the output voltage and the parasitic diode is reverse biased. However, when V_{IN} is below the value where the control circuity is alive, or the EN pin is low (LP38693-ADJ only), and the output voltage is more than 500 mV (typical) above the input voltage the parasitic diode becomes forward biased and current flows from the output pin to the input pin through the diode. The current in the parasitic diode should be limited to less than 1-A continuous and 5-A peak.

   If used in a dual-supply system where the regulator output load is returned to a negative supply, the OUT pin must be diode clamped to ground to limit the negative voltage transition. A Schottky diode is recommended for this protective clamp.

8.2.3 Application Curve

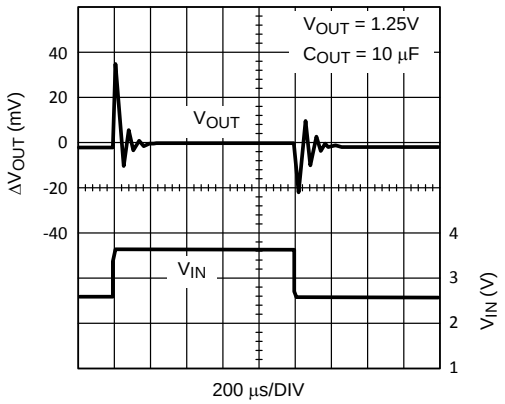


Figure 30. Line Transient Response

9 Power Supply Recommendations

The LP3869x-ADJ devices are designed to operate from an input supply voltage range of 2.7 V to 10 V. The input supply should be well regulated and free of spurious noise. To ensure that the device output voltage is well regulated, input supply should be at least V_{OUT} + 0.5 V, or 2.7 V, whichever is higher. A minimum capacitor value of 1-µF is required to be within 1 cm of the IN pin.

10 Layout

10.1 Layout Guidelines

Good PC layout practices must be used or instability can be induced because of ground loops and voltage drops. The input and output capacitors must be directly connected to the input, output, and ground pins of the regulator using traces which do not have other currents flowing in them (Kelvin connect).

The best way to do this is to lay out C_{IN} and C_{OUT} near the device with short traces to the IN, OUT, and GND pins. The regulator ground pin should be connected to the external circuit ground so that the regulator and its capacitors have a "single point ground."

It should be noted that stability problems have been seen in applications where "vias" to an internal ground plane were used at the ground points of the device and the input and output capacitors. This was caused by varying ground potentials at these nodes resulting from current flowing through the ground plane. Using a single point ground technique for the regulator and its capacitors fixed the problem. Because high current flows through the traces going into V_{IN} and coming from V_{OUT}, Kelvin connect the capacitor leads to these pins so there is no voltage drop in series with the input and output capacitors.

10.2 Layout Examples

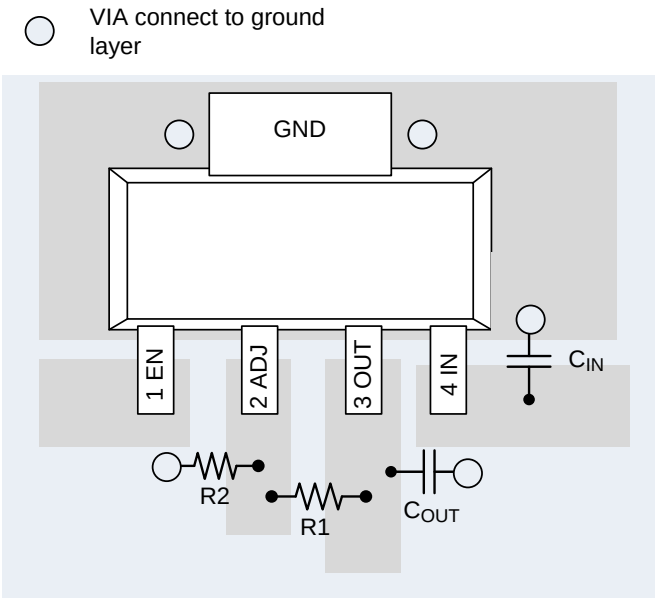


Figure 31. SOT-223 Layout

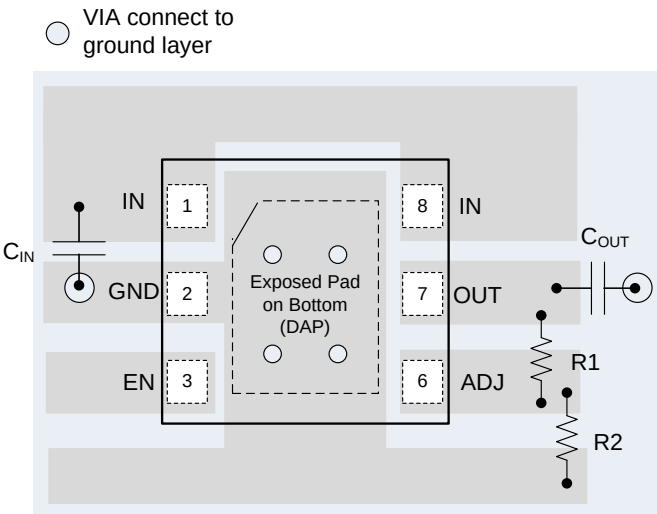


Figure 32. WSON LP38693 Layout

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10.3 WSON Mounting

The NGG0006A (No Pullback) 6-Lead WSON package requires specific mounting techniques which are detailed in the TI Application Report*Leadless Leadframe Package (LLP)* SNOA401. Referring to the section *PCB Design Recommendations*, it should be noted that the pad style which should be used with the WSON package is the NSMD (non-solder mask defined) type. Additionally, it is recommended the PCB terminal pads to be 0.2 mm longer than the package pads to create a solder fillet to improve reliability and inspection.

The thermal dissipation of the WSON package is directly related to the printed circuit board construction and the amount of additional copper area connected to the DAP. The DAP (exposed pad) on the bottom of the WSON package is connected to the die substrate with a conductive die attach adhesive. The DAP has no direct electrical (wire) connection to any of the pins. There is a parasitic PN junction between the die substrate and the device ground. As such, it is strongly recommend that the DAP be connected directly to the ground at device pin 2 (GND). Alternatively, but not recommended, the DAP may be left floating (no electrical connection). The DAP must not be connected to any potential other than ground.

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11 Device and Documentation Support

11.1 Documentation Support

11.1.1 Related Documentation

For related documentation see the following:

- *Leadless Leadframe Package (LLP)* (SNOA401)
- *Semiconductor and IC Package Thermal Metrics* (SPRA953)
- *Using New Thermal Metrics* (SBVA025)
- *Thermal Characteristics of Linear and Logic Packages Using JEDEC PCB Designs* (SZZA017)

11.2 Related Links

Table 2 lists quick access links. Categories include technical documents, support and community resources, tools and software, and quick access to sample or buy.

Table 2. Related Links

PARTS	PRODUCT FOLDER	SAMPLE & BUY	TECHNICAL DOCUMENTS	TOOLS & SOFTWARE	SUPPORT & COMMUNITY
LP38691-ADJ	Click here	Click here	Click here	Click here	Click here
LP38693-ADJ	Click here	Click here	Click here	Click here	Click here
LP38691-ADJ-Q1	Click here	Click here	Click here	Click here	Click here
LP38693-ADJ-Q1	Click here	Click here	Click here	Click here	Click here

11.3 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

TI E2E™ Online Community ***TI's Engineer-to-Engineer (E2E) Community.*** Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support ***TI's Design Support*** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

11.4 Trademarks

E2E is a trademark of Texas Instruments.
All other trademarks are the property of their respective owners.

11.5 Electrostatic Discharge Caution



These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

11.6 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

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PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
LP38691QSD-ADJ/NOPB	ACTIVE	WSON	NGG	6	1000	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 125	L251B	Samples
LP38691QSDX-ADJ/NOPB	ACTIVE	WSON	NGG	6	4500	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 125	L251B	Samples
LP38691SD-ADJ	NRND	WSON	NGG	6	1000	TBD	Call TI	Call TI	-40 to 125	L117B	
LP38691SD-ADJ/NOPB	ACTIVE	WSON	NGG	6	1000	Green (RoHS & no Sb/Br)	CU NIPDAU | CU SN	Level-1-260C-UNLIM	-40 to 125	L117B	Samples
LP38691SDX-ADJ/NOPB	ACTIVE	WSON	NGG	6	4500	Green (RoHS & no Sb/Br)	CU NIPDAU | CU SN	Level-1-260C-UNLIM	-40 to 125	L117B	Samples
LP38693MP-ADJ/NOPB	ACTIVE	SOT-223	NDC	5	1000	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 125	LJUB	Samples
LP38693MPX-ADJ/NOPB	ACTIVE	SOT-223	NDC	5	2000	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 125	LJUB	Samples
LP38693QSD-ADJ/NOPB	ACTIVE	WSON	NGG	6	1000	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 125	LLRB	Samples
LP38693QSDX-ADJ/NOPB	ACTIVE	WSON	NGG	6	4500	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 125	LLRB	Samples
LP38693SD-ADJ/NOPB	ACTIVE	WSON	NGG	6	1000	Green (RoHS & no Sb/Br)	CU NIPDAU | CU SN	Level-1-260C-UNLIM	-40 to 125	L127B	Samples
LP38693SDX-ADJ/NOPB	ACTIVE	WSON	NGG	6	4500	Green (RoHS & no Sb/Br)	CU NIPDAU | CU SN	Level-1-260C-UNLIM	-40 to 125	L127B	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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OTHER QUALIFIED VERSIONS OF LP38691-ADJ, LP38691-ADJ-Q1, LP38693-ADJ, LP38693-ADJ-Q1 :

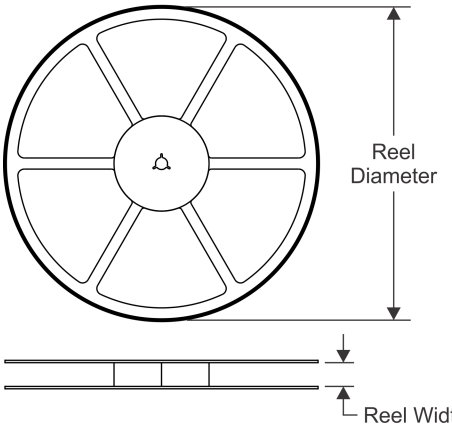
- Catalog: LP38691-ADJ, LP38693-ADJ
- Automotive: LP38691-ADJ-Q1, LP38693-ADJ-Q1

NOTE: Qualified Version Definitions:

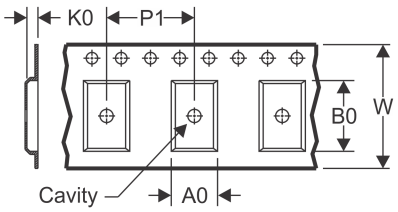
- Catalog - TI's standard catalog product
- Automotive - Q100 devices qualified for high-reliability automotive applications targeting zero defects

TAPE AND REEL INFORMATION

REEL DIMENSIONS

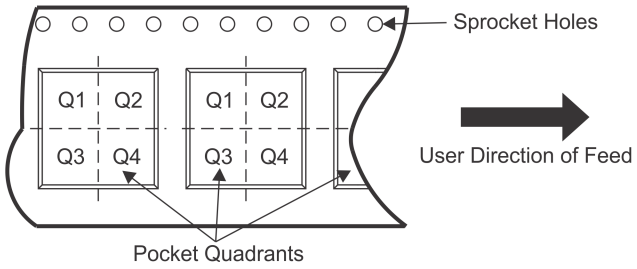


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

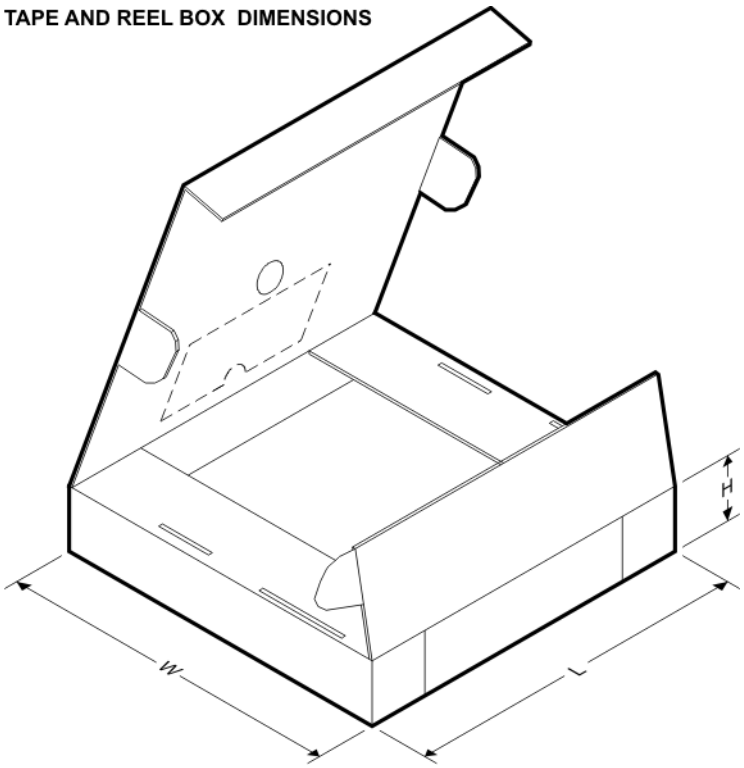
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
LP38691QSD-ADJ/NOPB	WSON	NGG	6	1000	178.0	12.4	3.3	3.3	1.0	8.0	12.0	Q1
LP38691QSDX-ADJ/NOPB	WSON	NGG	6	4500	330.0	12.4	3.3	3.3	1.0	8.0	12.0	Q1
LP38691SD-ADJ	WSON	NGG	6	1000	178.0	12.4	3.3	3.3	1.0	8.0	12.0	Q1
LP38691SD-ADJ/NOPB	WSON	NGG	6	1000	180.0	12.4	3.3	3.3	1.0	8.0	12.0	Q1
LP38691SDX-ADJ/NOPB	WSON	NGG	6	4500	330.0	12.4	3.3	3.3	1.0	8.0	12.0	Q1
LP38693MP-ADJ/NOPB	SOT-223	NDC	5	1000	330.0	16.4	7.0	7.5	2.2	12.0	16.0	Q3
LP38693MPX-ADJ/NOPB	SOT-223	NDC	5	2000	330.0	16.4	7.0	7.5	2.2	12.0	16.0	Q3
LP38693QSD-ADJ/NOPB	WSON	NGG	6	1000	178.0	12.4	3.3	3.3	1.0	8.0	12.0	Q1
LP38693QSDX-ADJ/NOPB	WSON	NGG	6	4500	330.0	12.4	3.3	3.3	1.0	8.0	12.0	Q1
LP38693SD-ADJ/NOPB	WSON	NGG	6	1000	180.0	12.4	3.3	3.3	1.0	8.0	12.0	Q1
LP38693SDX-ADJ/NOPB	WSON	NGG	6	4500	330.0	12.4	3.3	3.3	1.0	8.0	12.0	Q1

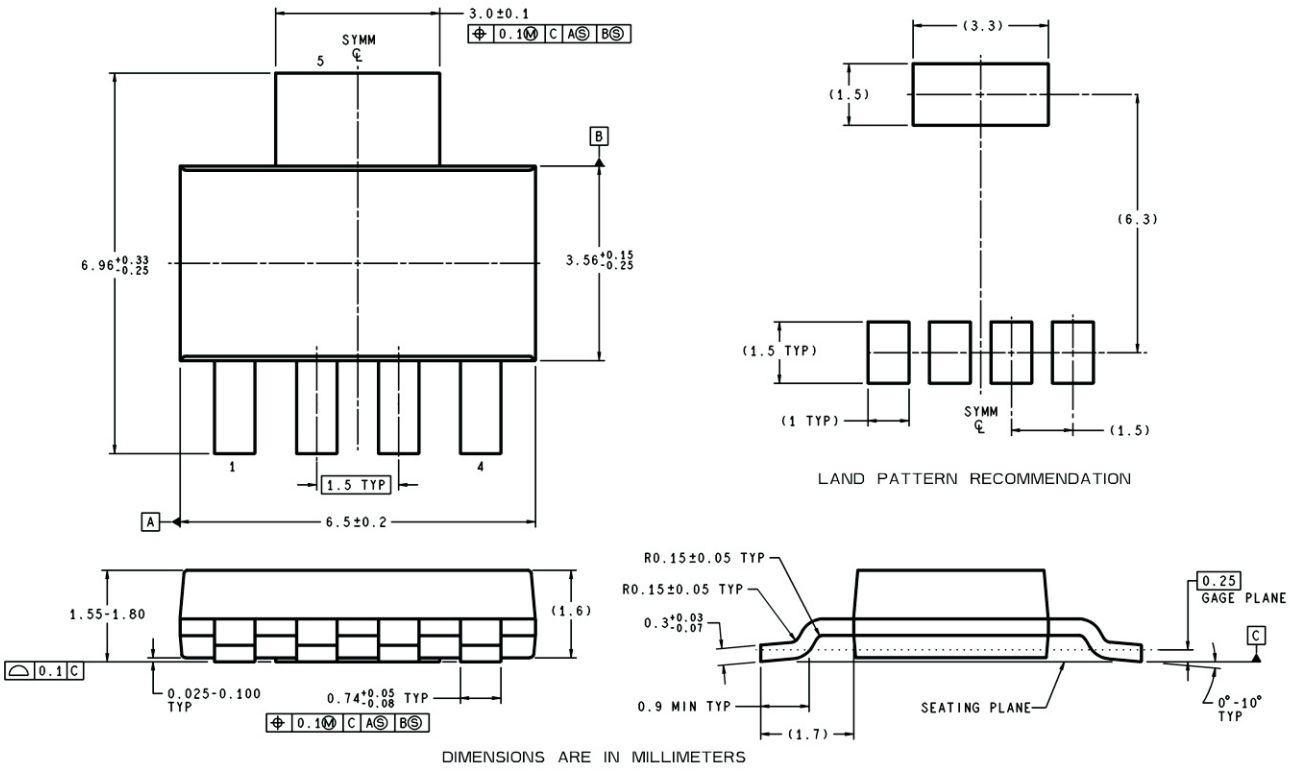
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

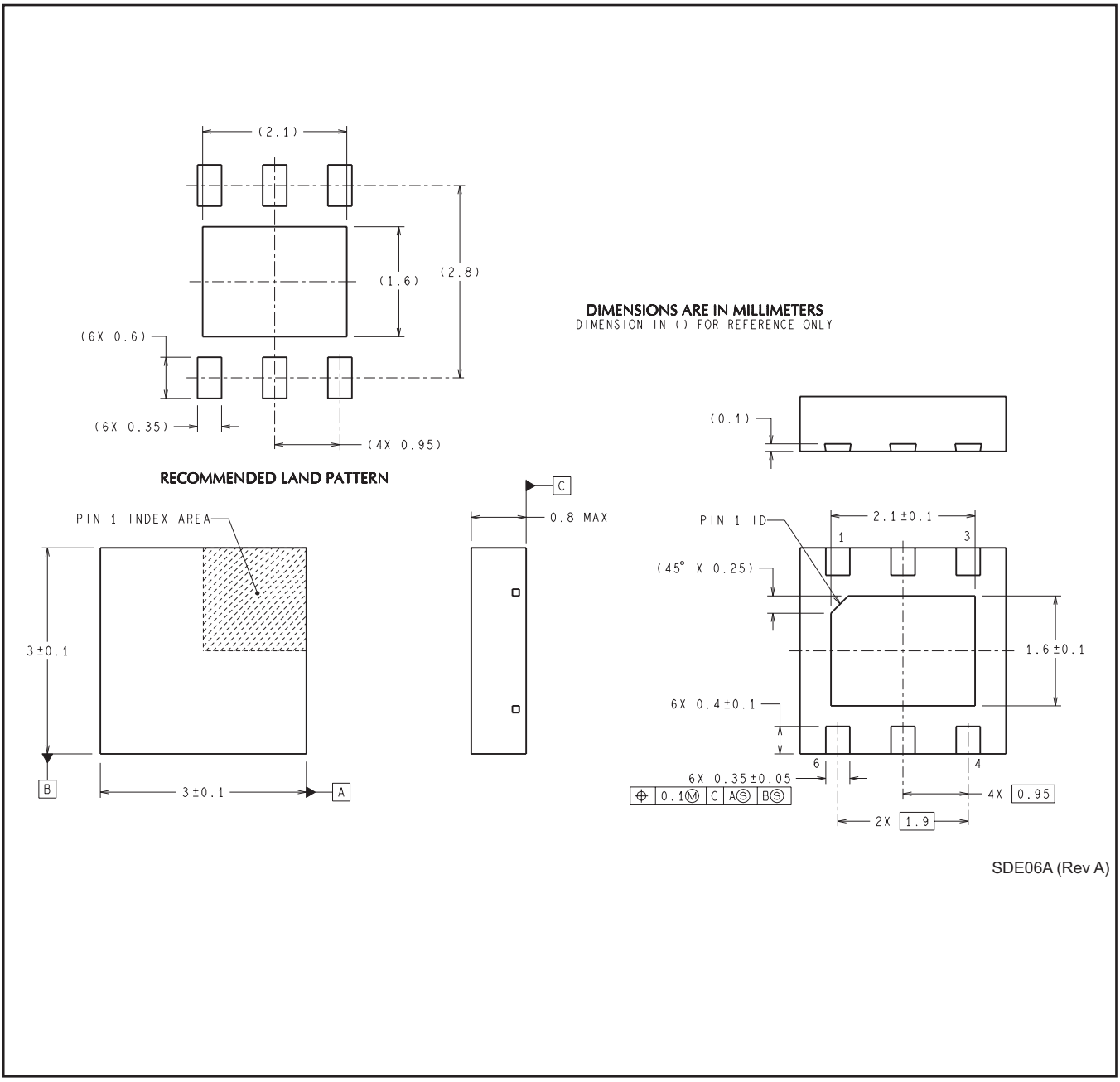
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
LP38691QSD-ADJ/NOPB	WSON	NGG	6	1000	210.0	185.0	35.0
LP38691QSDX-ADJ/NOPB	WSON	NGG	6	4500	367.0	367.0	35.0
LP38691SD-ADJ	WSON	NGG	6	1000	210.0	185.0	35.0
LP38691SD-ADJ/NOPB	WSON	NGG	6	1000	203.0	203.0	35.0
LP38691SDX-ADJ/NOPB	WSON	NGG	6	4500	367.0	367.0	35.0
LP38693MP-ADJ/NOPB	SOT-223	NDC	5	1000	367.0	367.0	35.0
LP38693MPX-ADJ/NOPB	SOT-223	NDC	5	2000	367.0	367.0	35.0
LP38693QSD-ADJ/NOPB	WSON	NGG	6	1000	210.0	185.0	35.0
LP38693QSDX-ADJ/NOPB	WSON	NGG	6	4500	367.0	367.0	35.0
LP38693SD-ADJ/NOPB	WSON	NGG	6	1000	203.0	203.0	35.0
LP38693SDX-ADJ/NOPB	WSON	NGG	6	4500	346.0	346.0	35.0

NDC0005A



MP05A (Rev A)

NGG0006A



SDE06A (Rev A)

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