LP2981-28, LP2981-29, LP2981-30
LP2981-33, LP2981-50, LP2981A-28
LP2981A-29, LP2981A-30, LP2981A-33, LP2981A-50
SLVS521G – JULY 2004 – REVISED AUGUST 2016

LP2981 100-mA Ultra-Low Dropout Regulators With Shutdown

1 Features

- Output Tolerance of
  - 0.75% (A Grade)
  - 1.25% (Standard Grade)
- Ultra-Low Dropout Typically:
  - 200 mV at Full Load of 100 mA
  - 7 mV at 1 mA
- Low I_Q: 600 µA Typical at Full Load of 100 mA
- Shutdown Current: 0.01 µA Typical
- Fast Transient Response to Line and Load
- Overcurrent and Thermal Protection
- High Peak Current Capability
- Low Z_{OUT} Over Wide Frequency Range
- −40°C to 125°C Temperature Range

2 Applications

- Smart Meters
- Servo and Motor Control
- Mobile Phones and Cameras
- Audio and Portable Speakers
- Telecommunication and Networking

3 Description

The LP2981 and LP2981A families of fixed-output, low-dropout regulators offer exceptional, cost-effective performance for both portable and non-portable applications. Available in fixed voltages of 2.8 V, 3 V, 3.3 V, and 5 V, the family has an output tolerance of 0.75% for the A-grade devices (1.25% for the standard grade) and is capable of delivering 100-mA continuous load current. Standard regulator features, such as overcurrent and overtemperature protection, are included.

The LP2981 and LP2981A have features that make the regulators ideal candidates for a variety of portable applications:

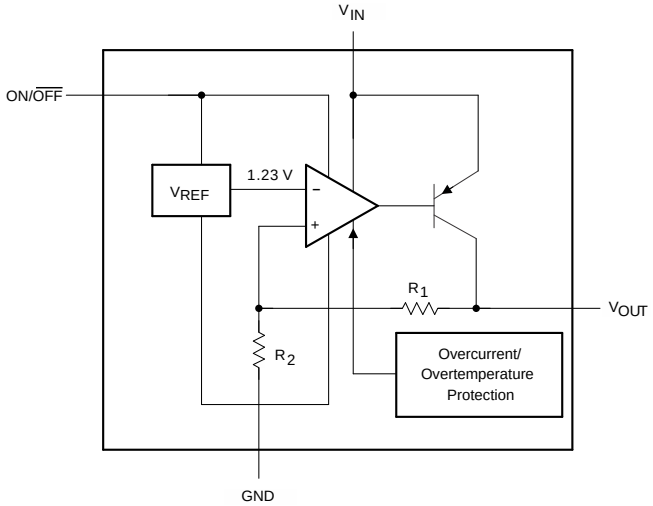
- Low dropout: A PNP pass element allows a typical dropout of 200 mV at 100-mA load current and 7 mV at 1-mA load.
- Low quiescent current: The use of a vertical PNP process allows for quiescent currents that are considerably lower than those associated with traditional lateral PNP regulators.
- Shutdown: A shutdown feature is available, allowing the regulator to consume only 0.01 µA when the ON/$\overline{\text{OFF}}$ pin is pulled low.

Device Information(1)

PART NUMBER	PACKAGE (PINS)	BODY SIZE (NOM)
LP2981-XXDBV LP2981A-XXDBV	SOT-23 (5)	2.90 mm × 1.60 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.

Block Diagram



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4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

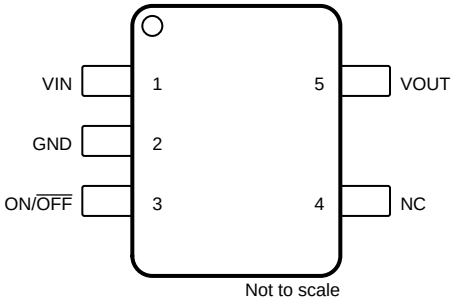
Changes from Revision F (August 2008) to Revision G **Page**

- Added *Device Information* table, *ESD Ratings* table, *Feature Description* section, *Device Functional Modes*, *Application and Implementation* section, *Power Supply Recommendations* section, *Layout* section, *Device and Documentation Support* section, and *Mechanical, Packaging, and Orderable Information* section ... 1
- Changed thermal table to align with JEDEC standards ... 4

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5 Pin Configuration and Functions

DBV Package
5-Pin SOT-23
Top View



Pin Functions

PIN		I/O	DESCRIPTION
NO.	NAME		
1	V_{IN}	I	Supply input
2	GND	—	Ground
3	ON/$\overline{OFF}$	I	Active-low shutdown pin. Tie to V_{IN} if unused.
4	NC	—	No connect
5	V_{OUT}	O	Voltage output

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

		MIN	MAX	UNIT
V_{IN}	Continuous input voltage(2)	–0.3	16	V
$V_{ON/\overline{OFF}}$	ON/$\overline{OFF}$ input voltage	–0.3	16	V
V_{OUT}	Output voltage(3)	–0.3	9	V
I_{OUT}	Output current	Internally limited (short-circuit protected)		
T_J	Operating virtual junction temperature		150	°C
T_{stg}	Storage temperature	–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) The PNP pass transistor has a parasitic diode connected between the input and output. This diode normally is reverse-biased ($V_{IN} > V_{OUT}$), but is forward-biased if the output voltage exceeds the input voltage by a diode drop (see *Application and Implementation* for more details).
(3) If load is returned to a negative power supply, the output must be diode clamped to GND.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	±2000	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101(2)	±1000	
		Machine model (MM)	±200	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

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6.3 Recommended Operating Conditions

		MIN	MAX	UNIT
V_{IN}	Supply input voltage	2.2 (1)	16	V
$V_{ON/\overline{OFF}}$	ON/$\overline{OFF}$ input voltage	0	V_{IN}	V
$V_{IN} - V_{OUT}$	Input-output differential	0.7	11	V
I_{OUT}	Output current		100	mA
T_J	Virtual junction temperature	–40	125	°C

(1) Minimum V_{IN} of 2.2 V is needed for proper biasing of LDO control circuitry.

6.4 Thermal Information

THERMAL METRIC (1)		LP2981-XX DBV (SOT-23) 5 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance (2) (3)	205.2	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	11.83	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	37.7	°C/W
ψ_{JT}	Junction-to-top characterization parameter	12.2	°C/W
ψ_{JB}	Junction-to-board characterization parameter	33.8	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.
(2) Maximum power dissipation is a function of $T_{J(max)}$, $R_{\theta JA}$, and T_A . The maximum allowable power dissipation at any allowable ambient temperature is $P_D = (T_{J(max)} – T_A)/ R_{\theta JA}$. Operating at the absolute maximum T_J of 150°C can affect reliability.
(3) The package thermal impedance is calculated in accordance with JESD 51-7.

6.5 Electrical Characteristics: LP2981-xx

at specified free-air temperature range, $V_{IN} = V_{OUT(NOM)} + 1$ V, $V_{ON/\overline{OFF}} = 2$ V, $C_{IN} = 1$ µF, $I_L = 1$ mA, $C_{OUT} = 4.7$ µF (unless otherwise noted)

PARAMETER		TEST CONDITIONS	T_A	MIN	TYP	MAX	UNIT
ΔV_{OUT}	Output voltage tolerance	$I_L = 1$ mA	25°C	–1.25		1.25	%V_{NOM}
		$I_L = 1$ mA to 100 mA	25°C	–2		2	
			–40°C to 125°C	–3.5		3.5	
$\Delta V_{OUT}/\Delta V_{IN}$	Output voltage line regulation	$V_{IN} = (V_{OUT(NOM)} + 1$ V) to 16 V	25°C		0.007	0.014	%/V
			–40°C to 125°C			0.032	
$V_{IN} - V_{OUT}$	Dropout voltage (1)	$I_L = 0$	25°C		1	3	mV
			–40°C to 125°C			5	
		$I_L = 1$ mA	25°C		7	10	
			–40°C to 125°C			15	
		$I_L = 25$ mA	25°C		70	100	
			–40°C to 125°C			150	
		$I_L = 100$ mA	25°C		200	250	
			–40°C to 125°C			375	

(1) Dropout voltage is defined as the input-to-output differential at which the output voltage drops 100 mV below the value measured with a 1-V differential. This dropout specification does not apply to the 1.8-V option, as the minimum $V_{IN} = 2.2$ V must be observed for proper biasing of LDO control circuitry.

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Electrical Characteristics: LP2981-xx (continued)

at specified free-air temperature range, $V_{IN} = V_{OUT(NOM)} + 1$ V, $V_{ON/\overline{OFF}} = 2$ V, $C_{IN} = 1$ µF, $I_L = 1$ mA, $C_{OUT} = 4.7$ µF (unless otherwise noted)

PARAMETER		TEST CONDITIONS	T_A	MIN	TYP	MAX	UNIT
I_{GND}	Ground pin current	$I_L = 0$	25°C		65	95	µA
			–40°C to 125°C			125	
		$I_L = 1$ mA	25°C		80	110	
			–40°C to 125°C			170	
		$I_L = 25$ mA	25°C		200	300	
			–40°C to 125°C			550	
		$I_L = 100$ mA	25°C		600	1000	
			–40°C to 125°C			1700	
		$V_{ON/\overline{OFF}} < 0.3$ V (OFF)	25°C		0.01	0.8	
		$V_{ON/\overline{OFF}} < 0.15$ V (OFF)	–40°C to 105°C		0.05	2	
			–40°C to 125°C			5	
$V_{ON/\overline{OFF}}$	ON/$\overline{OFF}$ input voltage(2)	High = O/P ON	25°C		1.4		V
			–40°C to 125°C	1.6			
		Low = O/P OFF	25°C		0.5		
			–40°C to 125°C			0.15	
$I_{ON/\overline{OFF}}$	ON/$\overline{OFF}$ input current	$V_{ON/\overline{OFF}} = 0$	25°C		0.01		µA
			–40°C to 125°C			–1	
		$V_{ON/\overline{OFF}} = 5$ V	25°C		5		
			–40°C to 125°C			15	
$I_{OUT(PK)}$	Peak output current	$V_{OUT} \geq V_{OUT(NOM)} - 5\%$	25°C		400		mA
V_n	Output noise voltage (RMS)	BW = 300 Hz to 50 kHz, $C_{OUT} = 10$ µF	25°C		160		µV
$\Delta V_{OUT}/\Delta V_{IN}$	Ripple rejection	f = 1 kHz, $C_{OUT} = 10$ µF	25°C		63		dB
$I_{OUT(MAX)}$	Short-circuit current	$R_L = 0$ (steady state)	25°C		150		mA

(2) The ON/$\overline{OFF}$ input must be actively terminated. Connect to V_{IN} if this function is not used (see *Application and Implementation*).

6.6 Electrical Characteristics: LP2981A-xx

at specified free-air temperature range, $V_{IN} = V_{OUT(NOM)} + 1$ V, $V_{ON/\overline{OFF}} = 2$ V, $C_{IN} = 1$ µF, $I_L = 1$ mA, $C_{OUT} = 4.7$ µF (unless otherwise noted)

PARAMETER		TEST CONDITIONS	T_A	MIN	TYP	MAX	UNIT
ΔV_{OUT}	Output voltage tolerance	$I_L = 1$ mA	25°C	–0.75		0.75	%V_{NOM}
		$I_L = 1$ mA to 100 mA	25°C	–1		1	
			–40°C to 125°C	–2.5		2.5	
$\Delta V_{OUT}/\Delta V_{IN}$	Output voltage line regulation	$V_{IN} = (V_{OUT(NOM)} + 1$ V) to 16 V	25°C		0.007	0.014	%/V
			–40°C to 125°C			0.032	
$V_{IN} - V_{OUT}$	Dropout voltage(1)	$I_L = 0$	25°C		1	3	mV
			–40°C to 125°C			5	
		$I_L = 1$ mA	25°C		7	10	
			–40°C to 125°C			15	
		$I_L = 25$ mA	25°C		70	100	
			–40°C to 125°C			150	
		$I_L = 100$ mA	25°C		200	250	
			–40°C to 125°C			375	

(1) Dropout voltage is defined as the input-to-output differential at which the output voltage drops 100 mV below the value measured with a 1-V differential. This dropout specification does not apply to the 1.8-V option, as the minimum $V_{IN} = 2.2$ V must be observed for proper biasing of LDO control circuitry.

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Electrical Characteristics: LP2981A-xx (continued)

at specified free-air temperature range, $V_{IN} = V_{OUT(NOM)} + 1$ V, $V_{ON/\overline{OFF}} = 2$ V, $C_{IN} = 1$ µF, $I_L = 1$ mA, $C_{OUT} = 4.7$ µF (unless otherwise noted)

PARAMETER		TEST CONDITIONS	T_A	MIN	TYP	MAX	UNIT
I_{GND}	Ground pin current	$I_L = 0$	25°C		65	95	µA
			–40°C to 125°C			125	
		$I_L = 1$ mA	25°C		80	110	
			–40°C to 125°C			170	
		$I_L = 25$ mA	25°C		200	300	
			–40°C to 125°C			550	
		$I_L = 100$ mA	25°C		600	1000	
			–40°C to 125°C			1700	
		$V_{ON/\overline{OFF}} < 0.3$ V (OFF)	25°C		0.01	0.8	
		$V_{ON/\overline{OFF}} < 0.15$ V (OFF)	–40°C to 105°C		0.05	2	
			–40°C to 125°C			5	
$V_{ON/\overline{OFF}}$	ON/$\overline{OFF}$ input voltage(2)	High = O/P ON	25°C		1.4		V
			–40°C to 125°C	1.6			
		Low = O/P OFF	25°C		0.5		
			–40°C to 125°C			0.15	
$I_{ON/\overline{OFF}}$	ON/$\overline{OFF}$ input current	$V_{ON/\overline{OFF}} = 0$	25°C		0.01		µA
			–40°C to 125°C			–1	
		$V_{ON/\overline{OFF}} = 5$ V	25°C		5		
			–40°C to 125°C			15	
$I_{OUT(PK)}$	Peak output current	$V_{OUT} \geq V_{OUT(NOM)} – 5\%$	25°C	150	400		mA
V_n	Output noise voltage (RMS)	BW = 300 Hz to 50 kHz, $C_{OUT} = 10$ µF	25°C		160		µV
$\Delta V_{OUT}/\Delta V_{IN}$	Ripple rejection	f = 1 kHz, $C_{OUT} = 10$ µF	25°C		63		dB
$I_{OUT(MAX)}$	Short-circuit current	$R_L = 0$ (steady state)	25°C		150		mA

(2) The ON/$\overline{OFF}$ input must be actively terminated. Connect to V_{IN} if this function is not used (see *Application and Implementation*).

6.7 Typical Characteristics

Unless otherwise specified: $T_A = 25°C$, $V_{IN} = V_{O(NOM)} + 1$ V, $C_{OUT} = 10$ µF, $C_{IN} = 1$ µF all voltage options, ON/$\overline{OFF}$ pin tied to V_{IN}.

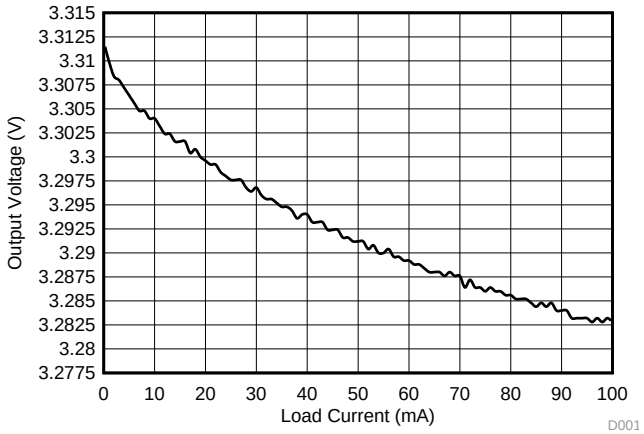


Figure 1. Load Regulation - LP2981-33

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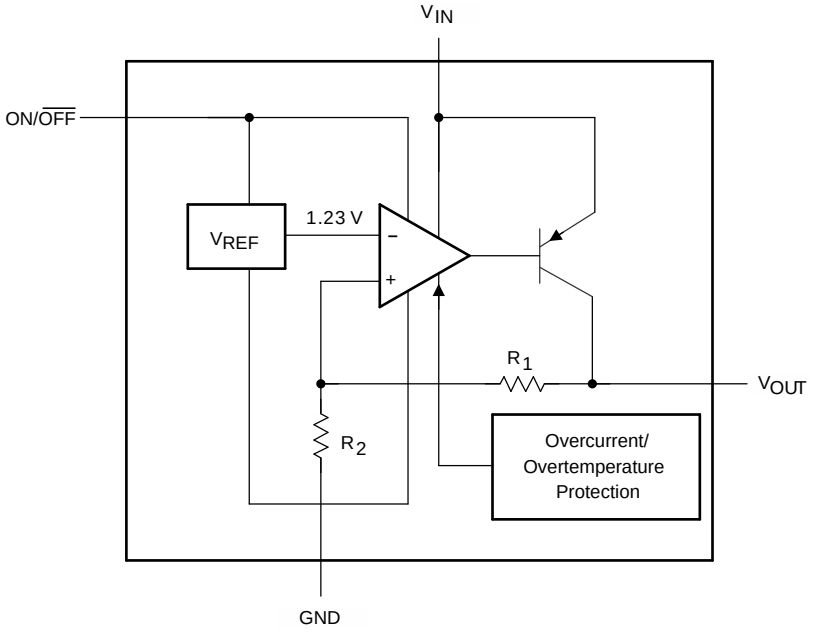
7 Detailed Description

7.1 Overview

The LP2981 and LP2981A are 100-mA fixed-output, low-dropout regulator. Available in assorted output voltages from 2.5 V to 5 V, the device has an output tolerance of 0.75% for the A grade (1.25% for the non-A version). The low-drop voltage and the ultra-low quiescent current make them suitable for low noise, low-power applications and in battery-powered systems:

- Low dropout: A PNP pass element allows a typical dropout of 200 mV at 100-mA load current and 7 mV at 1-mA load.
- Low quiescent current: The use of a vertical PNP process allows for quiescent currents that are considerably lower than those associated with traditional lateral PNP regulators.
- Shutdown: A shutdown feature is available, allowing the regulator to consume only 0.01 µA when the ON/$\overline{\text{OFF}}$ pin is pulled low.
- Small packaging: For the most space-constrained needs, the regulator is available in the SOT-23 package.

7.2 Functional Block Diagram



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7.3 Feature Description

7.3.1 Ultra-Low Dropout Voltage

The dropout voltage often refers to the voltage difference between the input and output voltage (V_{DO} = V_{IN} – V_{OUT}), where the main current pass-FET is fully on in the ohmic region of operation and is characterized by the classic $R_{DS(ON)}$ of the FET. V_{DO} indirectly specifies a minimum input voltage above the nominal programmed output voltage at which the output voltage is expected to remain within its accuracy boundary. The LP2981's pass-PNP allows a dropout of 200 mV at full load and 7 mV at 1 mA or lower loads. This allows for small voltage drop regulation and reduces the total power dissipation.

7.3.2 Low Ground Current

LP2981 uses a vertical PNP process which allows for quiescent currents that are considerably lower than those associated with traditional lateral PNP regulators, typically 600 µA at 100-mA load and 65 µA at 1-mA load.

Feature Description (continued)

7.3.3 Short-Circuit Protection (Current Limit)

The internal current-limit circuit is used to protect the LDO against high-load current faults or shorting events. The LDO is not designed to operate in a steady-state current limit. During a current-limit event, the LDO sources constant current. Therefore, the output voltage falls when load impedance decreases. If a current limit occurs and the resulting output voltage is low, excessive power may be dissipated across the LDO resulting in a thermal shutdown of the output. A foldback feature limits the short-circuit current to protect the regulator from damage under all load conditions. If V_{OUT} is forced below 0 V before ON/$\overline{OFF}$ goes high and the load current required exceeds the foldback current limit, the device may not start up correctly.

7.3.4 Capacitor Characteristics

7.3.4.1 Ceramic

Due to their very low ESR values, ceramic capacitors are not suitable for use as the output capacitor. For instance, a typical 2.2-µF ceramic capacitor has an ESR in the range of 10 mΩ to 20 mΩ and, thus, easily can fall out of minimum ESR requirements under certain operating conditions.

If a ceramic capacitor is used at the output, a 1-Ω resistor must be placed in series with the capacitor to raise the ESR seen by the regulator.

7.3.4.2 Tantalum

Solid tantalum capacitors are optimal choices for the LP2981, but they still must meet the minimum ESR requirement. Note that the ESR of a tantalum capacitor increases as temperature drops, as much as doubling from 25°C to –40°C. Thus, ESR margins must be maintained over the temperature range to prevent regulator instability. For operation at very low temperatures, paralleling a tantalum capacitor with a ceramic one keeps the combined ESR from increasing near the upper limit of the ESR curve.

7.3.4.3 Aluminum

Aluminum capacitors can be used, but use with the LP2981 is impractical due to their large physical dimensions. They also must meet the ESR requirements over the full temperature range. In this regard, aluminium capacitors are at a big disadvantage due to their sharp ESR increase as temperature drops. For example, over a temperature drop from 20°C to –40°C, the ESR of an aluminum electrolytic capacitor can increase by a factor of 50. In addition, some of the electrolytes used in these capacitors can freeze at –25°C, making the capacitor nonoperational.

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7.4 Device Functional Modes

7.4.1 ON/$\overline{\text{OFF}}$ Operation

The LP2981 allows for a shutdown mode through the ON/$\overline{\text{OFF}}$ pin. If the shutdown feature is not used, ON/$\overline{\text{OFF}}$ must be connected to the input to ensure that the regulator is on at all times. To drive ON/$\overline{\text{OFF}}$:

- A LOW (≤0.3 V) turns the regulator OFF; a HIGH (≥1.6 V) turns it ON.
  - Use either a totem-pole output or an open-collector output with a pullup resistor tied to V_{IN} (or another logic supply)
- The HIGH signal can exceed VIN, but must not exceed the absolute maximum ratings of 20 V for the ON/$\overline{\text{OFF}}$ pin
- Apply a signal with a slew rate of ≥40 mV/µs. A slow slew rate can cause the shutdown function to operate incorrectly

7.4.2 Reverse Input-Output Voltage

An inherent diode is present across the PNP pass element of the LP2981.

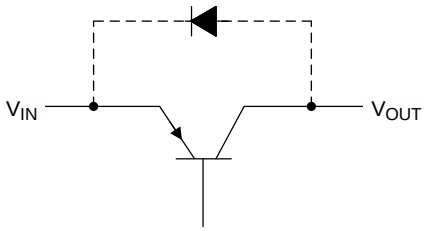
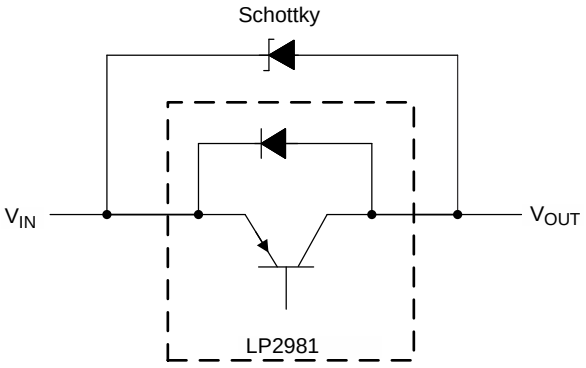


Figure 2. Internal PNP Diode Structure

With the anode connected to the output, this diode is reverse-biased during normal operation, because the input voltage is higher than the output. However, if the output is pulled one V_{BE} higher than the input, or if the input is abruptly stepped below the output, this diode is forward-biased and can cause a parasitic silicon-controlled rectifier (SCR) to latch, resulting in current flowing from the output to the input (values in excess of 100 mA can cause damage). Thus, to prevent possible damage to the regulator in any application where the output may be pulled above the input, an external Schottky diode must be connected between the output and input. With the anode on output, this Schottky limits the reverse voltage across the output and input pins to approximately 0.3 V, preventing the regulator's internal diode from forward biasing.



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Figure 3. Internal PNP Diode Bypass

8 Application and Implementation

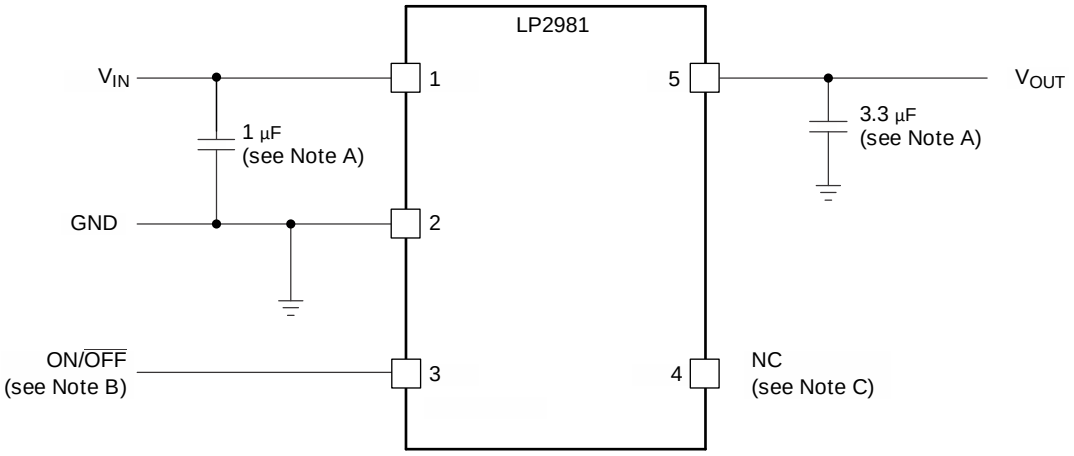
NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

8.1 Application Information

The LP2981 is a linear voltage regulator operating from 2.1 V to 16 V on the input and regulates voltages between 2.5 V to 5 V with 0.75% accuracy and 100-mA maximum output current. Efficiency is defined by the ratio of output voltage to input voltage because the LP2981 is a linear voltage regulator. To achieve high efficiency, the dropout voltage ($V_{IN} – V_{OUT}$) must be as small as possible, thus requiring a very-low-dropout LDO. Successfully implementing an LDO in an application depends on the application requirements. If the requirements are simply input voltage and output voltage, compliance specifications (such as internal power dissipation or stability) must be verified to ensure a solid design. If timing, start-up, noise, power supply rejection ratio (PSRR), or any other transient specification is required, then the design becomes more challenging.

8.2 Typical Application



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A. Minimum C_{OUT} value for stability (can be increased without limit for improved stability and transient response)

B. ON/$\overline{OFF}$ must be actively terminated. Connect to V_{IN} if shutdown feature is not used.

C. Pin 4 (NC) must be left open. Do not connect anything to this pin.

Figure 4. LP2981 Typical Application

8.2.1 Design Requirements

Table 1 lists the parameters for this application.

Table 1. Design Parameters

PARAMETER	DESIGN REQUIREMENT
Input voltage	5 V ±10%, provided by an external regulator
Output voltage	3.3 V ±5%
Output current	100 mA (maximum), 1 mA (minimum)
RMS noise, 300 Hz to 50kHz	< 1 mV_{RMS}
PSRR at 1kHz	> 40 dB

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8.2.2 Detailed Design Procedure

8.2.2.1 External Capacitors

Like any low-dropout regulator, the external capacitors used with the LP2981 must be carefully selected to assure regulator loop stability.

8.2.2.1.1 Input Capacitor (C_{in})

A minimum value of 1 µF (over the entire operating temperature range) is required at the input of the LP2981. In addition, this input capacitor must be placed within 1 cm of the input pin and connected to a clean analog ground. There is no Equivalent Series Resistance (ESR) requirement for this capacitor, and the capacitance can be increased without limit. A good-quality ceramic or tantalum capacitor can be used.

8.2.2.1.2 Output Capacitor (C_{out})

As a PNP regulator, the LP2981 requires the output capacitor to meet both a minimum capacitance and ESR value. Required ESR values as a function of load current are provided for various output voltages, load currents, and capacitances (see Figure 5 through Figure 8).

- Minimum C_{out}: 3.3 µF (can be increased without limit to improve transient response stability margin)
- ESR range: see Figure 5 through Figure 8

It is critical that both the minimum capacitance and ESR requirement be met over the entire operating temperature range. Depending on the type of capacitor used, both of these parameters can vary significantly with temperature (see *Capacitor Characteristics*).

8.2.3 Application Curves

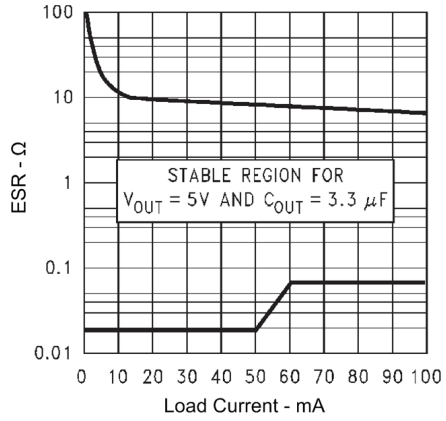


Figure 5. 5-V/3.3-µF ESR Curves

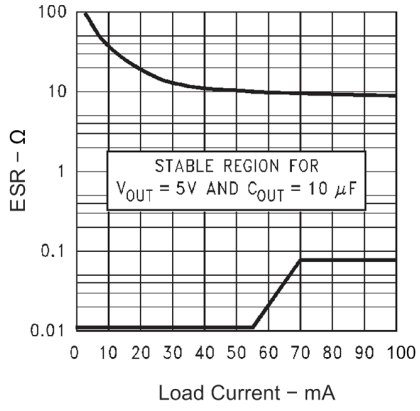


Figure 6. 5-V/10-µF ESR Curves

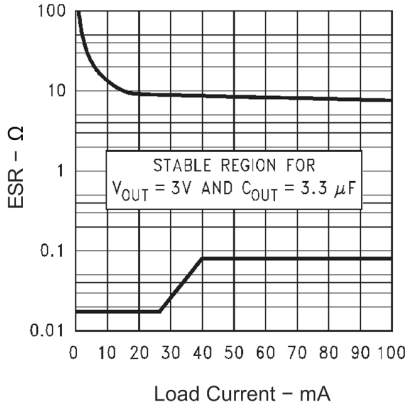


Figure 7. 3-V/3.3-µF ESR Curves

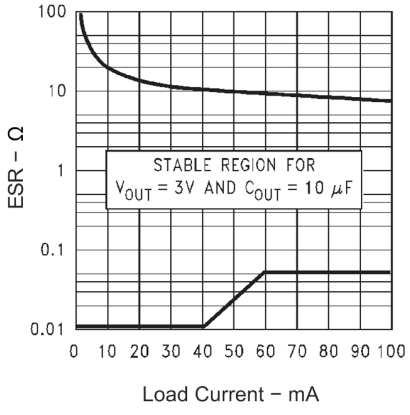


Figure 8. 3-V/10-µF ESR Curves

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9 Power Supply Recommendations

The LP2981 is designed to operate from an input voltage supply range between 2.2 V and 16 V. The input voltage range provides adequate headroom for the device to have a regulated output. This input supply must be well regulated. If the input supply is noisy, additional input capacitors with low ESR can help improve the output noise performance.

10 Layout

10.1 Layout Guidelines

For best overall performance, place all circuit components on the same side of the printed-circuit board and as near as practical to the respective LDO pin connections. Place ground return connections to the input and output capacitors, and to the LDO ground pin as close to each other as possible, connected by a wide, component-side, copper surface. The use of vias and long traces to create LDO circuit connections is strongly discouraged and negatively affects system performance. This grounding and layout scheme minimizes inductive parasitics, and thereby reduces load-current transients, minimizes noise, and increases circuit stability. A ground reference plane is also recommended and is either embedded in the PCB itself or located on the bottom side of the PCB opposite the components. This reference plane serves to assure accuracy of the output voltage, shield noise, and behaves similar to a thermal plane to spread (or sink) heat from the LDO device. In most applications, this ground plane is necessary to meet thermal requirements.

10.2 Layout Example

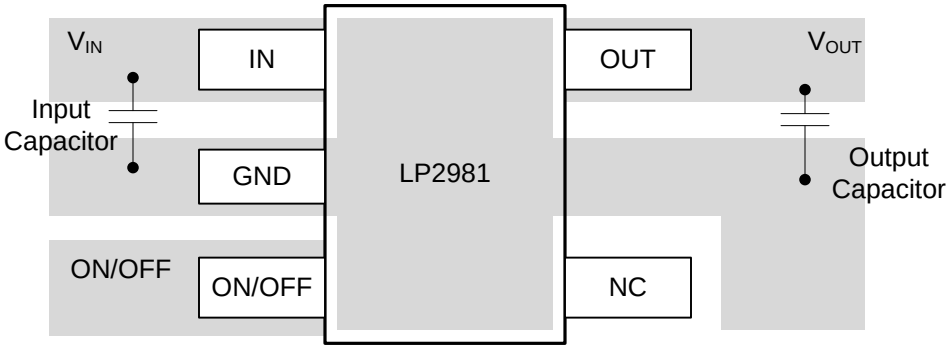


Figure 9. Recommended Layout

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11 Device and Documentation Support

11.1 Related Links

The table below lists quick access links. Categories include technical documents, support and community resources, tools and software, and quick access to sample or buy.

Table 2. Related Links

PARTS	PRODUCT FOLDER	SAMPLE & BUY	TECHNICAL DOCUMENTS	TOOLS & SOFTWARE	SUPPORT & COMMUNITY
LP2981-28	Click here	Click here	Click here	Click here	Click here
LP2981-29	Click here	Click here	Click here	Click here	Click here
LP2981-30	Click here	Click here	Click here	Click here	Click here
LP2981-33	Click here	Click here	Click here	Click here	Click here
LP2981-33	Click here	Click here	Click here	Click here	Click here
LP2981-50	Click here	Click here	Click here	Click here	Click here
LP2981A-28	Click here	Click here	Click here	Click here	Click here
LP2981A-29	Click here	Click here	Click here	Click here	Click here
LP2981A-30	Click here	Click here	Click here	Click here	Click here
LP2981A-33	Click here	Click here	Click here	Click here	Click here
LP2981A-50	Click here	Click here	Click here	Click here	Click here

11.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. In the upper right corner, click on *Alert me* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

11.3 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

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Design Support ***TI's Design Support*** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

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11.5 Electrostatic Discharge Caution



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

11.6 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

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12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

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PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
LP2981-28DBVR	ACTIVE	SOT-23	DBV	5	3000	Green (RoHS & no Sb/Br)	NIPDAU | SN	Level-1-260C-UNLIM	-40 to 125	(LP5G, LP5L)	Samples
LP2981-28DBVT	ACTIVE	SOT-23	DBV	5	250	Green (RoHS & no Sb/Br)	NIPDAU | SN	Level-1-260C-UNLIM	-40 to 125	(LP5G, LP5L)	Samples
LP2981-28DBVTG4	ACTIVE	SOT-23	DBV	5	250	Green (RoHS & no Sb/Br)	NIPDAU	Level-1-260C-UNLIM	-40 to 125	LP5G	Samples
LP2981-30DBVR	ACTIVE	SOT-23	DBV	5	3000	Green (RoHS & no Sb/Br)	NIPDAU | SN	Level-1-260C-UNLIM	-40 to 125	(LP7G, LP7L)	Samples
LP2981-30DBVT	ACTIVE	SOT-23	DBV	5	250	Green (RoHS & no Sb/Br)	NIPDAU | SN	Level-1-260C-UNLIM	-40 to 125	(LP7G, LP7L)	Samples
LP2981-33DBVR	ACTIVE	SOT-23	DBV	5	3000	Green (RoHS & no Sb/Br)	NIPDAU | SN	Level-1-260C-UNLIM	-40 to 125	(LPBG, LPBL)	Samples
LP2981-33DBVT	ACTIVE	SOT-23	DBV	5	250	Green (RoHS & no Sb/Br)	NIPDAU | SN	Level-1-260C-UNLIM	-40 to 125	(LPBG, LPBL)	Samples
LP2981-33DBVTE4	ACTIVE	SOT-23	DBV	5	250	Green (RoHS & no Sb/Br)	NIPDAU	Level-1-260C-UNLIM	-40 to 125	LPBG	Samples
LP2981-33DBVTG4	ACTIVE	SOT-23	DBV	5	250	Green (RoHS & no Sb/Br)	NIPDAU	Level-1-260C-UNLIM	-40 to 125	LPBG	Samples
LP2981-50DBVR	ACTIVE	SOT-23	DBV	5	3000	Green (RoHS & no Sb/Br)	NIPDAU	Level-1-260C-UNLIM	-40 to 125	(LPDG, LPDL)	Samples
LP2981-50DBVRG4	ACTIVE	SOT-23	DBV	5	3000	Green (RoHS & no Sb/Br)	NIPDAU	Level-1-260C-UNLIM	-40 to 125	(LPDG, LPDL)	Samples
LP2981-50DBVT	ACTIVE	SOT-23	DBV	5	250	Green (RoHS & no Sb/Br)	NIPDAU	Level-1-260C-UNLIM	-40 to 125	(LPDG, LPDL)	Samples
LP2981A-28DBVR	ACTIVE	SOT-23	DBV	5	3000	Green (RoHS & no Sb/Br)	NIPDAU | SN	Level-1-260C-UNLIM	-40 to 125	(LP6G, LP6L)	Samples
LP2981A-28DBVT	ACTIVE	SOT-23	DBV	5	250	Green (RoHS & no Sb/Br)	NIPDAU | SN	Level-1-260C-UNLIM	-40 to 125	(LP6G, LP6L)	Samples
LP2981A-29DBVR	ACTIVE	SOT-23	DBV	5	3000	Green (RoHS & no Sb/Br)	NIPDAU	Level-1-260C-UNLIM	-40 to 125	(LRBG, LRBL)	Samples
LP2981A-30DBVR	ACTIVE	SOT-23	DBV	5	3000	Green (RoHS & no Sb/Br)	NIPDAU | SN	Level-1-260C-UNLIM	-40 to 125	(LP8G, LP8L)	Samples
LP2981A-30DBVRG4	ACTIVE	SOT-23	DBV	5	3000	Green (RoHS & no Sb/Br)	NIPDAU	Level-1-260C-UNLIM	-40 to 125	LP8G	Samples

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
LP2981A-30DBVT	ACTIVE	SOT-23	DBV	5	250	Green (RoHS & no Sb/Br)	NIPDAU | SN	Level-1-260C-UNLIM	-40 to 125	(LP8G, LP8L)	Samples
LP2981A-30DBVTG4	ACTIVE	SOT-23	DBV	5	250	Green (RoHS & no Sb/Br)	NIPDAU	Level-1-260C-UNLIM	-40 to 125	LP8G	Samples
LP2981A-33DBVR	ACTIVE	SOT-23	DBV	5	3000	Green (RoHS & no Sb/Br)	NIPDAU | SN	Level-1-260C-UNLIM	-40 to 125	(LPCG, LPCL)	Samples
LP2981A-33DBVRG4	ACTIVE	SOT-23	DBV	5	3000	Green (RoHS & no Sb/Br)	NIPDAU	Level-1-260C-UNLIM	-40 to 125	LPCG	Samples
LP2981A-33DBVT	ACTIVE	SOT-23	DBV	5	250	Green (RoHS & no Sb/Br)	NIPDAU | SN	Level-1-260C-UNLIM	-40 to 125	(LPCG, LPCL)	Samples
LP2981A-33DBVTG4	ACTIVE	SOT-23	DBV	5	250	Green (RoHS & no Sb/Br)	NIPDAU	Level-1-260C-UNLIM	-40 to 125	LPCG	Samples
LP2981A-50DBVR	ACTIVE	SOT-23	DBV	5	3000	Green (RoHS & no Sb/Br)	NIPDAU	Level-1-260C-UNLIM	-40 to 125	(LPEG, LPEL)	Samples
LP2981A-50DBVRG4	ACTIVE	SOT-23	DBV	5	3000	Green (RoHS & no Sb/Br)	NIPDAU	Level-1-260C-UNLIM	-40 to 125	(LPEG, LPEL)	Samples
LP2981A-50DBVT	ACTIVE	SOT-23	DBV	5	250	Green (RoHS & no Sb/Br)	NIPDAU	Level-1-260C-UNLIM	-40 to 125	(LPEG, LPEL)	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

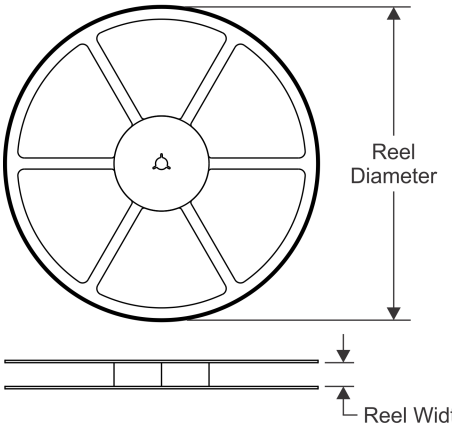
(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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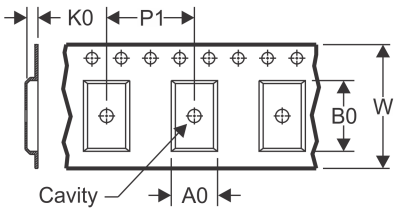
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TAPE AND REEL INFORMATION

REEL DIMENSIONS

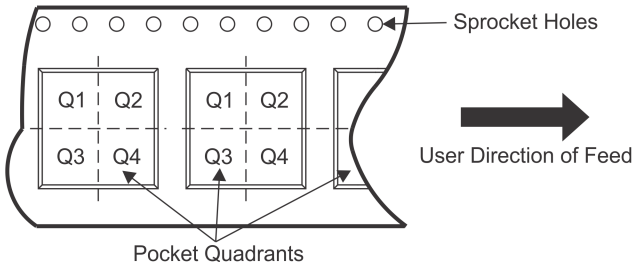


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

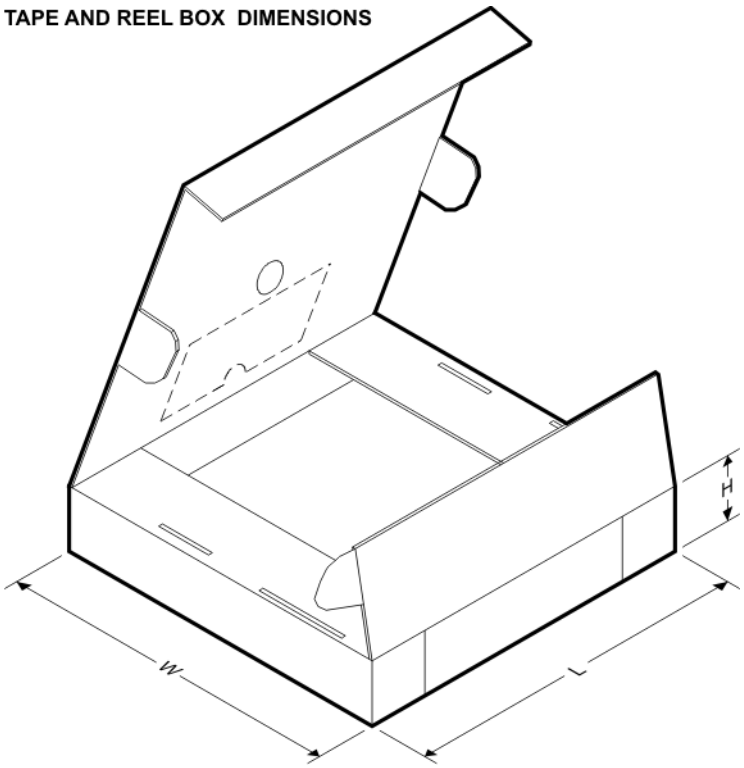
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
LP2981-28DBVR	SOT-23	DBV	5	3000	178.0	9.0	3.23	3.17	1.37	4.0	8.0	Q3
LP2981-30DBVR	SOT-23	DBV	5	3000	178.0	9.0	3.23	3.17	1.37	4.0	8.0	Q3
LP2981-33DBVR	SOT-23	DBV	5	3000	178.0	9.0	3.23	3.17	1.37	4.0	8.0	Q3
LP2981-33DBVTG4	SOT-23	DBV	5	250	178.0	9.0	3.23	3.17	1.37	4.0	8.0	Q3
LP2981A-28DBVR	SOT-23	DBV	5	3000	178.0	9.0	3.23	3.17	1.37	4.0	8.0	Q3
LP2981A-30DBVR	SOT-23	DBV	5	3000	178.0	9.0	3.3	3.2	1.4	4.0	8.0	Q3
LP2981A-30DBVRG4	SOT-23	DBV	5	3000	178.0	9.0	3.3	3.2	1.4	4.0	8.0	Q3
LP2981A-30DBVTG4	SOT-23	DBV	5	250	178.0	9.0	3.23	3.17	1.37	4.0	8.0	Q3
LP2981A-33DBVR	SOT-23	DBV	5	3000	178.0	9.0	3.3	3.2	1.4	4.0	8.0	Q3
LP2981A-33DBVT	SOT-23	DBV	5	250	180.0	9.2	3.17	3.23	1.37	4.0	8.0	Q3
LP2981A-33DBVTG4	SOT-23	DBV	5	250	178.0	9.0	3.23	3.17	1.37	4.0	8.0	Q3

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

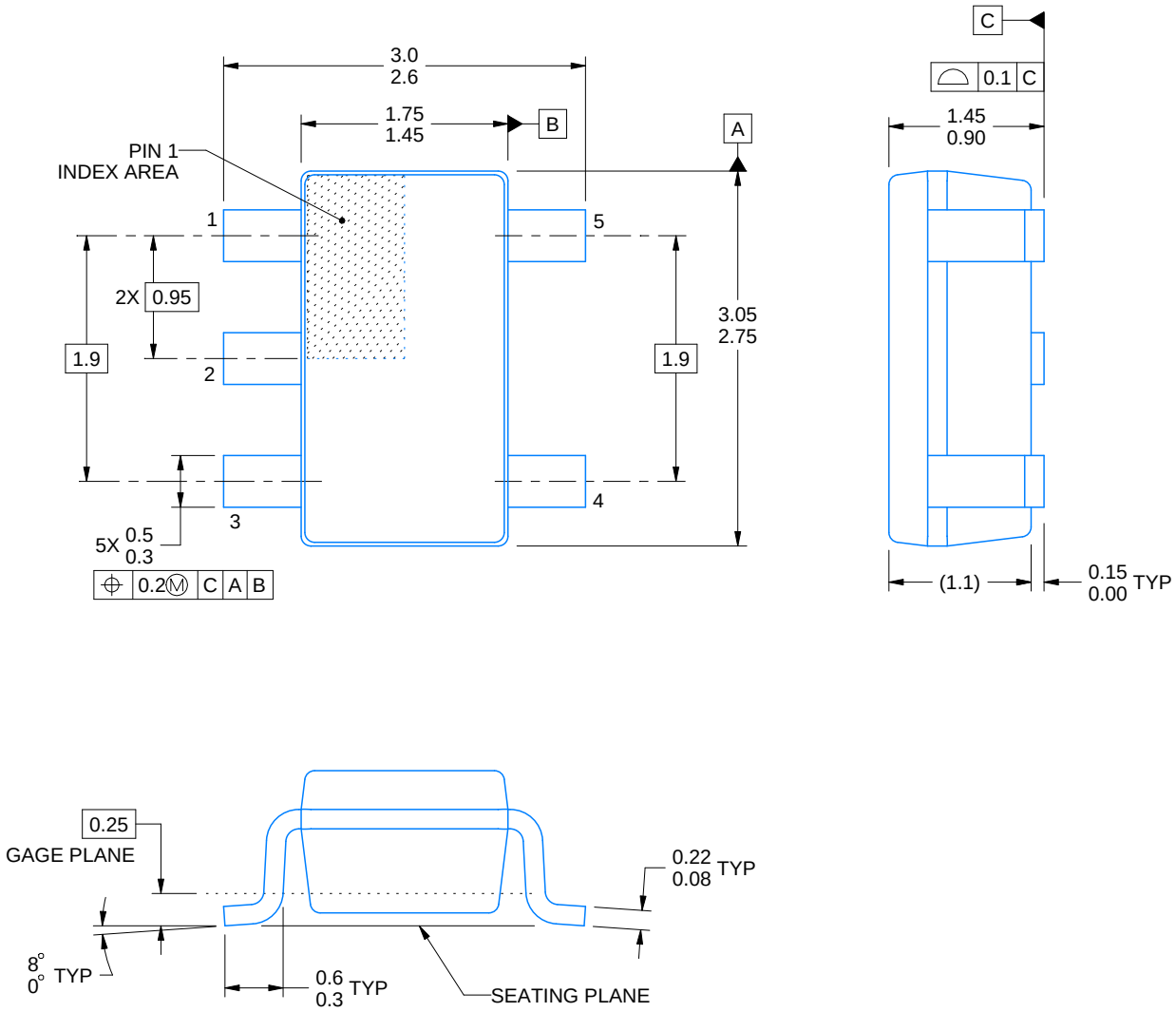
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
LP2981-28DBVR	SOT-23	DBV	5	3000	180.0	180.0	18.0
LP2981-30DBVR	SOT-23	DBV	5	3000	180.0	180.0	18.0
LP2981-33DBVR	SOT-23	DBV	5	3000	180.0	180.0	18.0
LP2981-33DBVTG4	SOT-23	DBV	5	250	180.0	180.0	18.0
LP2981A-28DBVR	SOT-23	DBV	5	3000	180.0	180.0	18.0
LP2981A-30DBVR	SOT-23	DBV	5	3000	180.0	180.0	18.0
LP2981A-30DBVRG4	SOT-23	DBV	5	3000	180.0	180.0	18.0
LP2981A-30DBVTG4	SOT-23	DBV	5	250	180.0	180.0	18.0
LP2981A-33DBVR	SOT-23	DBV	5	3000	180.0	180.0	18.0
LP2981A-33DBVT	SOT-23	DBV	5	250	205.0	200.0	33.0
LP2981A-33DBVTG4	SOT-23	DBV	5	250	180.0	180.0	18.0

PACKAGE OUTLINE

DBV0005A

SOT-23 - 1.45 mm max height

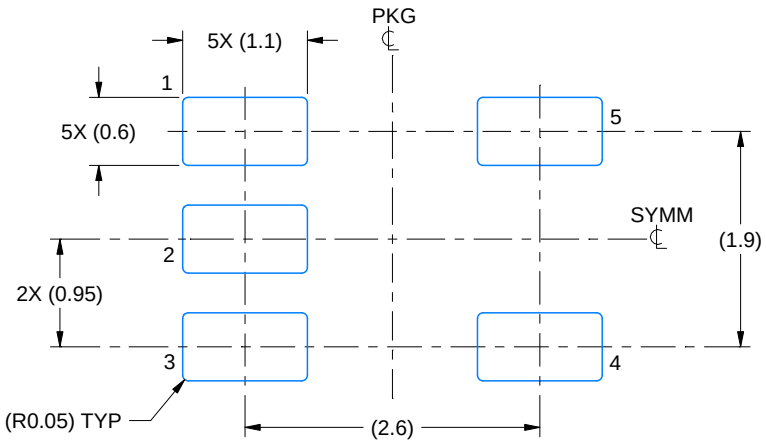
SMALL OUTLINE TRANSISTOR



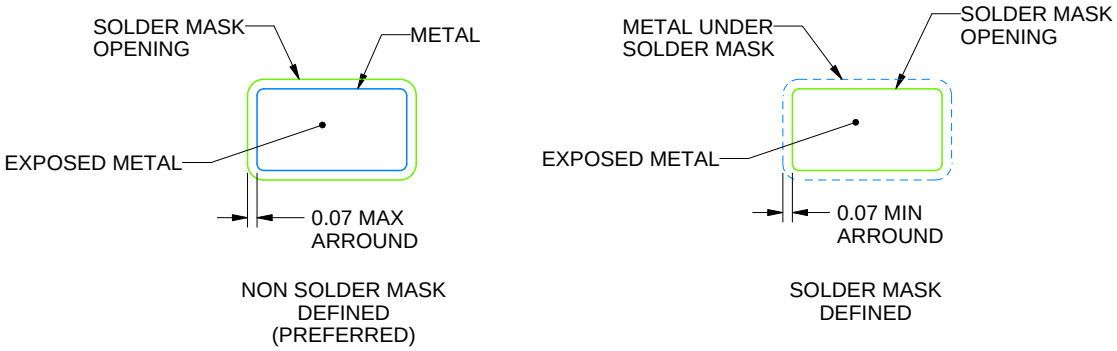
4214839/E 09/2019

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Refernce JEDEC MO-178.
4. Body dimensions do not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:15X

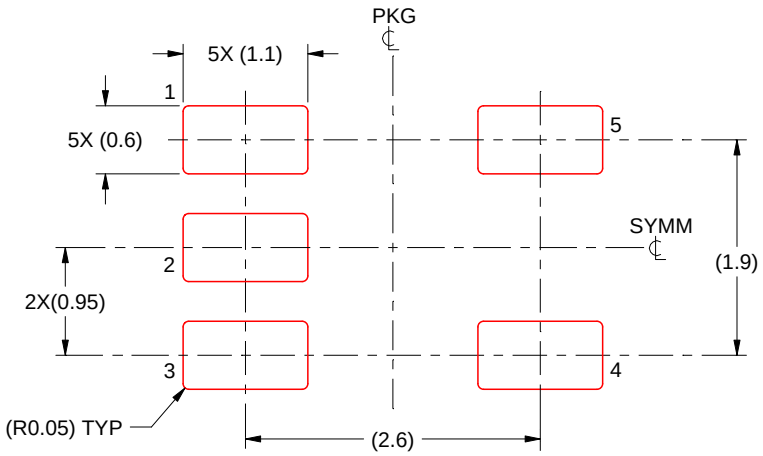


SOLDER MASK DETAILS

4214839/E 09/2019

NOTES: (continued)

5. Publication IPC-7351 may have alternate designs.
6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:15X

4214839/E 09/2019

NOTES: (continued)

7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
8. Board assembly site may have different recommendations for stencil design.

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