Dual 150mA Ultra Low-Dropout Regulator

Check for Samples: LP2966

FEATURES

- **Ultra Low Drop-Out Voltage**
- **Low Ground Pin Current**
- **<1µA Quiescent Current in Shutdown Mode**
- **Independent Shutdown of Each LDO Regulator**
- **Output Voltage Accuracy ±1%**
- **Ensured 150mA Output Current at Each Output**
- **Low Output Noise**
- **Error Flags Indicate Status of Each Output**
- **Available in VSSOP-8 Surface Mount Package**
- **Low Output Capacitor Requirements (1µF)**
- **Operates with Low ESR Ceramic Capacitors in Most Applications**
- **Over Temperature/Over Current Protection**
- **-40°C to +125°C Junction Temperature Range**

APPLICATIONS

- **Cellular and Wireless Applications**
- **Palmtop/Laptop Computer**
- **GPS Systems**
- **Flat Panel Displays**
- **Post Regulators**
- **USB Applications**
- **Hand Held Equipment and Multimeters**
- **Wireless Data Terminals**
- **Other Battery Powered Applications**

KEY SPECIFICATIONS

- **Dropout Voltage: Varies Linearly with Load Current. Typically 0.9 mV at 1mA Load Current and 135mV at 150mA Load Current**
- **Ground Pin Current: Typically 300µA at 1mA Load Current and 340µA at 100mA Load Current (with One Shutdown Pin Pulled Low)**
- **Shutdown Mode: Less than 1µA Quiescent Current when Both Shutdown Pins are Pulled Low**
- **Error Flag: Open Drain Output, Goes Low when the Corresponding Output Drops 10% Below Nominal**
- **Precision Output Voltage: Multiple Output Voltage Options Available Ranging from 1.8V to 5.0V with an Ensured Accuracy of ±1% at Room Temperature**

DESCRIPTION

The LP2966 dual ultra low-dropout (LDO) regulator operates from a +2.70V to +7.0V input supply. Each output delivers 150mA over full temperature range. The IC operates with extremely low drop-out voltage and quiescent current, which makes it very suitable for battery powered and portable applications. Each LDO in the LP2966 has independent shutdown capability. The LP2966 provides low noise performance with low ground pin current in an extremely small VSSOP-8 package (refer to package dimensions and CONNECTION DIAGRAM for more information on VSSOP-8 package). A wide range of preset voltage options are available for each output. In addition, many more are available upon request with minimum orders. In all, 256 voltage combinations are possible.

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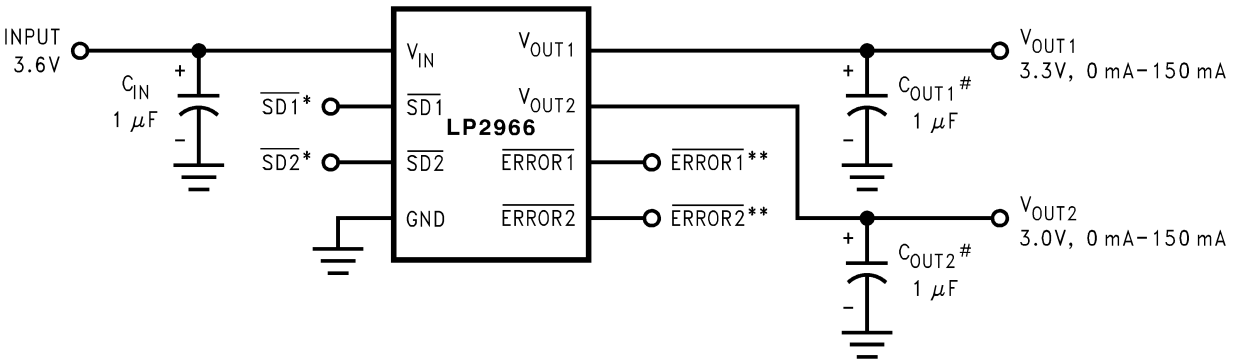
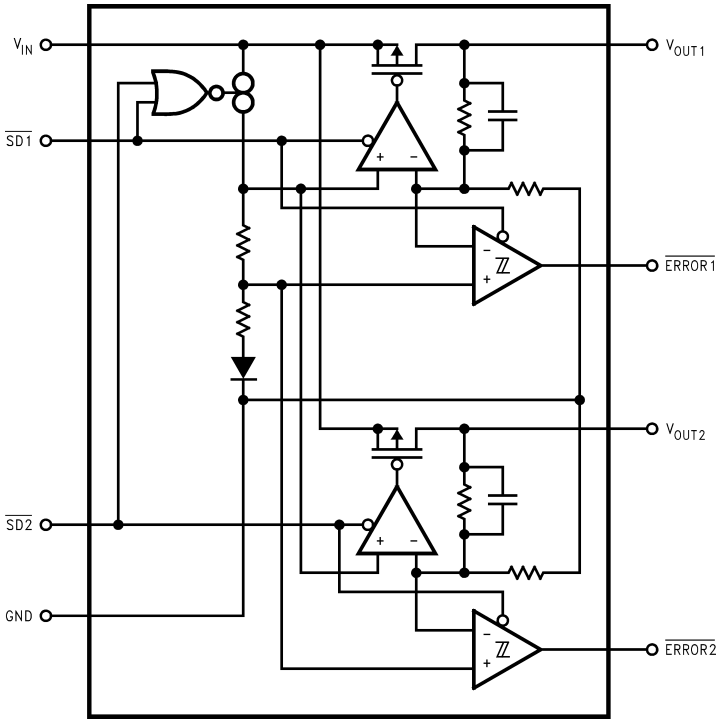
TYPICAL APPLICATION CIRCUIT



*$\overline{SD1}$ and $\overline{SD2}$ must be actively terminated through a pull up resistor. Tie to V_{IN} if not used.
**$\overline{ERROR1}$ and $\overline{ERROR2}$ are open drain outputs. These pins must be connected to ground if not used.
Minimum output capacitance is 1µF to insure stability over full load current range. More capacitance improves superior dynamic performance and provides additional stability margin.

BLOCK DIAGRAM



CONNECTION DIAGRAM

Top View

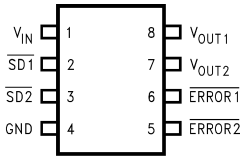


Figure 1. VSSOP-8 Package
8-Lead Small Outline Integrated Circuit
See Package Number DGK0008A

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PIN DESCRIPTIONS

Pin	Name	Function
1	VIN	Input Supply pin
2	$\overline{SD1}$	Active low shutdown pin for output 1
3	$\overline{SD2}$	Active low shutdown pin for output 2
4	GND	Ground
5	$\overline{ERROR2}$	Error flag for output 2 - Normally high impedance, should be connected to ground if not used.
6	$\overline{ERROR1}$	Error flag for output 1 - Normally high impedance, should be connected to ground if not used.
7	VOUT2	Output 2
8	VOUT1	Output 1

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

ABSOLUTE MAXIMUM RATINGS(1)(2)

Storage Temperature Range	−65 to +150°C
Lead Temp. (Soldering, 5 sec.)	260°C
Power Dissipation(3)	Internally Limited
ESD Rating(4)	2kV
Input Supply Voltage (Survival)	−0.3V to 7.5V
Shutdown Input Voltage (Survival)	−0.3V to (Vin + 0.3V)
Maximum Voltage for $\overline{ERROR}$ Pins	10V
I_{OUT} (Survival)	Short Circuit Protected
Output Voltage (Survival)(5)(6)	−0.3V to (Vin + 0.3V)

(1) Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Operating ratings indicate conditions for which the device is intended to be functional, but do not ensure specific performance limits. For ensured specifications and test conditions, see ELECTRICAL CHARACTERISTICS. The ensured specifications apply only for the test conditions listed. Some performance characteristics may degrade when the device is not operated under the listed test conditions.
(2) If Military/Aerospace specified devices are required, please contact the Texas Instruments Sales Office/ Distributors for availability and specifications.
(3) At elevated temperatures, devices must be derated based on package thermal resistance. The device in the surface-mount package must be derated at θ_{jA} = 235°C/W, junction-to-ambient. Please refer to APPLICATIONS INFORMATION: Maximum Current Capability for further information. The device has internal thermal protection.
(4) The human body model is a 100pF capacitor discharged through a 1.5kΩ resistor into each pin.
(5) If used in a dual-supply system where the regulator load is returned to a negative supply, the LP2966 output must be diode-clamped to ground.
(6) The output PMOS structure contains a diode between the V_{IN} and V_{OUT} terminals that is normally reverse-biased. Reversing the polarity from V_{IN} and V_{OUT} will turn on this diode.

OPERATING RATINGS(1)

Input Supply Voltage	2.7V to 7.0V
Shutdown Input Voltage	−0.3V to (Vin + 0.3V)
Operating Junction Temperature Range	−40°C to +125°C
Maximum Voltage for $\overline{ERROR}$ pins	10V

(1) Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Operating ratings indicate conditions for which the device is intended to be functional, but do not ensure specific performance limits. For ensured specifications and test conditions, see ELECTRICAL CHARACTERISTICS. The ensured specifications apply only for the test conditions listed. Some performance characteristics may degrade when the device is not operated under the listed test conditions.

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ELECTRICAL CHARACTERISTICS

Limits in standard typeface are for T_j = 25°C, and limits in **boldface type** apply over the full operating junction temperature range. Unless otherwise specified, $V_{IN} = V_{O(NOM)} + 1V$[1], C_{OUT} = 1µF, I_{OUT} = 1mA, C_{IN} = 1µF, $V_{SD1} = V_{SD2} = V_{IN}$.

Symbol	Parameter	Conditions	Typ[2]	LP2966IMM[3]		Unit
				Min	Max	
V_O[4]	Output Voltage Tolerance	V_{OUT} + 1V < V_{IN} < 7.0V	0.0	−1	1	%V_{NOM}
				-3	**3**	
		1mA < I_L < 100mA	0.0	−1.5	1.5	%V_{NOM}
				-3.5	**3.5**	
$\Delta V_O/\Delta V_{IN}$[4][5]	Output Voltage Line Regulation		0.1			mV/V
$\Delta V_O/\Delta I_{OUT}$	Output Voltage Load Regulation[6]	1mA < I_L< 100mA[6]	0.1			mV/mA
$\Delta V_{O2}/\Delta I_{OUT1}$	Output Voltage Cross Regulation[7]	1mA < I_{L1}< 100mA[7]	0.0004			mV/mA
V_{IN} -V_{OUT}	Dropout Voltage[8]	I_L = 1mA	0.9		2.0	mV
					3.0	
		I_L = 100mA	90		130	
					180	
		I_L = 150mA	135		195	
					270	
$I_{GND(1,0)}$[9]	Ground Pin Current (One LDO On)	I_L = 1mA V_{SD2} ≤ 0.1V, V_{SD1}= V_{IN}	**300**			µA
		I_L = 100mA V_{SD2} ≤ 0.1V, V_{SD1}= V_{IN}	**340**			
$I_{GND(1,1)}$	Ground Pin Current (Both LDOs On)	I_L = 1mA	340		450	µA
					500	
		I_L = 100mA	420		540	
					600	
$I_{GND(0,0)}$	Ground Pin Current in Shutdown Mode	V_{SD1}= V_{SD2} ≤ 0.1V	0.006		0.3	µA
					10	
$I_{O(PK)}$	Peak Output Current	See[10] V_{OUT}≥ $V_{OUT(NOM)}$- 5%	500	350		mA
				150		
Short Circuit Foldback Protection						
I_{FB}	Short Circuit Foldback Knee	See[10][11]	600			mA

(1) The condition $V_{IN} = V_{O(NOM)}$ + 1V applies when Vout1 = Vout2. If Vout1 ≠ Vout2, then this condition would apply to the output which is greater in value. As an example, if Vout1 = 3.3V and Vout2 = 5V, then the condition $V_{IN} = V_{O(NOM)}$+ 1V would apply to Vout2 only.
(2) :Typical numbers are at 25°C and represent the most likely parametric norm.
(3) :Limits are 100% production tested at 25°C. Limits over the operating temperature range are ensured through correlation using Statistical Quality Control (SQC) methods. The limits are used to calculate Averaging Outgoing Quality Level (AOQL).
(4) Output voltage tolerance specification also includes the line regulation and load regulation.
(5) Output voltage line regulation is defined as the change in output voltage from the nominal value due to change in input line voltage.
(6) Output voltage load regulation is defined as the change in output voltage from the nominal value when the load current changes from 1mA to 100mA.
(7) Output voltage cross regulation is defined as the percentage change in the output voltage from the nominal value at one output when the load current changes from 1mA to full load in the other output. This is an important parameter in multiple output regulators. The specification for $\Delta V_{O1}/\Delta I_{OUT2}$ is equal to the specification for $\Delta V_{O2}/\Delta I_{OUT1}$.
(8) Dropout voltage is defined as the input to output differential at which the output voltage drops 100mV below the nominal value. Drop-out voltage specification applies only to output voltages greater than 2.7V. For output voltages below 2.7V, the drop-out voltage is nothing but the input to output differential, since the minimum input voltage is 2.7V.
(9) The limits for the ground pin current specification, $I_{GND(0,1)}$ will be same as the limits for the specification, $I_{GND(1,0)}$.
(10) At elevated temperatures, devices must be derated based on package thermal resistance. The device in the surface-mount package must be derated at θ_{jA} = 235°C/W, junction-to-ambient. Please refer to APPLICATIONS INFORMATION: Maximum Current Capability for further information. The device has internal thermal protection.
(11) LP2966 has fold back current limited short circuit protection. The knee is the current at which the output voltage drops 10% below the nominal value.

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ELECTRICAL CHARACTERISTICS (continued)

Limits in standard typeface are for T_j = 25°C, and limits in **boldface type** apply over the full operating junction temperature range. Unless otherwise specified, $V_{IN} = V_{O(NOM)} + 1V$[1], C_{OUT} = 1µF, I_{OUT} = 1mA, C_{IN} = 1µF, $V_{SD1} = V_{SD2} = V_{IN}$.

Symbol	Parameter	Conditions	Typ[2]	LP2966IMM[3]		Unit
				Min	Max	
Over Temperature Protection						
Tsh(t)	Shutdown Threshold		165			°C
Tsh(h)	Thermal Shutdown Hysteresis		25			°C
Shutdown Input						
V_{SDT}	Shutdown Threshold[12]	Output = Low	0		**0.1**	V
		Output = High	V_{IN}	**V_{IN} - 0.1**		
T_{dOFF}	Turn-off Delay[13]	I_L = 100 mA	20			µsec
T_{dON}	Turn-on Delay[13]	I_L = 100 mA	25			µsec
I_{SD}	SD Input Current	$V_{SD} = V_{IN}$	1			nA
		V_{SD} = 0 V	1			
Error Flag Comparators						
V_T	Threshold (output goes high to low)	See[14]	10	**5**	**16**	%
V_{TH}	Threshold Hysteresis	See[14]	5	**2**	**8**	%
$V_{ERR(Sat)}$	Error Flag Saturation	I_{Fsink} = 100µA	0.015		**0.1**	V
$I_{EF(leak)}$	Error Flag Pin Leakage Current		1			nA
$I_{(EFsink)}$	Error Flag Pin Sink Current		1			mA
AC Parameters						
PSRR	Ripple Rejection	$V_{IN} = V_{OUT}$ + 1V, f = 120Hz, V_{OUT} = 3.3V	60			dB
		$V_{IN} = V_{OUT}$ + 0.3V, f = 120Hz, V_{OUT} = 3.3V	40			
ρn(1/f)	Output Noise Density	f =120Hz	1			µV/√Hz
e_n	Output Noise Voltage (rms)	BW = 10Hz − 100kHz, C_{OUT} = 10µF	150			µV(rms)
		BW = 300Hz − 300kHz, C_{OUT} = 10µF	100			

(12) V_{SDT} is the shutdown pin voltage threshold below which the output is disabled.
(13) Turn-on delay is the time interval between the low to high transition on the shutdown pin to the output voltage settling to within 5% of the nominal value. Turn-off delay is the time interval between the high to low transition on the shutdown pin to the output voltage dropping below 50% of the nominal value. The external load impedance influences the output voltage decay in shutdown mode.
(14) Error Flag threshold and hysteresis are specified as the percentage below the regulated output voltage.

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TYPICAL PERFORMANCE CHARACTERISTICS

Unless otherwise specified, V_{IN} =$V_{O(NOM)}$ + 1V, V_{OUT}= 3.3V, C_{OUT} =1µF, I_{OUT} = 1mA, C_{IN} =1µF, V_{SD1} = V_{SD2} = V_{IN}, and T_A = 25°C.

Ground Pin Current vs Supply Voltage (one LDO on)

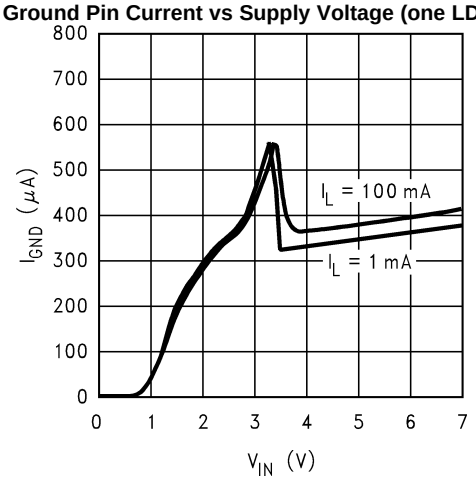

Figure 2.

Ground Pin Current vs Supply Voltage (both LDOs on)

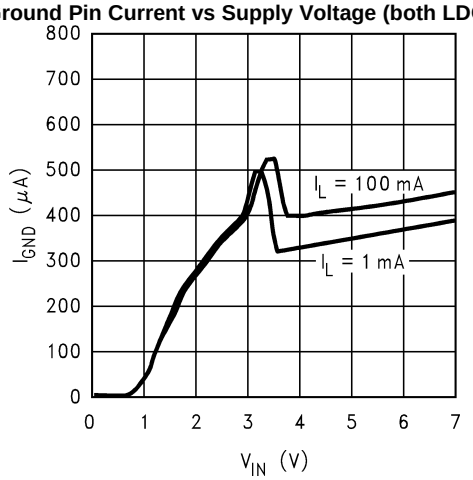

Figure 3.

Ground Pin Current vs Load Current over temperature (one LDO on)

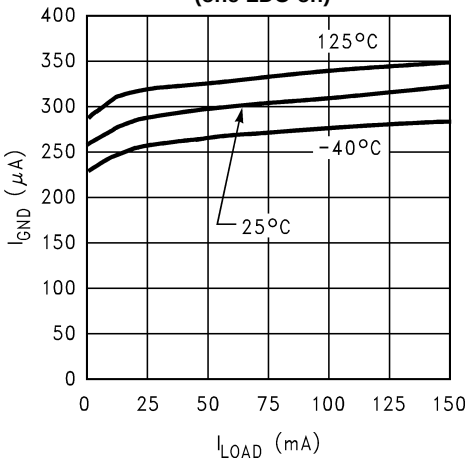

Figure 4.

Ground Pin Current vs Load Current over temperature (both LDOs on)

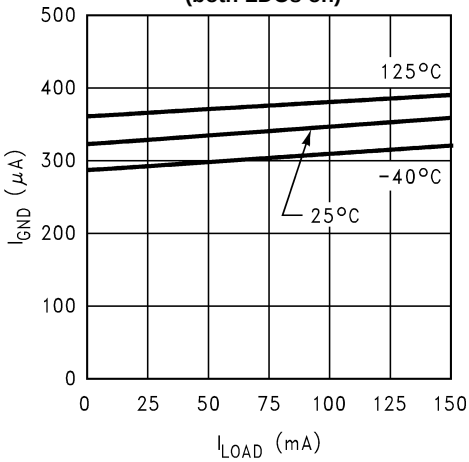

Figure 5.

Output Voltage vs Temperature

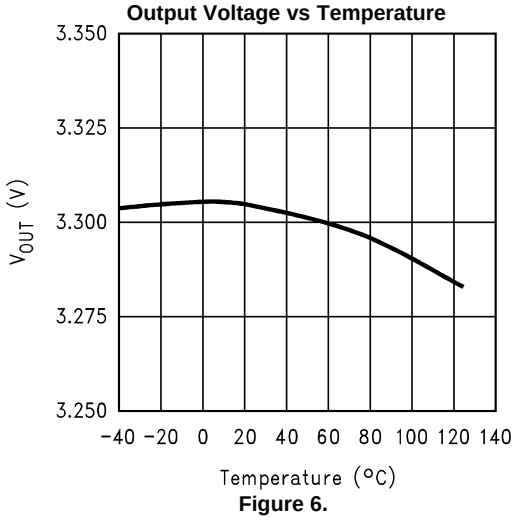

Figure 6.

Drop-out Voltage vs Temperature

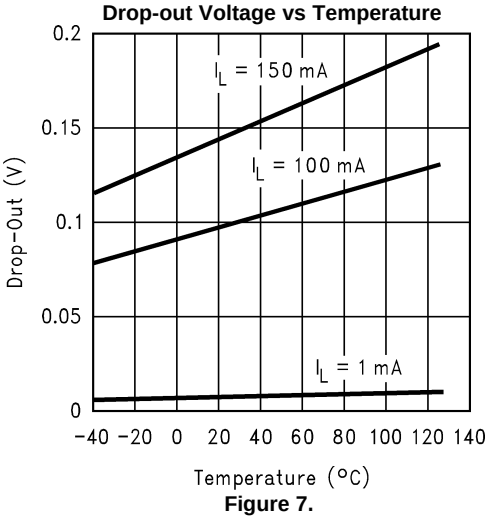

Figure 7.

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TYPICAL PERFORMANCE CHARACTERISTICS (continued)

Unless otherwise specified, V_{IN} =$V_{O(NOM)}$ + 1V, V_{OUT}= 3.3V, C_{OUT} =1µF, I_{OUT} = 1mA, C_{IN} =1µF, V_{SD1} = V_{SD2} = V_{IN}, and T_A = 25°C.

Input Voltage vs Output Voltage

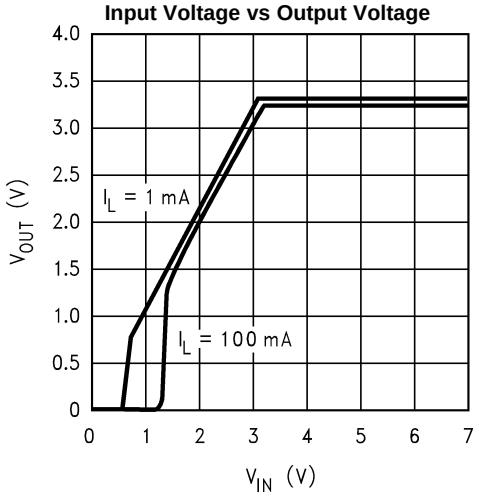

Figure 8.

Ground Pin Current vs Shutdown Pin Voltage

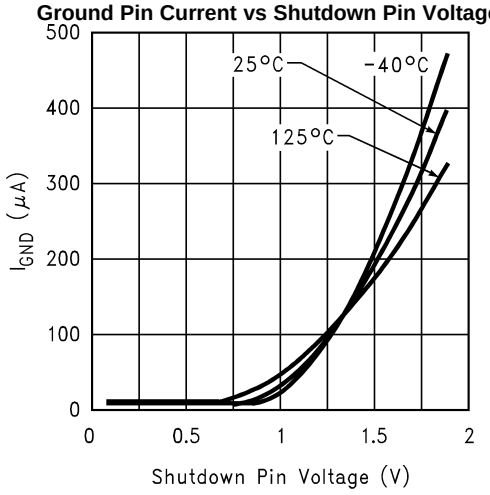

Figure 9.

Ground Pin Current vs Input Voltage (Both LDOs off)

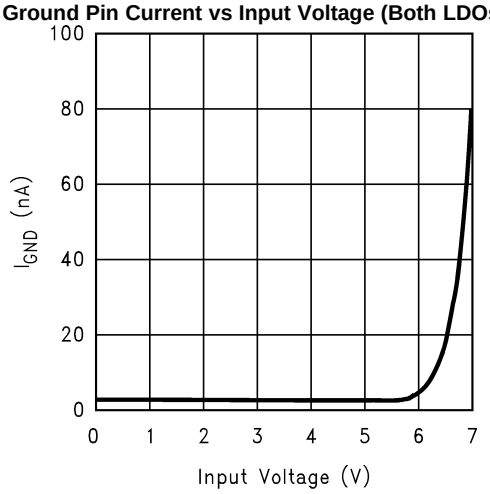

Figure 10.

Short-Circuit Foldback Protection

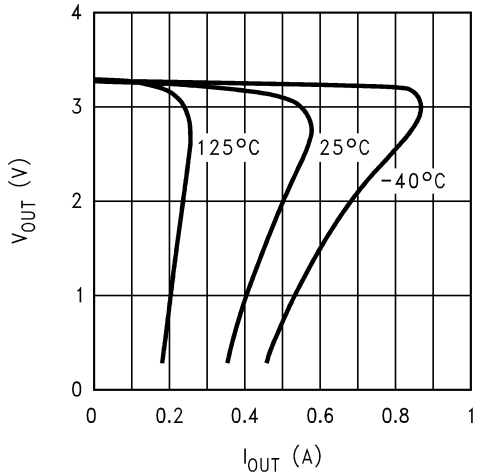

Figure 11.

Line Transient Response
(C_{OUT} = 2.2µF, I_{OUT} = 1mA)

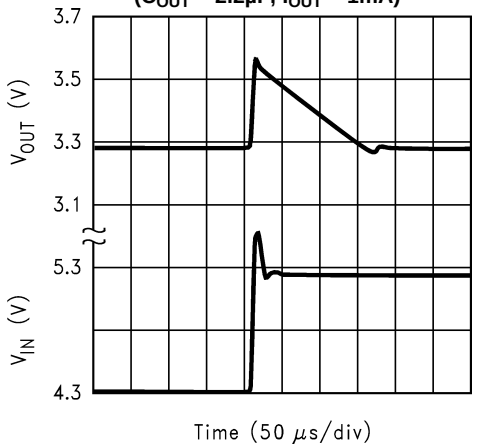

Figure 12.

Line Transient Response
(C_{OUT} = 2.2µF, I_{OUT} = 1mA)

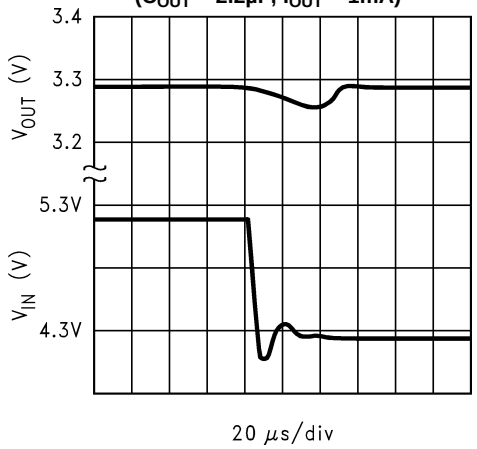

Figure 13.

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TYPICAL PERFORMANCE CHARACTERISTICS (continued)

Unless otherwise specified, V_{IN} =$V_{O(NOM)}$ + 1V, V_{OUT}= 3.3V, C_{OUT} =1µF, I_{OUT} = 1mA, C_{IN} =1µF, V_{SD1} = V_{SD2} = V_{IN}, and T_A = 25°C.

Line Transient Response
(C_{OUT} = 2.2µF, I_{OUT} = 100mA)

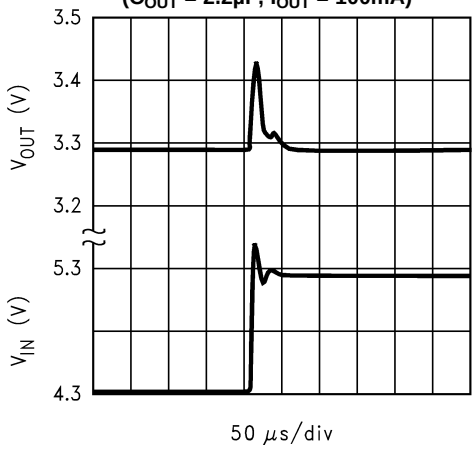

Figure 14.

Line Transient Response
(C_{OUT} = 2.2µF, I_{OUT} = 100mA)

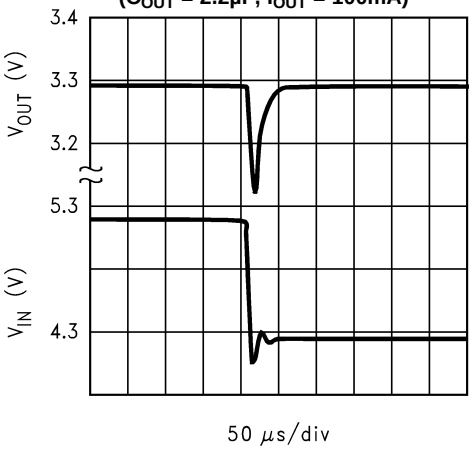

Figure 15.

Line Transient Response
(C_{OUT} = 10µF, I_{OUT} = 1mA)

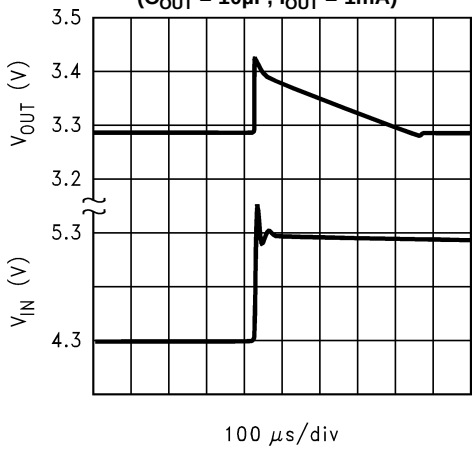

Figure 16.

Line Transient Response
(C_{OUT} = 10µF, I_{OUT} = 1mA)

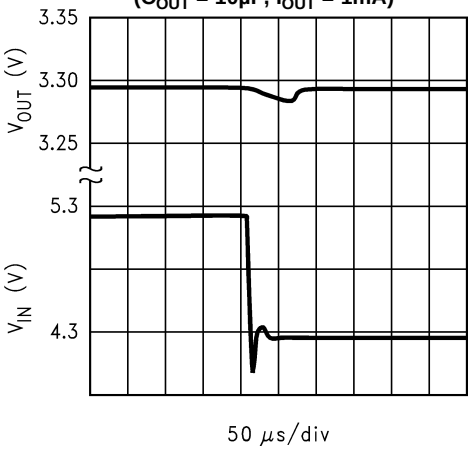

Figure 17.

Line Transient Response
(C_{OUT} = 10µF, I_{OUT} = 100mA)

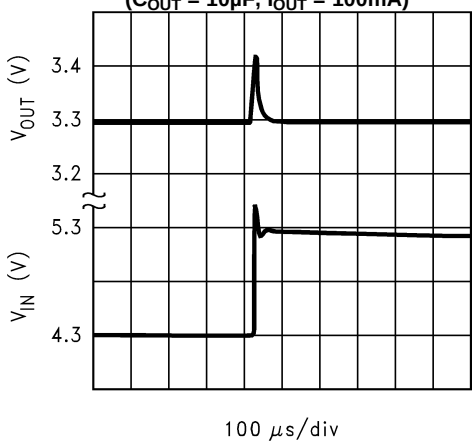

Figure 18.

Line Transient Response
(C_{OUT} = 10µF, I_{OUT} = 100mA)

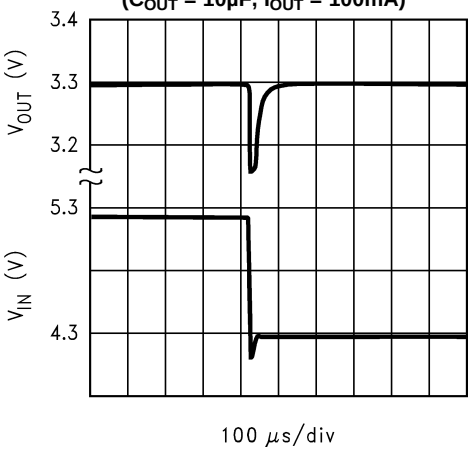

Figure 19.

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TYPICAL PERFORMANCE CHARACTERISTICS (continued)

Unless otherwise specified, $V_{IN} = V_{O(NOM)} + 1V$, $V_{OUT} = 3.3V$, $C_{OUT} = 1\mu F$, $I_{OUT} = 1mA$, $C_{IN} = 1\mu F$, $V_{SD1} = V_{SD2} = V_{IN}$, and $T_A = 25°C$.

Load Transient Response (C_{OUT} = 2.2µF)

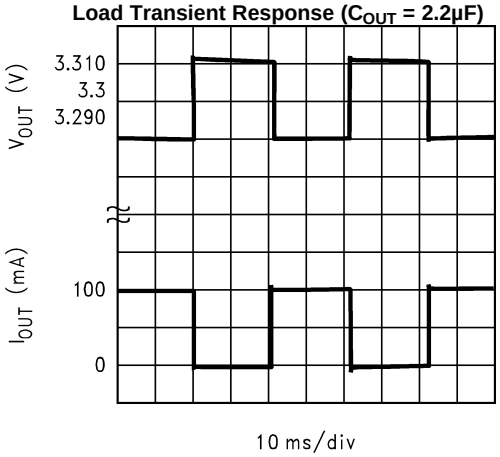

Figure 20.

Load Transient Response (C_{OUT} = 10µF)

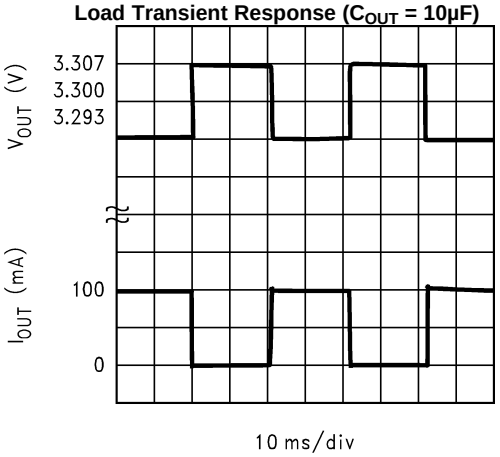

Figure 21.

Load Transient Response (C_{OUT} = 10µF)

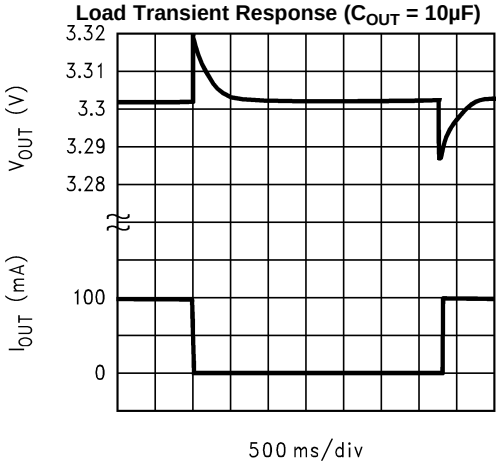

Figure 22.

Load Transient Response (C_{OUT} = 2.2µF)

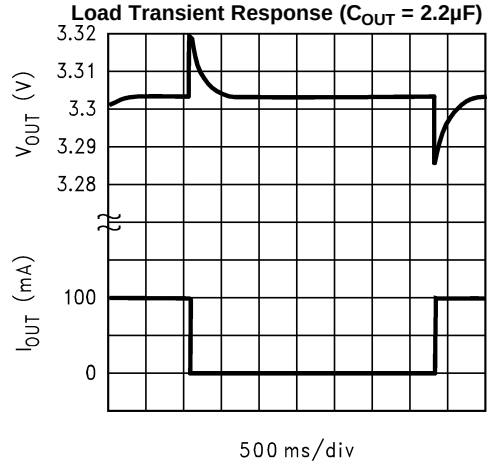

Figure 23.

Cross-Channel Isolation vs Frequency (I_{OUT1} =1mA, I_{OUT2} = 1mA)

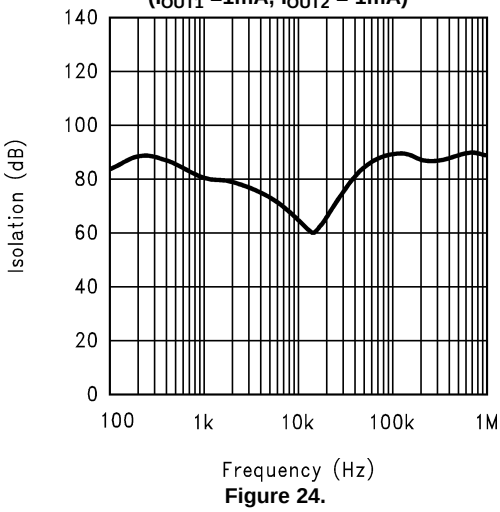

Figure 24.

Cross-Channel Isolation vs Frequency (I_{OUT1} = I_{OUT2} = 100mA)

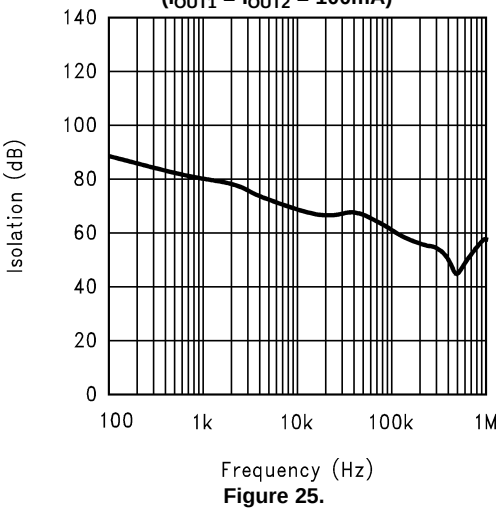

Figure 25.

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TYPICAL PERFORMANCE CHARACTERISTICS (continued)

Unless otherwise specified, $V_{IN} = V_{O(NOM)} + 1V$, $V_{OUT} = 3.3V$, $C_{OUT} = 1\mu F$, $I_{OUT} = 1mA$, $C_{IN} = 1\mu F$, $V_{SD1} = V_{SD2} = V_{IN}$, and $T_A = 25°C$.

Output Voltage Cross-Coupling

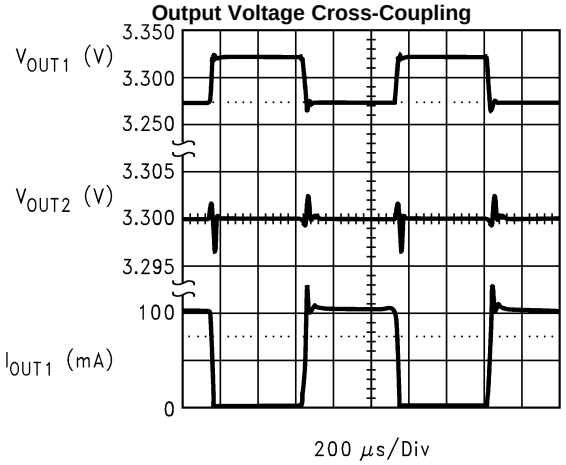

Figure 26.

Output Noise Density

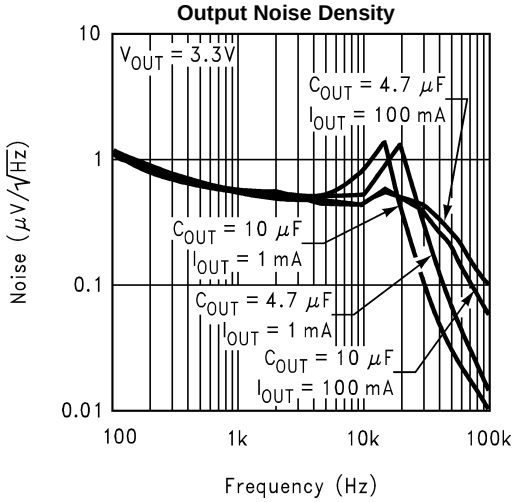

Figure 27.

Power Supply Ripple Rejection

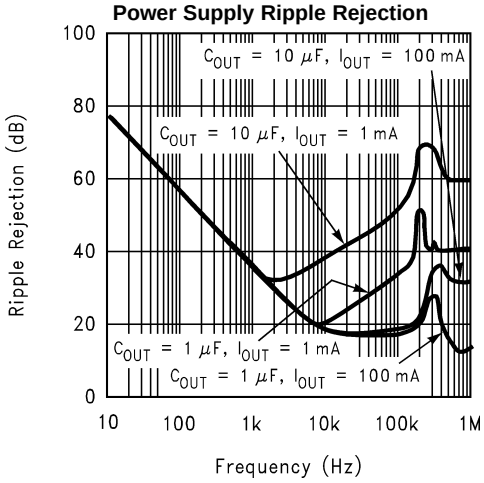

Figure 28.

Peak Output Current vs Temperature

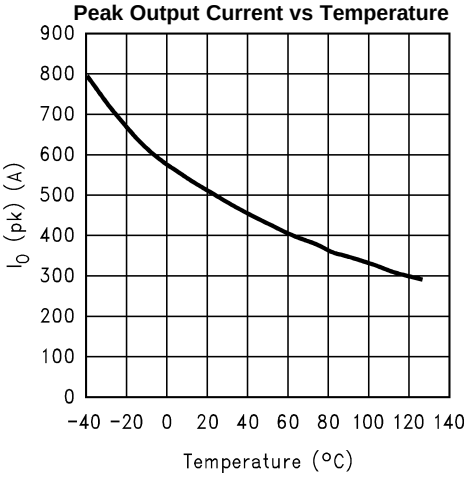

Figure 29.

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APPLICATIONS INFORMATION

Input Capacitor Selection

LP2966 requires a minimum input capacitance of 1µF between the input and ground pins to prevent any impedance interactions with the supply. This capacitor should be located very close to the input pin. This capacitor can be of any type such as ceramic, tantalum, or aluminium. Any good quality capacitor which has good tolerance over temperature and frequency is recommended.

Output Capacitor Selection

The LP2966 requires a minimum of 1µF capacitance on each output for proper operation. To insure stability, this capacitor should maintain its ESR (equivalent series resistance) in the stable region of the ESR curves (Figure 30 and Figure 31) over the full operating temperature range of the application. The output capacitor should have a good tolerance over temperature, voltage, and frequency. The output capacitor can be increased without limit. Larger capacitance provides better stability and noise performance. The output capacitor should be connected very close to the Vout pin of the IC.

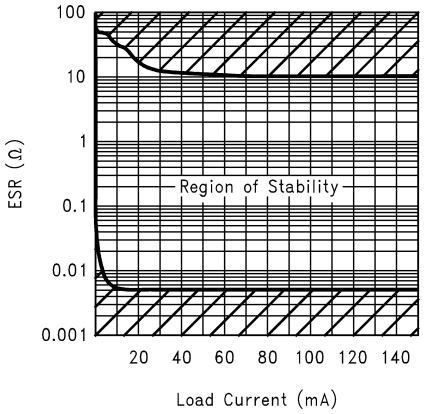

Figure 30. ESR Curve for V_{OUT} = 5V and C_{OUT} = 2.2µF

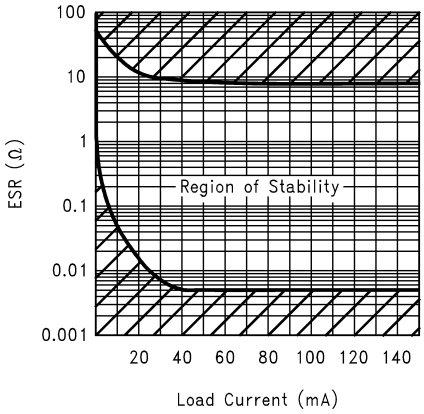

Figure 31. ESR Curve for V_{OUT} = 3.3V and C_{OUT} = 2.2µF

LP2966 works best with Tantalum capacitors. However, the ESR and the capacitance value of these capacitors vary a lot with temperature, voltage, and frequency. So while using Tantalum capacitors, it should be ensured that the ESR is within the limits for stability over the full operating temperature range.

For output voltages greater than 2.5V, good quality ceramic capacitors (such as the X7R series from Taiyoyuden) can also be used with LP2966 in applications not requiring light load operation (< 5mA for the 5V output option). Once again, it should be ensured that the capacitance value and the ESR are within the limits for stability over the full operating temperature range.

The ESRD Series Polymer Aluminium Electrolytic capacitors from Cornell Dubilier are very stable over temperature and frequency. The excellent capacitance and ESR tolerance of these capacitors over voltage, temperature and frequency make these capacitors very suitable for use with LDO regulators.

Output Noise

Noise is specified in two ways:

Spot Noise or **Output Noise Density** is the RMS sum of all noise sources, measured at the regulator output, at a specific frequency (measured with a 1Hz bandwidth). This type of noise is usually plotted on a curve as a function of frequency.

Total Output Noise or **Broad-Band Noise** is the RMS sum of spot noise over a specified bandwidth, usually several decades of frequencies.

Attention should be paid to the units of measurement. Spot noise is measured in units µV/$\sqrt{Hz}$ or nV/$\sqrt{Hz}$ and total output noise is measured in µV(rms).

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The primary source of noise in low-dropout regulators is the internal reference. In CMOS regulators, noise has a low frequency component and a high frequency component, which storngly depend on the silicon area and quiescent current. Noise can be reduced in two ways: by increasing the transistor area or by increasing the current drawn by the internal reference. Increasing the area will increase the die size and decreases the chance of fitting the die into a small package. Increasing the current drawn by the internal reference increases the total supply current (ground pin current) of the IC. Using an optimized trade-off of ground pin current and die size, LP2966 achieves low noise performance with low quiescent current in an VSSOP-8 package.

Short-Circuit Foldback Protection

In the presence of a short or excessive load current condition, the LP2966 uses an internal short circuit foldback mechanism that regulates the maximum deliverable output current. A strong negative temperature coefficient is designed into the circuit to enable extremely higher peak output current capability (in excess of 400mA per output at room temperature, see TYPICAL PERFORMANCE CHARACTERISTICS). Thus, a system designer using the LP2966 can achieve higher peak output current capability in applications where the LP2966 internal junction temperature is kept below 125°C. Refer to APPLICATIONS INFORMATION on calculating the maximum output current capability of the LP2966 for your application.

Error Flag Operation

The LP2966 produces a logic low signal at the Error Flag pin ($\overline{\text{ERROR}}$) when the corresponding output drops out of regulation due to low input voltage, current limiting, or thermal limiting. This flag has a built in Hysteresis. The timing diagram in Figure 32 shows the relationship between the $\overline{\text{ERROR}}$ and the output voltage. In this example, the input voltage is changed to demonstrate the functionality of the Error Flag.

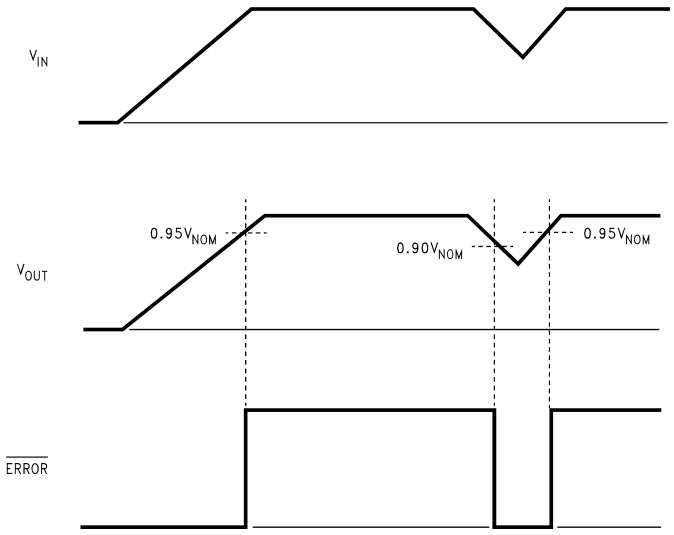

Figure 32. Error Flag Operation

The internal error flag comparators have open drain output stages. Hence, the $\overline{\text{ERROR}}$ pins should be pulled high through a pull up resistor. Although the $\overline{\text{ERROR}}$ pin can sink current of 1mA, this current adds to the battery drain. Hence, the value of the pull up resistor should be in the range of 100kΩ to 1MΩ. **The $\overline{\text{ERROR}}$ pins must be connected to ground if this function is not used.** It should also be noted that when the shutdown pins are pulled low, the $\overline{\text{ERROR}}$ pins are forced to be invalid for reasons of saving power in shutdown mode.

Shutdown Operation

The two LDO regulators in the LP2966 have independent shutdown. A CMOS Logic level signal at the shutdown ($\overline{\text{SD}}$) pin will turn-off the corresponding regulator. Pins $\overline{\text{SD1}}$ and $\overline{\text{SD2}}$ must be actively terminated through a 100kΩ pull-up resistor for a proper operation. If these pins are driven from a source that actively pulls high and low (such as a CMOS rail to rail comparator), the pull-up resistor is not required. These pins must be tied to Vin if not used.

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Drop-Out Voltage

The drop-out voltage of a regulator is defined as the minimum input-to-output differential required to stay within 100mV of the output voltage measured with a 1V differential. The LP2966 uses an internal MOSFET with an Rds(on) of 1Ω. For CMOS LDOs, the drop-out voltage is the product of the load current and the Rds(on) of the internal MOSFET.

Reverse Current Path

The internal MOSFET in the LP2966 has an inherent parasitic diode. During normal operation, the input voltage is higher than the output voltage and the parasitic diode is reverse biased. However, if the output is pulled above the input in an application, then current flows from the output to the input as the parasitic diode gets forward biased. The output can be pulled above the input as long as the current in the parasitic diode is limited to 150mA.

Maximum Output Current Capability

Each output in the LP2966 can deliver a current of more than 150mA over the full operating temperature range. However, the maximum output current capability should be derated by the junction temperature. Under all possible conditions, the junction temperature must be within the range specified under operating conditions. The LP2966 is available in VSSOP-8 package. This package has a junction to ambient temperature coefficient (θ_{ja}) of 235 °C/W with minimum amount of copper area. The total power dissipation of the device is approximately given by:

$$P_D = (V_{in} - V_{OUT1})I_{OUT1} + (V_{in}-V_{OUT2})I_{OUT2} \quad (1)$$

The maximum power dissipation, P_{Dmax}, that the device can tolerate can be calculated by using the formula:

$$P_{Dmax} = (T_{jmax} - T_A)/\theta_{ja}$$

where

- T_{jmax} is the maximum specified junction temperature (125°C)
- T_A is the ambient temperature (2)

Figure 33 through Figure 37 show the variation of thermal coefficient with different layout scenarios.

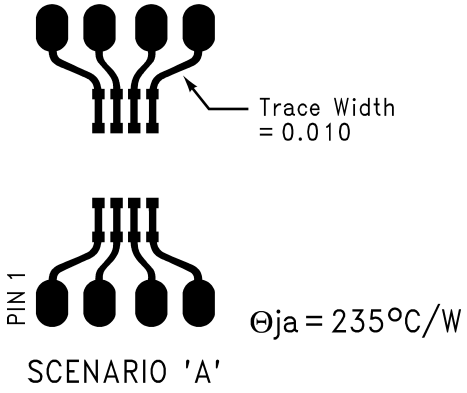

Figure 33.

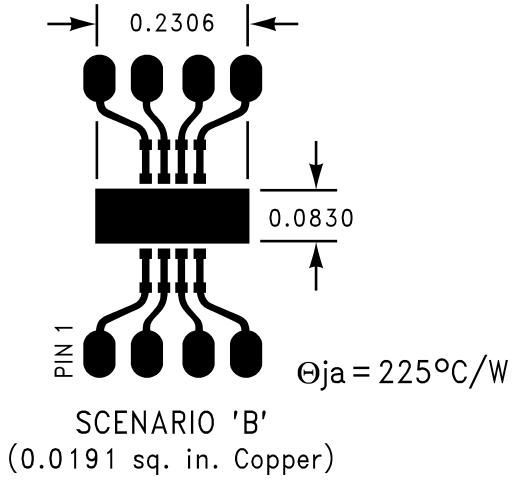

Figure 34.

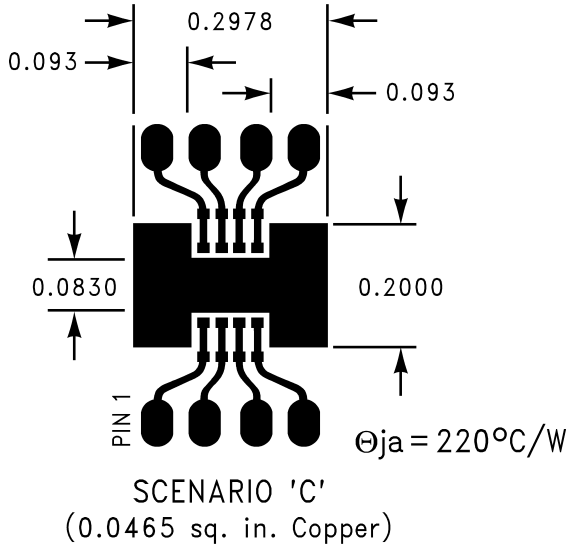

Figure 35.

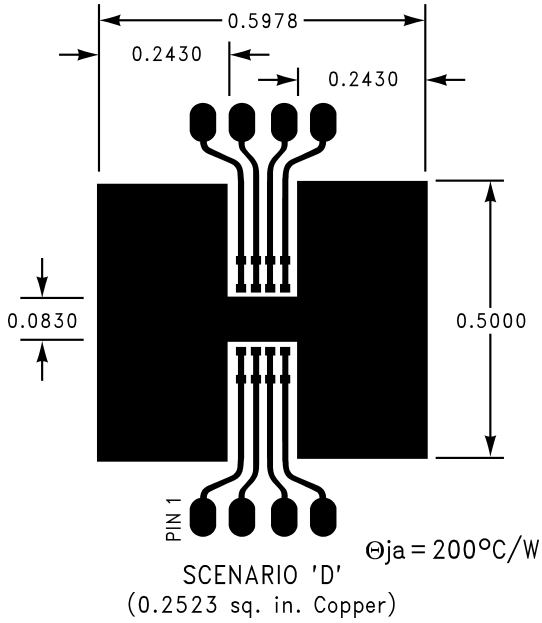

Figure 36.

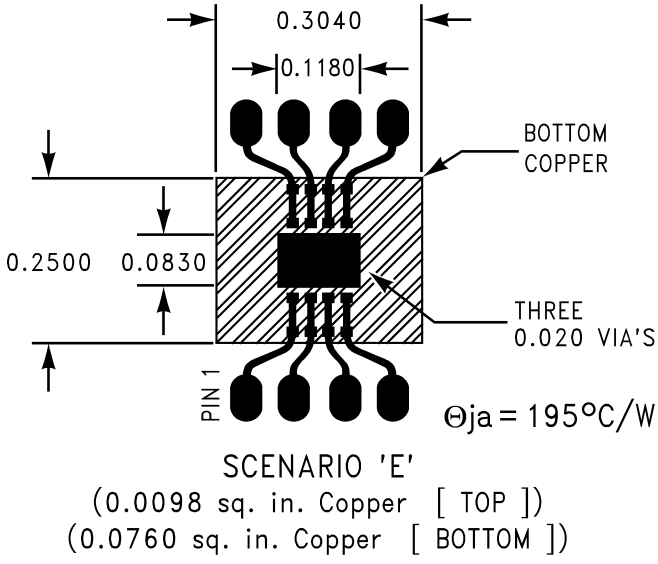

Figure 37.

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REVISION HISTORY

Changes from Revision D (April 2013) to Revision E	Page
• Changed layout of National Data Sheet to TI format	14

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PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
LP2966IMM-1833/NOPB	ACTIVE	VSSOP	DGK	8	1000	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 125	LCFB	Samples
LP2966IMM-2518/NOPB	ACTIVE	VSSOP	DGK	8	1000	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM		LJKB	Samples
LP2966IMM-2525/NOPB	ACTIVE	VSSOP	DGK	8	1000	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 125	LAAB	Samples
LP2966IMM-2828/NOPB	ACTIVE	VSSOP	DGK	8	1000	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 125	LABB	Samples
LP2966IMM-3325	NRND	VSSOP	DGK	8	1000	TBD	Call TI	Call TI		LARB	
LP2966IMM-3325/NOPB	ACTIVE	VSSOP	DGK	8	1000	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM		LARB	Samples
LP2966IMM-5050/NOPB	ACTIVE	VSSOP	DGK	8	1000	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 125	LAFB	Samples
LP2966IMMX-3325/NOPB	ACTIVE	VSSOP	DGK	8	3500	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM		LARB	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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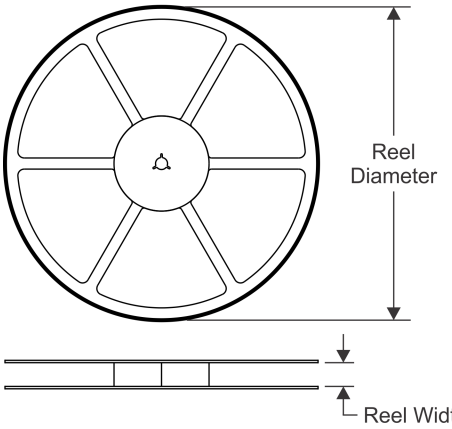
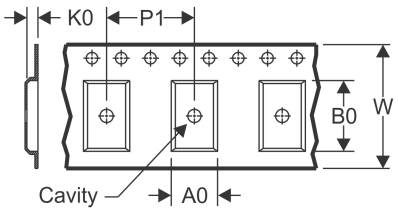
TAPE AND REEL INFORMATION

REEL DIMENSIONS

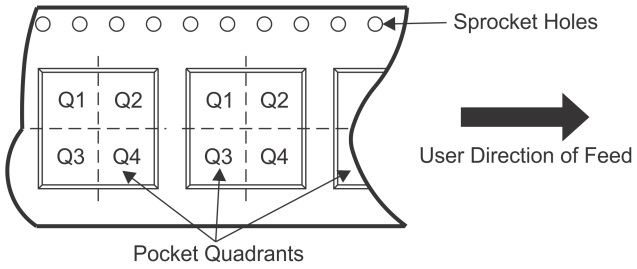


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

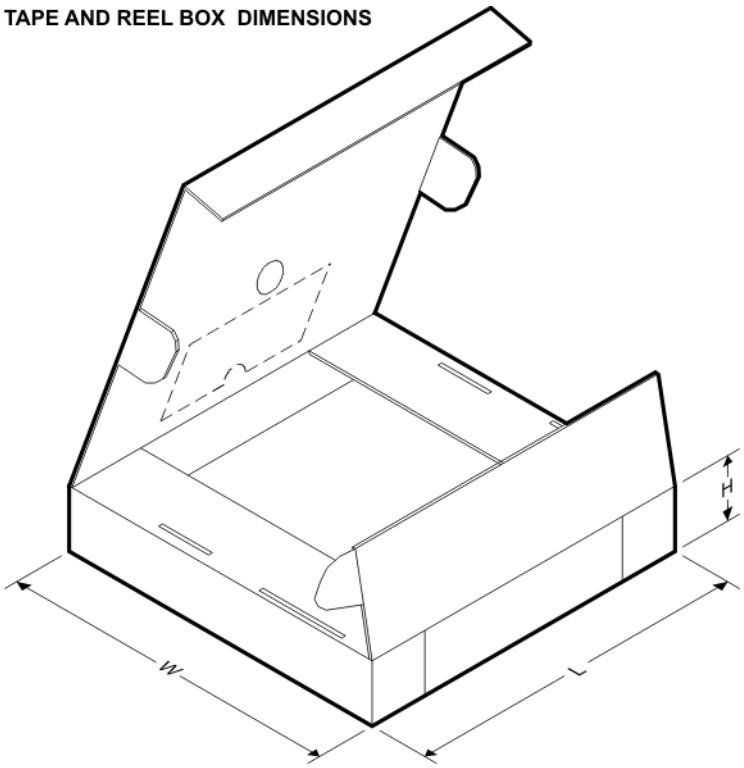
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
LP2966IMM-1833/NOPB	VSSOP	DGK	8	1000	178.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
LP2966IMM-2518/NOPB	VSSOP	DGK	8	1000	178.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
LP2966IMM-2525/NOPB	VSSOP	DGK	8	1000	178.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
LP2966IMM-2828/NOPB	VSSOP	DGK	8	1000	178.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
LP2966IMM-3325	VSSOP	DGK	8	1000	178.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
LP2966IMM-3325/NOPB	VSSOP	DGK	8	1000	178.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
LP2966IMM-5050/NOPB	VSSOP	DGK	8	1000	178.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
LP2966IMMX-3325/NOPB	VSSOP	DGK	8	3500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1

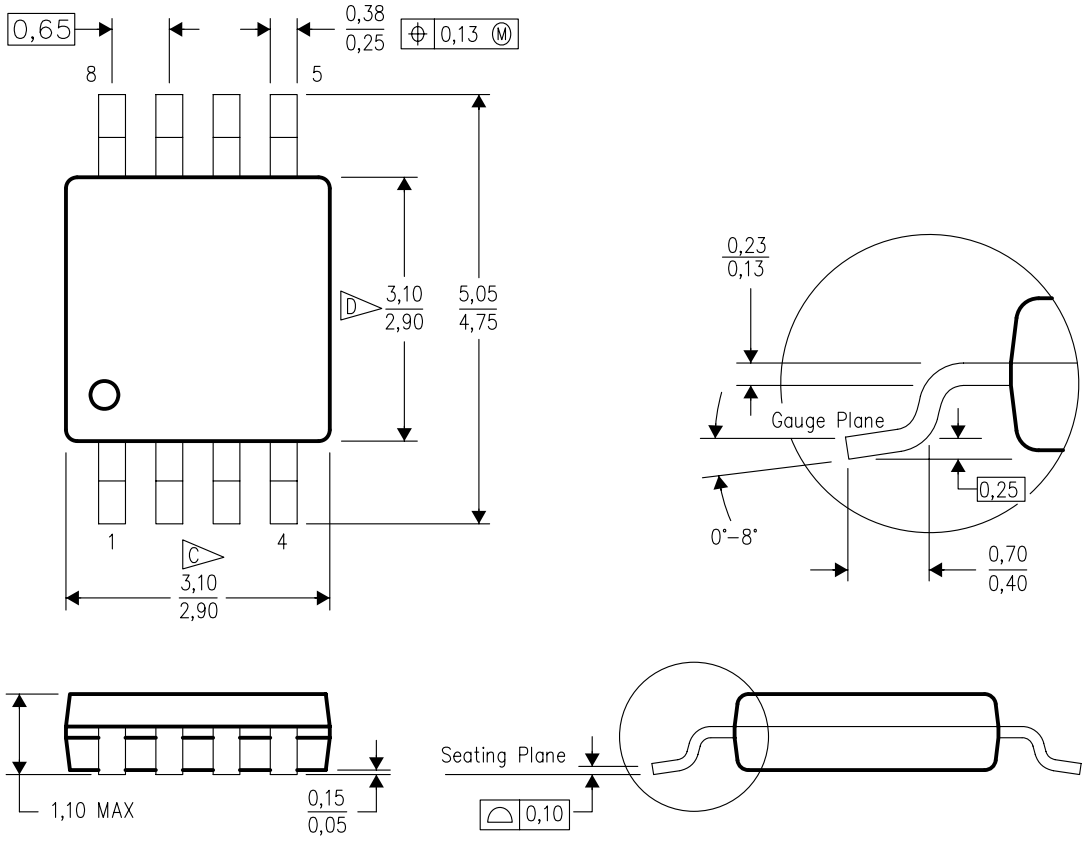
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
LP2966IMM-1833/NOPB	VSSOP	DGK	8	1000	210.0	185.0	35.0
LP2966IMM-2518/NOPB	VSSOP	DGK	8	1000	210.0	185.0	35.0
LP2966IMM-2525/NOPB	VSSOP	DGK	8	1000	210.0	185.0	35.0
LP2966IMM-2828/NOPB	VSSOP	DGK	8	1000	210.0	185.0	35.0
LP2966IMM-3325	VSSOP	DGK	8	1000	210.0	185.0	35.0
LP2966IMM-3325/NOPB	VSSOP	DGK	8	1000	210.0	185.0	35.0
LP2966IMM-5050/NOPB	VSSOP	DGK	8	1000	210.0	185.0	35.0
LP2966IMMX-3325/NOPB	VSSOP	DGK	8	3500	367.0	367.0	35.0

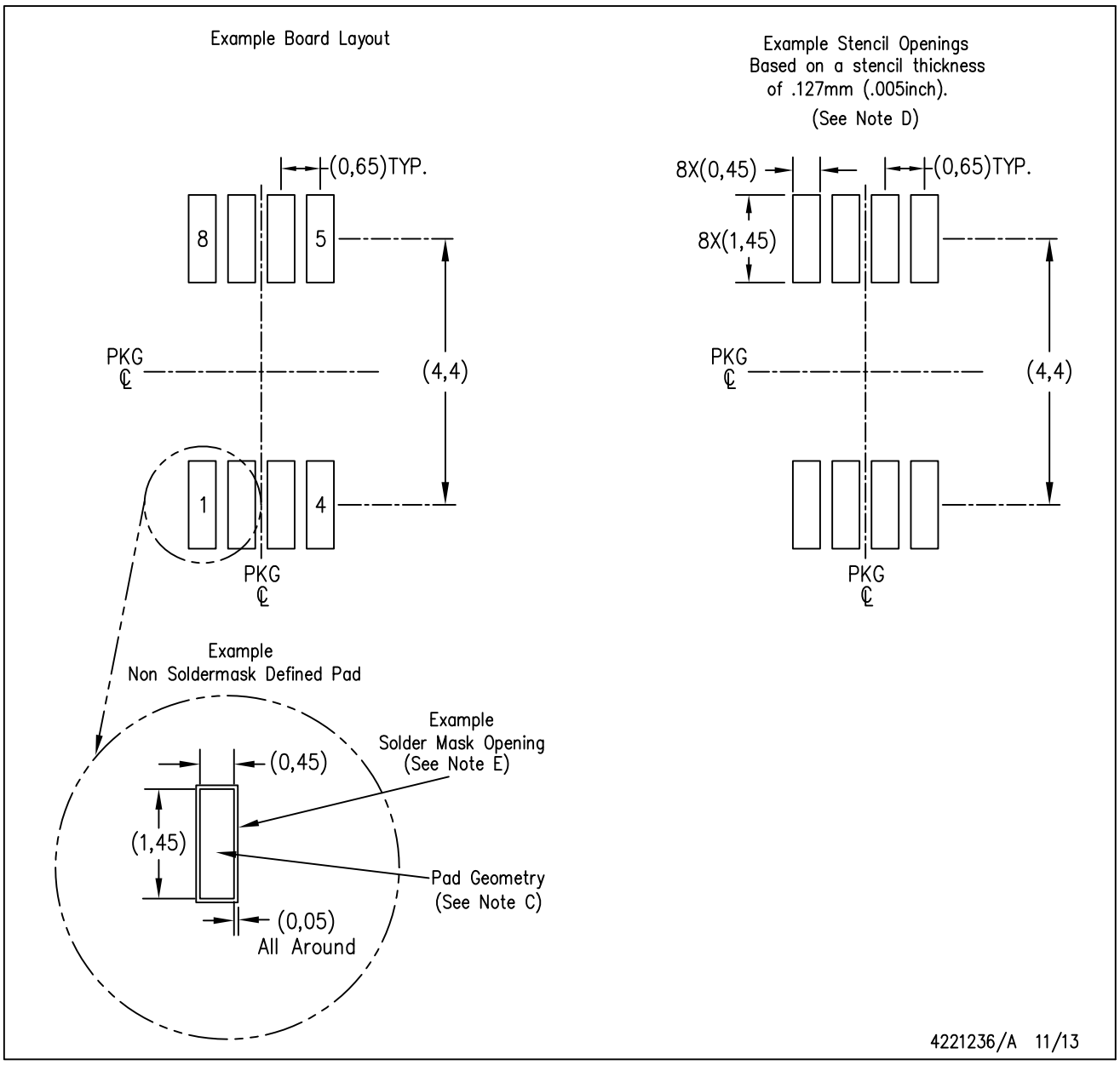
DGK (S–PDSO–G8) PLASTIC SMALL–OUTLINE PACKAGE



4073329/E 05/06

NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 per end.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0.50 per side.
E. Falls within JEDEC MO–187 variation AA, except interlead flash.

DGK (S–PDSO–G8) PLASTIC SMALL OUTLINE PACKAGE



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC–7525 for other stencil recommendations.
E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

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