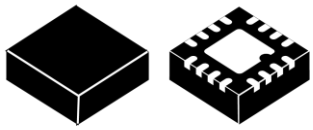
LNBH30

LNB supply and control IC with step-up and I²C interface

Datasheet - production data



QFN16 (4x4 mm)

Features

- Complete interface between LNB and I²C bus
- Built-in DC-DC converter for single 12 V supply operation and high efficiency (typ. 93% @ 0.5 A)
- Selectable output current limit by external resistor
- Compliant with main satellite receiver output voltage specifications
- Low drop post regulator and high efficiency step-up PWM with integrated power NMOS allowing low power losses
- Overload and overtemperature internal protection with I²C diagnostic bits
- LNB short-circuit dynamic protection
- +/- 4 kV ESD tolerant on output power pins

Applications

- STB satellite receivers
- TV satellite receivers
- PC card satellite receivers

Description

Intended for the Japanese market for digital dual satellite receivers/Sat-TV, and Sat-PC cards, the LNBH30 is a monolithic voltage regulator and interface IC, assembled in QFN16 (4x4 mm) specifically designed to provide the power supply to the LNB down-converter in the antenna dish or to the multi-switch box. In this application field, it offers a complete solution with extremely low component count, low power dissipation together with simple design and I²C standard interfacing.

Table 1: Device summary

Order code	Package	Packing
LNBH30QTR	QFN16 (4x4)	Tape and reel

This is information on a product in full production.

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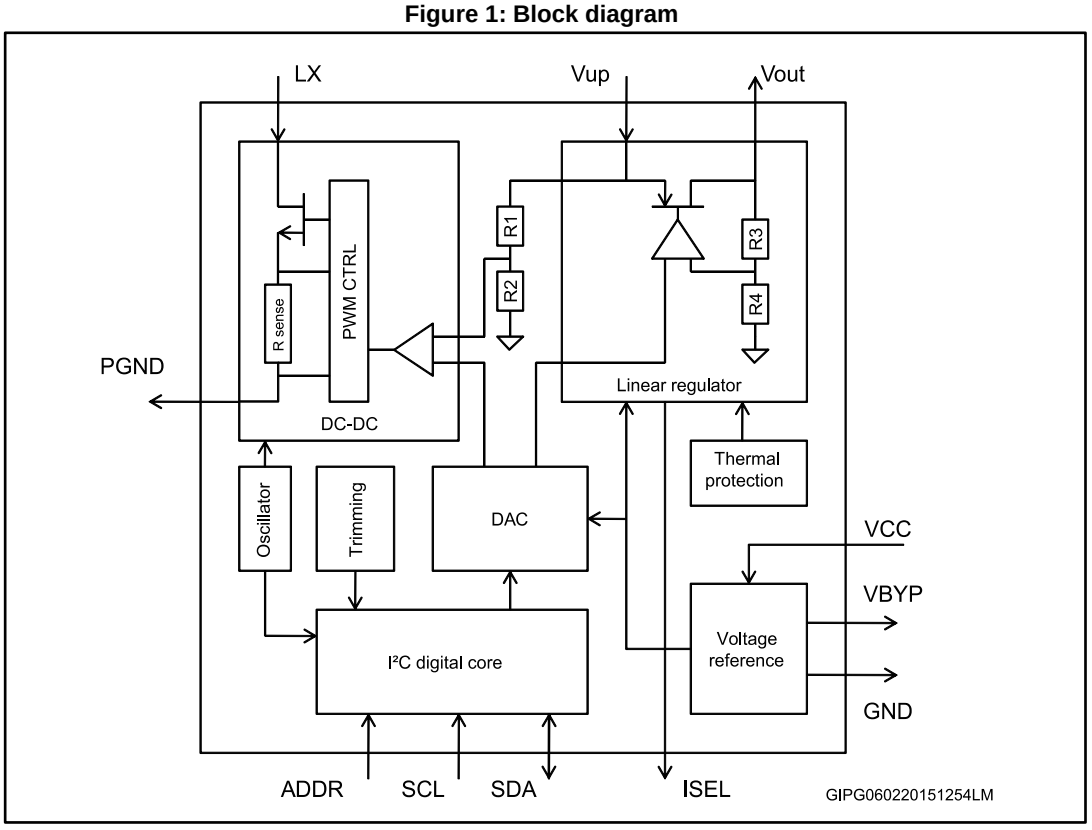
1 Block diagram

Figure 1: Block diagram



2 Application information

This IC has a built-in DC-DC step-up converter that, from a single source of typically 12 V, generates the voltages (V_{UP}) that allow the linear post-regulator to work at a minimum dissipated power of 0.5 W typ. @ 500 mA load (it is internally kept at V_{UP} - V_{OUT} = 1 V typ.). An undervoltage lockout circuit disables the whole circuit when the supplied V_{CC} drops below a fixed threshold (4.7 V typ.). The step-up converter is provided with a soft-start function which reduces the in-rush current during startup. The SS time is internally fixed at 5 ms typ. to switch from 0 to 15 V.

2.1 Output current limit selection

The linear regulator current limit threshold can be set by an external resistor connected to the ISEL pin. The resistor value defines the output current limit as per the following equation:

$$I_{MAX}(typ.) = \frac{13915}{RSEL^{1.111}}$$

where RSEL is the resistor connected between ISEL and GND expressed in kΩ and I_{MAX}(typ.) is the typical current limit threshold expressed in mA. I_{MAX} can be set up to 0.55 A.

2.2 Output voltage selection

The linear regulator channel output voltage level can be easily programmed in order to accomplish application specific requirements, using 3 bits of the internal DATA register see *Section 7.1: "Write mode transmission"* and *Table 6: "Data (read/write register, register address = 0x1)"* for exact programmable values. Register writing is accessible via the I²C bus.

2.3 COMP: boost capacitors and inductor

The DC-DC converter compensation loop can be optimized in order to properly work with both ceramic and electrolytic capacitors (V_{UP} pin). For this purpose, one I²C bit in the DATA register (see COMP) can be set to “1” or “0” as follows:

COMP = 0 for electrolytic capacitors

COMP = 1 for ceramic capacitors

For recommended DC-DC capacitor and inductor values refer to *Section 5: "Typical application circuits"* and to the BOM in *Table 5: "Typical application circuit bill of material"*.

2.4 Diagnostic and protection functions

The LNBH30 has 5 diagnostic internal functions provided by the I²C bus, by reading 5 bits on the status register (in read mode). All the diagnostic bits are, in normal operation, set to LOW. Two diagnostic bits are dedicated to the overtemperature and overload protection status (OTF and OLF) while the remaining 3 bits are dedicated to the output voltage level (VMON), to external voltage source presence on the VOUT pin (PDO) and to the input

voltage power not good function (PNG). Once the OLF (or OTF or PNG) bit is active (set to “1”), it is latched to “1” until the relevant cause is removed and a new register reading operation is performed.

2.5 VMON: output voltage diagnostic

When the device output voltage is active (VOUT pin), its value is internally monitored and, as long as the output voltage level is below the guaranteed limits, the relevant VMON I²C bit is set to “1” (see *Table 12: "Output voltage diagnostic (VMON bit, status register) characteristics"* for more details).

2.6 PDO: overcurrent detection on output pull-down stage

When an overcurrent occurs on the pull-down output stage due to an external voltage source greater than the LNBH30 nominal V_{OUT}, and for a time longer than $I_{SINK_TIME_OUT}$ (10 ms typ.), the corresponding PDO I²C bit is set to “1”. This may happen due to an external voltage source presence on the LNB output (VOUT pin).

For current threshold and deglitch time details, see *Table 9: "Electrical characteristics"*.

2.7 Power-on I²C interface reset and undervoltage lockout

The I²C interface built into the LNBH30 is automatically reset at power-on. As long as the V_{CC} stays below the undervoltage lockout (UVLO) threshold (4.7 V typ.), the interface does not respond to any I²C command and all DATA register bits are initialized to zeroes, therefore keeping the power blocks disabled. Once the V_{CC} rises above 4.8 V typ., the I²C interface becomes operative and the DATA registers can be configured by the main microprocessor.

2.8 PNG: input voltage minimum detection

When input voltage (V_{CC} pin) is lower than LPD (low power diagnostic) minimum thresholds, the PNG I²C bit is set to “1”. Refer to *Table 9: "Electrical characteristics"* for threshold details.

2.9 OLF: overcurrent and short-circuit protection and diagnostic

In order to reduce the total power dissipation during an overload or a short-circuit condition, the device is provided with a dynamic short-circuit protection. The overcurrent protection circuit works dynamically: as soon as an overload is detected, the output current is provided for T_{ON} time (90 ms) and after that, the output is set in shutdown for a T_{OFF} time of typically 900 ms. Simultaneously, the corresponding diagnostic OLF I²C bit of the status register is set to “1”. After this time has elapsed, the involved output is resumed for a time T_{ON}. At the end of T_{ON}, if the overload is still detected, the protection circuit cycles again through T_{OFF} and T_{ON}. At the end of a full T_{ON} in which no overload is detected, normal operation is resumed and the OLF diagnostic bit is reset to LOW after register reading is performed. Typical T_{ON} +T_{OFF} time is 990 ms and is determined by an internal timer. This dynamic operation can greatly reduce the power dissipation in short-circuit condition, still ensuring excellent power-on startup in most conditions.

2.10 OTF: thermal protection and diagnostic

The LNBH30 is also protected against overheating: when the junction temperature exceeds 150 °C (typ.), the step-up converter and the liner regulators are shut off, the diagnostic OTF bit in the status register is set to “1”. As soon as the overtemperature condition is removed, normal operation is automatically re-enabled while the OTF bit is reset to “0” after a register reading operation.

3 Pin configuration

Figure 2: Pin connections (top view)

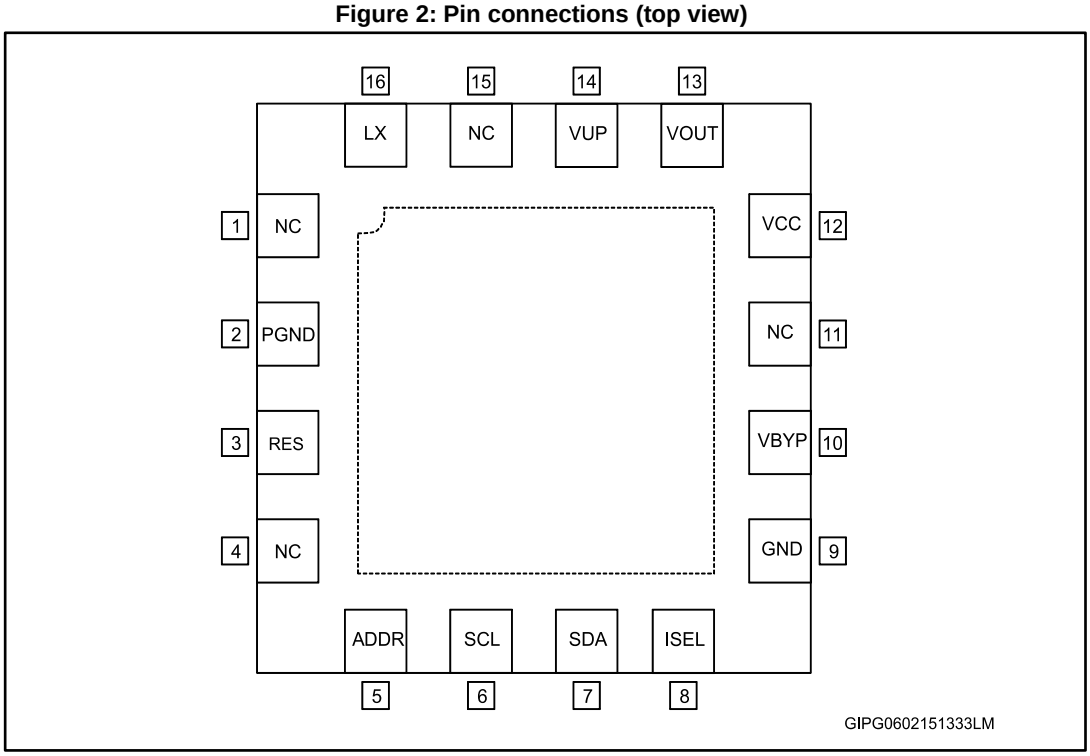


Table 2: Pin description

Pin	Symbol	Name	Pin function
2	PGND	Power ground	DC-DC converter power ground. To be connected directly to the exposed pad
3	RES	Reserved	Reserved pin. To be left floating. Do not connect to GND
5	ADDR	Address setting	Two I^2C bus addresses available by setting the address pin level voltage. See *Table 11: "Address pin characteristics"*
6	SCL	Serial clock	Clock from I²C bus
7	SDA	Serial data	Bi-directional data from/to I²C bus
8	ISEL	Current selection	The resistor “RSEL” connected between ISEL and GND defines the linear regulator current limit threshold. Refer to *Section 2.1: "Output current limit selection"*
9	GND	Analog ground	Analog circuit ground. To be connected directly to the exposed pad
10	BYP	Bypass capacitor	Needed for internal pre-regulator filtering. The BYP pin is intended to connect an external ceramic capacitor only. Any connection of this pin to external current or voltage sources may cause permanent damage to the device
12	VCC	Supply input	10 to 17.5 V IC DC-DC power supply
13	VOUT	LNB output port	Output of the integrated very low drop linear regulator. See *Table 8: "Output voltage selection (data register, write mode)"*
14	VUP	Step-up voltage	Input of linear post-regulator. The voltage on this pin is monitored by the internal step-up controller to keep a minimum dropout across the linear pass transistor

Pin	Symbol	Name	Pin function
16	LX	NMOS drain	Integrated N-channel power MOSFET drain
1,4,11, 15	NC	Not internally connected output	Not internally connected pins. These pins may be connected to GND to improve thermal performance
Epad	Epad	Exposed pad	To be connected with power ground and to the ground layer through vias to dissipate heat

4 Maximum ratings

Table 3: Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_{CC}	DC power supply input voltage pins	-0.3 to 20	V
V_{UP}	DC input voltage	-0.3 to 40	V
I_{OUT}	Output current	Internally limited	mA
V_{OUT}	DC output pin voltage	-0.3 to 40	V
V_I	Logic input pin voltage (SDA, SCL, DSQIN, ADDR pins)	-0.3 to 7	V
LX	LX input voltage	-0.3 to 30	V
V_{BYP}	Internal reference pin voltage	-0.3 to 4.6	V
ISEL	Current selection pin voltage	-0.3 to 3.5	V
T_{STG}	Storage temperature range	-50 to 150	°C
T_J	Operating junction temperature range	-25 to 125	°C
ESD	ESD rating with human body model (HBM) for all pins, except power output pins	2	kV
	ESD rating with human body model (HBM) for power output pins	4	

Table 4: Thermal data

Symbol	Parameter	Value	Unit
R_{thJC}	Thermal resistance junction-case	2	°C/W
RthJA	Thermal resistance junction-ambient with device soldered on 2s2p 4-layer PCB provided with thermal vias below exposed pad	40	°C/W



Absolute maximum ratings are those values beyond which damage to the device may occur. These are stress ratings only and functional operation of the device at these conditions is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect the device reliability. All voltage values are with respect to network ground terminal.

5 Typical application circuits

Figure 3: Application circuit

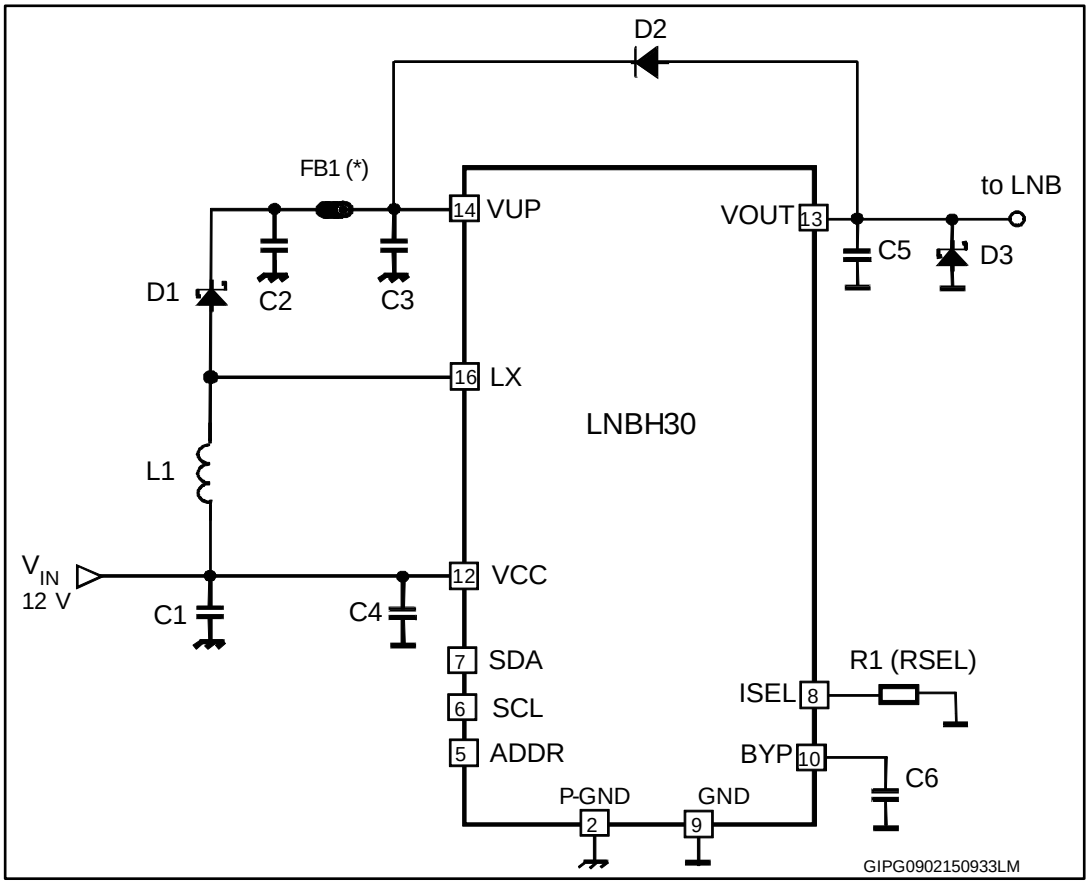


Table 5: Typical application circuit bill of material

Component	Notes
C1	> 25 V electrolytic capacitor, 100 µF or higher is suitable or > 25 V ceramic capacitor, 10 µF or higher is suitable
C2	With COMP = 0, > 25 V electrolytic capacitor, 100 µF or higher is suitable or with COMP = 1, > 35 V ceramic capacitor, 22 µF (or 2 x 10 µF) or higher is suitable
C3	2.2 µF ceramic capacitor placed as close as possible to VUP pins. Higher values allow lower DC-DC noise
C5	From 100 nF to 220 nF ceramic capacitor. Higher values allow lower DC-DC noise
C4, C6	220 nF ceramic capacitors
D1	STPS130A or similar Schottky diode
D2	1N4001-07, S1A-S1M, or any similar general purpose rectifier
D3	BAT54, BAT43, 1N5818, or any low power Schottky diode with $I_F(AV)$ > 0.2 A, V_{RRM} > 25 V, V_F < 0.5 V. To be placed as close as possible to VOUT pin

Component	Notes
L1	With COMP=0, use 10 µH inductor with $I_{SAT} > I_{PEAK}$ where I_{PEAK} is the boost converter peak current or with COMP=1 and C2 = 22 µF, use 6.8 µH inductor with $I_{SAT} > I_{PEAK}$ where I_{PEAK} is the boost converter peak current
FB1	Optional. Ferrite bead to be added if lower DC-DC noise is required

6 I²C bus interface

Data transmission from the main microprocessor to the LNBH30 and vice versa takes place through the 2-wire I²C bus interface, consisting of the 2-line SDA and SCL (pull-up resistors must be externally connected to positive supply voltage).

6.1 Data validity

As shown in *Figure 4: "Data validity on the I²C bus"*, the data on the SDA line must be stable during the high semi-period of the clock. The HIGH and LOW state of the data line can only change when the clock signal on the SCL line is LOW.

6.2 Start and stop condition

As shown in *Figure 5: "Timing diagram of I²C bus"*, a start condition is a HIGH to LOW transition of the SDA line while SCL is HIGH. The stop condition is a LOW to HIGH transition of the SDA line while SCL is HIGH. A STOP condition must be sent before than each START condition.

6.3 Byte format

Every byte transferred to the SDA line must contain 8 bits. Each byte must be followed by an acknowledge bit. The MSB is transferred first.

6.4 Acknowledge

The master (microprocessor) puts a resistive HIGH level on the SDA line during the acknowledge clock pulse (see *Figure 6: "Acknowledge on the I²C bus"*). The peripheral (LNBH30), which acknowledges, must pull down (LOW) the SDA line during the acknowledge clock pulse, so that the SDA line is stable LOW during this clock pulse. The peripheral, which has been addressed, must generate acknowledge after the reception of each byte, otherwise the SDA line remains at the HIGH level during the nin^{th} clock pulse time. In this case the master transmitter can generate the STOP information in order to abort the transfer. The LNBH30 does not generate acknowledge if the V_{CC} supply is below the undervoltage lockout threshold (4.7 V typ.).

6.5 Transmission without acknowledge

If detection of the acknowledge of the LNBH30 is not required, the microprocessor can use a simpler transmission: it simply waits for one clock without checking the slave acknowledging, and sends the new data. This approach is of course less protected from misworking and decreases noise immunity.

Figure 4: Data validity on the I²C bus

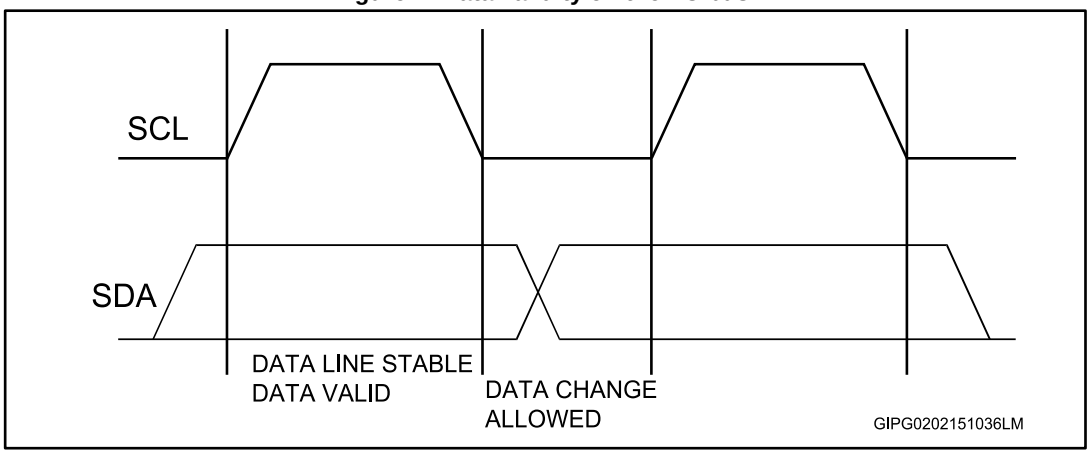


Figure 5: Timing diagram of I²C bus

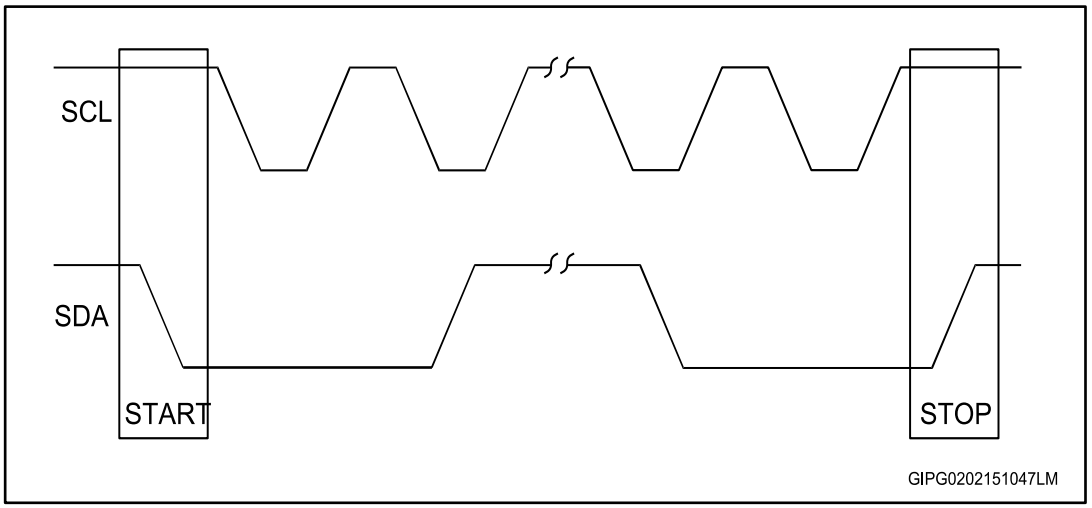
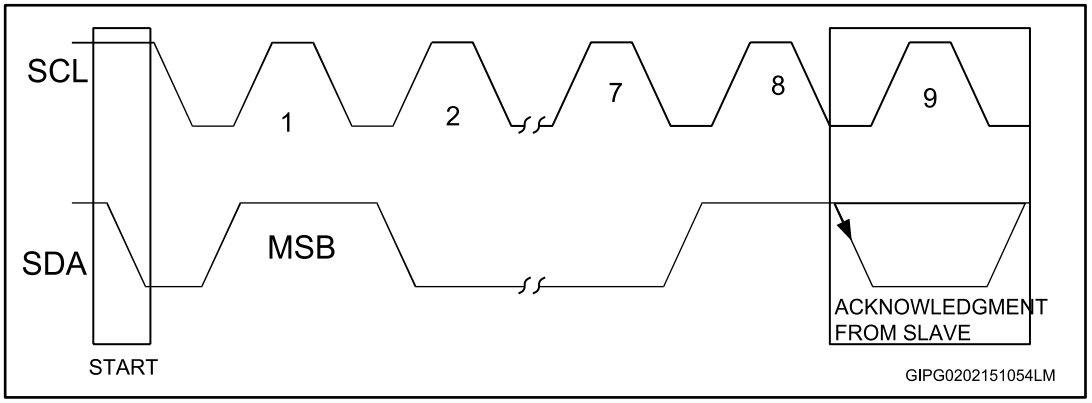


Figure 6: Acknowledge on the I²C bus



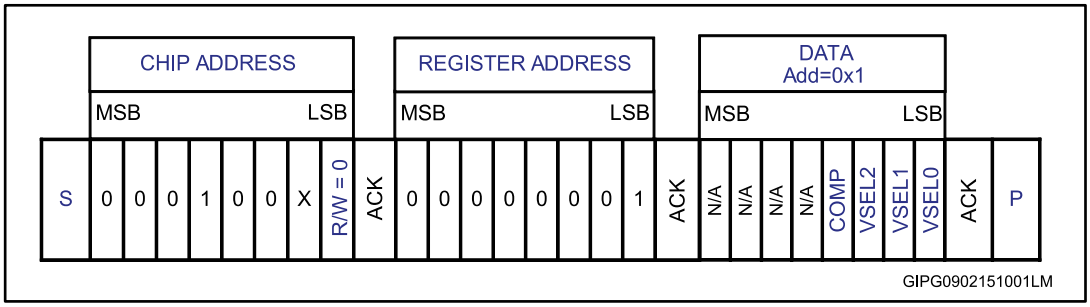
7 I²C interface protocol

7.1 Write mode transmission

The LNBH30 interface protocol is made up of:

- a start condition (S)
- a chip address byte with the LSB bit R/W = 0
- a register address (internal address of the first register to be accessed)
- a sequence of data (byte to write to the addressed internal register + acknowledge)
- a stop condition (P). The transfer lasts until a stop bit is encountered
- the LNBH30, as slave, acknowledges every byte transfer

Figure 7: Example of writing procedure starting with first data address 0x1



ACK = acknowledge

S = start

P = stop

R/W = 1/0, read/write bit

X = 0/1, set the values to select the chip address

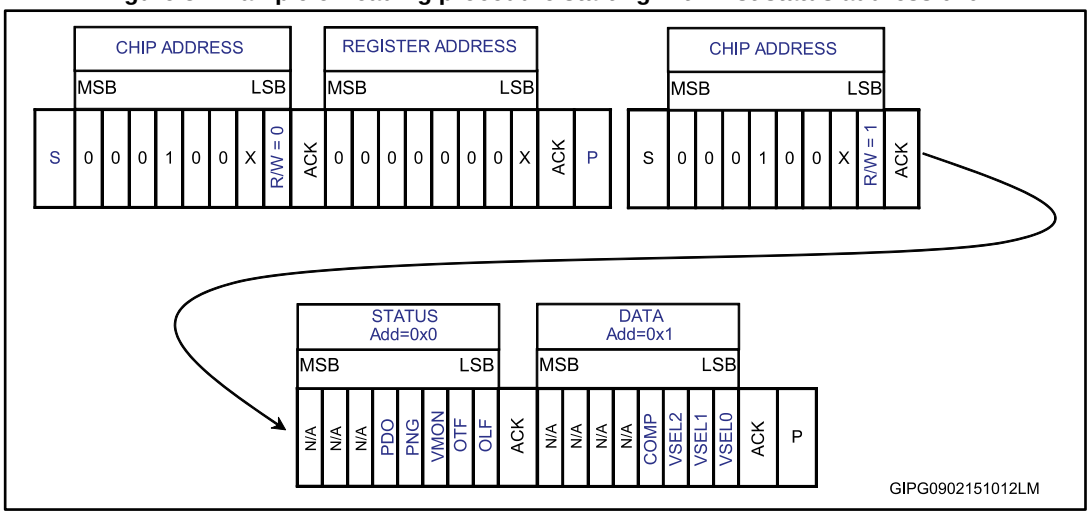
Only one data register address 0x1 is available for the writing procedure.

7.2 Read mode transmission

In read mode the byte sequence must be as follows:

- a start condition (S)
- a chip address byte with the LSB bit R/W=0
- the register address byte of the internal first register to be accessed
- a stop condition (P)
- a new master transmission with the chip address byte and the LSB bit R/W=1
- after the acknowledge the LNBH30 starts sending the addressed register content. As long as the master keeps the acknowledge LOW, the LNBH30 transmits the next address register byte content
- the transmission is terminated when the master sets the acknowledge HIGH with a following stop bit

Figure 8: Example of reading procedure starting with first status address 0x0



ACK = acknowledge

S = start

P = stop

R/W = 1/0, read/write bit

X = 0/1, sets the values to select the chip address and to select the register address (0x0 for status register and 0x1 for data register)

The reading procedure can start from any register address (status or data) by simply setting the X values in the register address byte (after the first chip address in the above figure). It can be also stopped by the master by sending a stop condition after any acknowledge bit.

7.3 Data registers

The data register can be addressed both to write and read mode. In read mode it returns the last writing byte status received in the previous write transmission.

The following table provides the data register values and a function description of each bit.

Table 6: Data (read/write register, register address = 0x1)

Bit	Name	Value	Description
Bit 0 (LSB)	VSEL0	0/1	Output voltage selection bits
Bit 1	VSEL1	0/1	
Bit 2	VSEL2	0/1	
Bit 3	COMP	0/1	DC-DC converter internal compensation: set to “0” to use standard ESR capacitors (VUP pin) Set to “1” to use very low ESR capacitors or ceramic caps (VUP pin)
Bit 4	N/A	0	Reserved. Keep to “0”

Bit	Name	Value	Description
Bit 5	N/A	0	
Bit 6	N/A	0	
Bit 7(MSB)	N/A	0	

N/A=reserved bit

All bits reset to "0" at power-on

7.4 Status registers

The status register can be only addressed to read mode and provides the diagnostic functions described in the following tables.

Table 7: Status (read register, register address = 0x0)

Bit	Name	Value	Description
Bit 0 (LSB)	OLF	1	Output short-circuit or VOUT pin overload protection has been triggered ($I_{OUT} > I_{MAX}$)
		0	No overload protection has been triggered to VOUT pin ($I_{OUT} < I_{MAX}$)
Bit 1	OTF	1	Junction overtemperature is detected, $T_J > 150$ °C
		0	Junction overtemperature is not detected, $T_J <$ 135 °C. T_J is below thermal protection threshold
Bit 2	VMON	1	Output voltage (VOUT pin) lower than VMON specification thresholds. Refer to *Table 9: "Electrical characteristics"*
		0	Output voltage (VOUT pin) is within the VMON specifications
Bit 3	PNG	1	Input voltage (VCC pin) lower than LPD minimum thresholds. Refer to *Table 9: "Electrical characteristics"*
		0	Input voltage (VCC pin) higher than LPD minimum thresholds. Refer to *Table 9: "Electrical characteristics"*
Bit 4	PDO	1	Overcurrent detected on output pull-down stage for a time longer than the deglitch period. This may happen due to an external voltage source present on the LNB output (VOUT pin)
		0	No overcurrent detected on output pull-down stage
Bit 5	N/A	-	Reserved
Bit 6	N/A	-	
Bit 7 (MSB)	N/A	-	

N/A = reserved bit

All bits reset to 0 at power-on

Table 8: Output voltage selection (data register, write mode)

VSEL2	VSEL1	VSEL0	VOUT min.	VOUT pin voltage	VOUT max.	Function
0	0	0		0.000		VOUT disabled. The LNBH30 is set in standby mode
0	0	1	11.387	11.800	12.213	
0	1	0	11.580	12.000	12.420	
0	1	1	11.900	12.333	12.765	
1	0	0	14.475	15.000	15.525	
1	0	1	14.796	15.333	15.870	
1	1	0	15.119	15.667	16.215	
1	1	1	15.440	16.000	16.560	

8 Electrical characteristics

Refer to *Section 5: "Typical application circuits"*, T_J from 0 to 85 °C, data register bits set to 0 except VSEL0 = 1, RSEL = 16.2 kΩ, V_{IN} = 12 V, I_{OUT} = 50 mA, unless otherwise stated. Typical values are referred to T_J = 25 °C. V_{OUT}= VOUT pin voltage. See *Section 7: "I²C interface protocol"*.

Table 9: Electrical characteristics

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
V_{IN}	Supply voltage		10	12	17.5	V
I_{IN}	Supply current	I_{OUT} = 0 mA		6		mA
		VSEL0=VSEL1=VSEL2=0		1		
V_{OUT}	Output voltage total accuracy	Valid at any V_{OUT} selected level	-3.5		+3.5	%
V_{OUT}	Line regulation	V_{IN} = 8 to 16 V			40	mV
V_{OUT}	Load regulation	I_{OUT} from 50 to 500 mA			100	
I_{MAX}	Output current limiting thresholds	RSEL = 16.2 kΩ	500	650	750	mA
		RSEL = 22 kΩ	350		550	
I_{SC}	Output short-circuit current	RSEL = 16.2 kΩ		400		mA
SS	Soft-start time	V_{OUT} from 0 to 11.8 V		4		ms
SS	Soft-start time	V_{OUT} from 0 to 15 V		5		ms
T11-15	Soft transition rise time	V_{OUT} from 11.8 V to 15 V		1.5		ms
T15-11	Soft transition fall time	V_{OUT} from 15 V to 11.8 V		1.5		ms
T_{OFF}	Dynamic overload protection off-time	Output shorted		900		ms
T_{ON}	Dynamic overload protection on-time	Output shorted		T_{OFF}/10		
$Eff_{DC/DC}$	DC-DC converter efficiency	I_{OUT} = 500 mA		93		%
F_{SW}	DC-DC converter switching frequency			440		kHz
UVLO	Undervoltage lockout thresholds	UVLO threshold rising		4.8		V
		UVLO threshold falling		4.7		
V_{LPD}	Low power diagnostic (LPD) thresholds	V_{LPD} threshold rising		7.2		V
		V_{LPD} threshold falling		6.7		
I_{OBK}	Output backward current	All VSELx = 0, V_{OBK} = 30 V		-3	-6	mA
I_{SINK}	Output low-side sink current	V_{OUT} forced at V_{OUT_NOM} + 0.1 V		50		mA
$I_{SINK_TIME-OUT}$	Low-side sink current timeout	V_{OUT} forced at V_{OUT_NOM} + 0.1 V, PDO I²C bit is set to 1 after this time has elapsed		10		ms

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
I_{REV}	Max. reverse current	V_{OUT} forced at V_{OUT_NOM} + 0.1 V, after PDO bit is set to 1 ($I_{SINK_TIME\text{-}OUT}$ elapsed)		2		mA
T_{SHDN}	Thermal shutdown threshold			150		°C
ΔT_{SHDN}	Thermal shutdown hysteresis			15		°C

T_J from 0 to 85 °C, V_I = 12 V

Table 10: I^2C electrical characteristics

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
V_{IL}	Low level input voltage	SDA, SCL			0.8	V
V_{IH}	High level input voltage	SDA, SCL	2			
I_{IN}	Input current	SDA, SCL V_{IN} = 0.4 to 4.5 V	-10		10	µA
V_{OL}	Low level output voltage	SDA (open drain), I_{OL} = 6 mA			0.6	V
F_{MAX}	Maximum clock frequency	SCL			400	kHz

T_J from 0 to 85 °C, V_I = 12 V

Table 11: Address pin characteristics

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{ADDR\text{-}1}$	“0001000(R/W)” address pin voltage range	R/W bit determines the transmission mode: read (R/W=1) write (R/W=0)	0		0.8	V
$V_{ADDR\text{-}2}$	“0001001(R/W)” address pin voltage range	R/W bit determines the transmission mode: read (R/W=1) write (R/W=0)	2		5	V

Refer to *Section 5: "Typical application circuits"*, T_J from 0 to 85 °C, data register bits set to "0", RSEL = 16.2 kΩ, DSQIN = low, V_{IN} = 12 V, I_{OUT} = 50 mA, unless otherwise stated. Typical values are referred to T_J = 25 °C. V_{OUT} = VOUT pin voltage.

Table 12: Output voltage diagnostic (VMON bit, status register) characteristics

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
V_{TH-L}	Diagnostic low threshold at V_{OUT} = 11.8 V	VSEL0 = 1, VSEL1 = VSEL2 =0	80	90	95	%
V_{TH-L}	Diagnostic low threshold at V_{OUT} = 15 V	VSEL1=0, VSEL0 = VSEL2 = 1	80	90	95	%

If the output voltage is lower than the min. value the VMON I²C bit is set to 1.

If VMON=0 then V_{OUT} > 80% of V_{OUT} (typ.)

If VMON=1 then V_{OUT} < 95% of V_{OUT} (typ.)

9 Package information

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: ***www.st.com***. ECOPACK® is an ST trademark.

9.1 QFN16 (4x4 mm) package information

Figure 9: QFN16 (4x4 mm) package outline

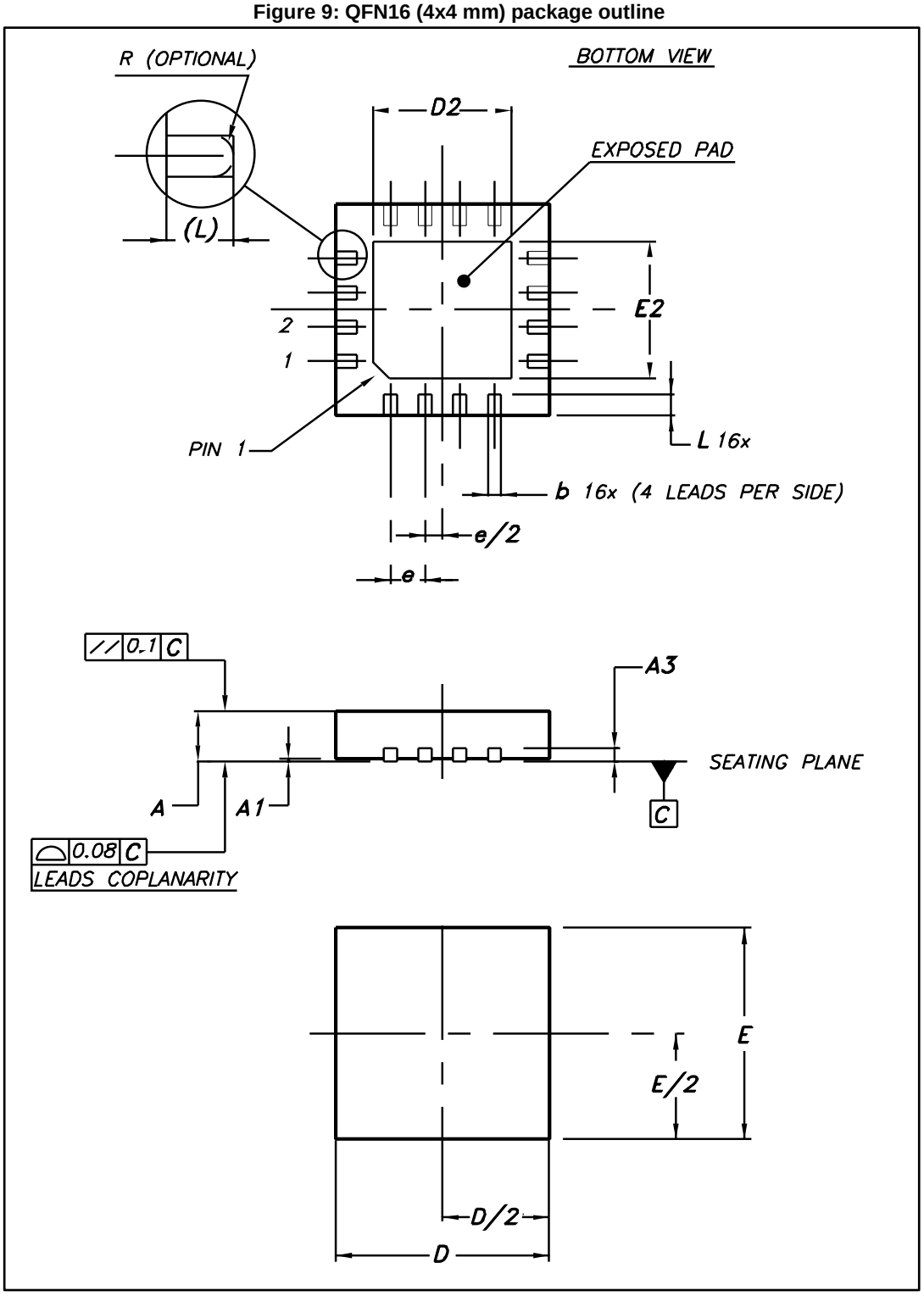
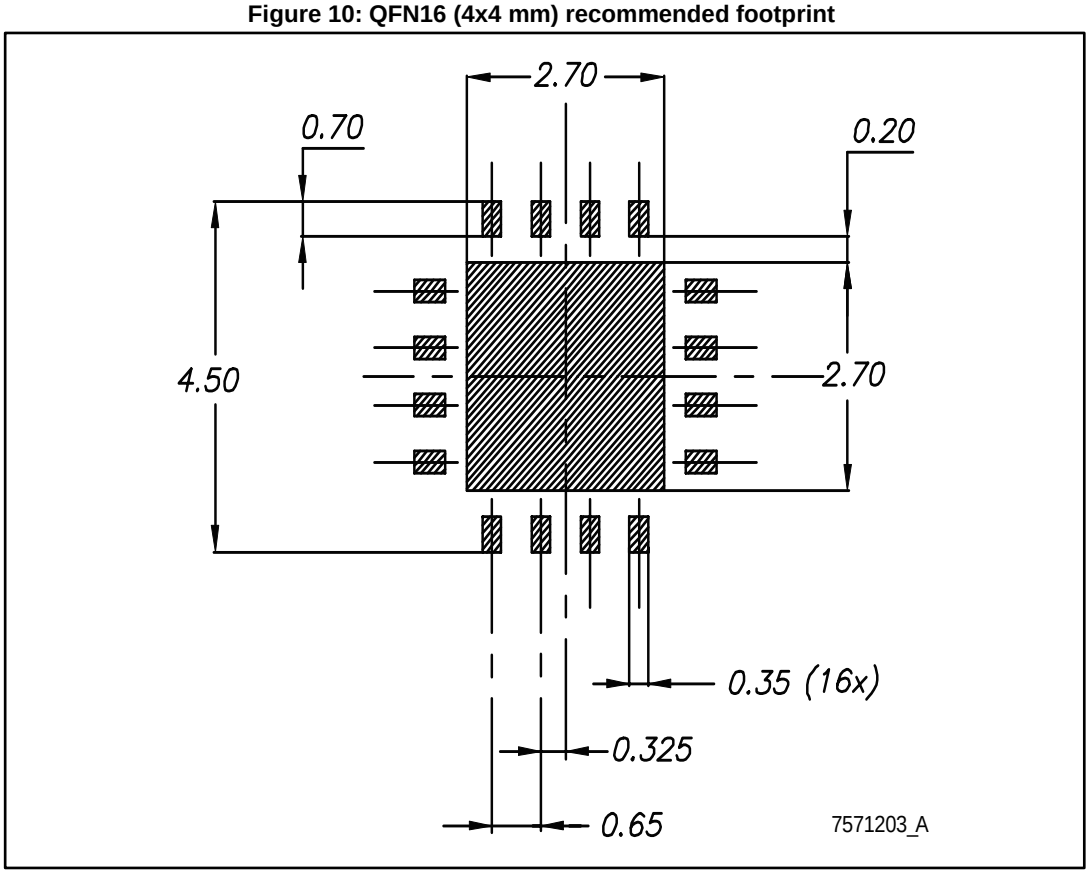


Table 13: QFN16 (4x4 mm) mechanical data

Dim.	mm		
	Min.	Typ.	Max.
A	0.80	0.90	1.00
A1	0.00	0.02	0.05
A3		0.20	
b	0.25	0.30	0.35
D	3.90	4.00	4.10
D2	2.50		2.80
E	3.90	4.00	4.10
E	3.90	4.00	4.10
E2	2.50		2.80
e		0.65	
L	0.30	0.40	0.50

Figure 10: QFN16 (4x4 mm) recommended footprint



10 Revision history

Table 14: Document revision history

Date	Revision	Changes
16-Oct-2012	1	Initial release.
19-Mar-2015	2	Update *Section 2.1: "Output current limit selection"* and *Table 9: "Electrical characteristics"*.

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