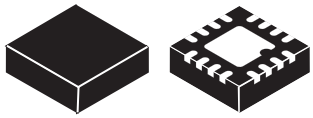
LNBH29

LNB supply and control IC with step-up and I²C interface

Datasheet - production data



QFN16 (4x4) / (3x3)

Features

- Complete interface between LNB and I²C bus
- Built-in DC-DC converter for single 12 V supply operation and high efficiency (typ. 93% @ 0.5 A)
- Selectable output current limit by external resistor
- Compliant with main satellite receiver output voltage specifications
- Accurate built-in 22 kHz tone generator suits widely accepted standards
- EXTM pin, auxiliary 22 kHz modulation input (LNBH29E) extends design flexibility
- 22 kHz tone waveform integrity guaranteed also at no load condition
- Low-drop post regulator and high efficiency step-up PWM with integrated power N-MOS allowing low power losses
- Overload and overtemperature internal protection with I²C diagnostic bits
- LNB short-circuit dynamic protection
- +/- 4 kV ESD tolerant on output power pins

Applications

- STB satellite receivers
- TV satellite receivers
- PC card satellite receivers

Description

Intended for analog and digital satellite receivers/Sat-TV and Sat-PC cards, the LNBH29 series is a monolithic voltage regulator and interface IC, assembled in QFN16 (3x3) and QFN16 (4x4) specifically designed to provide the 13 / 18 V power supply and the 22 kHz tone signaling to the LNB down-converter in the antenna dish or to the multi-switch box. In this application field, it offers a complete solution with extremely low component count, low power dissipation together with a simple design and I²C standard interfacing.

Table 1. Device summary

Order codes	Packages	Packaging
LNBH29PTR	QFN16 (3x3)	Tape and reel
LNBH29EPTR	QFN16 (3x3)	Tape and reel
LNBH29QTR	QFN16 (4x4)	Tape and reel
LNBH29EQTR	QFN16 (4x4)	Tape and reel

This is information on a product in full production. www.st.com

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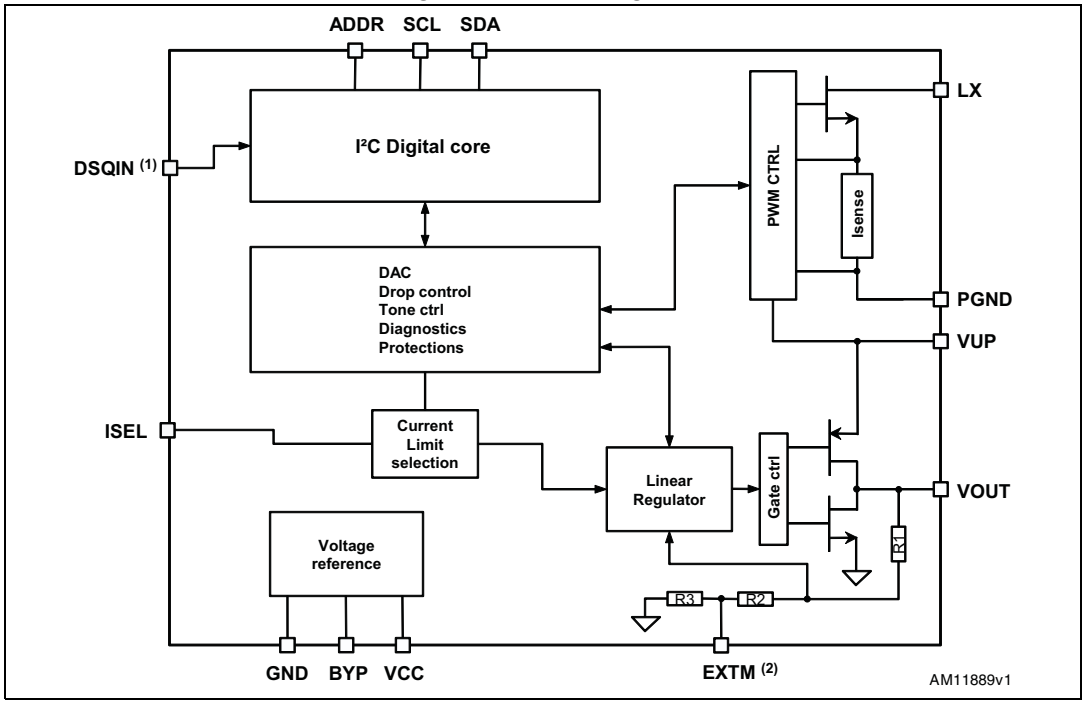
1 Block diagram

Figure 1. Block diagram



1. DSQIN pin available only on the LNBH29.
2. EXTM pin available only on the LNBH29E.

2 Application information

This IC has a built-in DC-DC step-up converter that, from a single source from 9 V to 17.5 V, generates the voltages (V_{UP}) that allow the linear post-regulator to work with a minimum dissipated power of 0.5 W typ. @ 500 mA load (the linear post-regulator drop voltage is internally kept at V_{UP} - V_{OUT} = 1 V typ.). The IC is also provided with an undervoltage lockout circuit that disables the whole circuit when the supplied V_{CC} drops below a fixed threshold (4.7 V typically). The step-up converter is provided with a soft-start function which reduces the inrush current during startup. The SS time is internally fixed at 4 ms typ. to switch from 0 to 13 V and 6 ms typ. to switch from 0 to 18 V.

2.1 DiSEqC™ data encoding

The LNBH29 series includes two versions with different DiSEqC control pin solutions: LNBH29 with DSQIN pin and LNBH29E with EXTM pin.

The LNBH29 is provided with the DSQIN logic input pin (TTL compatible) to be controlled by an external DiSEqC data envelope source which activates the internal 22 kHz tone generator factory trimmed. This guarantees the tone output waveform in accordance with the DiSEqC standards.

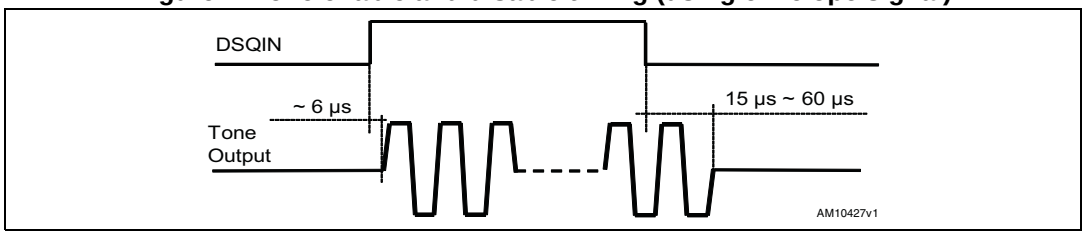
The LNBH29E is provided with the EXTM analogic modulation input pin to be connected to an external 22 kHz DiSEqC tone source. The tone output waveform depends on the characteristics of an external signal injected by means of the EXTM pin.

2.2 LNBH29: data encoding by external DiSEqC envelope control through the DSQIN pin

If an external DiSEqC code envelope source is available, it is possible to use the internal 22 kHz generator activated during the tone transmission by connecting the DiSEqC envelope source to the DSQIN pin (see *Section 5: Typical application circuits*). In this way, the internal 22 kHz signal is superimposed to the V_{OUT} DC voltage to generate the LNB output 22 kHz tone. During the period in which the DSQIN is kept HIGH, the internal control circuit activates the 22 kHz tone output.

The 22 kHz tone on the V_{OUT} pin is activated with about 6 µs delay from the DSQIN TTL signal rising edge, and it stops with a delay time in the range of 15 µs to 60 µs after the 22 kHz TTL signal on DSQIN has expired (refer to *Figure 2*).

Figure 2. Tone enable and disable timing (using envelope signal)



2.3 LNBH29E: DISEQC data encoding by external 22 kHz signal connected to the EXTM pin

In order to improve design flexibility, an analogic modulation input pin is available (EXTM) to generate the 22 kHz tone superimposed to the V_{OUT} DC output voltage. An appropriate DC blocking capacitor must be used to couple the 22 kHz modulating signal source to the EXTM pin. The EXTM pin modulates the V_{OUT} voltage through the series decoupling capacitor, so that:

$V_{OUT}(AC) = VEXTM(AC) \times GEXTM$

where $V_{OUT}(AC)$ and VEXTM(AC) are, respectively, the peak-to-peak AC voltage on the V_{OUT} pin and on the EXTM pin, while GEXTM is the voltage gain between the EXTM voltage and V_{OUT} signal.

2.4 Output current limit selection

The linear regulator current limit threshold can be set by an external resistor connected to the ISEL pin. The resistor value defines the output current limit by the equation:

Equation 1

$$I_{MAX}(typ.) = \frac{13915}{RSEL^{1.111}}$$

where R_{SEL} is the resistor connected between ISEL and GND expressed in kΩ and I_{MAX}(typ.) is the typical current limit threshold expressed in mA. I_{MAX} can be set up to 550 mA.

2.5 Output voltage selection

The linear regulator output voltage level can be easily programmed in order to accomplish application specific requirements, using 3 bits of the internal DATA register (see *Section 7.1: Write mode transmission* and *Table 7* for exact programmable values). Register writing is accessible via the I²C bus.

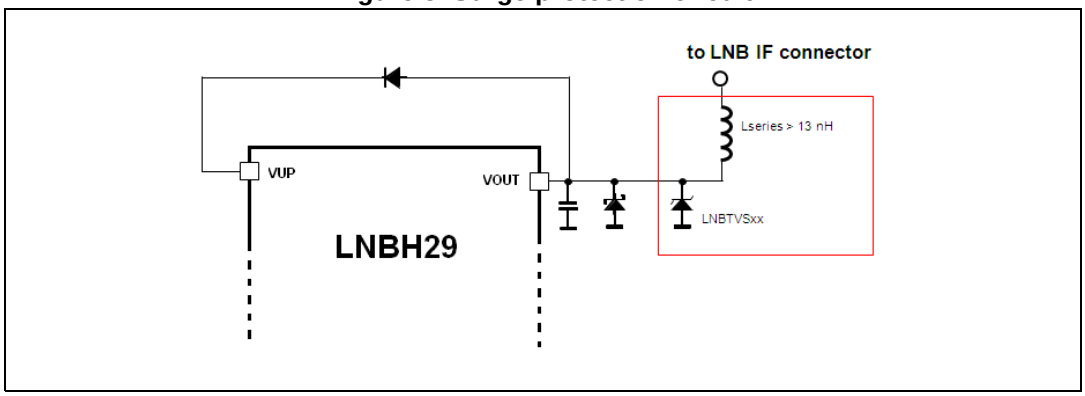
2.6 Diagnostic and protection functions

The LNBH29 series has 5 diagnostic internal functions provided via the I²C bus, by reading 5 bits on the STATUS register (in Read mode). All the diagnostic bits are, in normal operation, set to LOW. Two diagnostic bits are dedicated to the overtemperature and overload protection status (OTF and OLF) while the remaining 3 bits are dedicated to the output voltage level (VMON), to external voltage source presence on the V_{OUT} pin (PDO) and to the input voltage power not good function (PNG). Once the OLF (or OTF or PNG) bit has been activated (set to “1”), it is latched to “1” until the relevant cause is removed and a new register reading operation is done (see *Table 8*).

2.7 Surge protection and TVS diodes

The LNBH29 series is directly connected to the antenna cable in a set-top box. Atmospheric phenomenon can cause high voltage discharges on the antenna cable causing damage to the attached devices. Surge pulses occur due to direct or indirect lightning strikes to an external (outdoor) circuit. This leads to currents or electromagnetic fields causing high voltage or current transients. Transient voltage suppressor (TVS) devices are usually placed, as shown in *Figure 3*, to protect the STB output circuits where the LNBH29 and other devices are electrically connected to the antenna cable.

Figure 3. Surge protection circuit



For this purpose the use of LNBTVSxx surge protection diodes specifically designed by ST is recommended. The selection of the LNBTVS diode should be made based on the maximum peak power dissipation that the diode is capable of supporting (see the LNBTVS datasheet for further details).

2.8 VMON: output voltage diagnostic

When device output voltage is activated (V_{OUT} pin), its value is internally monitored and, as long as the output voltage level is below the guaranteed limits, the VMON I²C bit is set to “1”. See *Table 12* for more details.

2.9 PDO: overcurrent detection on output pull-down stage

When an overcurrent occurs on the pull-down output stage due to an external voltage source greater than the LNBH29 nominal V_{OUT} and for a time longer than $I_{SINK_TIME\text{-}OUT}$ (10 ms typ.), the PDO I²C bit is set to “1”. This may happen due to an external voltage source presence on the LNB output (V_{OUT} pin).

For current threshold and de-glitch time details, see *Table 9*.

2.10 Power-on I²C interface reset and undervoltage lockout

The I²C interface built into the LNBH29 series is automatically reset at power-on. As long as the V_{CC} stays below the undervoltage lockout (UVLO) threshold (4.7 V typ.), the interface does not respond to any I²C command and all DATA register bits are initialized to zeroes, therefore keeping the power blocks disabled. Once the V_{CC} rises above 4.8 V typ. the I²C interface becomes operative and the DATA registers can be configured by the main microprocessor.

2.11 PNG: input voltage minimum detection

When input voltage (V_{CC} pin) is lower than LPD (low power diagnostic) minimum thresholds, the PNG I²C bit is set to “1”. Refer to *Table 9* for threshold details.

2.12 COMP: boost capacitors and inductor

The DC-DC converter compensation loop can be optimized in order to properly work with both ceramic and electrolytic capacitors (V_{UP} pin). For this purpose, one I²C bit in the DATA register (COMP) can be set to “1” or “0” as follows:

COMP=0 for electrolytic capacitors

COMP=1 for ceramic capacitors

For recommended DC-DC capacitor and inductor values refer to *Section 5: Typical application circuits* and to the BOM in *Table 5*.

2.13 OLF: overcurrent and short-circuit protection and diagnostic

In order to reduce the total power dissipation during an overload or a short-circuit condition, the device is provided with a dynamic short-circuit protection. The overcurrent protection circuit works dynamically: as soon as an overload is detected, the output current is provided only for T_{ON} time (90 ms typ.) and after that, the output is set in shutdown for a T_{OFF} time of typically 900 ms. Simultaneously, the diagnostic OLF I²C bit of the STATUS register is set to “1”. After this time has elapsed, the output is resumed for a time T_{ON}. At the end of T_{ON}, if the overload is still detected, the protection circuit cycles again through T_{OFF} and T_{ON}. At the end of a full T_{ON} in which no overload is detected, normal operation is resumed and the OLF diagnostic bit is reset to LOW after a register reading is done. Typical T_{ON} + T_{OFF} time is 990 ms, determined by an internal timer. This dynamic operation can greatly reduce the power dissipation in short-circuit conditions, while ensuring excellent power-on startup in most conditions.

2.14 OTF: thermal protection and diagnostic

The LNBH29 series is also protected against overheating: when the junction temperature exceeds 150 °C (typ.), the step-up converter and the linear regulator are shut off and the diagnostic OTF bit in the STATUS register is set to “1”. As soon as the overtemperature condition is removed, normal operation is automatically re-enabled, while the OTF bit is reset to “0” after a register reading operation.

3 Pin configuration

Figure 4. Pin connections QFN16 (3x3) and (4x4) (top view)

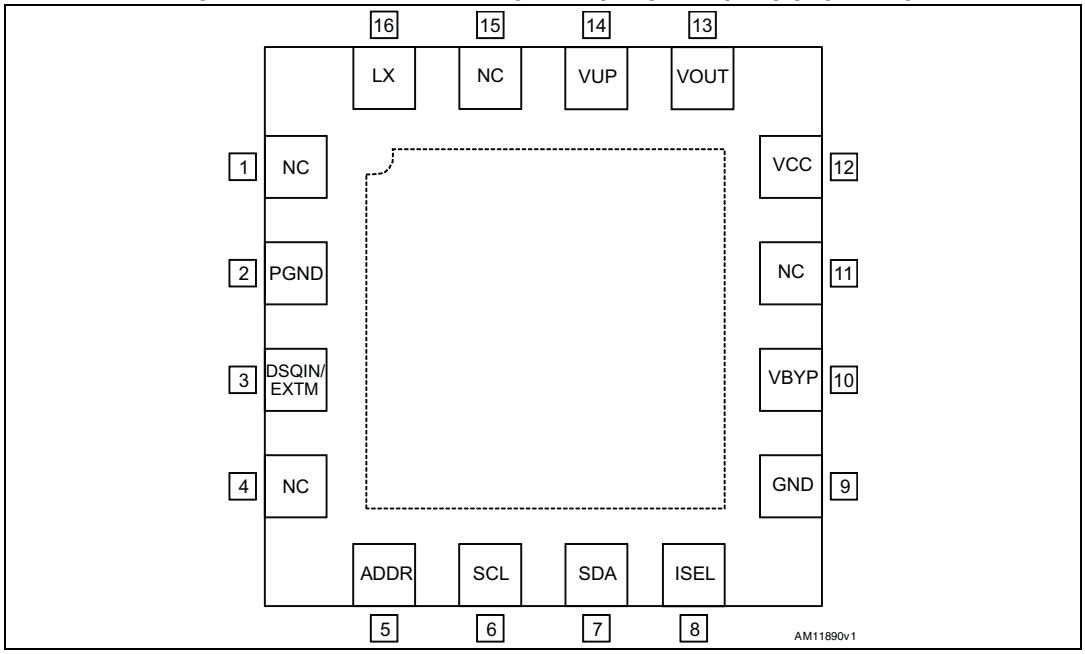


Table 2. Pin description

Pin n°	Symbol	Name	Pin function
16	LX	N-Mos drain	Integrated N-channel Power MOSFET drain.
2	P-GND	Power ground	DC-DC converter power ground. To be connected directly to the Epad.
5	ADDR	Address setting	Two I²C bus addresses available by setting the address pin level voltage. See *Table 11*.
6	SCL	Serial clock	Clock from I²C bus.
7	SDA	Serial data	Bi-directional data from/to I²C bus.
8	ISEL	Current selection	The resistor “RSEL” connected between ISEL and GND defines the linear regulator current limit threshold. Refer to *Section 2.4*.
9	GND	Analog ground	Analog circuits ground. To be connected directly to the Epad.
10	BYP	Bypass capacitor	Needed for internal pre-regulator filtering. The BYP pin is intended only to connect an external ceramic capacitor. Any connection of this pin to external current or voltage sources may cause permanent damage to the device.
12	V_{CC}	Supply input	8 to 17.5 V IC DC-DC power supply.
13	V_{OUT}	LNB output port	Output of the integrated very low drop linear regulator. See *Table 7* for voltage selection and description.
14	V_{UP}	Step-up voltage	Input of the linear post-regulator. The voltage on this pin is monitored by the internal step-up controller to keep a minimum dropout across the linear pass transistor.

Table 2. Pin description (continued)

Pin n°	Symbol	Name	Pin function
3	DSQIN (LNBH29)	DiSEqC tone envelope input	Available for LNBH29 version: this pin accepts DiSEqC envelope codes (TTL compatible) from the main DiSEqC microcontroller. The LNBH29 uses this code to enable the internally generated 22 kHz carrier superimposed to the V_{OUT} pin DC voltage. See *Figure 5*.
3	EXTM (LNBH29E)	External 22 kHz tone input	Available for LNBH29E version: the “external tone modulation” input acts on the integrated linear regulator loop to superimpose an external 22 kHz signal to the V_{OUT} pin DC voltage. Needs DC decoupling to the AC source. See *Figure 6*.
Epad	Epad	Exposed pad	To be connected with power grounds and to the ground layer through vias to dissipate the heat.
1, 4, 11, 15	N.C.	Not internally connected	Not internally connected pins. These pins can be connected to GND to improve thermal performance.

4 Maximum ratings

Table 3. Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_{CC}	DC power supply input voltage pins	-0.3 to 20	V
V_{UP}	DC input voltage	-0.3 to 40	V
I_{OUT}	Output current	Internally limited	mA
V_{OUT}	DC output pin voltage	-0.3 to 40	V
V_I	Logic input pins voltage (SDA, SCL, DSQIN, ADDR pins)	-0.3 to 7	V
V_{EXTM}	EXTM pin voltage	-0.3 to 2	V
LX	LX input voltage	-0.3 to 30	V
V_{BYP}	Internal reference pin voltage	-0.3 to 4.6	V
ISEL	Current selection pin voltage	-0.3 to 3.5	V
T_{STG}	Storage temperature range	-50 to 150	°C
T_J	Operating junction temperature range	-25 to 125	°C
ESD	ESD rating with human body model (HBM) all pins, unless power output pins	2	kV
	ESD rating with human body model (HBM) for power output pins	4	

Note: Absolute maximum ratings are those values beyond which damage to the device may occur. These are stress ratings only and functional operation of the device at these conditions is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability. All voltage values are with respect to the network ground terminal.

Table 4. Thermal data

Symbol	Parameter	QFN (3x3)	QFN (4x4)	Unit
R_{thJC}	Thermal resistance junction-case	2	2	°C/W
R_{thJA}	Thermal resistance junction-ambient with device soldered on 2s2p 4-layer PCB provided with thermal vias below exposed pad	55	40	°C/W

5 Typical application circuits

Figure 5. LNBH29: DiSEqC tone envelope pin control

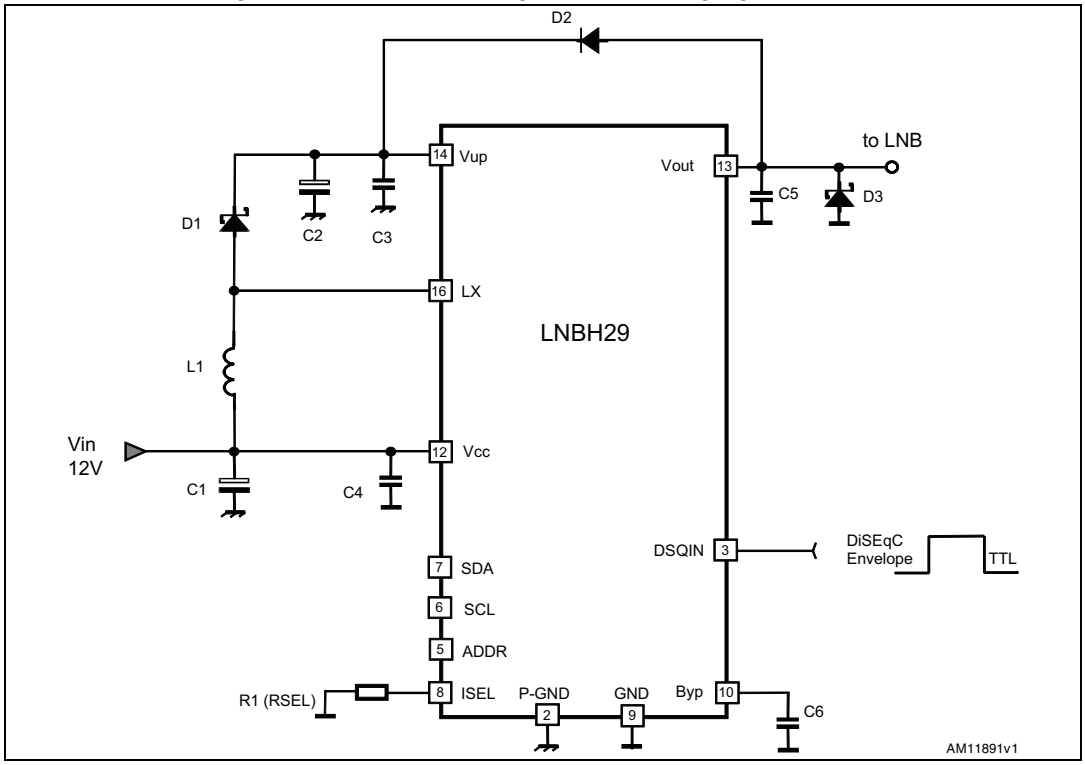


Figure 6. LNBH29E: external 22 kHz DiSEqC pin control

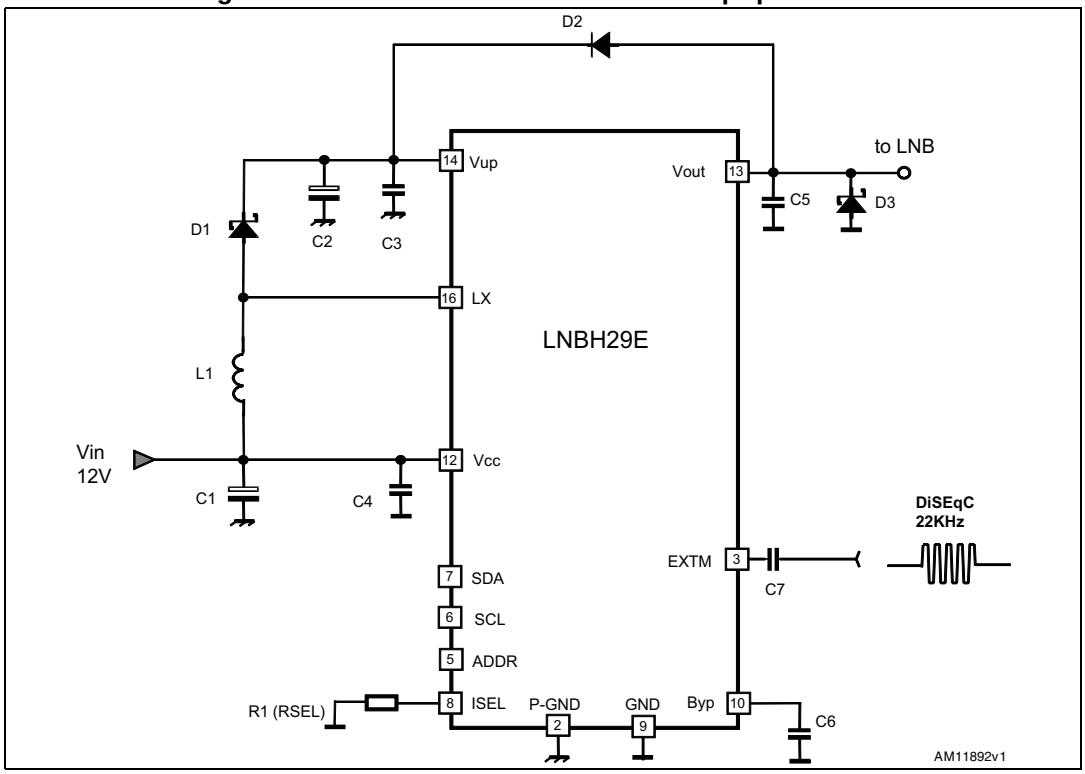


Table 5. Typical application circuit bill of material

Component	Notes
R1 (RSEL)	SMD resistor. Refer to I_{MAX} current limit selection resistor values (*Table 9*).
C1	> 25 V electrolytic capacitor, 100 µF or higher is suitable. or > 25 V ceramic capacitor, 10 µF or higher is suitable.
C2	With COMP=0, > 25 V electrolytic capacitor, 100 µF or higher is suitable. or With COMP=1, > 35 V ceramic capacitor, 22 µF (or 2 x 10 µF) or higher is suitable.
C3	From 470 nF to 2.2 µF ceramic capacitor. Higher values allow lower DC-DC noise.
C5	From 100 nF to 220 nF ceramic capacitor. Higher values allow lower DC-DC noise.
C4, C6	220 nF ceramic capacitors.
C7	100 nF or higher is suitable.
D1	STPS130A or similar Schottky diode.
D3	BAT54, BAT43, 1N5818, or any low power Schottky diode with I_F(AV) > 0.2 A, VRRM > 25 V, V_F < 0.5 V. To be placed as close as possible to V_{OUT} pin.
D2	1N4001-07, S1A-S1M, or any similar general purpose rectifier.
L1	With COMP=0, use 10 µH inductor with I_{sat}>I_{peak} where I_{peak} is the boost converter peak current. or With COMP=1 and C2 = 22 µF, use 6.8 µH inductor with I_{sat}>I_{peak} where I_{peak} is the boost converter peak current.

6 I²C bus interface

Data transmission from the main microprocessor to the LNBH29 and vice versa takes place through the 2-wire I²C bus interface, consisting of the 2 lines SDA and SCL (pull-up resistors to positive supply voltage must be externally connected).

6.1 Data validity

As shown in *Figure 7*, the data on the SDA line must be stable during the high semi-period of the clock. The HIGH and LOW state of the data line can only change when the clock signal on the SCL line is LOW.

6.2 Start and stop condition

As shown in *Figure 8*, a start condition is a HIGH to LOW transition of the SDA line while SCL is HIGH. The stop condition is a LOW to HIGH transition of the SDA line while SCL is HIGH. A stop condition must be sent before each start condition.

6.3 Byte format

Every byte transferred to the SDA line must contain 8 bits. Each byte must be followed by an acknowledge bit. The MSB is transferred first.

6.4 Acknowledge

The master (microprocessor) puts a resistive HIGH level on the SDA line during the acknowledge clock pulse (see *Figure 9*). The peripheral (LNBH29) that acknowledges must pull down (LOW) the SDA line during the acknowledge clock pulse, so that the SDA line is stable LOW during this clock pulse. The peripheral which has been addressed must generate an acknowledge after the reception of each byte, otherwise the SDA line remains at the HIGH level during the ninth clock pulse time. In this case the master transmitter can generate the STOP information in order to abort the transfer. The LNBH29 does not generate an acknowledge if the V_{CC} supply is below the undervoltage lockout threshold (4.7 V typ.).

6.5 Transmission without acknowledge

If the detection of an acknowledge from the LNBH29 is not required, the microprocessor can use a simpler transmission: it simply waits one clock cycle without checking the slave acknowledging, and sends the new data. This approach is of course less protected from misworking and decreases the noise immunity.

Figure 7. Data validity on the I²C bus

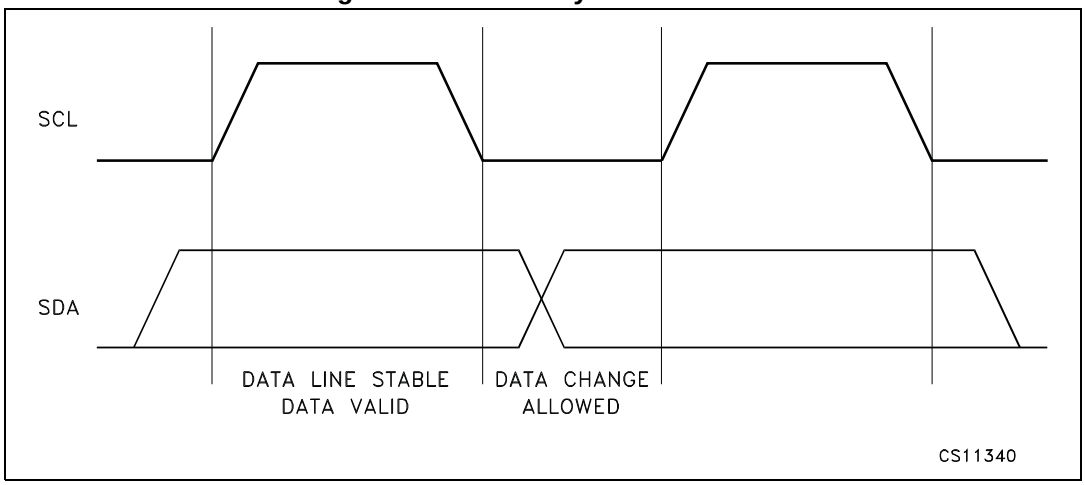


Figure 8. Timing diagram of I²C bus

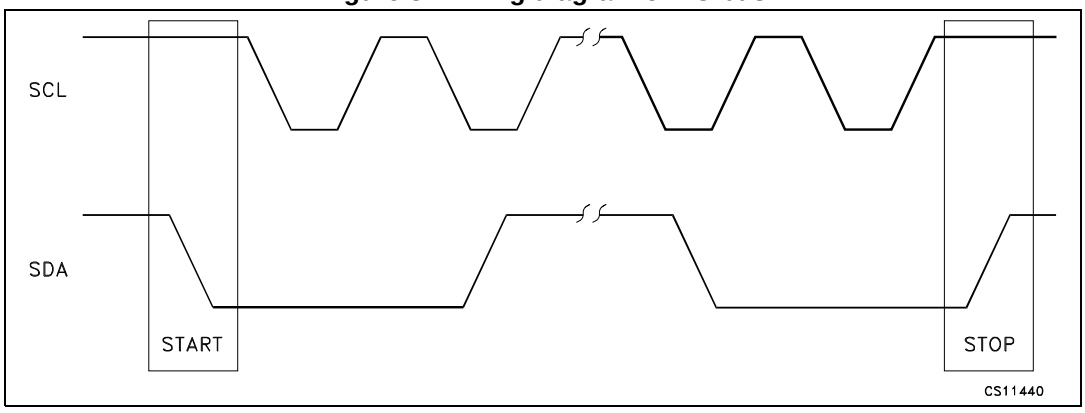
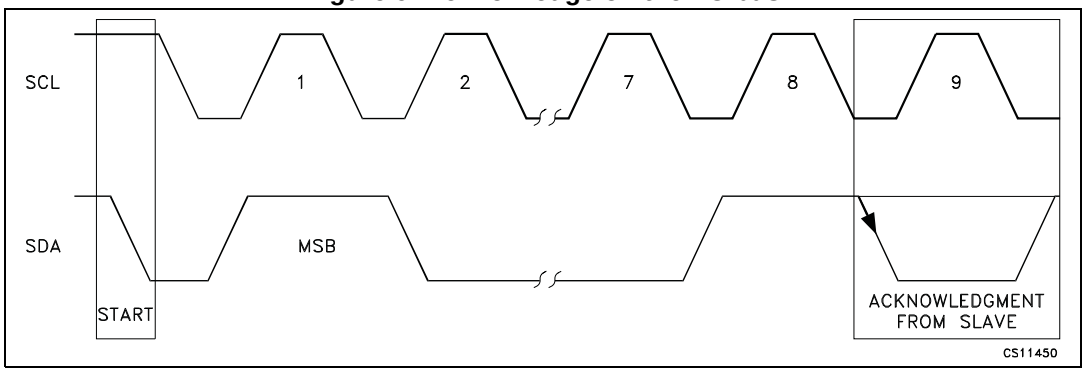


Figure 9. Acknowledge on the I²C bus



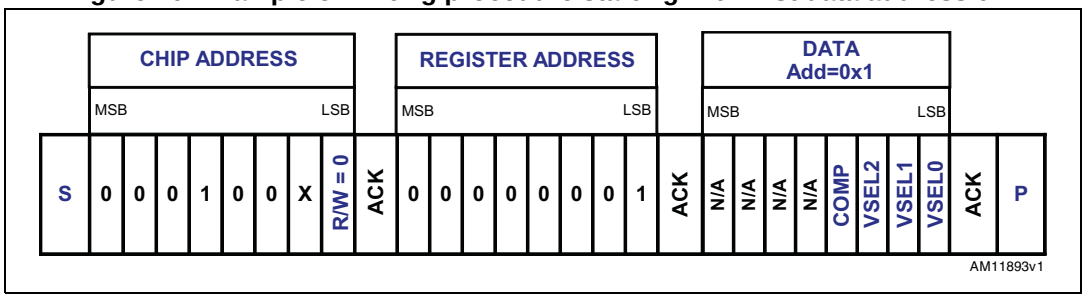
7 I²C interface protocol

7.1 Write mode transmission

The LNBH29 series interface protocol comprises:

- a start condition (S)
- a chip address byte with the LSB bit R/W = 0
- a register address (internal address of the first register to be accessed)
- a sequence of data (byte to write in the addressed internal register + acknowledge)
- a stop condition (P). The transfer lasts until a stop bit is encountered
- the LNBH29, as slave, acknowledges every byte transfer.

Figure 10. Example of writing procedure starting with first data address 0x2



ACK = Acknowledge

S = Start

P = Stop

R/W = 1/0, Read/Write bit

X = 0/1, set the values to select the chip address (see *Table 11* for pin selection).

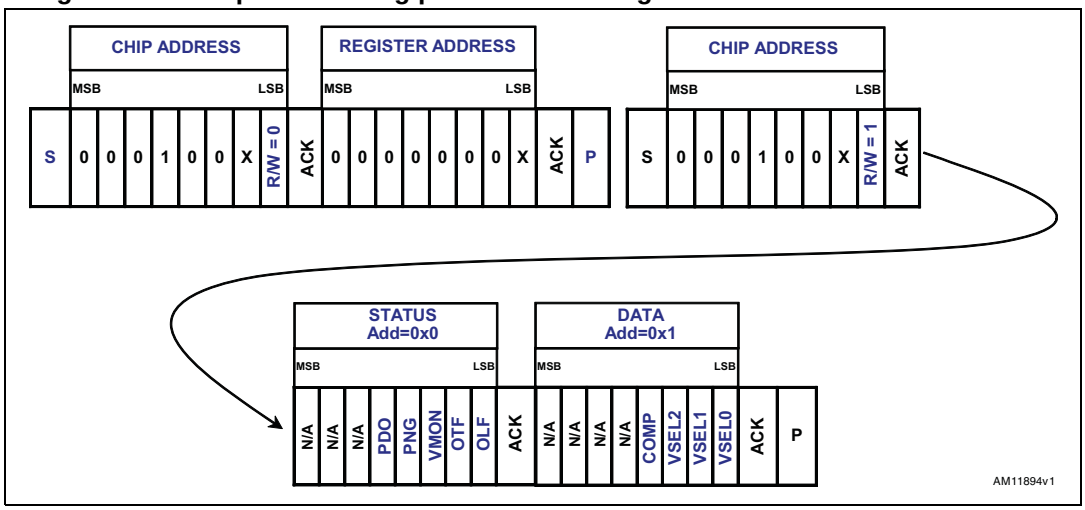
Note: One only DATA register address 0x1 is available for the writing procedure.

7.2 Read mode transmission

In Read mode the bytes sequence must be as follows:

- a start condition (S)
- a chip address byte with the LSB bit R/W=0
- the register address byte of the internal first register to be accessed
- a stop condition (P)
- a new master transmission with the chip address byte and the LSB bit R/W=1
- after the acknowledge the LNBH29 starts to send the addressed register content. As long as the master keeps the acknowledge LOW, the LNBH29 transmits the next address register byte content.
- the transmission is terminated when the master sets the acknowledge HIGH with a following stop bit.

Figure 11. Example of reading procedure starting with first status address 0X0 (a)



ACK = Acknowledge
S = Start
P = Stop
R/W = 1/0, Read/Write bit
X = 0/1, set the values to select the chip address (see Chip Address pin selection table) and to select the register address (0x0 for STATUS register and 0x1 for DATA register).

7.3 DATA register

The DATA register can be addressed both in Write and Read mode. In Read mode it returns the last writing byte status received in the previous write transmission.

Table 6 provides the DATA register values with relevant function description of each bit.

a. The reading procedure can start from any register address (STATUS or DATA) by simply setting the X values in the register address byte (after the first chip address in *Figure 11*). It can be also stopped from the master by sending a stop condition after any acknowledge bit.

Table 6. DATA (READ/WRITE register. Register address = 0X1)

BIT	Name	Value	Description
Bit 0 (LSB)	VSEL0	0/1	Output voltage selection bits. (Refer to *Table 7*)
Bit 1	VSEL1	0/1	
Bit 2	VSEL2	0/1	
Bit 3	COMP	1	DC-DC converter compensation: set to “1” for using very low E.S.R. capacitors or ceramic caps (V_{UP} pin).
		0	DC-DC converter compensation: set to “0” for using standard E.S.R. capacitors (V_{UP} pin).
Bit 4	N/A	0	Reserved. Keep to “0”
Bit 5	N/A	0	Reserved. Keep to “0”
Bit 6	N/A	0	Reserved. Keep to “0”
Bit 7 (MSB)	N/A	0	Reserved. Keep to “0”

N/A = Reserved bit.

All bits reset to “0” at power-on.

Table 7. Output voltage selection table (DATA register, Write mode)

VSEL2	VSEL1	VSEL0	V_{OUT} min.	V_{OUT} pin voltage	V_{OUT} max.	Function
0	0	0		0.000		V_{OUT} disabled. LNBH29/LNBH29E set in Standby mode
0	0	1	12.545	13.000	13.455	
0	1	0	12.867	13.333	13.800	
0	1	1	13.188	13.667	14.000	
1	0	1	17.515	18.150	18.785	
1	1	0	17.836	18.483	19.130	
1	1	1	18.158	18.817	19.475	

7.4 STATUS register

The STATUS register can be addressed only in Read mode and provides the diagnostic functions described in *Table 8*.

Table 8. STATUS (READ register. Register address = 0X0)

BIT	Name	Value	Description
Bit 0 (LSB)	OLF	1	Output short-circuit or V_{OUT} pin overload protection has been triggered ($I_{OUT} > I_{MAX}$).
		0	No overload protection has been triggered to V_{OUT} pin ($I_{OUT} < I_{MAX}$).
Bit 1	OTF	1	Junction overtemperature is detected, $T_J > 150$ °C.
		0	Junction overtemperature not detected, $T_J < 135$ °C. T_J is below thermal protection threshold.
Bit 2	VMON	1	Output voltage (V_{OUT} pin) lower than VMON specification thresholds. Refer to *Table 12*.
		0	Output voltage (V_{OUT} pin) is within the VMON specifications.
Bit 3	PNG	1	Input voltage (V_{CC} pin) lower than LPD minimum thresholds. Refer to VLP in *Table 9*.
		0	Input voltage (V_{CC} pin) higher than LPD thresholds. Refer to VLP in *Table 9*.
Bit 4	PDO	1	Overcurrent detected on output pull-down stage for a time longer than de-glitch period. This may happen due to an external voltage source present on the LNB output (V_{OUT} pin).
		0	No overcurrent detected on output pull-down stage.
Bit 5	N/A	-	Reserved
Bit 6	N/A	-	Reserved
Bit 7 (MSB)	N/A		Reserved

N/A = Reserved bit.

All bits reset to “0” at power-on.

8 Electrical characteristics

Refer to the *Section 5: Typical application circuits*, T_J from 0 to 85 °C, DATA register bits set to “0” except VSEL0 = 1, RSEL = 16.2 kΩ, DSQIN = LOW, V_{IN} = 12 V, I_{OUT} = 50 mA, unless otherwise stated. Typical values are referred to T_J = 25 °C. V_{OUT} = V_{OUT} pin voltage. See software description section for I²C access to the system register (*Section 6* and *Section 7*).

Table 9. Electrical characteristic

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
V_{IN}	Supply voltage (1)		8	12	17.5	V
I_{IN}	Supply current	I_{OUT} = 0 mA		6		mA
		22 kHz tone enabled (DSQIN=high), I_{OUT} = 0 mA		10		
		VSEL0=VSEL1=VSEL2=0		1		
V_{OUT}	Output voltage total accuracy	Valid at any V_{OUT} selected level	-3.5		+3.5	%
V_{OUT}	Line regulation	V_{IN} = 8 to 17.5 V			40	mV
V_{OUT}	Load regulation	I_{OUT} from 50 to 500 mA			100	
I_{MAX}	Output current limiting thresholds	RSEL = 16.2 kΩ	500		750	mA
		RSEL = 22 kΩ	350		550	
I_{SC}	Output short-circuit current	RSEL= 16.2 kΩ		400		mA
SS	Soft-start time	V_{OUT} from 0 to 13 V		4		ms
SS	Soft-start time	V_{OUT} from 0 to 18 V		6		ms
T13-18	Soft transition rise time	V_{OUT} from 13 V to 18 V		1.5		ms
T18-13	Soft transition fall time	V_{OUT} from 18 V to 13 V		1.5		ms
T_{OFF}	Dynamic overload protection OFF-time	Output shorted		900		ms
T_{ON}	Dynamic overload protection ON-time	Output shorted		T_{OFF}/ 10		
A_{TONE}	Tone amplitude	DSQIN = “1” (using internal tone generator) I_{OUT} from 0 to 500 mA C_{BUS} from 0 to 750 nF	0.55	0.675	0.8	V_{PP}
F_{TONE}	Tone frequency	DSQIN = “1” (using internal tone generator)	20	22	24	kHz
D_{TONE}	Tone duty cycle		43	50	57	%
tr, tf	Tone rise or fall time (2)		5	8	15	µs
G_{EXTM}	External modulation gain (3)	Δ_{VOUT}/ Δ_{VEXTM}, freq. from 10 kHz to 30 kHz		10		
V_{EXTM}	External modulation input voltage (3)	EXTM AC coupling (4)			400	mV_{PP}
Z_{EXTM}	External modulation impedance (3)			230		W

Table 9. Electrical characteristic (continued)

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$Eff_{DC/DC}$	DC-DC converter efficiency	I_{OUT} = 500 mA		93		%
F_{SW}	DC-DC converter switching frequency			440		kHz
UVLO	Undervoltage lockout thresholds	UVLO threshold rising		4.8		V
		UVLO threshold falling		4.7		
V_{LP}	Low power diagnostic (LPD) thresholds	V_{LP} threshold rising		7.2		V
		V_{LP} threshold falling		6.7		
V_{IL}	DSQIN, pin logic LOW				0.8	V
V_{IH}	DSQIN, pin logic HIGH		2			V
I_{IH}	DSQIN, pin input current	V_{IH} = 5 V		15		µA
I_{OBK}	Output backward current	All VSELx=0 V, V_{OBK}=30 V		-3	-6	mA
I_{SINK}	Output low-side sink current	V_{OUT} forced at V_{OUT_nom} + 0.1 V		50		mA
$I_{SINK_TIME-OUT}$	Low-side sink current timeout	V_{OUT} forced at V_{OUT_nom} + 0.1 V PDO I²C bit is set to “1” after this time has elapsed		10		ms
I_{REV}	Max. reverse current	V_{OUT} forced at V_{OUT_nom} + 0.1 V, after PDO bit is set to “1” ($I_{SINK_TIME-OUT}$ has elapsed)		2		mA
T_{SHDN}	Thermal shutdown threshold			150		°C
ΔT_{SHDN}	Thermal shutdown hysteresis			15		°C

1. In applications where (V_{CC} - V_{OUT}) > 1.3 V, the increased power dissipation inside the integrated LDO must be taken into account in the application thermal management design.
2. Guaranteed by design.
3. Only for type LNBH29E.
4. External signal maximum voltage for which the EXTM function is guaranteed.

T_J from 0 to 85 °C, V_I = 12 V.

Table 10. I²C electrical characteristics

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
V_{IL}	Low level input voltage	SDA, SCL			0.8	V
V_{IH}	High level input voltage	SDA, SCL	2			V
I_{IN}	Input current	SDA, SCL, V_{IN} = 0.4 to 4.5 V	-10		10	µA
V_{OL}	Low level output voltage	SDA (open drain), I_{OL} = 6 mA			0.6	V
F_{MAX}	Maximum clock frequency	SCL			400	kHz

T_J from 0 to 85 °C, V_I = 12 V.

Table 11. Address pin characteristics

Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
V_{ADDR-1}	“0001000(R/W)” address pin voltage range	R/W bit determines the transmission mode: read (R/W=1) write (R/W=0)	0		0.8	V
V_{ADDR-2}	“0001001(R/W)” address pin voltage range	R/W bit determines the transmission mode: read (R/W=1) write (R/W=0)	2		5	V

Refer to *Section 5: Typical application circuits*, T_J from 0 to 85 °C, DATA register bits set to “0”, RSEL = 16 kΩ, DSQIN = LOW, V_{IN} = 12 V, I_{OUT} = 50 mA, unless otherwise stated. Typical values are referred to T_J = 25 °C. V_{OUT} = V_{OUT} pin voltage. See software description section for I²C access to the STATUS register.

Table 12. Output voltage diagnostic (VMON BIT, STATUS register) characteristics

Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
V_{TH-L}	Diagnostic low threshold at V_{OUT} = 13.0 V	VSEL0=1, VSEL1=VSEL2=0	80	90	95	%
V_{TH-L}	Diagnostic low threshold at V_{OUT} = 18.15 V	VSEL1=0, VSEL0=VSEL2=1	80	90	95	%

Note: If the output voltage is lower than the min. value the VMON I²C bit is set to 1.

If VMON = 0 then V_{OUT} > 80% of V_{OUT} typical.

If VMON = 1 then V_{OUT} < 95% of V_{OUT} typical.

9 Package mechanical data

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK specifications, grade definitions and product status are available at: *www.st.com*. ECOPACK is an ST trademark.

Table 13. QFN16 (4 x 4 mm.) mechanical data

Dim.	mm		
	Min.	Typ.	Max.
A	0.80	0.90	1.00
A1	0.00	0.02	0.05
A3		0.20	
b	0.25	0.30	0.35
D	3.90	4.00	4.10
D2	2.50		2.80
E	3.90	4.00	4.10
E2	2.50		2.80
e		0.65	
L	0.30	0.40	0.50

Figure 12. QFN16 (4 x 4 mm) drawing

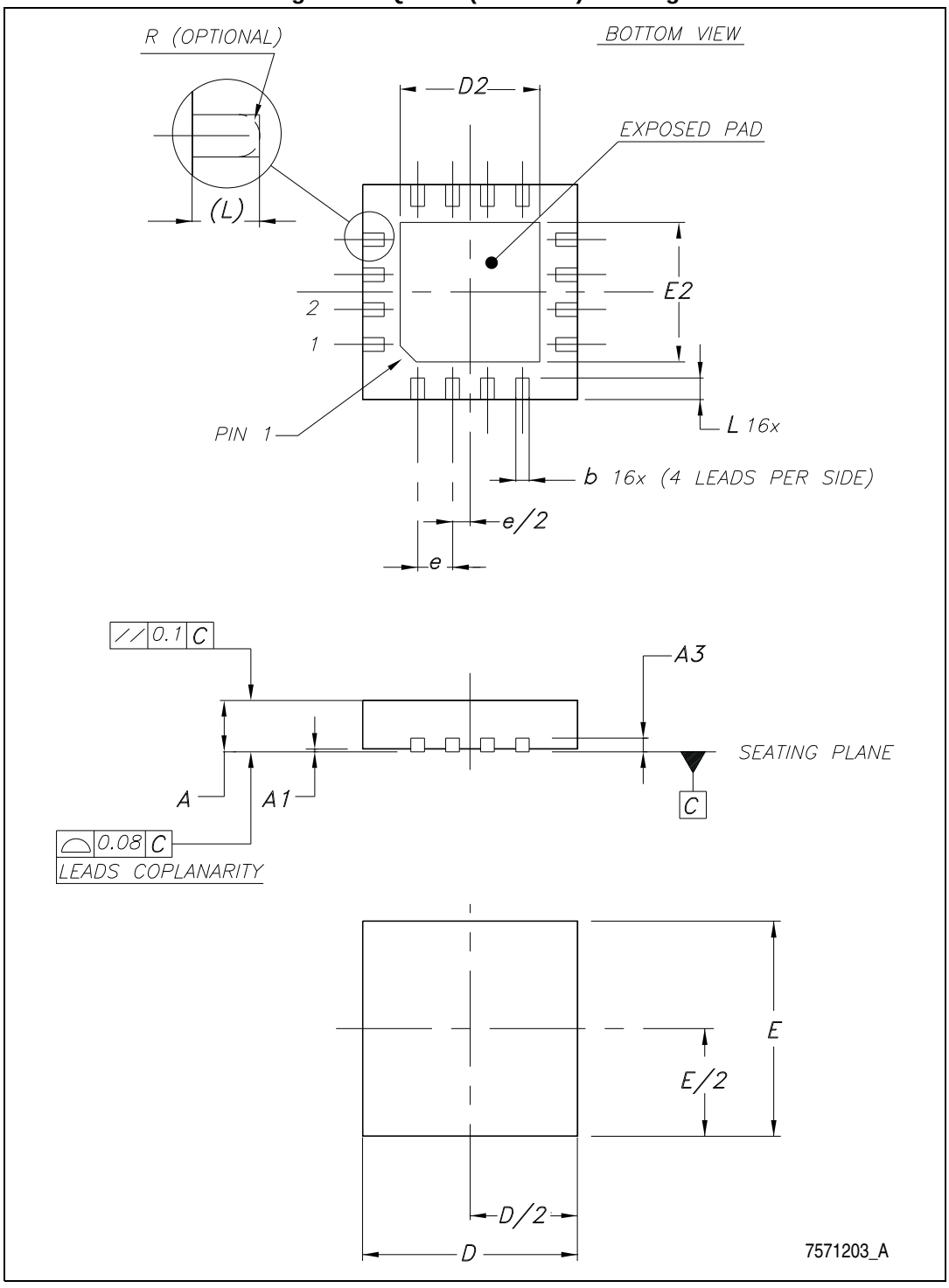
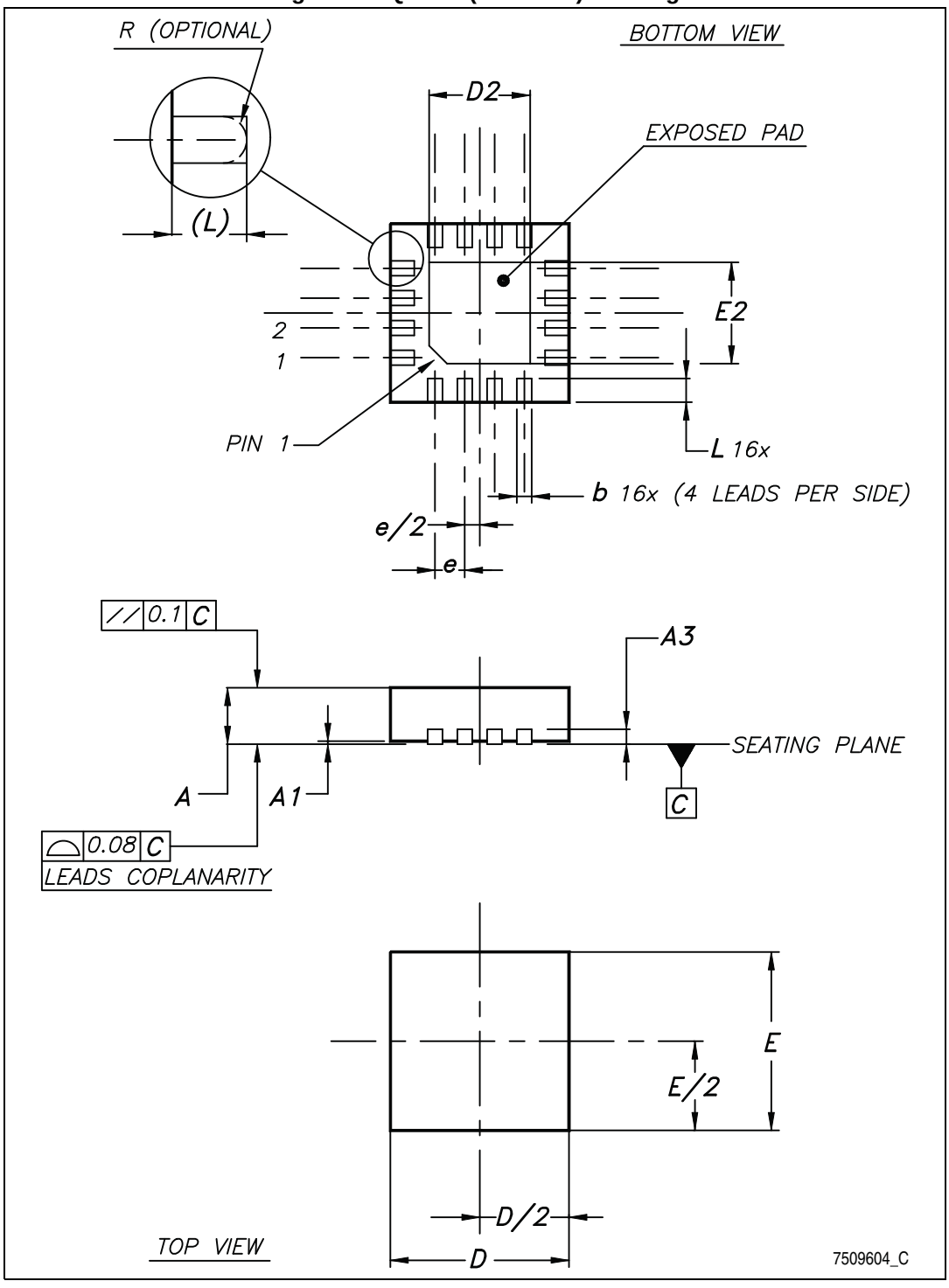


Table 14. QFN16 (3 x 3 mm) mechanical data

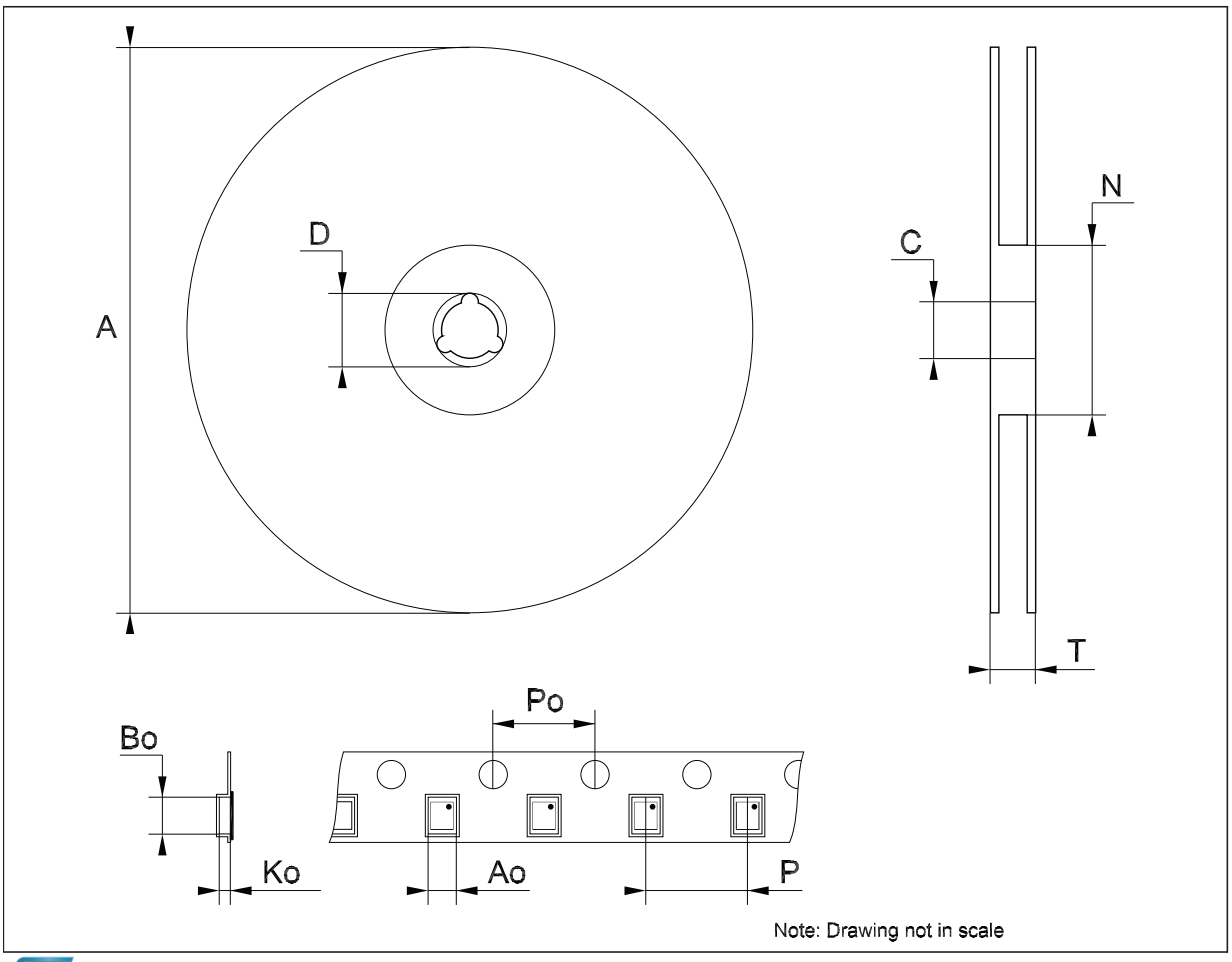
Dim.	mm.		
	Min.	Typ.	Max.
A	0.80	0.90	1.00
A1	0.00		0.05
A3		0.20	
b	0.18		0.30
D	2.90	3.00	3.10
D2	1.50		1.80
E	2.90	3.00	3.10
E2	1.50		1.80
e		0.50	
L	0.30		0.50

Figure 13. QFN16 (3 x 3 mm) drawing



Tape & reel QFNxx/DFNxx (4x4) mechanical data

Dim.	mm.			inch.		
	Min.	Typ.	Max.	Min.	Typ.	Max.
A			330			12.992
C	12.8		13.2	0.504		0.519
D	20.2			0.795		
N	99		101	3.898		3.976
T			14.4			0.567
Ao		4.35			0.171	
Bo		4.35			0.171	
Ko		1.1			0.043	
Po		4			0.157	
P		8			0.315	



Tape and reel QFNxx/DFNxx (3x3 mm) mechanical data

Dim.	mm.			inch.		
	Min.	Typ.	Max.	Min.	Typ.	Max.
A			330			12.992
C	12.8		13.2	0.504		0.519
D	20.2			0.795		
N	60			2.362		
T			18.4			0.724
Ao		3.3			0.130	
Bo		3.3			0.130	
Ko		1.1			0.043	
Po		4			0.157	
P		8			0.315	

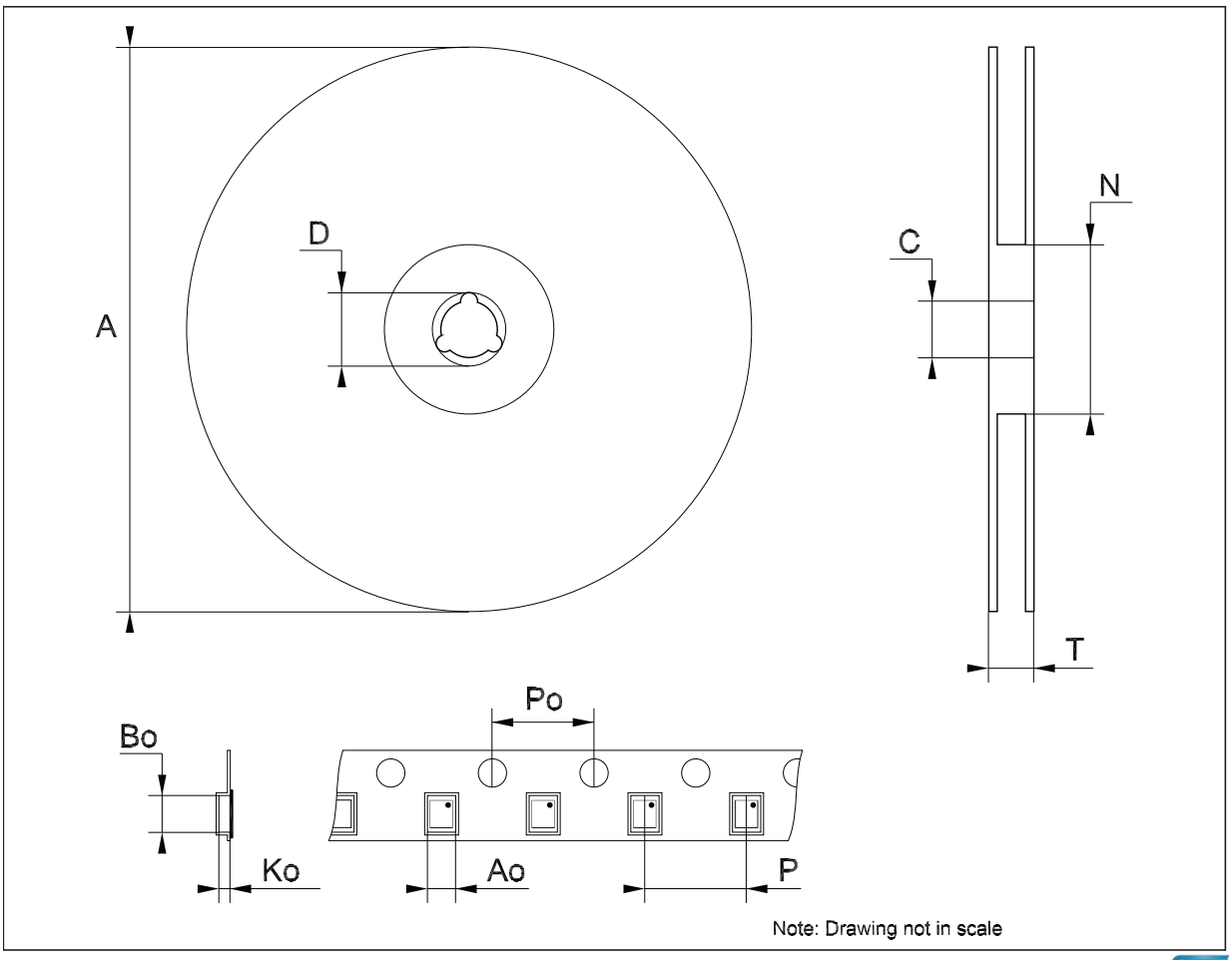


Figure 14. QFN16 (4 x 4) footprint recommended data (mm)

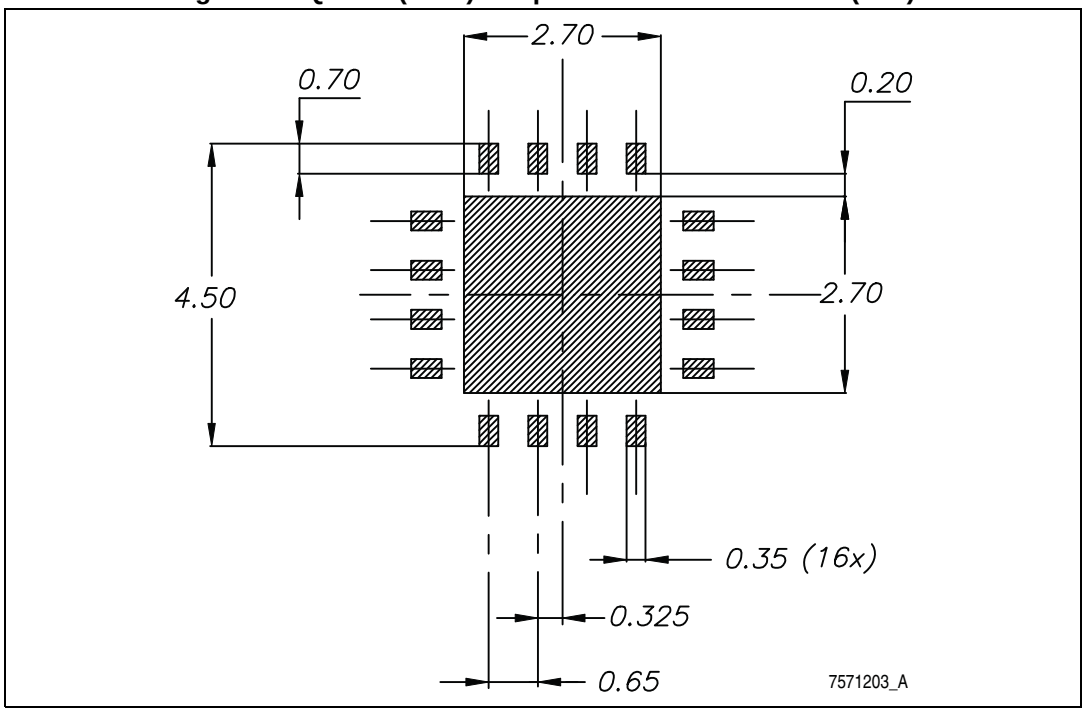
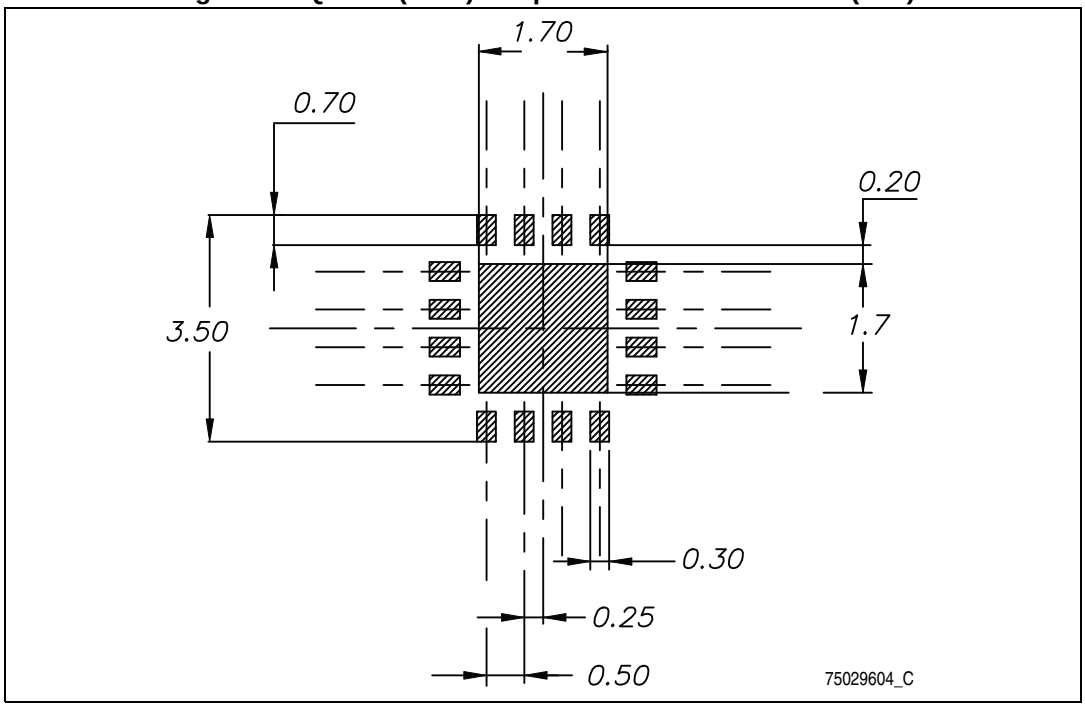


Figure 15. QFN16 (3 x 3) footprint recommended data (mm)



10 Revision history

Table 15. Document revision history

Date	Revision	Changes
03-Aug-2012	1	Initial release.
01-Oct-2012	2	Modified: L1 notes *Table 5 on page 13*.
15-Mar-2013	3	Modified: Maximum clock frequency Max. value *Table 10 on page 21*.

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