LMZ22010 10-A SIMPLE SWITCHER® Power Module With 20-V Maximum Input Voltage and Current Sharing

1 Features

- Integrated Shielded Inductor
- Simple PCB Layout
- Frequency Synchronization Input (350 kHz to 600 kHz)
- Current Sharing Capability
- Flexible Start-up Sequencing Using External Soft-Start, Tracking and Precision Enable
- Protection Against Inrush Currents and Faults Such as Input UVLO and Output Short Circuit
- Junction Temperature Range –40°C to 125°C
- Single Exposed Pad and Standard Pinout for Easy Mounting and Manufacturing
- Fully Enabled for WEBENCH® Power Designer
- Pin Compatible With LMZ22008/06, LMZ12010/08/06, LMZ23610/08/06, and LMZ13610/08/06
- Electrical Specifications
  - 50-W Maximum Total Output Power
  - Up to 10-A Output Current
  - Input Voltage Range 6 V to 20 V
  - Output Voltage Range 0.8 V to 6 V
  - Efficiency up to 92%
- Performance Benefits
  - High Efficiency Reduces System Heat Generation
  - Low Radiated Emissions (EMI) Tested to EN55022
  - Only 7 External Components
  - Low Output Voltage Ripple
  - No External Heat Sink Required
  - Simple Current sharing for Higher Current Applications

NOTE: EN 55022:2006, +A1:2007, FCC Part 15 Subpart B, tested on Evaluation Board with EMI configuration.

2 Applications

- Point-of-load Conversions from 12-V Input Rail
- Time-Critical Projects
- Space Constrained and High Thermal Requirement Applications
- Negative Output Voltage Applications See AN-2027 SNVA425

3 Description

The LMZ22010 SIMPLE SWITCHER® power module is an easy-to-use step-down DC-DC solution capable of driving up to 10-A load. The LMZ22010 is available in an innovative package that enhances thermal performance and allows for hand or machine soldering.

The LMZ22010 can accept an input voltage rail between 6 V and 20 V and can deliver an adjustable and highly accurate output voltage as low as 0.8 V. The LMZ22010 only requires two external resistors and external capacitors to complete the power solution.

The LMZ22010 is a reliable and robust design with the following protection features: thermal shutdown, programmable input under-voltage lockout, output over-voltage protection, short-circuit protection, output current limit, and allows startup into a pre-biased output. The sync input allows synchronization over the 314- to 600-kHz switching frequency range and up to 6 modules can be connected in parallel for higher load currents.

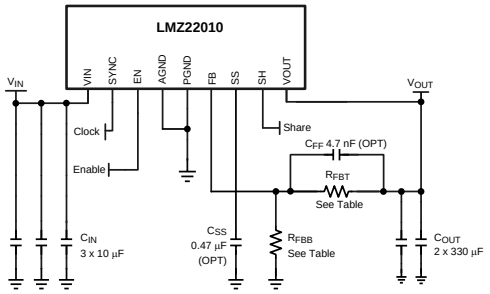
Device Information(1)(2)

PART NUMBER	PACKAGE	BODY SIZE (NOM)
LMZ22010	NDY (11)	15.00 mm × 15.00 mm

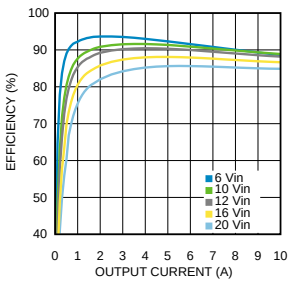
(1) For all available packages, see the orderable addendum at the end of the data sheet.

(2) Peak reflow temperature equals 245°C. See SNAA214 for more details.

Simplified Application Schematic



Efficiency 3.3-V Output at 25°C



An IMPORTANT NOTICE at the end of this data sheet addresses availability, warranty, changes, use in safety-critical applications, intellectual property matters and other important disclaimers. PRODUCTION DATA.

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4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision G (October 2013) to Revision H **Page**

- Added *Pin Configuration and Functions* section, *ESD Ratings* table, *Feature Description* section, *Device Functional Modes*, *Application and Implementation* section, *Power Supply Recommendations* section, *Layout* section, *Device and Documentation Support* section, and *Mechanical, Packaging, and Orderable Information* section ... 1
- Deleted Easy-to-Use Pin Package image ... 1

Changes from Revision F (March 2013) to Revision G **Page**

- Deleted 12 mils ... 3
- Deleted 12 mil ... 4
- Changed 12 mil ... 24
- Changed 12 mil ... 27
- Added *Power Module SMT Guidelines* ... 27

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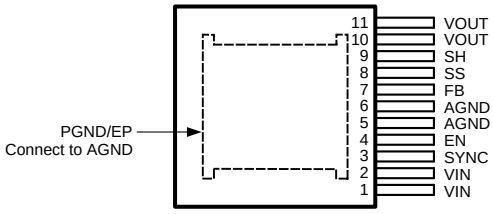
5 Pin Configuration and Functions

NDY Package
11-Pin
Top View



Pin Functions

PIN		TYPE	DESCRIPTION
NAME	NO.		
AGND	5	Ground	Analog Ground — Reference point for all stated voltages. Must be externally connected to PGND(EP).
	6		
EN	4	Analog	Enable — Input to the precision enable comparator. Rising threshold is 1.274 V typical. Once the module is enabled, a 13-µA source current is internally activated to facilitate programmable hysteresis.
FB	7	Analog	Feedback — Internally connected to the regulation amplifier and overvoltage comparator. The regulation reference point is 0.795 V at this input pin. Connect the feedback resistor divider between VOUT and AGND to set the output voltage.
PGND	—	Ground	Exposed Pad / Power Ground — Electrical path for the power circuits within the module. PGND is not internally connected to AGND (pin 5,6). Must be electrically connected to pins 5 and 6 external to the package. The exposed pad is also used to dissipate heat from the package during operation. Use one hundred thermal vias from top to bottom copper for best thermal performance.
SH	9	Analog	Share — Connect this pin to the share pin of other LMZ22010 modules to share the load between the devices. One device must be configured as the master by connecting FB normally. All other devices must be configured as slaves by leaving their respective FB pins floating. Leave SH floating if current sharing is not used. Do Not Ground. See *Design Steps for the LMZ22010 Application* section.
SS	8	Analog	Soft-Start/Track Input — To extend the 1.6-ms internal soft-start connect an external soft-start capacitor. For tracking connect to an external resistive divider connected to a higher priority supply rail. See *Design Steps for the LMZ22010 Application* section.
SYNC	3	Analog	Synchronization — Apply a CMOS logic level square wave whose frequency is between 314 kHz and 600 kHz to synchronize the PWM operating frequency to an external frequency source. When not using synchronization this pin must be tied to ground. The module free-running PWM frequency is 359 kHz (typical).
VIN	1	Power	Input supply — Nominal operating range is 6 V to 20 V. A small amount of internal capacitance is contained within the package assembly. Additional external input capacitance is required between this pin and the exposed pad (PGND).
	2		
VOUT	10	Power	Output Voltage — Output from the internal inductor. Connect the output capacitor between this pin and exposed pad (PGND).
	11		

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6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)(2)(3)

	MIN	MAX	UNIT
VIN to PGND	–0.3	24	V
EN, SYNC to AGND	–0.3	5.5	V
SS, FB, SH to AGND	–0.3	2.5	V
AGND to PGND	–0.3	0.3	V
Junction Temperature		150	°C
Peak Reflow Case Temperature (30 sec)		245	°C
Storage Temperature	–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) If Military/Aerospace specified devices are required, please contact the Texas Instruments Sales Office/ Distributors for availability and specifications.
(3) For soldering specifications, refer to the following document: SNOA549

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)(2)	±2000	V

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) The human body model is a 100-pF capacitor discharged through a 1.5-kΩ resistor into each pin. Test method is per JESD-22-114.

6.3 Recommended Operating Conditions

	MIN	MAX	UNIT
VIN	6	20	V
EN, SYNC	0	5	V
Operation Junction Temperature	−40	125	°C

6.4 Thermal Information

THERMAL METRIC(1)			LMZ22010 NDY 11 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance(2)	Natural Convection	9.9	°C/W
		225 LFPM	6.8	
		500 LFPM	5.2	
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance		1.0	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report, SPRA953.
(2) Theta JA measured on a 3.0-in x 3.5-in 4-layer board, with 2-oz. copper on outer layers and 1-oz. copper on inner layers, two hundred and ten thermal vias, and 2-W power dissipation. Refer to evaluation board application note layout diagrams.

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6.5 Electrical Characteristics

Limits are for T_J = 25°C unless otherwise specified. Minimum and Maximum limits are ensured through test, design or statistical correlation. Typical values represent the most likely parametric norm at T_J = 25°C, and are provided for reference purposes only. Unless otherwise stated the following conditions apply: V_{IN} = 12 V, V_{OUT} = 3.3 V.

PARAMETER		TEST CONDITIONS		MIN(1)	TYP(2)	MAX(1)	UNIT
SYSTEM PARAMETERS							
ENABLE CONTROL							
V_{EN}	EN threshold	V_{EN} rising			1.274		V
			over the junction temperature (T_J) range of –40°C to +125°C	1.096		1.452	
I_{EN-HYS}	EN hysteresis source current	V_{EN} > 1.274 V			13		µA
SOFT-START							
I_{SS}	SS source current	V_{SS} = 0 V			50		µA
			over the junction temperature (T_J) range of –40°C to +125°C	40		60	
t_{SS}	Internal soft-start interval				1.6		ms
CURRENT LIMIT							
I_{CL}	Current limit threshold	DC average		12.5			A
INTERNAL SWITCHING OSCILLATOR							
f_{osc}	Free-running oscillator frequency	Sync input connected to ground		314	359	404	kHz
f_{sync}	Synchronization range	V_{sync} = 3.3 Vp-p		314		600	kHz
$V_{IL-sync}$	Synchronization logic zero amplitude	Relative to AGND	over the junction temperature (T_J) range of –40°C to +125°C			0.4	V
$V_{IH-sync}$	Synchronization logic one amplitude	Relative to AGND	over the junction temperature (T_J) range of –40°C to +125°C	1.8			V
$Sync_{DC}$	Synchronization duty cycle range			15%	50%	85%	
REGULATION AND OVERVOLTAGE COMPARATOR							
V_{FB}	In-regulation feedback voltage	V_{SS} >+ 0.8 V I_O = 10 A			0.795		V
			over the junction temperature (T_J) range of –40°C to +125°C	0.775		0.815	
V_{FB-OV}	Feedback over-voltage protection threshold				0.86		V
I_{FB}	Feedback input bias current				5		nA
I_Q	Non-switching quiescent current	SYNC = 3 V			3		mA
I_{SD}	Shutdown quiescent current	V_{EN} = 0 V			32		µA
D_{max}	Maximum duty factor				85%		
THERMAL CHARACTERISTICS							
T_{SD}	Thermal shutdown	Rising			165		°C
$T_{SD-HYST}$	Thermal shutdown hysteresis	Falling			15		°C
PERFORMANCE PARAMETERS(3)							
ΔV_O	Output voltage ripple	BW at 20 MHz			24		mV_{PP}
$\Delta V_O/\Delta V_{IN}$	Line regulation	V_{IN} = 12 V to 20 V, I_{OUT}= 10 A			±0.2%		
$\Delta V_O/\Delta I_{OUT}$	Load regulation	V_{IN} = 12 V, I_{OUT}= 0.001 A to 10 A			1		mV/A
η	Peak efficiency	V_{IN} = 12 V, V_{OUT} = 3.3 V, I_{OUT} = 5 A			89.5%		
η	Full load efficiency	V_{IN} = 12V, V_{OUT} = 3.3 V, I_{OUT} = 10 A			87.5%		

(1) Minimum and Maximum limits are 100% production tested at 25°C. Limits over the operating temperature range are ensured through correlation using Statistical Quality Control (SQC) methods. Limits are used to calculate Average Outgoing Quality Level (AOQL).
(2) Typical numbers are at 25°C and represent the most likely parametric norm.
(3) Refer to BOM in Table 1.

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6.6 Typical Characteristics

Unless otherwise specified, the following conditions apply: V_{IN} = 12 V; C_{IN} = three × 10 µF + 47-nF X7R Ceramic; C_{OUT} = two × 330-µF Specialty Polymer + 47-µF Ceramic + 47-nF Ceramic; C_{FF} = 4.7 nF; T_A = 25° C for waveforms. All indicated temperatures are ambient.

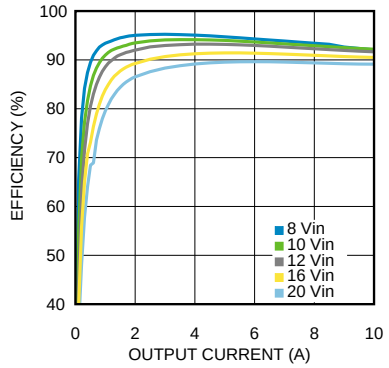

Figure 1. Efficiency 5-V Output at 25°C

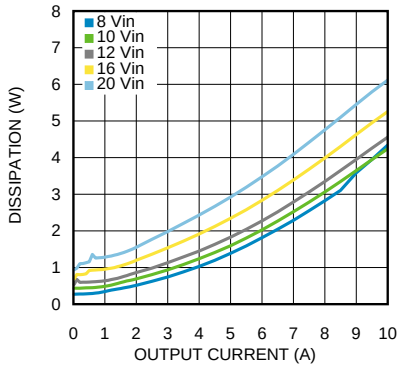

Figure 2. Dissipation 5-V Output at 25°C

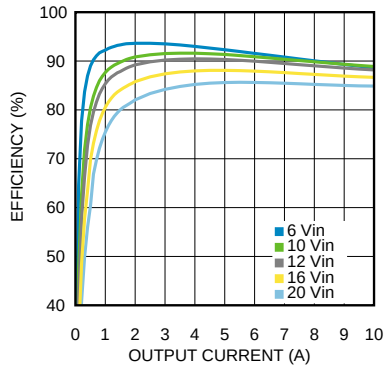

Figure 3. Efficiency 3.3-V Output at 25°C

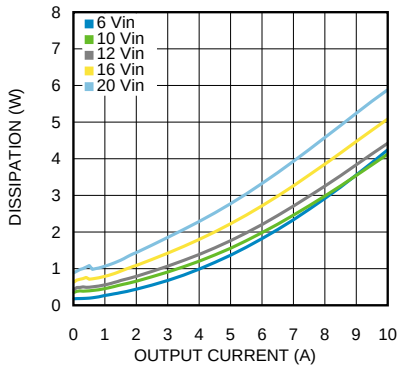

Figure 4. Dissipation 3.3-V Output at 25°C

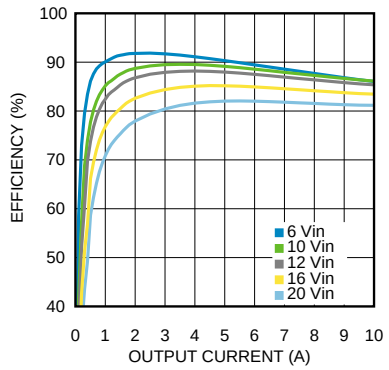

Figure 5. Efficiency 2.5-V Output at 25°C

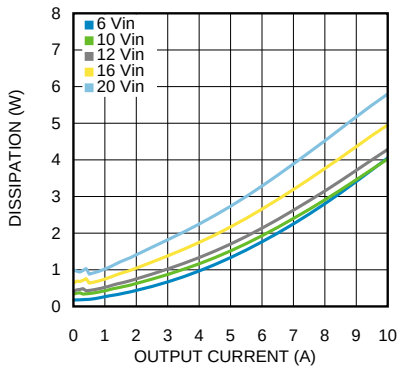

Figure 6. Dissipation 2.5-V Output at 25°C

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Typical Characteristics (continued)

Unless otherwise specified, the following conditions apply: V_{IN} = 12 V; C_{IN} = three × 10 µF + 47-nF X7R Ceramic; C_{OUT} = two × 330-µF Specialty Polymer + 47-µF Ceramic + 47-nF Ceramic; C_{FF} = 4.7 nF; T_A = 25° C for waveforms. All indicated temperatures are ambient.

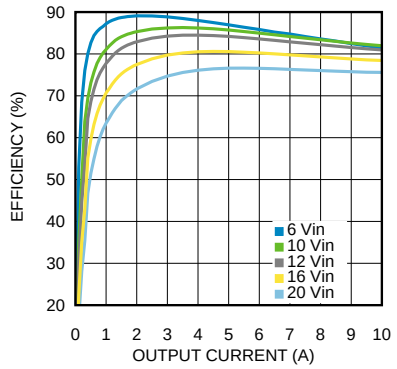

Figure 7. Efficiency 1.8-V Output at 25°C

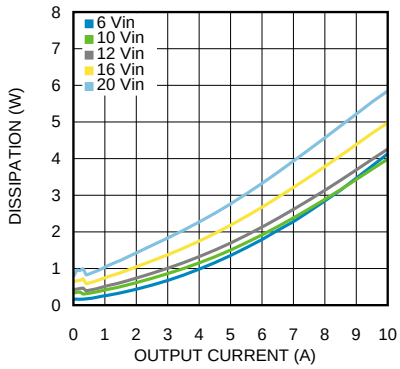

Figure 8. Dissipation 1.8-V Output at 25°C

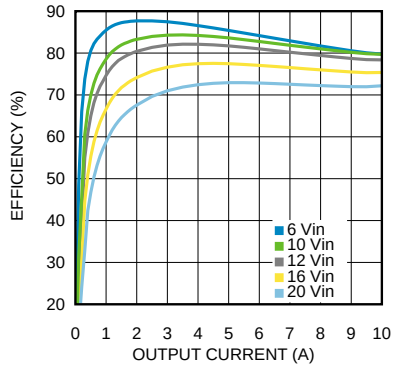

Figure 9. Efficiency 1.5-V Output at 25°C

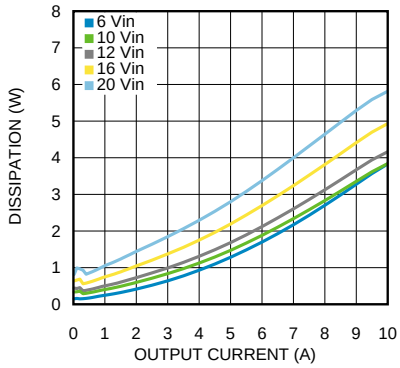

Figure 10. Dissipation 1.5-V Output at 25°C

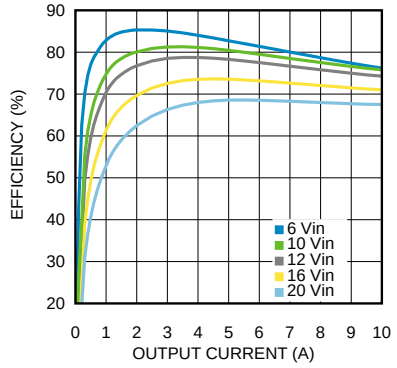

Figure 11. Efficiency 1.2-V Output at 25°C

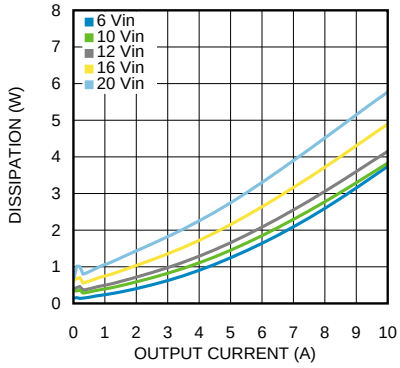

Figure 12. Dissipation 1.2-V Output at 25°C

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Typical Characteristics (continued)

Unless otherwise specified, the following conditions apply: V_{IN} = 12 V; C_{IN} = three × 10 µF + 47-nF X7R Ceramic; C_{OUT} = two × 330-µF Specialty Polymer + 47-µF Ceramic + 47-nF Ceramic; C_{FF} = 4.7 nF; T_A = 25° C for waveforms. All indicated temperatures are ambient.

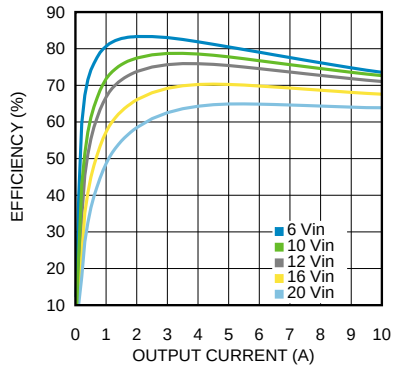

Figure 13. Efficiency 1-V Output at 25°C

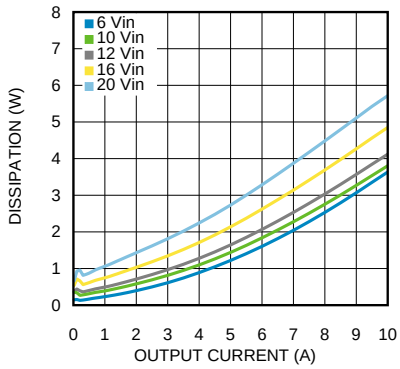

Figure 14. Dissipation 1-V Output at 25°C

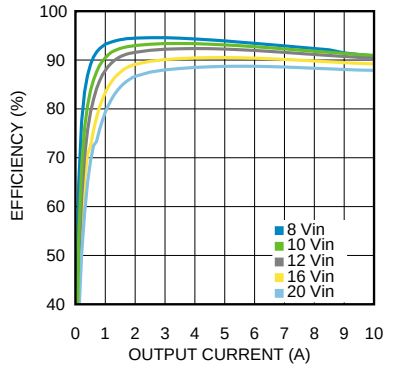

Figure 15. Efficiency 5-V Output at 85°C

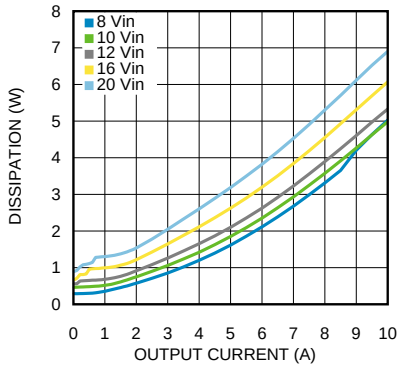

Figure 16. Dissipation 5-V Output at 85°C

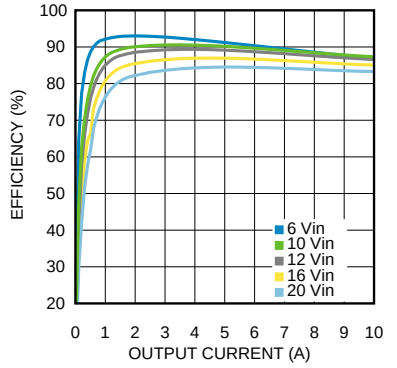

Figure 17. Efficiency 3.3-V Output at 85°C

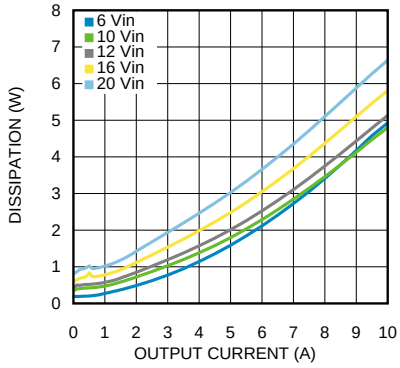

Figure 18. Dissipation 3.3-V Output at 85°C

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Typical Characteristics (continued)

Unless otherwise specified, the following conditions apply: V_{IN} = 12 V; C_{IN} = three × 10 µF + 47-nF X7R Ceramic; C_{OUT} = two × 330-µF Specialty Polymer + 47-µF Ceramic + 47-nF Ceramic; C_{FF} = 4.7 nF; T_A = 25° C for waveforms. All indicated temperatures are ambient.

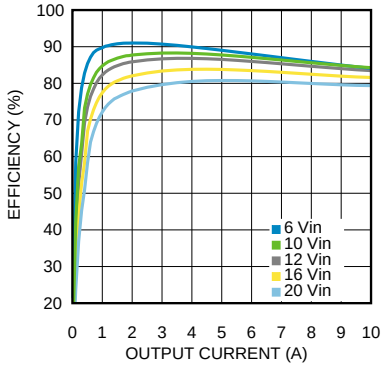

Figure 19. Efficiency 2.5-V Output at 85°C

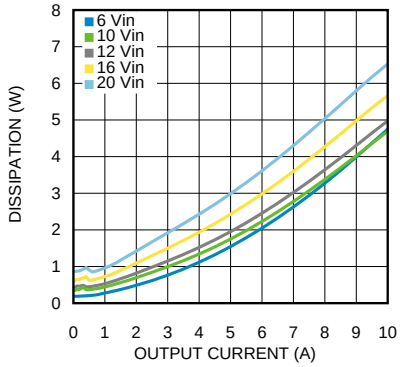

Figure 20. Dissipation 2.5-V Output at 85°C

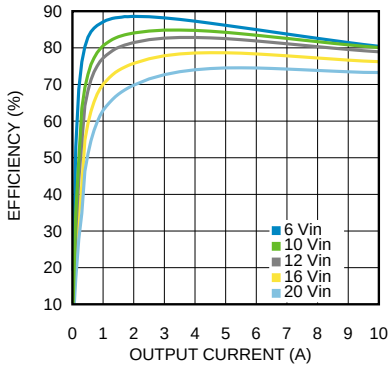

Figure 21. Efficiency 1.8-V Output at 85°C

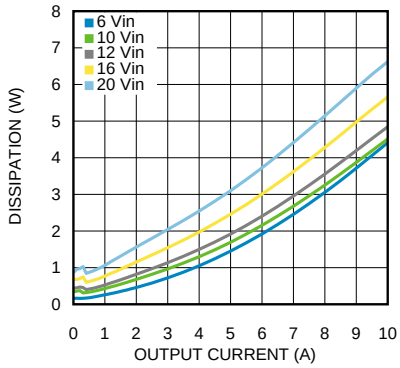

Figure 22. Dissipation 1.8-V Output at 85°C

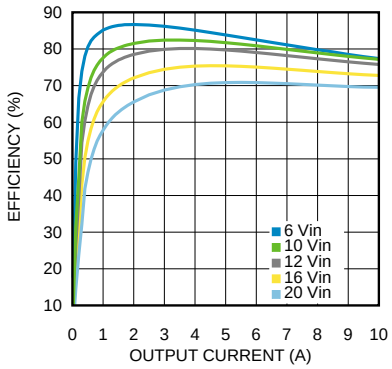

Figure 23. Efficiency 1.5-V Output at 85°C

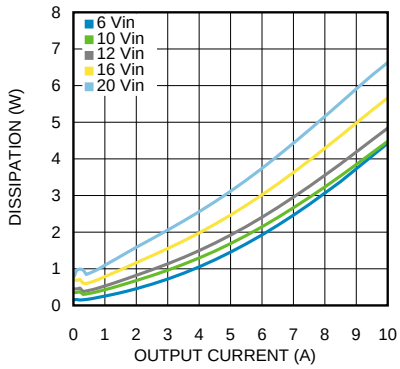

Figure 24. Dissipation 1.5-V Output at 85°C

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Typical Characteristics (continued)

Unless otherwise specified, the following conditions apply: V_{IN} = 12 V; C_{IN} = three × 10 µF + 47-nF X7R Ceramic; C_{OUT} = two × 330-µF Specialty Polymer + 47-µF Ceramic + 47-nF Ceramic; C_{FF} = 4.7 nF; T_A = 25° C for waveforms. All indicated temperatures are ambient.

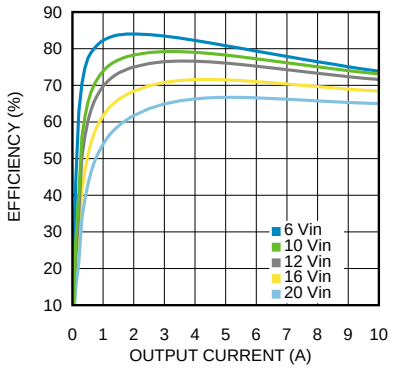


Figure 25. Efficiency 1.2-V Output at 85°C

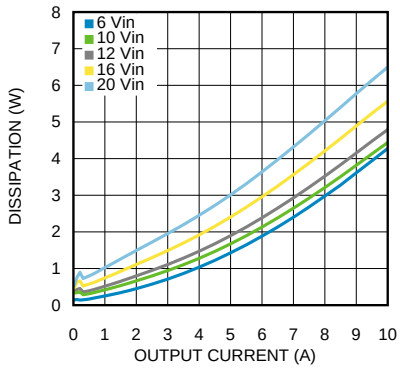


Figure 26. Dissipation 1.2-V Output at 85°C

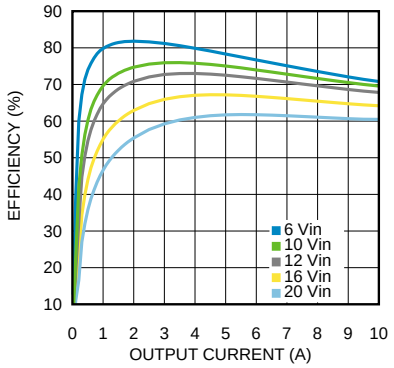


Figure 27. Efficiency 1-V Output at 85°C

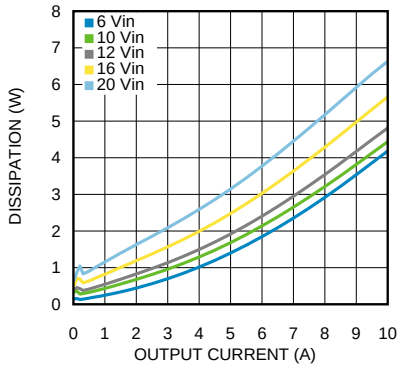
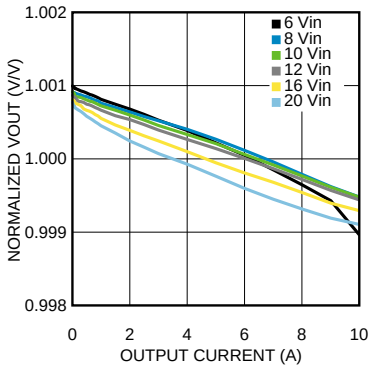
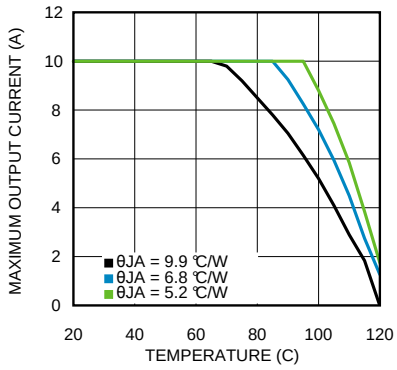


Figure 28. Dissipation 1-V Output at 85°C



V_{OUT} = 3.3 V

Figure 29. Normalized Line and Load Regulation



V_{IN} = 12 V, V_{OUT} = 5 V

Figure 30. Thermal Derating

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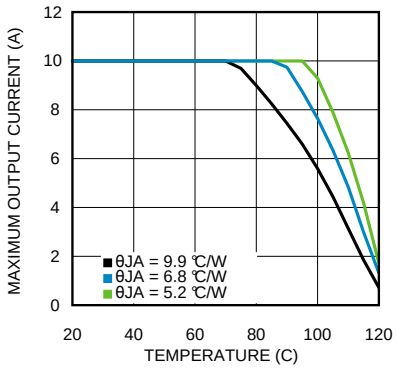
Typical Characteristics (continued)

Unless otherwise specified, the following conditions apply: V_{IN} = 12 V; C_{IN} = three × 10 µF + 47-nF X7R Ceramic; C_{OUT} = two × 330-µF Specialty Polymer + 47-µF Ceramic + 47-nF Ceramic; C_{FF} = 4.7 nF; T_A = 25° C for waveforms. All indicated temperatures are ambient.



V_{IN} = 12 V, V_{OUT} = 3.3 V

Figure 31. Thermal Derating

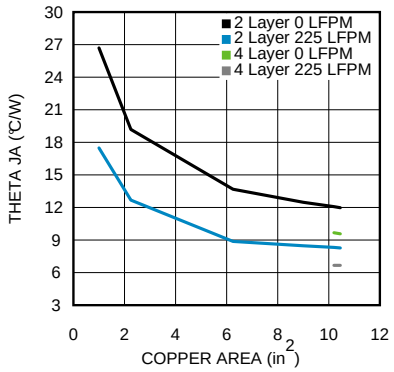
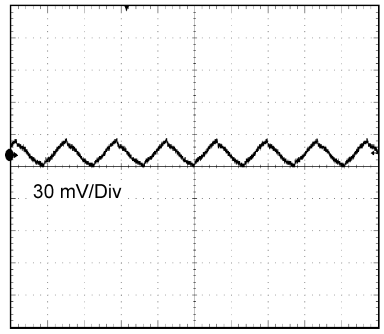
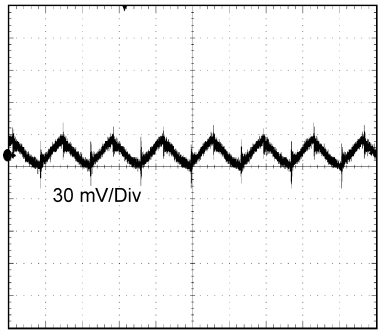


Figure 32. θ_{JA} vs Copper Heat Sinking Area



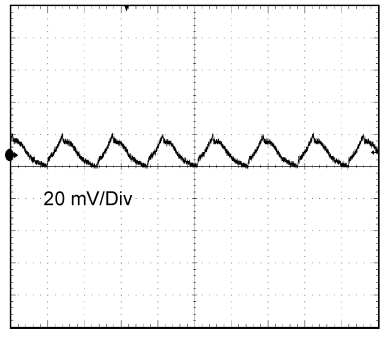
12 V_{IN}, 5 V_{OUT} at Full Load, BW = 20 MHz

Figure 33. Output Ripple



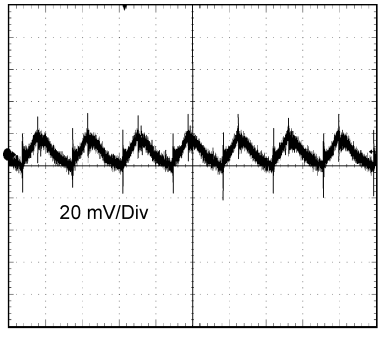
12 V_{IN}, 5 V_{OUT} at Full Load, BW = 250 MHz

Figure 34. Output Ripple



12 V_{IN}, 3.3 V_{OUT} at Full Load, BW = 20 MHz

Figure 35. Output Ripple



12 V_{IN}, 3.3 V_{OUT} at Full Load, BW = 250 MHz

Figure 36. Output Ripple

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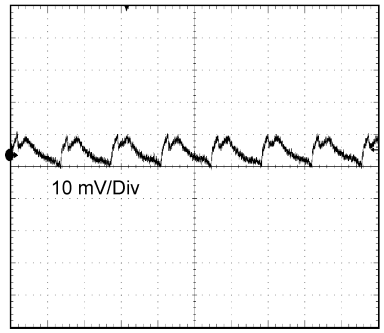
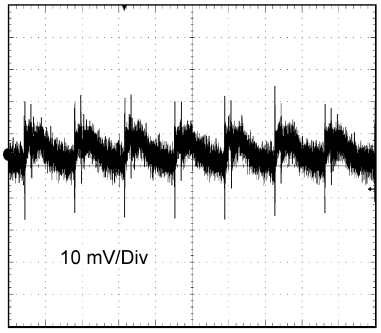
Typical Characteristics (continued)

Unless otherwise specified, the following conditions apply: V_{IN} = 12 V; C_{IN} = three × 10 µF + 47-nF X7R Ceramic; C_{OUT} = two × 330-µF Specialty Polymer + 47-µF Ceramic + 47-nF Ceramic; C_{FF} = 4.7 nF; T_A = 25° C for waveforms. All indicated temperatures are ambient.



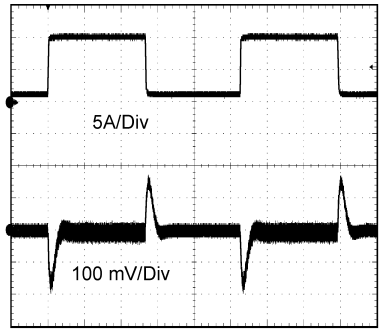
12 V_{IN}, 1.2 V_{OUT} at Full Load, BW = 20 MHz

Figure 37. Output Ripple



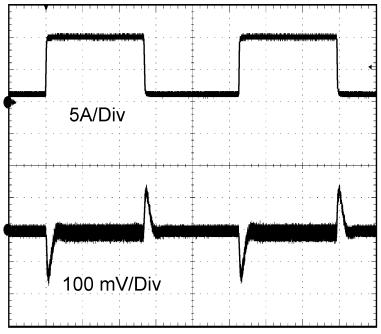
12 V_{IN}, 1.2 V_{OUT} at Full Load, BW = 250 MHz

Figure 38. Output Ripple



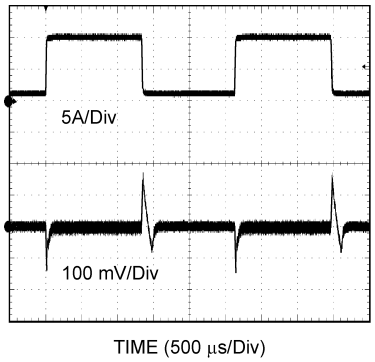
12 V_{IN}, 5 V_{OUT} 1- to 10-A Step

Figure 39. Transcient Response



12 V_{IN}, 3.3 V_{OUT} 1- to 10-A Step

Figure 40. Transcient Response



12 V_{IN}, 1.2 V_{OUT} 1- to 10-A Step

Figure 41. Transcient Response

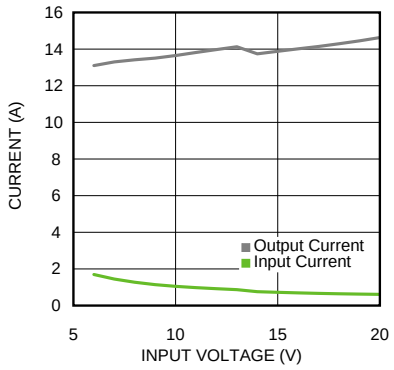


Figure 42. Short Circuit Current vs Input Voltage

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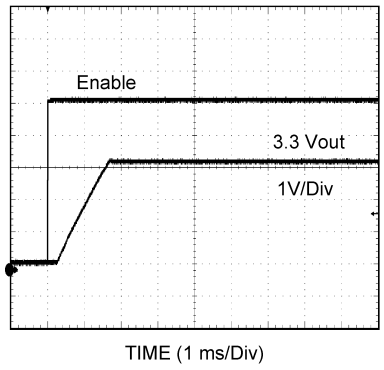
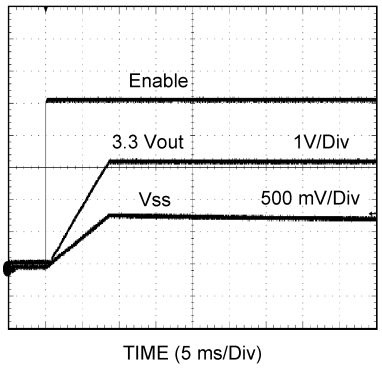
Typical Characteristics (continued)

Unless otherwise specified, the following conditions apply: V_{IN} = 12 V; C_{IN} = three × 10 µF + 47-nF X7R Ceramic; C_{OUT} = two × 330-µF Specialty Polymer + 47-µF Ceramic + 47-nF Ceramic; C_{FF} = 4.7 nF; T_A = 25° C for waveforms. All indicated temperatures are ambient.



No C_{SS}

Figure 43. 3.3 V_{OUT} Soft-Start



C_{SS} = 0.47 µF

Figure 44. 3.3 V_{OUT} Soft-Start

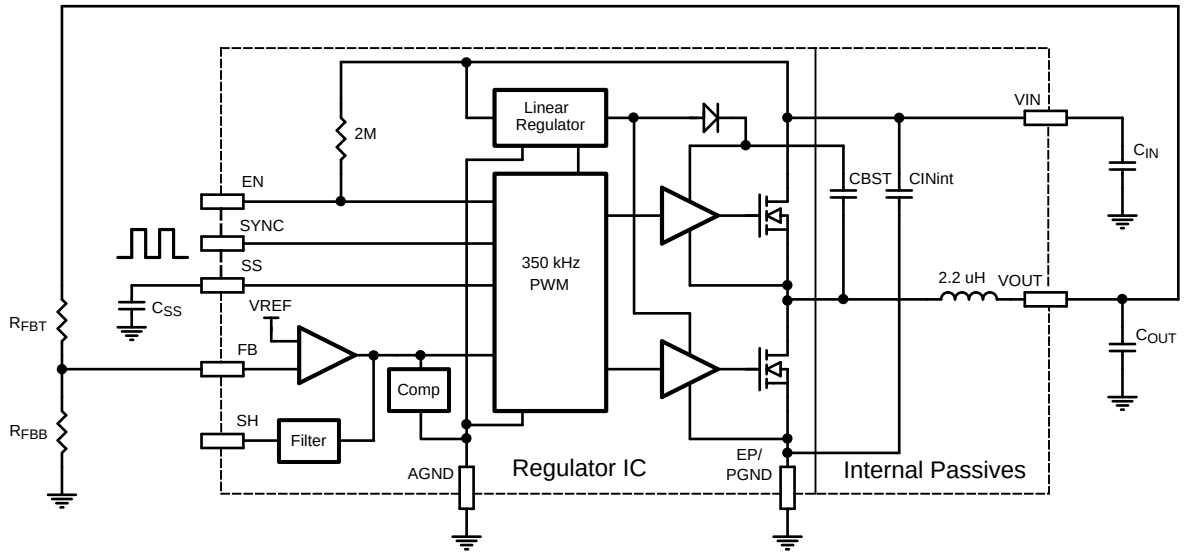
7 Detailed Description

7.1 Overview

The architecture used is an internally compensated emulated peak current mode control, based on a monolithic synchronous SIMPLE SWITCHER core capable of supporting high load currents. The output voltage is maintained through feedback compared with an internal 0.8-V reference. For emulated peak current-mode, the valley current is sampled on the down-slope of the inductor current. This is used as the DC value of current to start the next cycle.

The primary application for emulated peak current-mode is high input voltage to low output voltage operating at a narrow duty cycle. By sampling the inductor current at the end of the switching cycle and adding an external ramp, the minimum on-time can be significantly reduced, without the need for blanking or filtering which is normally required for peak current-mode control.

7.2 Functional Block Diagram



7.3 Feature Description

7.3.1 Synchronization Input

The PWM switching frequency can be synchronized to an external frequency source. The PWM switching will be in phase with the external frequency source. If this feature is not used, connect this input either directly to ground, or connect to ground through a resistor of 1.5 kΩ or less. The allowed synchronization frequency range is 314 kHz to 600 kHz. The typical input threshold is 1.4 V. Ideally, the input clock must overdrive the threshold by a factor of 2, so direct drive from 3.3-V logic via a 1.5-kΩ or less Thevenin source resistance is recommended.

NOTE

Applying a sustained logic 1 corresponds to zero Hz PWM frequency and will cause the module to stop switching.

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Feature Description (continued)

7.3.2 Current Sharing

When a load current higher than 10 A is required by the application, the LMZ22010 can be configured to share the load between multiple devices. To share the load current between the devices, connect the SH pin of all current sharing LMZ22010 modules. One device must be configured as the master by connecting FB normally. All other devices must be configured as slaves by leaving their respective FB pins floating. The modules must be synchronized by a clock signal to avoid beat frequencies in the output voltage caused by small differences in the internal 359-kHz clock. If the modules are not synchronized, the magnitude of the ripple voltage will depend on the phase relationship of the internal clocks. The external synchronizing clocks can be in phase for all modules, or out of phase to reduce the current stress on the input and output capacitors. As an example, two modules can be run 180 degrees out of phase, and three modules can be run 120 degrees out of phase. The VIN, VOUT, PGND, and AGND pins must also be connected with low impedance paths. It is particularly important to pay close attention to the layout of AGND and SH, as offsets in grounding or noise picked up from other devices will be seen as a mismatch in current sharing and could cause noise issues.

Current sharing modules can be configured to share the same set of bulk input and output capacitors, while each having their own local input and output bypass capacitors. A C_{IN_BYP} >= 30 µF is still recommended for each module that is connected in a current sharing configuration. A C_{OUT_BYP} consisting of 47-nF X7R ceramic capacitor in parallel with a 22-µF ceramic capacitor is recommended to locally bypass the output voltage for each module. These capacitors will provide local bypassing of high-frequency switched currents.

In a current sharing system using two or more modules, the slaves have their error amp circuitry disconnected. The master over-rides the error amplifier outputs of the slaves. This signal is then compared to each module's individual current sense circuitry. Due to this, the current sense gain of the entire system increases according to the number of modules slaved to the master. To compensate for this and ensure good stability, the total output capacitance has to be increased. For example, two modules configured to provide 1.2 V_{OUT} and 20 amps have a required total bulk output capacitance of C_{OUT_BULK} = 2 × 450 µF (ESR 25 mΩ). This is a thirty six percent increase in the required output capacitance of a stand alone module. Up to 6 modules can be connected in parallel for loads up to 60A. For more information on current sharing refer to AN-2093 (SNVA460).

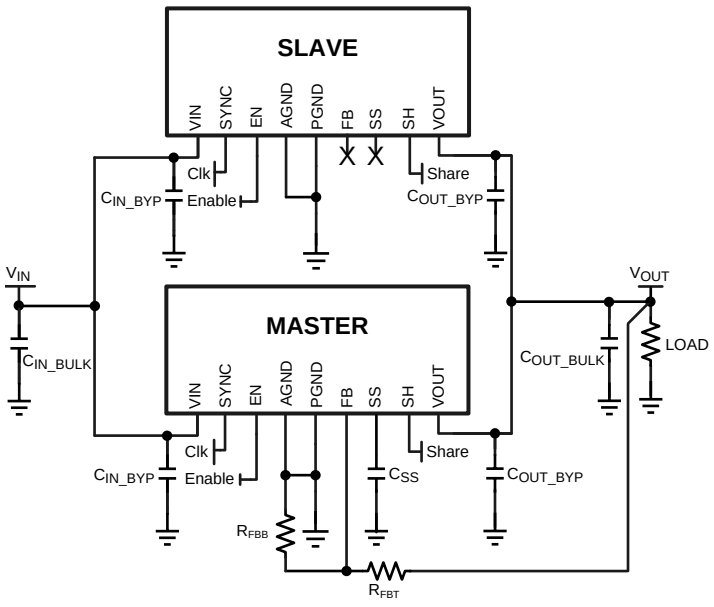

Figure 45. Current-Sharing Example Schematic

Feature Description (continued)

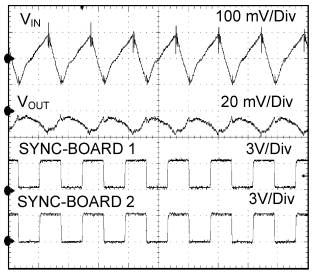

Figure 46. Output Voltage Ripple of Two Modules With Synchronization Clocks in Phase

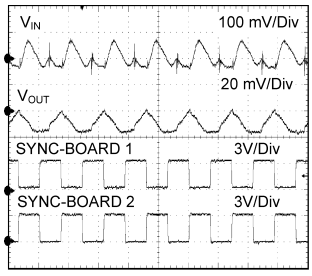

Figure 47. Output Voltage Ripple of Two Modules With Synchronization Clocks 180 Degrees Out of Phase

7.3.3 Output Overvoltage Protection

If the voltage at FB is greater than a 0.86V internal reference, the output of the error amplifier is pulled toward ground, causing V_{OUT} to fall.

7.3.4 Current Limit

The LMZ22010 is protected by both low-side (LS) and high-side (HS) current limit circuitry. The LS current limit detection is carried out during the OFF-time by monitoring the current through the LS synchronous MOSFET. Referring to the *Functional Block Diagram*, when the top MOSFET is turned off, the inductor current flows through the load, the PGND pin and the internal synchronous MOSFET. If this current exceeds 13 A (typical) the current limit comparator disables the start of the next switching period. Switching cycles are prohibited until current drops below the limit.

NOTE

DC current limit is dependent on duty cycle as illustrated in the graph in the *Typical Characteristics* section.

The HS current limit monitors the current of top side MOSFET. Once HS current limit is detected (16 A typical) , the HS MOSFET is shutoff immediately, until the next cycle. Exceeding HS current limit causes V_{OUT} to fall. Typical behavior of exceeding LS current limit is that f_{SW} drops to 1/2 of the operating frequency.

7.3.5 Thermal Protection

The junction temperature of the LMZ22010 must not be allowed to exceed its maximum ratings. Thermal protection is implemented by an internal Thermal Shutdown circuit which activates at 165°C (typical) causing the device to enter a low power standby state. In this state the main MOSFET remains off causing V_{OUT} to fall, and additionally the C_{SS} capacitor is discharged to ground. Thermal protection helps prevent catastrophic failures for accidental device overheating. When the junction temperature falls back below 150°C (typical hysteresis = 15°C) the SS pin is released, V_{OUT} rises smoothly, and normal operation resumes.

Applications requiring maximum output current especially those at high input voltage may require additional derating at elevated temperatures.

7.3.6 Prebiased Start-Up

The LMZ22010 will properly start up into a prebiased output. This startup situation is common in multiple rail logic applications where current paths may exist between different power rails during the startup sequence. The following scope capture shows proper behavior in this mode. Trace one is Enable going high. Trace two is 1.8-V prebias rising to 3.3 V. Trace three is the SS voltage with a C_{SS}= 0.47 µF. Rise-time determined by C_{SS}.

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Feature Description (continued)

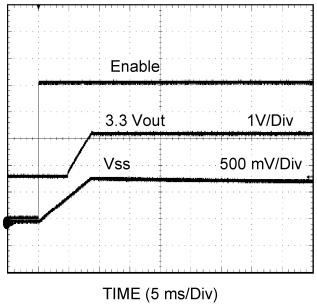


Figure 48. Prebiased Start-Up

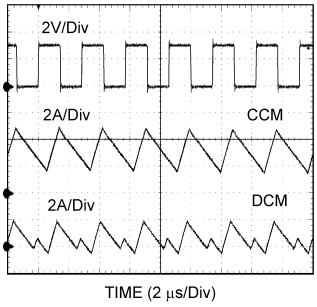
7.4 Device Functional Modes

7.4.1 Discontinuous Conduction and Continuous Conduction Modes

At light load the regulator will operate in discontinuous conduction mode (DCM). With load currents above the critical conduction point, it will operate in continuous conduction mode (CCM). When operating in DCM, inductor current is maintained to an average value equaling I_{OUT}. In DCM the low-side switch will turn off when the inductor current falls to zero, this causes the inductor current to resonate. Although it is in DCM, the current is allowed to go slightly negative to charge the bootstrap capacitor.

In CCM, current flows through the inductor through the entire switching cycle and never falls to zero during the off-time.

Figure 49 is a comparison pair of waveforms showing both the CCM (upper) and DCM operating modes.



V_{IN} = 12 V, V_O = 3.3 V, I_O = 3 A / 0.3 A

Figure 49. CCM and DCM Operating Modes

8 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

8.1 Application Information

The LMZ22010 is a step-down DC-to-DC power module. It is typically used to convert a higher DC voltage to a lower DC voltage with a maximum output current of 10 A. The following design procedure can be used to select components for the LMZ22010. Alternately, the WEBENCH software may be used to generate complete designs.

When generating a design, the WEBENCH software uses iterative design procedure and accesses comprehensive databases of components. Please go to www.ti.com for more details.

8.2 Typical Application

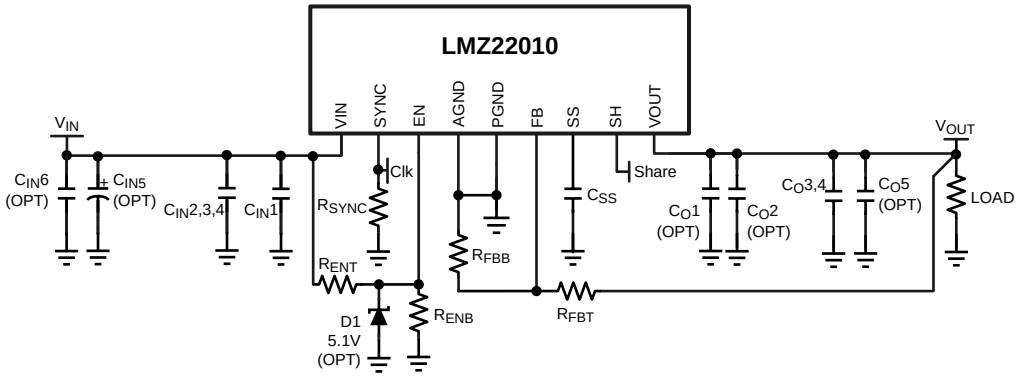


Figure 50. Typical Application Schematic Diagram

8.2.1 Design Requirements

For this example the following application parameters exist.

- V_{IN} Range = Up to 20 V
- V_{OUT} = 0.8 V to 6 V
- I_{OUT} = 10 A

8.2.2 Detailed Design Procedure

8.2.2.1 Design Steps

The LMZ22010 is fully supported by WEBENCH which offers: component selection, electrical and thermal simulations. Additionally, there are both evaluation and demonstration boards that may be used as a starting point for design. The following list of steps can be used to manually design the LMZ22010 application.

All references to values refer to the typical applications schematic Figure 50.

1. Select minimum operating V_{IN} with enable divider resistors
2. Program V_{OUT} with FB resistor divider selection
3. Select C_{OUT}
4. Select C_{IN}
5. Determine module power dissipation
6. Layout PCB for required thermal performance

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Typical Application (continued)

8.2.2.2 Enable Divider, R_{ENT}, R_{ENB} and R_{ENH} Selection

Internal to the module is a 2-MΩ pullup resistor connected from V_{IN} to Enable. For applications not requiring precision undervoltage lockout (UVLO), the Enable input may be left open circuit and the internal resistor will always enable the module. In such case, the internal UVLO occurs typically at 4.3 V (V_{IN} rising).

In applications with separate supervisory circuits Enable can be directly interfaced to a logic source. In the case of sequencing supplies, the divider is connected to a rail that becomes active earlier in the power-up cycle than the LMZ22010 output rail.

Enable provides a precise 1.274-V threshold to allow direct logic drive or connection to a voltage divider from a higher enable voltage such as V_{IN}. Additionally there is 13 µA (typical) of switched offset current allowing programmable hysteresis. See Figure 51.

The function of the enable divider is to allow the designer to choose an input voltage below which the circuit will be disabled. This implements the feature of a programmable UVLO. The two resistors must be chosen based on the following ratio:

$$R_{ENT} / R_{ENB} = (V_{IN\ UVLO} / 1.274\ V) - 1 \quad (1)$$

The LMZ22010 typical application shows 12.7 kΩ for R_{ENB} and 42.2kΩ for R_{ENT} resulting in a rising UVLO of 5.51 V. This divider presents 4.62 V to the EN input when V_{IN} is raised to 20 V. This upper voltage must always be checked, making sure that it never exceeds the Abs Max 5.5-V limit for Enable. A 5.1-V Zener clamp can be applied in cases where the upper voltage would exceed the EN input's range of operation. The Zener clamp is not required if the target application prohibits the maximum Enable input voltage from being exceeded.

Additional enable voltage hysteresis can be added with the inclusion of R_{ENH}. It is possible to select values for R_{ENT} and R_{ENB} such that R_{ENH} is a value of zero allowing it to be omitted from the design.

Rising threshold can be calculated as follows:

$$V_{EN}(rising) = 1.274\ (\ 1 + (R_{ENT} || \ 2\ meg) / R_{ENB}) \quad (2)$$

Whereas the falling threshold level can be calculated using:

$$V_{EN}(falling) = V_{EN}(rising) - 13\ \mu A\ (\ R_{ENT} || \ 2\ meg\ ||\ R_{ENTB} + R_{ENH}\ ) \quad (3)$$

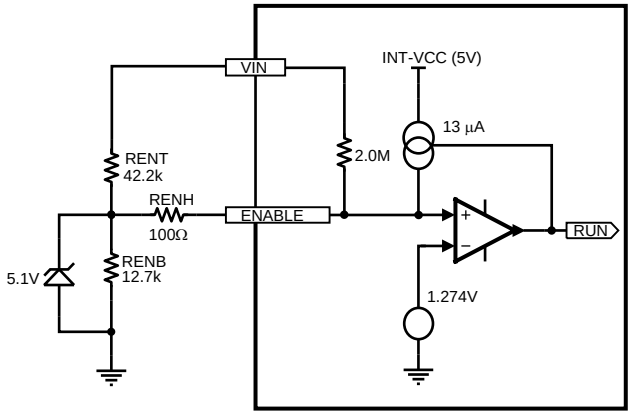

Figure 51. Enable Input Detail

8.2.2.3 Output Voltage Selection

Output voltage is determined by a divider of two resistors connected between V_{OUT} and AGND. The midpoint of the divider is connected to the FB input.

The regulated output voltage determined by the external divider resistors R_{FBT} and R_{FBB} is:

$$V_{OUT} = 0.795\ V \times (1 + R_{FBT} / R_{FBB}) \quad (4)$$

Rearranging terms; the ratio of the feedback resistors for a desired output voltage is:

$$R_{FBT} / R_{FBB} = (V_{OUT} / 0.795\ V) - 1 \quad (5)$$

These resistors must generally be chosen from values in the range of 1.0 kΩ to 10.0 kΩ.

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Typical Application (continued)

For V_{OUT} = 0.8 V the FB pin can be connected to the output directly and R_{FBB} can be set to 8.06 kΩ to provide minimum output load.

Table 1 list the values for R_{FBT} , and R_{FBB}.

Table 1. Typical Application Bill of Materials

REF DES	DESCRIPTION	CASE SIZE	MANUFACTURER	MANUFACTURER P/N
U1	SIMPLE SWITCHER	PFM-11	Texas Instruments	LMZ22010TZ
C_{IN}1,6 (OPT)	0.047 µF, 50 V, X7R	1206	Yageo America	CC1206KRX7R9BB473
C_{IN}2,3,4	10 µF, 50 V, X7R	1210	Taiyo Yuden	UMK325BJ106MM-T
C_{IN}5 (OPT)	CAP, AL, 150 µF, 50 V	Radial G	Panasonic	EEE-FK1H151P
C_O1,5 (OPT)	0.047 µF, 50 V, X7R	1206	Yageo America	CC1206KRX7R9BB473
C_O2 (OPT)	47 µF, 10 V, X7R	1210	Murata	GRM32ER61A476KE20L
C_O3,4	330 µF, 6.3 V, 0.015 Ω	CAPSMT_6_UE	Kemet	T520D337M006ATE015
R_{FBT}	3.32 kΩ	0805	Panasonic	ERJ-6ENF3321V
R_{FBB}	1.07 kΩ	0805	Panasonic	ERJ-6ENF1071V
R_{SYNC}	1.50 kΩ	0805	Vishay Dale	CRCW08051K50FKEA
R_{ENT}	42.2 kΩ	0805	Panasonic	ERJ-6ENF4222V
R_{ENB}	12.7 kΩ	0805	Panasonic	ERJ-6ENF1272V
C_{SS}	0.47 µF, ±10%, X7R, 16 V	0805	AVX	0805YC474KAT2A
D1 (OPT)	5.1 V, 0.5 W	SOD-123	Diodes Inc.	MMSZ5231BS-7-F

8.2.2.4 Soft-Start Capacitor Selection

Programmable soft-start permits the regulator to slowly ramp to its steady-state operating point after being enabled, thereby reducing current inrush from the input supply and slowing the output voltage rise-time.

Upon turnon, after all UVLO conditions have been passed, an internal 1.6-ms circuit slowly ramps the SS input to implement internal soft start. If 1.6 ms is an adequate turnon time then the Css capacitor can be left unpopulated. Longer soft-start periods are achieved by adding an external capacitor to this input.

Soft-start duration is given by the formula:

$$t_{SS} = V_{REF} \times C_{SS} / Iss = 0.795\ V \times C_{SS} / 50\ \mu A \quad (6)$$

This equation can be rearranged as follows:

$$C_{SS} = t_{SS} \times 50\ \mu A / 0.795\ V \quad (7)$$

Using a 0.22-µF capacitor results in 3.5-ms typical soft-start duration; and 0.47 µF results in 7.5 ms typical. 0.47 µF is a recommended initial value.

As the soft-start input exceeds 0.795 V the output of the power stage will be in regulation and the 50-µA current is deactivated. The following conditions will reset the soft-start capacitor by discharging the SS input to ground with an internal current sink.

- The Enable input being *pulled low*
- A thermal shutdown condition
- V_{IN} falling below 4.3 V (typical) and triggering the V_{CC} UVLO

8.2.2.5 Tracking Supply Divider Option

The tracking function allows the module to be connected as a slave supply to a primary voltage rail (often the 3.3-V system rail) where the slave module output voltage is lower than that of the master. Proper configuration allows the slave rail to power up coincident with the master rail such that the voltage difference between the rails during ramp-up is small (that is, < 0.15 V typical). The values for the tracking resistive divider must be selected such that the effect of the internal 50-µA current source is minimized. In most cases the ratio of the tracking

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divider resistors is the same as the ratio of the output voltage setting divider. Proper operation in tracking mode dictates the soft-start time of the slave rail be shorter than the master rail; a condition that is easy to satisfy because the C_{SS} cap is replaced by R_{TKB}. The tracking function is only supported for the power up interval of the master supply; once the SS/TRK rises past 0.795 V the input is no longer enabled and the 50-µA internal current source is switched off.

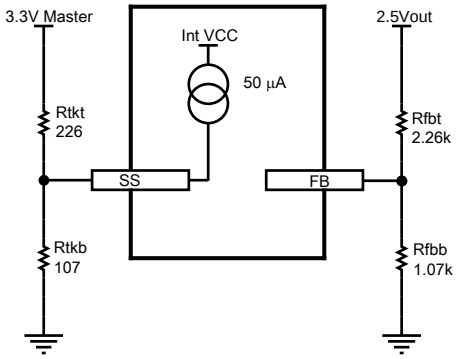

Figure 52. Tracking Option Input Detail

8.2.2.6 C_{OUT} Selection

None of the required C_{OUT} output capacitance is contained within the module. A minimum value ranging from 330 µF for 6-V_{OUT} to 660 µF for 1.2-V_{OUT} applications is required based on the values of internal compensation in the error amplifier. These minimum values can be decreased if the effective capacitor ESR is higher than 15 mΩ.

A Low ESR (15 mΩ) tantalum, organic semiconductor or specialty polymer capacitor types in parallel with a 47-nF X7R ceramic capacitor for high-frequency noise reduction is recommended for obtaining lowest ripple. The output capacitor C_{OUT} may consist of several capacitors in parallel placed in close proximity to the module. The output voltage ripple of the module depends on the equivalent series resistance (ESR) of the capacitor bank, and can be calculated by multiplying the ripple current of the module by the effective impedance of your chosen output capacitors. Electrolytic capacitors will have large ESR and lead to larger output ripple than ceramic or polymer types. For this reason a combination of ceramic and polymer capacitors is recommended for low output ripple performance.

The output capacitor assembly must also meet the worst case ripple current rating of Δi_L, as calculated in Equation 8. Loop response verification is also valuable to confirm closed loop behavior.

For applications with dynamic load steps; the following equation provides a good first pass approximation of C_{OUT} for load transient requirements.

$$C_{OUT} \geq \frac{I_{step}}{(\Delta V_{OUT} - I_{STEP} \times ESR) \times (\frac{f_{SW}}{V_{OUT}})} \tag{8}$$

For 12 V_{IN}, 3.3 V_{OUT}, a transient voltage of 5% of V_{OUT} = 0.165 V (ΔV_{OUT}), a 9A load step (I_{STEP}), an output capacitor effective ESR of 3 mΩ, and a switching frequency of 350kHz (f_{SW}):

$$C_{OUT} \geq \frac{9A}{(0.165V - 9A \times 0.003) \times (\frac{350e3}{3.3V})}$$

$$\geq 615\ \mu F \tag{9}$$

NOTE

The stability requirement for minimum output capacitance must always be met.

One recommended output capacitor combination is two 330-µF, 15-mΩ ESR tantalum polymer capacitors connected in parallel with a 47-µF 6.3-V X5R ceramic. This combination provides excellent performance that may exceed the requirements of certain applications. Additionally some small 47-nF ceramic capacitors can be used for high-frequency EMI suppression.

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8.2.2.7 C_{IN} Selection

The LMZ22010 module contains two internal ceramic input capacitors. Additional input capacitance is required external to the module to handle the input ripple current of the application. The input capacitor can be several capacitors in parallel. This input capacitance must be located in very close proximity to the module. Input capacitor selection is generally directed to satisfy the input ripple current requirements rather than by capacitance value. Input ripple current rating is dictated by the equation:

$$I_{CIN\text{-}RMS} = I_{OUT} \times \sqrt{D(1\text{-}D)}$$

where

- $D \cong V_{OUT} / V_{IN}$ (10)

As a point of reference, the worst case ripple current will occur when the module is presented with full load current and when $V_{IN} = 2 \times V_{OUT}$.

Recommended minimum input capacitance is 30-µF X7R (or X5R) ceramic with a voltage rating at least 25% higher than the maximum applied input voltage for the application. TI also recommends to pay attention to the voltage and temperature derating of the capacitor selected.

NOTE

Ripple current rating of ceramic capacitors may be missing from the capacitor data sheet and you may have to contact the capacitor manufacturer for this parameter.

If the system design requires a certain minimum value of peak-to-peak input ripple voltage (ΔV_{IN}) to be maintained then the following equation may be used.

$$C_{IN} \geq \frac{I_{OUT} \times D \times (1 - D)}{f_{SW} \times \Delta V_{IN}} \quad (11)$$

If ΔV_{IN} is 200 mV or 1.66% of V_{IN} for a 12-V input to 3.3-V output application and f_{SW} = 350 kHz then:

$$C_{IN} \geq \frac{10A \times \left(\frac{3.3V}{12V}\right) \times \left(1 - \frac{3.3V}{12V}\right)}{350\ kHz \times 200\ mV} \geq 28\ \mu F \quad (12)$$

Additional bulk capacitance with higher ESR may be required to damp any resonant effects of the input capacitance and parasitic inductance of the incoming supply lines. The LMZ22010 typical applications schematic and evaluation board include a 150-µF 50-V aluminum capacitor for this function. There are many situations where this capacitor is not necessary.

8.2.2.8 Discontinuous Conduction and Continuous Conduction Modes Selection

The approximate formula for determining the DCM/CCM boundary is as follows:

$$I_{DCB} = \frac{(V_{IN} - V_{OUT}) \times D}{2 \times L \times f_{SW}} \quad (13)$$

The inductor internal to the module is 2.2 µH. This value was chosen as a good balance between low and high input voltage applications. The main parameter affected by the inductor is the amplitude of the inductor ripple current (Δi_L). Δi_L can be calculated with:

$$\Delta i_L = \frac{(V_{IN} - V_{OUT}) \times D}{L \times f_{SW}}$$

where

- V_{IN} is the maximum input voltage
- and f_{SW} is typically 359 kHz. (14)

If the output current I_{OUT} is determined by assuming that $I_{OUT} = I_L$, the higher and lower peak of Δi_L can be determined.

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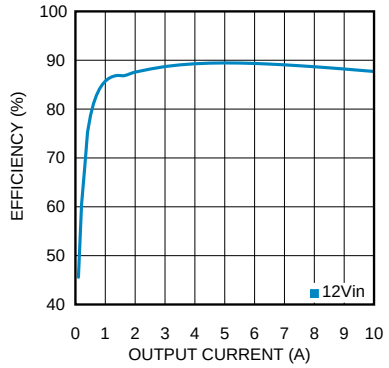
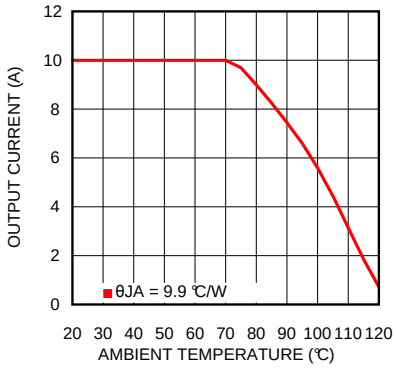
8.2.3 Application Curves



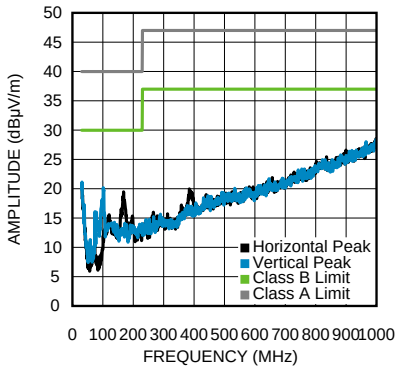
V_{IN} = 12 V, V_{OUT} = 3.3 V

Figure 53. Efficiency



V_{IN} = 12 V, V_{OUT} = 3.3 V

Figure 54. Thermal Derating Curve



V_{IN} = 12 V, V_{OUT} = 5 V,
I_{OUT} = 10 A

Figure 55. Radiated EMI (EN 55022)

9 Power Supply Recommendations

The LMZ22010 device is designed to operate from an input voltage supply range between 6 V and 20 V. This input supply must be well regulated and able to withstand maximum input current and maintain a stable voltage. The resistance of the input supply rail must be low enough that an input current transient does not cause a high enough drop at the LMZ22010 supply voltage that can cause a false UVLO fault triggering and system reset. If the input supply is more than a few inches from the LMZ22010, additional bulk capacitance may be required in addition to the ceramic bypass capacitors. The amount of bulk capacitance is not critical, but a 47-µF or 100-µF electrolytic capacitor is a typical choice.

10 Layout

10.1 Layout Guidelines

PCB layout is an important part of DC-DC converter design. Poor board layout can disrupt the performance of a DC-DC converter and surrounding circuitry by contributing to EMI, ground bounce and resistive voltage drop in the traces. These can send erroneous signals to the DC-DC converter resulting in poor regulation or instability. Good layout can be implemented by following a few simple design rules. A good layout example is shown in Figure 59.

1. **Minimize area of switched current loops.**

   From an EMI reduction standpoint, it is imperative to minimize the high di/dt paths during PCB layout as shown in the figure above. The high current loops that do not overlap have high di/dt content that will cause observable high frequency noise on the output pin if the input capacitor (C_{IN}) is placed at a distance away from the LMZ22010. Therefore place C_{IN} as close as possible to the LMZ22010 VIN and PGND exposed pad. This will minimize the high di/dt area and reduce radiated EMI. Additionally, grounding for both the input and output capacitor must consist of a localized top side plane that connects to the PGND exposed pad (EP).

2. **Have a single point ground.**

   The ground connections for the feedback, soft-start, and enable components must be routed to the AGND pin of the device. This prevents any switched or load currents from flowing in the analog ground traces. If not properly handled, poor grounding can result in degraded load regulation or erratic output voltage ripple behavior. Additionally provide a single point ground connection from pin 4 (AGND) to EP/PGND.

3. **Minimize trace length to the FB pin.**

   Both feedback resistors, R_{FBT} and R_{FBB} must be located close to the FB pin. Since the FB node is high impedance, maintain the copper area as small as possible. The traces from R_{FBT}, R_{FBB} must be routed away from the body of the LMZ22010 to minimize possible noise pickup.

4. **Make input and output bus connections as wide as possible.**

   This reduces any voltage drops on the input or output of the converter and maximizes efficiency. To optimize voltage accuracy at the load, ensure that a separate feedback voltage sense trace is made to the load. Doing so will correct for voltage drops and provide optimum output accuracy.

5. **Provide adequate device heat-sinking.**

   Use an array of heat-sinking vias to connect the exposed pad to the ground plane on the bottom PCB layer. If the PCB has multiple copper layers, these thermal vias can also be connected to inner layer heat-spreading ground planes. For best results use a 10 × 10 via array or larger with a minimum via diameter of 8 mil thermal vias spaced 46.8 mil (1.5 mm). Ensure enough copper area is used for heat-sinking to keep the junction temperature below 125°C.

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10.2 Layout Examples

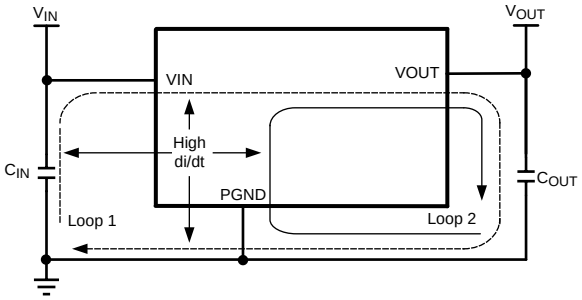

Figure 56. Critical Current Loops to Minimize

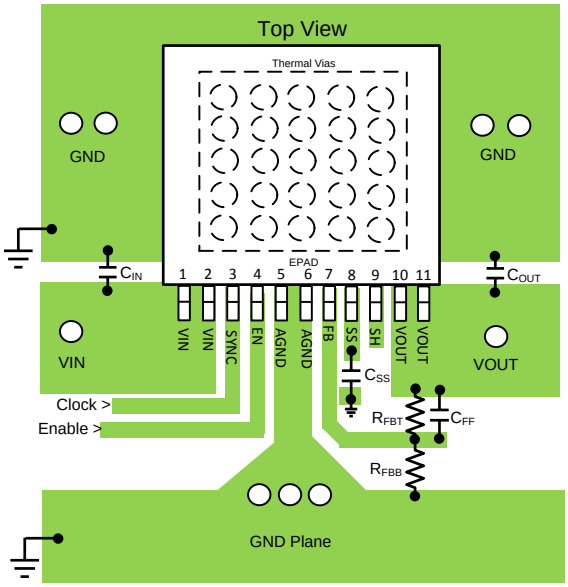

Figure 57. PCB Layout Guide

Layout Examples (continued)

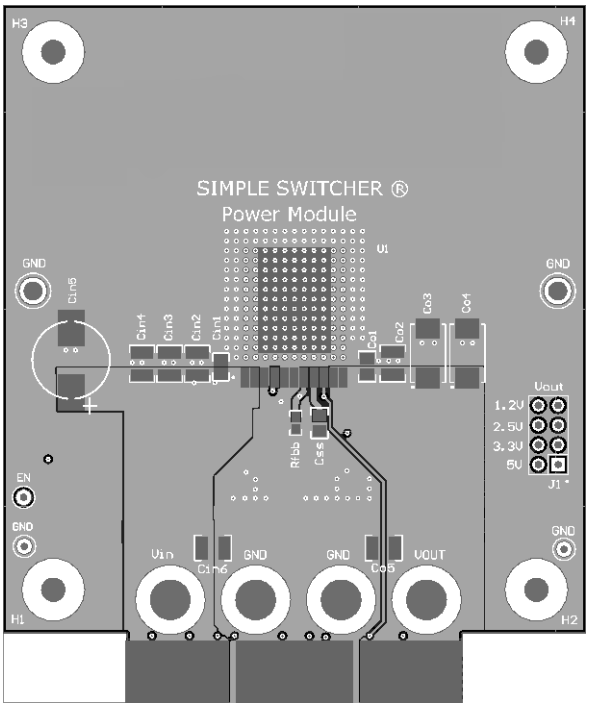

Figure 58. Top View of Evaluation PCB

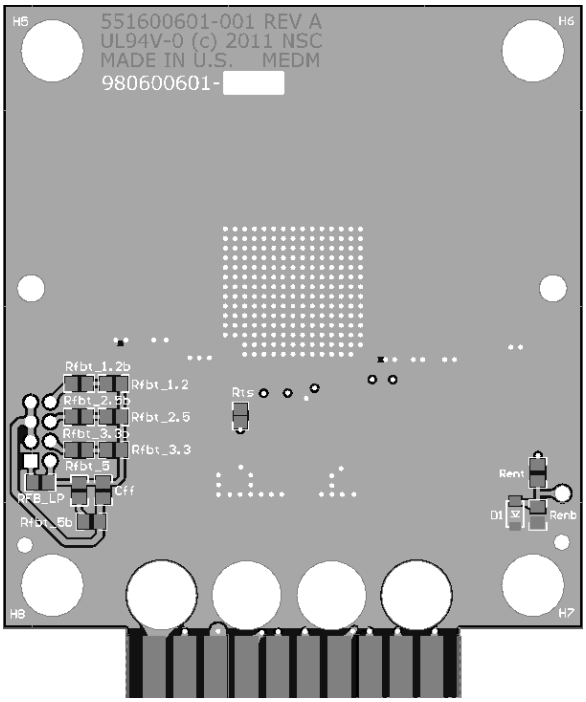

Figure 59. Bottom View of Evaluation PCB

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10.3 Power Dissipation and Thermal Considerations

When calculating module dissipation use the maximum input voltage and the average output current for the application. Many common operating conditions are provided in the characteristic curves such that less common applications can be derived through interpolation. In all designs, the junction temperature must be kept below the rated maximum of 125°C.

For the design case of V_{IN} = 12 V, V_{OUT} = 3.3 V, I_{OUT} = 10 A, and $T_{A\text{-}MAX}$ = 50°C, the module must see a thermal resistance from case to ambient (θ_{CA}) of less than:

$$\theta_{CA} < \frac{T_{J\text{-}MAX} - T_{A\text{-}MAX}}{P_{IC_LOSS}} - \theta_{JC} \tag{15}$$

Given the typical thermal resistance from junction to case (θ_{JC}) to be 1.0°C/W. Use the 85°C power dissipation curves in the *Typical Characteristics* section to estimate the $P_{IC\text{-}LOSS}$ for the application being designed. In this application it is 5.3W.

$$\theta_{CA} < \frac{125℃ - 50℃}{3.9\ W} - 1.0\frac{℃}{W} < 18.23\frac{℃}{W} \tag{16}$$

To reach θ_{CA} = 13.15, the PCB is required to dissipate heat effectively. With no airflow and no external heat-sink, a good estimate of the required board area covered by 2-oz. copper on both the top and bottom metal layers is:

$$\text{Board Area_cm}^2 \geq \frac{500}{\theta_{CA}} \cdot \frac{℃ \times \text{cm}^2}{W} \tag{17}$$

As a result, approximately 38.02 square cm of 2-oz. copper on top and bottom layers is the minimum required area for the example PCB design. This is 6.16 × 6.16 cm (2.42 x 2.42 in) square. The PCB copper heat sink must be connected to the exposed pad. For best performance, use approximately 100, 8 mil thermal vias spaced 59 mil (1.5 mm) apart connect the top copper to the bottom copper.

Another way to estimate the temperature rise of a design is using θ_{JA}. An estimate of θ_{JA} for varying heat sinking copper areas and airflows can be found in the typical applications curves. If our design required the same operating conditions as before but had 225 LFPM of airflow. We locate the required θ_{JA} of

$$\theta_{JA} < \frac{T_{J\text{-}MAX} - T_{A\text{-}MAX}}{P_{IC_LOSS}}$$

$$\theta_{JA} < \frac{(125 - 50)\ ℃}{3.9\ W} < 19.23\frac{℃}{W} \tag{18}$$

On the θ_{JA} vs copper heatsinking curve, the copper area required for this application is now only 2 square inches. The airflow reduced the required heat sinking area by a factor of three.

To reduce the heat sinking copper area further, this package is compatable with D3-PAK surface mount heat sinks.

For an example of a high thermal performance PCB layout for SIMPLE SWITCHER© power modules, refer to AN-2093 SNVA460, AN-2084 SNVA456, AN-2125 SNVA473, AN-2020 SNVA419 and AN-2026 SNVA424.

10.4 Power Module SMT Guidelines

The recommendations below are for a standard module surface mount assembly

- Land Pattern — Follow the PCB land pattern with either soldermask defined or non-soldermask defined pads
- Stencil Aperture
  - For the exposed die attach pad (DAP), adjust the stencil for approximately 80% coverage of the PCB land pattern
  - For all other I/O pads use a 1:1 ratio between the aperture and the land pattern recommendation
- Solder Paste — Use a standard SAC Alloy such as SAC 305, type 3 or higher
- Stencil Thickness — 0.125 to 0.15mm
- Reflow — Refer to solder paste supplier recommendation and optimized per board size and density
- Refer to *Design Summary LMZ1xxx and LMZ2xxx Power Modules Family* (SNAA214) for reflow information

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Power Module SMT Guidelines (continued)

- Maximum number of reflows allowed is one

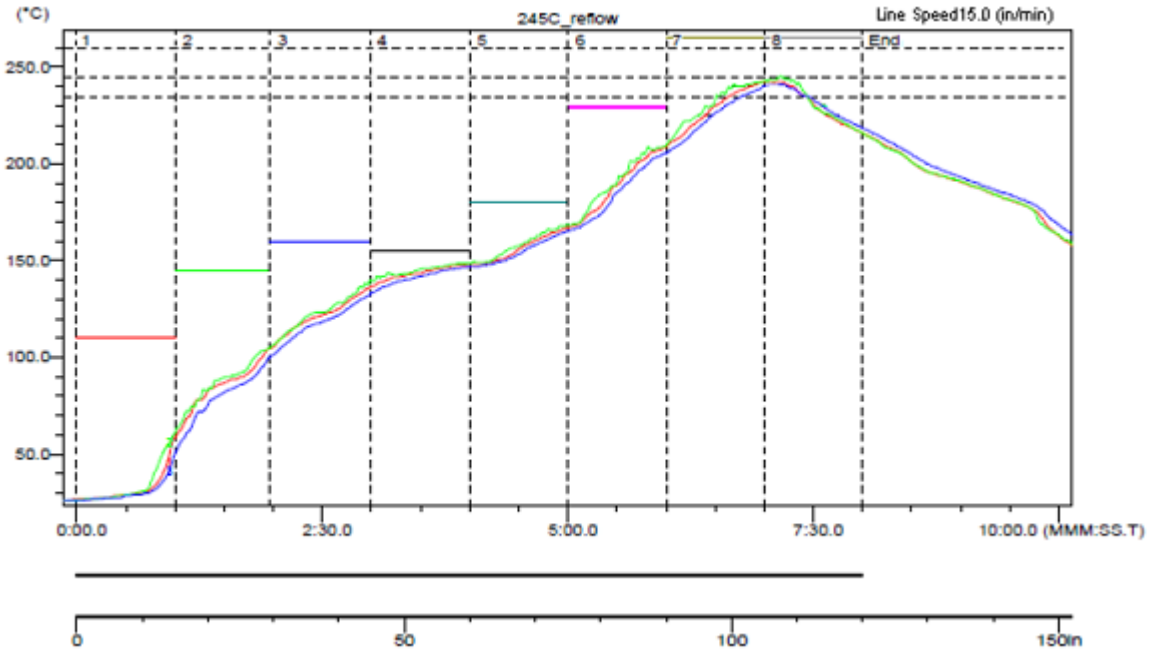

Figure 60. Sample Reflow Profile

Table 2. Sample Reflow Profile Table

PROBE	MAX TEMP (°C)	REACHED MAX TEMP	TIME ABOVE 235°C	REACHED 235°C	TIME ABOVE 245°C	REACHED 245°C	TIME ABOVE 260°C	REACHED 260°C
1	242.5	6.58	0.49	6.39	0.00	–	0.00	–
2	242.5	7.10	0.55	6.31	0.00	7.10	0.00	–
3	241.0	7.09	0.42	6.44	0.00	–	0.00	–

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11 Device and Documentation Support

11.1 Device Support

11.1.1 Third-Party Products Disclaimer

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11.1.2 Development Support

For developmental support, see the following:

WEBENCH Tool, http://www.ti.com/webench

11.2 Documentation Support

11.2.1 Related Documentation

For related documentation, see the following:

- AN-2027 *Inverting Application for the LMZ14203 SIMPLE SWITCHER Power Module*, (SNVA425)
- *Absolute Maximum Ratings for Soldering*, (SNOA549)
- AN-2024 *LMZ1420x / LMZ1200x Evaluation Board* (SNVA422)
- AN-2085 *LMZ23605/03, LMZ22005/03 Evaluation Board* (SNVA457)
- AN-2054 *Evaluation Board for LM10000 - PowerWise AVS System Controller* (SNVA437)
- AN-2020 *Thermal Design By Insight, Not Hindsight* (SNVA419)
- AN-2093 *LMZ23610/8/6 and LMZ22010/8/6 Current Sharing Evaluation Board* (SNVA460)
- AN-2026 *Effect of PCB Design on Thermal Performance of SIMPLE SWITCHER Power Modules* (SNVA424)
- *Design Summary LMZ1xxx and LMZ2xxx Power Modules Family* (SNAA214)

11.3 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

TI E2E™ Online Community ***TI's Engineer-to-Engineer (E2E) Community.*** Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support ***TI's Design Support*** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

11.4 Trademarks

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11.5 Electrostatic Discharge Caution



These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

11.6 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

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12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

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PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
LMZ22010TZ/NOPB	ACTIVE	PFM	NDY	11	32	Green (RoHS & no Sb/Br)	CU SN	Level-3-245C-168 HR	-40 to 85	LMZ22010	Samples
LMZ22010TZE/NOPB	ACTIVE	PFM	NDY	11	250	Green (RoHS & no Sb/Br)	CU SN	Level-3-245C-168 HR	-40 to 85	LMZ22010	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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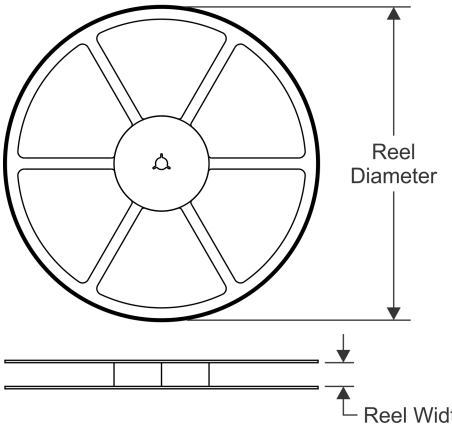
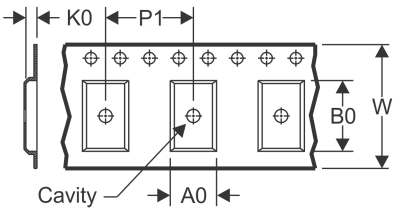
TAPE AND REEL INFORMATION

REEL DIMENSIONS

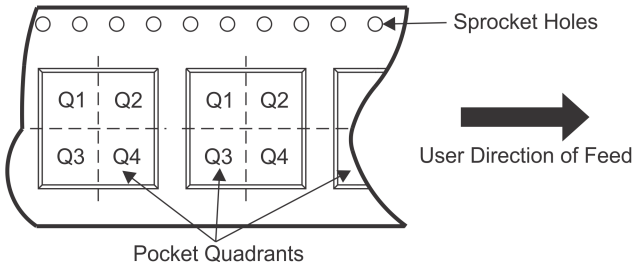


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

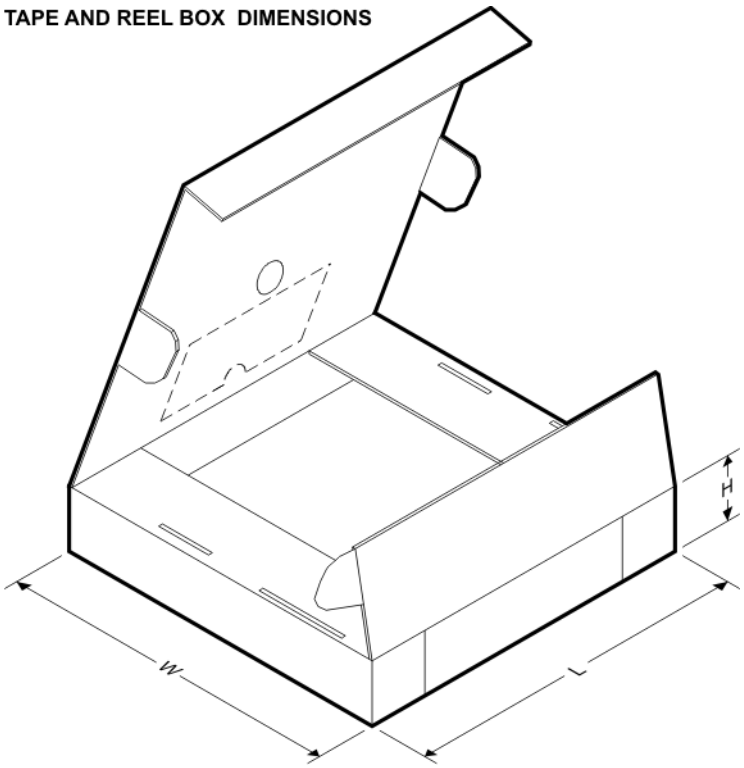
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
LMZ22010TZE/NOPB	PFM	NDY	11	250	330.0	32.4	15.45	18.34	6.2	20.0	32.0	Q2

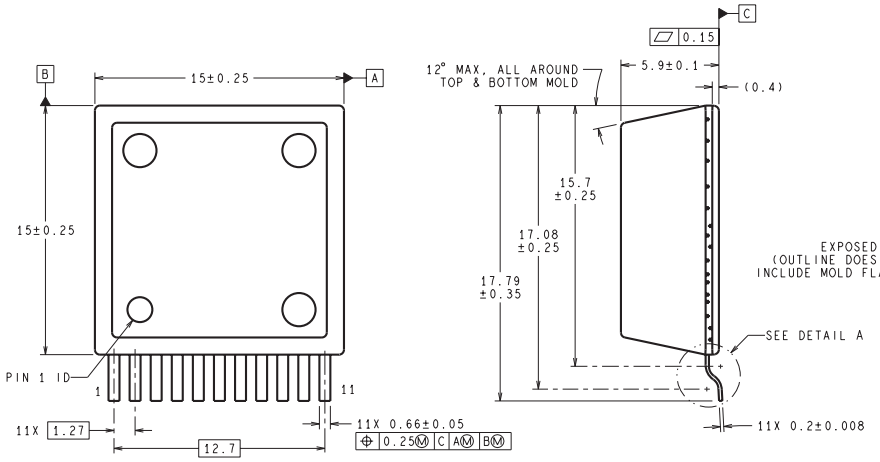
TAPE AND REEL BOX DIMENSIONS



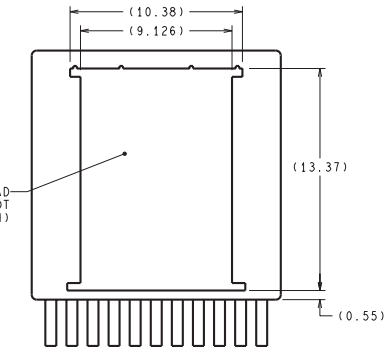
*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
LMZ22010TZE/NOPB	PFM	NDY	11	250	367.0	367.0	55.0

NDY0011A

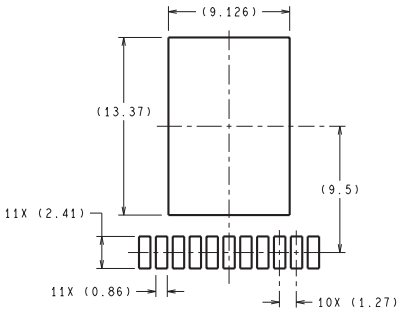


TOP SIDE OF PACKAGE

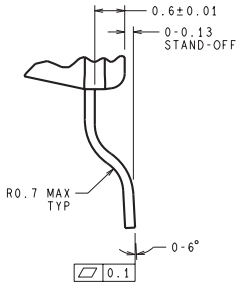


BOTTOM SIDE OF PACKAGE

DIMMENSIONS ARE IN MILLIMETERS
DIMENSIONS IN ( ) FOR REFERENCE ONLY



RECOMMENDED LAND PATTERN



DETAIL A
TYPICAL

TZA11A (Rev F)

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