Bluetooth™ Radio

Check for Samples: LMX5252

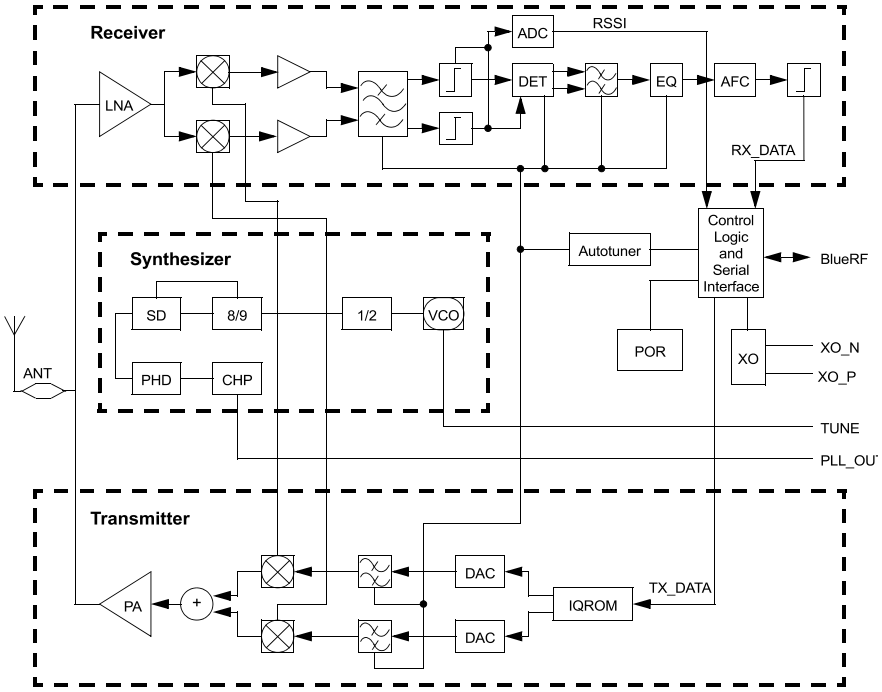
FEATURES

- **The LMX5252 provides a very compact radio solution for Bluetooth™ applications that put extra strong requirements on low cost and small form factors. In addition, the application benefits from very low signal loss between the antenna and the radio.**
- **The radio completely integrates the receiver and transmitter baluns, the antenna switch, and filter together with the voltage-controlled oscillator (VCO) tank on one single die. The fractional-N delta-sigma synthesizer and the crystal offer support for a wide range of external reference frequency clocks or crystals. The digital Received Signal Strength Indicator (RSSI) allows for efficient power control and communication with Bluetooth Class 2 devices. Several current saving modes are available.**
- **The baseband interface is completely digital and compatible with 8-pin bi-directional BlueRF using the RXMODE2 configuration. It can automatically adapt to the voltage levels used by different baseband controllers, independently of the supply voltage.**

APPLICATIONS

- **The LMX5252 is primarily targeting cost-sensitive consumer applications that require fast design-in, low power consumption and small designs. It is ideal for applications such as:**
  - **2G, 2.5G, and 3G handsets**
  - **PDAs**
  - **Notebook PCs**
  - **Computer peripherals**
  - **Office network equipment**
  - **Home applications**

FUNCTIONAL BLOCK DIAGRAM



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These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

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DESCRIPTION

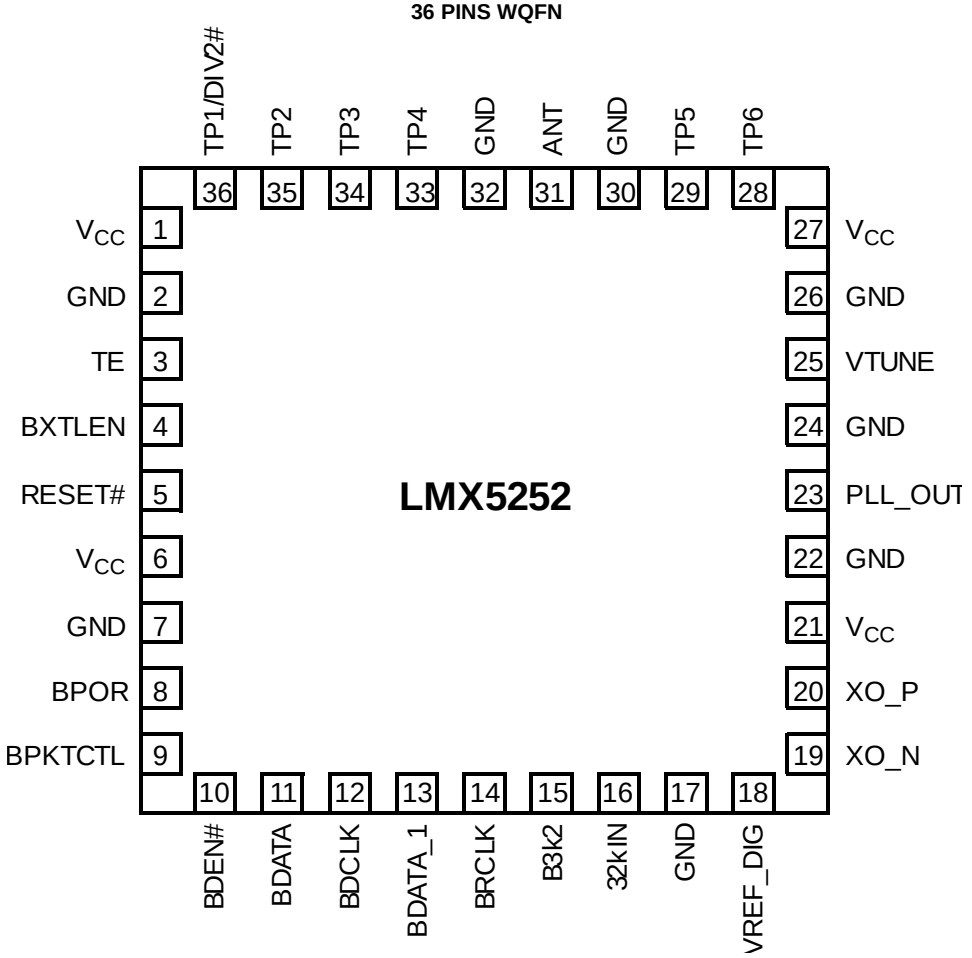
The Texas Instruments LMX5252 Bluetooth Radio is a part of the third generation Bluetooth solution designed for use with short-range wireless applications.

The radio integrates a complete Bluetooth Class 2 transceiver, operating in the ISM frequency band (2.4-2.5 GHz). The modulation is Gaussian Frequency Shift Keying (GF- SK) with a Bluetooth product of 0.5 and a modulation index ranging from 0.28 to 0.35. Fast frequency hopping (1600 hops/s) is used over a total of 79 channels between 2.402 GHz up to 2.480 GHz. The channel bandwidth is 1 MHz.

The LMX5252 is designed in 0.18 µm RF CMOS technology for small die size and low power consumption. The LMX5252 is available in a 6.0 mm x 6.0 mm 36 pin thin quad flatpack no lead (WQFN) package.

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CONNECTION DIAGRAM
36 PINS WQFN



NOTE: Ground pad layout under ground slug of LMX5252 is required and must be soldered to the PCB ground.

PIN FUNCTIONS

PIN		TYPE	DEFAULT LAYOUT	DESCRIPTION
NAME	NO.			
VCC	1	I	VCC	Power connection.
GND	2		GND	Ground connection.
TE	3		NC	Scan test enable. Leave unconnected for normal operation.
BXTLEN	4	I	Baseband	BRCLK enable. System clock enable signal (active high).
RESET#	5	I	Reset	External reset (active low).
VCC	6	I	VCC	Power connection.
GND	7		GND	Ground connection.
BPOR	8	O	NC	Reset signal to baseband controller.
BPKTCTL	9	I	Baseband	Access code indication from baseband controller. In transmit mode this controls the transmitter state, high = TX ON. In receive mode this controls the filter bandwidth, high = narrow, low = wide.
BDEN#	10	I	Baseband	DBUS enable (active low). Latch enable, data latched from low to high.
BDDATA	11	I/O	Baseband	DBUS data.
BDCLK	12	I	Baseband	DBUS clock. Maximum 4 MHz.
BDATA_1	13	I/O	Baseband	Transmit/receive Bluetooth data and sync signal for transmit.

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PIN FUNCTIONS (continued)

PIN		TYPE	DEFAULT LAYOUT	DESCRIPTION
NAME	NO.			
BRCLK	14	O	Baseband	Buffered system clock output. Pin36 = high then same as crystal. Pin 36 = low then divide by 2 output.
B3k2	15	O	NC	3.2 kHz clock output. Connect to ground for normal operation.
32kIN	16	I	32kHz Crystal	Optional 32.0 or 32.768 kHz Input frequency for generating 3.2KHz clk. Connect to ground for normal operation.
GND	17		GND	Ground connection.
VREF_DIG	18	I	IO Voltage	Reference voltage for digital I/O. Control signals to baseband are level shifted depending on this input voltage.
XO_N	19	I/O	Crystal	Crystal negative input.
XO_P	20	I/O	Crystal	Crystal positive input or external clock input.
VCC	21	I	VCC	Power connection.
GND	22		GND	Ground connection.
PLL_OUT	23	O	Loop Filter Input	Charge pump output to loop filter.
GND	24		GND	Ground connection.
VTUNE	25	I	Loop Filter Output	VCO tune input from loop filter.
GND	26		GND	Ground connection.
VCC	27	I	VCC	Power connection.
TP6	28	I	PLL_OUT	Test point 6. Vtune calibration input. Pin with 0 ohm resistor for VTune.
TP5	29		NC	Test point 5. Do not connect.
GND	30		GND	Ground connection.
ANT	31	I/O	Antenna	Antenna I/O.
GND	32		GND	Ground connection.
TP4	33		NC	Test point 4. Do not connect.
TP3	34		GND	Test point 3. Connect to ground.
TP2	35		GND	Test point 2. Connect to ground.
TP1/DIV2#	36		NC	Not supported.

ELECTRICAL SPECIFICATIONS

ABSOLUTE MAXIMUM RATINGS indicate limits beyond which damage to the device may occur. RECOMMENDED OPERATING CONDITIONS indicate conditions for which the device is intended to be functional, but do not specify specific performance limits.

This device is a high performance RF integrated circuit and is ESD sensitive. Handling and assembly of this device should be performed at ESD free workstations. A 2 kV ESD rating applies to all pins.

ABSOLUTE MAXIMUM RATINGS

		MIN	MAX	UNIT
V_{CC}	Supply voltage	–0.3	3.3	V
V_{ANT}	Applied voltage to ANT pin	–0.3	1.95	V
V_I	Applied voltage to all other pins	–0.3	V_{CC} + 0.3	V
I_{LATCH}	Latchup current	100		mA
ESD_{MM}	ESD Machine model (1)		200	V
ESD_{HBM}	ESD Human Body		2000	V
P_{IN}	RF Input power		4	dBm
T_L	Lead temperature (soldering)		260	°C
T_S	Storage temperature	–65	150	°C

(1) A 200V ESD rating applies to all pins except antenna pin (pin 31) = 150V.

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RECOMMENDED OPERATING CONDITIONS

		MIN	TYP	MAX	UNIT
V_{CC}	Supply Voltage (V_{CC})	2.5	2.75	3	V
T_A	Temperature, Ambient. Fully functional Blue- tooth Mode	–40	25	85	°C
HUM_{OP}	Humidity across operating temperature range			8%5	

DC ELECTRICAL CHARACTERISTICS, V_{CC} = 2.75 V

PARAMETER		MIN	TYP	MAX	UNIT
VREF_DIG	Reference voltage	1.5		V_{CC}	V
V_{IH}	Logical high input voltage	$0.75\times V_{CC}$		$1.1\times V_{CC}$	V
V_{IL}	Logical low input voltage	$-0.15\times V_{CC}$		$0.36\times V_{CC}$	V
V_{OH}	Logical high output voltage	$0.8\times V_{CC}$	2.75		V
V_{OL}	Logical low output voltage		0	$0.2\times V_{CC}$	V
C_{INP}	Input capacitance, digital pins			10	pF
$C_{L\text{-}DIG}$	Load capacitance, digital pins			10	pF
$C_{L\text{-}AN}$	Load capacitance, analog pins			25	pF
$I_{CC\text{-}L}$	Input leakage current			5	µA
T_{RISE}	Rise/Fall time, digital inputs			20	ns
T_{FALL}	Rise/Fall time, digital outputs		5	10	ns
$I_{CC\text{-}PWDN}$	Supply current in standby mode, XO Inactive		28	50	µA
$I_{CC\text{-}XO}$	Supply current in standby mode, XO Active			271	µA
$I_{CC\text{-}RX}$	Supply current in static RX mode		39	47	mA
$I_{CC\text{-}TX}$	Supply current in static TX mode		44	55	mA

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RF PERFORMANCE CHARACTERISTICS

In the performance characteristics tables the following applies:

- V_{CC} = 2.75V unless otherwise specified.
- Temperature range from –40°C to +85°C unless otherwise specified.
- RF system performance specifications are specified on TI reference design platforms.“
- All tests performed based on Bluetooth Test Specification rev 0.92.

RECEIVER PERFORMANCE CHARACTERISTICS

PARAMETER		CONDITION		MIN	TYP(1)	MAX	UNIT
RX_{sense}(2)	Receive sensitivity	BER < 0.001	2.402 GHz		–80	–75	dBm
			2.441 GHz		–80	–75	
			2.480 GHz		–80	–75	
$P_{in}RF$	Maximum input level			–10	0		dBm
IMP(3)	Intermodulation performance	F_1 = + 3 MHz, F_2 = + 6 MHz, $P_{in}RF$ = –64 dBm		–38	–36		dBm
RSSI	RSSI Dynamic range at LNA input			–72		–52	dBm
Z_{RFIN}(4)	Input impedance of RF port (RF_inout)	Single input impedance F_{in} = 2.4 GHz			32		Ω
Return Loss	Return loss(3)(5)					–8	dB
OOB(3)	Out of band blocking performance	$P_{in}RF$ = –10 dBm, 30 MHz < F_{CWI} < 2 GHz, BER < 0.001		–10			dBm
		$P_{in}RF$ = –27 dBm, 2000 MHz < F_{CWI} < 2399 MHz, BER < 0.001		–27			
		$P_{in}RF$ =–27 dBm, 2498 MHz < F_{CWI} < 3000 MHz, BER < 0.001		–27			
		$P_{in}RF$ =–0 dBm, 3000 MHz < F_{CWI} < 12.75 GHz, BER < 0.001		–10			

(1) Typical operating conditions are at 2.85V operating voltage and 25°C ambient temperature.
(2) The receiver sensitivity is measured at the device interface.
(3) The f_0 = –64 dBm Bluetooth modulated signal, f_1 = –39dbm sine wave, f_2 = –39 dBm Bluetooth modulated signal, $f_0 = 2f_1 – f_2$, and $|f_2 - f_1| = n \times 1MHz$, where n is 3, 4, or 5. For the typical case, n = 3.*f*
(4) Reference Table 2
(5) Reference Table 3

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TRANSMITTER PERFORMANCE CHARACTERISTICS

PARAMETER		CONDITION	MIN	TYP(1)	MAX	UNIT
$P_{OUT}RF$(2)	Transmit output power	2.402 GHz	–3	+1	+3	dBm
		2.441 GHz	–3	+1	+3	dBm
		2.480 GHz	–3	+1	+3	dBm
Power Density(3)	Power density		–4	1	2	dBm
MOD $\Delta F1_{AVG}$	Modulation characteristics	Data = 00001111	140	165	175	kHz
MOD $\Delta F2_{MAX}$(4)		Data = 10101010	115	125		kHz
$\Delta F2_{AVG}/\Delta F1_{AVG}$(5)			0.8			
	20 dB Bandwidth				1000	kHz
ACP(3)	Adjacent channel power (In-band spurious)	| M - N | = 2		–48	–20	dBm
		| M - N | ≥ 3		–51	–40	dBm
$P_{OUT}2\times f_o$(6)	PA 2nd Harmonic suppression	Maximum gain setting: f_0 = 2402 MHz, P_{out} = 4804 MHz			–30	dBm
$PO_{UT}3\times f_o$(3)	PA 3rd Harmonic suppression	Maximum gain setting: f_0 = 2402 MHz, P_{out} = 7206 MHz			–30	dBm
Z_{RFOUT}(7)	RF Output/Input Impedance of RF Port (RF_inout)	P_{out} at 2.4 GHz		47		Ω
Return Loss(3)(8)	Return Loss				–14	dB

(1) Typical operating conditions are at V_{CC} = 2.75V.
(2) The output power is measure at the device interface.
(3) Not tested in production.
(4) ΔF2max > 115 kHz for at least 99.9% of all ΔF2max.
(5) Modulation index set between 0.28 and 0.35.
(6) Out-of-Band spurs only exist at 2nd and 3rd harmonics of the CW frequency for each channel.
(7) Reference Table 1.
(8) Reference Table 4.

SYNTHESIZER PERFORMANCE CHARACTERISTICS

PARAMETER		CONDITION	MIN	TYP	MAX	UNIT
f_{VCO}	VCO Frequency range			5000		MHz
t_{LOCK}	Lock time	f_0 ± 50 kHz		120		µs
Δf_0offset(1)(2)	Initial carrier frequency tolerance	During preamble	–75	0	75	kHz
Δf_0drift(1)(2)	Initial carrier frequency drift	DH1 data packet	–25	0	25	kHz
		DH3 data packet	–40	0	40	kHz
		DH5 data packet	–40	0	40	kHz
		Drift Rate	–20	0	20	kHz/50µs
t_D -Tx	Transmitter delay time	From Tx data to antenna		4		µs

(1) Frequency accuracy is dependent on crystal oscillator chosen. The crystal must have a cumulative accuracy of < ±20ppm to meet Bluetooth specifications.
(2) Not tested in production.

CRYSTAL REQUIREMENTS

The LMX5252 contains a crystal driver circuit. This circuit operates with an external crystal and capacitors to form an oscillator. Figure 1 shows the recommended crystal circuit. Figure 3 specifies system clock requirements.

The RF local oscillator and internal digital clocks for the LMX5252 is derived from the reference clock at the CLK+ input. This reference may either come from an external clock or a dedicated crystal oscillator. The crystal oscillator connections require an Xtal and two grounded capacitors.Ÿ

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It is also important to consider board and design dependant capacitance in tuning crystal circuit. Equations that follow allow a close approximation of crystal tuning capacitance required, but actual values on board will vary with capacitive properties of the board. As a result, there is some fine tuning of crystal circuit that has to be done that can not be calculated, must be tuned by testing different values of load capacitance.

Many different crystals can be used with the LMX5252. Key requirements from Bluetooth specification is ±20ppm. Additionally, ESR (Equivalent Series Resistance) must be carefully considered. LMX5252 can support maximum of 230Ω ESR, but it is recommended to stay <100Ω ESR for best performance over voltage and temperature. See Figure 2 for ESR as part of crystal circuit for more information. ESR of the crystal also has impact on the startup time of the crystal oscillator circuit of the LMX5252. TRANSMIT MODE STATE MACHINE, for system start up timing and Table 7.

CRYSTAL

The crystal appears inductive near its resonant frequency. It forms a resonant circuit with its load capacitors. The resonant frequency may be trimmed with the crystal load capacitance.

Load Capacitance

For resonance at the correct frequency, the crystal should be loaded with its specified load capacitance, which is the value of capacitance used in conjunction with the crystal unit. Load capacitance is a parameter specified by the crystal, typically expressed in pF. The crystal circuit shown in Figure 2 is composed of:

- C1 (motional capacitance
- R1 (motional resistance)
- L1 (motional inductance)
- C0 (static or shunt capacitance)

The LMX5252 provides some of the load with internal capacitors C_{int}. The remainder must come from the external capacitors and tuning capacitors labeled Ct1 and Ct2 as shown in Figure 1. Ct1 and Ct2 should have the same the value for best noise performance.

The LMX5252 has XOC_{TUNE} which can be changed in register 2. There are 7 bits of tuning for XOC_{TUNE}. Default value of 0028h, which results in an additional 2.6pF internal capacitance. This register can be used in production testing for additional tuning, if necessary. (See Table 4 for range of XOC_{TUNE}).

Crystal load capacitance (C_L) is calculated as the following:

$$C_L = C_{int} + XOC_{TUNE} + Ct1//Ct2T$$

The C_L above does not include the crystal internal self-capacitance C0 as shown in Figure 2, so the total capacitance is:

$$C_{total} = C_L + C_0$$

Based on crystal spec and equation:

$$C_L = {}_{Cint} + XOC_{TUNE} + Ct1//Ct2m$$
$$C_L = 8pF + 2.6pF + 6pF = 16.6pF$$

16.6pF is very close to the TEW crystal requirement of 16pF load capacitance. With the internal shunt capacitance C_{total}:

$$C_{total} = 16.6pF + 5pF = 21.6pF$$

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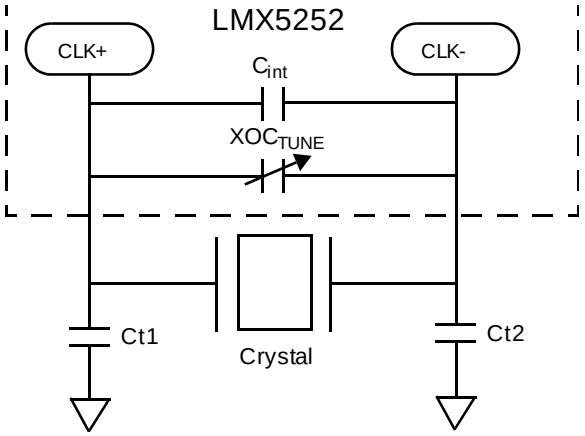


Figure 1. LMX5252 Crystal Recommended Circuit•

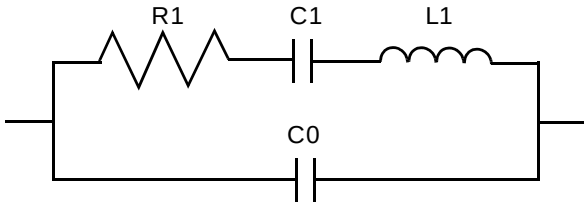


Figure 2. Crystal Equivalent Circuit

Crystal Pullability

Pullability is another important parameter for a crystal, which is the change in frequency of a crystal with units of ppm/pF, either from the natural resonant frequency to a load resonant frequency, or from one load resonant frequency to another. The frequency can be pulled in a parallel resonant circuit by changing the value of load capacitance. A decrease in load capacitance causes an increase in frequency, and an increase in load capacitance causes a decrease in frequency.

Frequency Tuning

Frequency Tuning is achieved by adjusting the crystal load capacitance with external capacitors. It is a Bluetooth requirement that the frequency is always within ±20 ppm. Crystal/oscillator must have cumulative accuracy specifications of **±15 ppm** to provide margin for frequency drift with aging and temperature.

TEW Crystal

The LMX5252 has been tested with the TEW TAS-4025A crystal, reference Table 1 for specification. Since the internal capacitance of the crystal circuit is 8 pF and the load capacitance is 16 pF, 12 pF is a good starting point for both Ct1 and Ct2. The 2480 MHz RF frequency offset is then tested. Figure 3 shows the RF frequency offset test results.

Figure 3 shows the results are –20 kHz off the center frequency, which is –1 ppm. The pullability of the crystal is 2 ppm/pF, so the load capacitance must be decreased by about 1.0 pF. By changing Ct1 or Ct2 to 10 pF, the total load capacitance is decreased by 1.0 pF. Figure 4 shows the frequency offset test resuts. The frequency offset is now zero with Ct1 = 10 pF, Ct2 = 10 pF.

Reference Table 2 for crystal tuning values used on Phoenix Development Board with TEW crystal.

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Table 1. TEW TAS-4025A

SPECIFICATION	VALUE
Package	4.0x2.5x0.65 mm - 4 pads
Frequency	13.000 MHz
Mode	Fundamental
Stability	> ±15ppm at –40 to +85C
CL Load Capacitance	16pF
ESR	80 Ω max.
C0 Shunt Capacitance	5pF
Drive Level	50 ±10uV
Pullability	2 ppm/pF min
Storage Temperature	–40 to +85C

Table 2. TEW on Tucson Board

REFERENCE	LMX5252
Ct1	10pF
Ct2	10pF

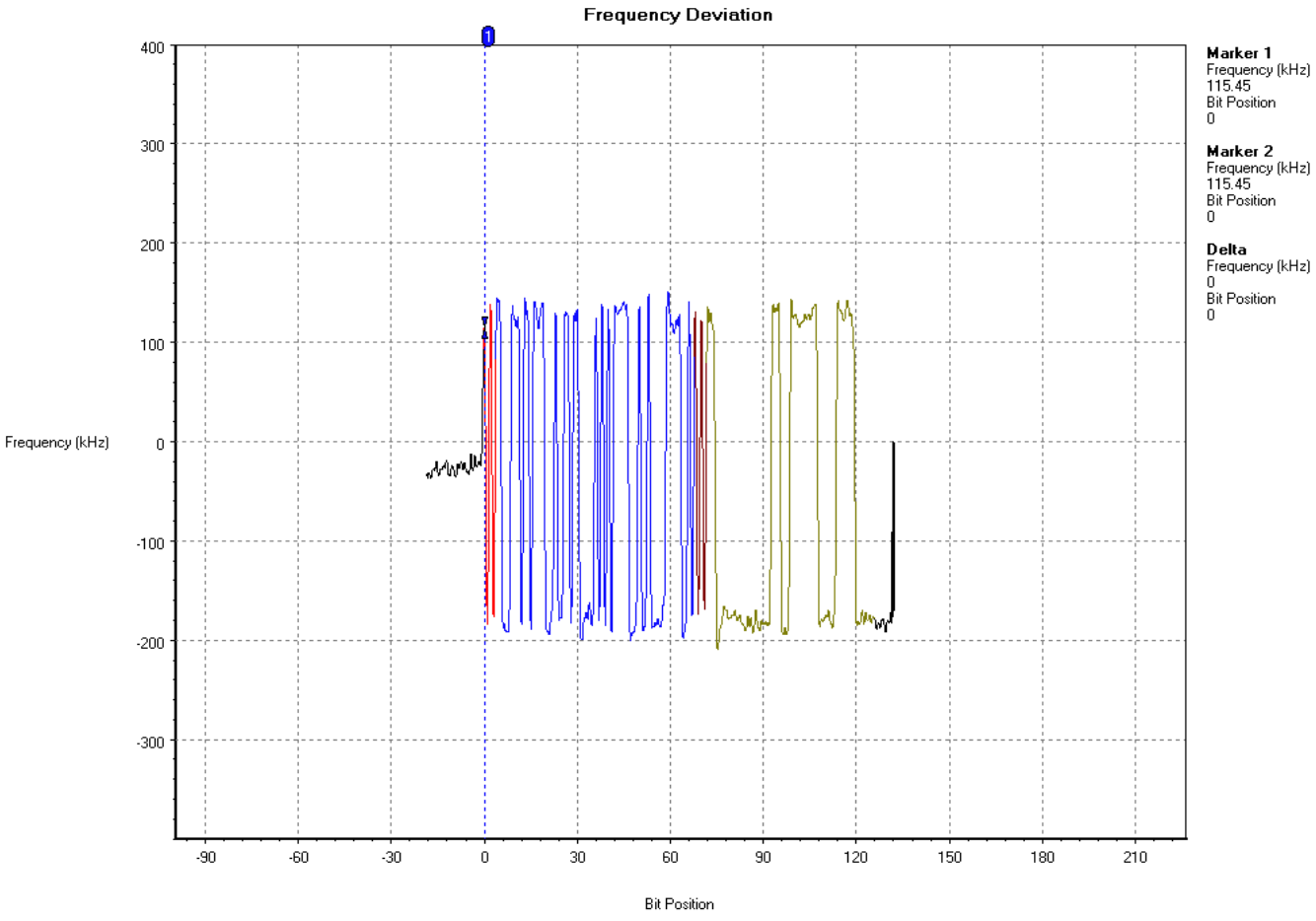


Figure 3. Frequency Offset with 12pF //12 pF Capacitors

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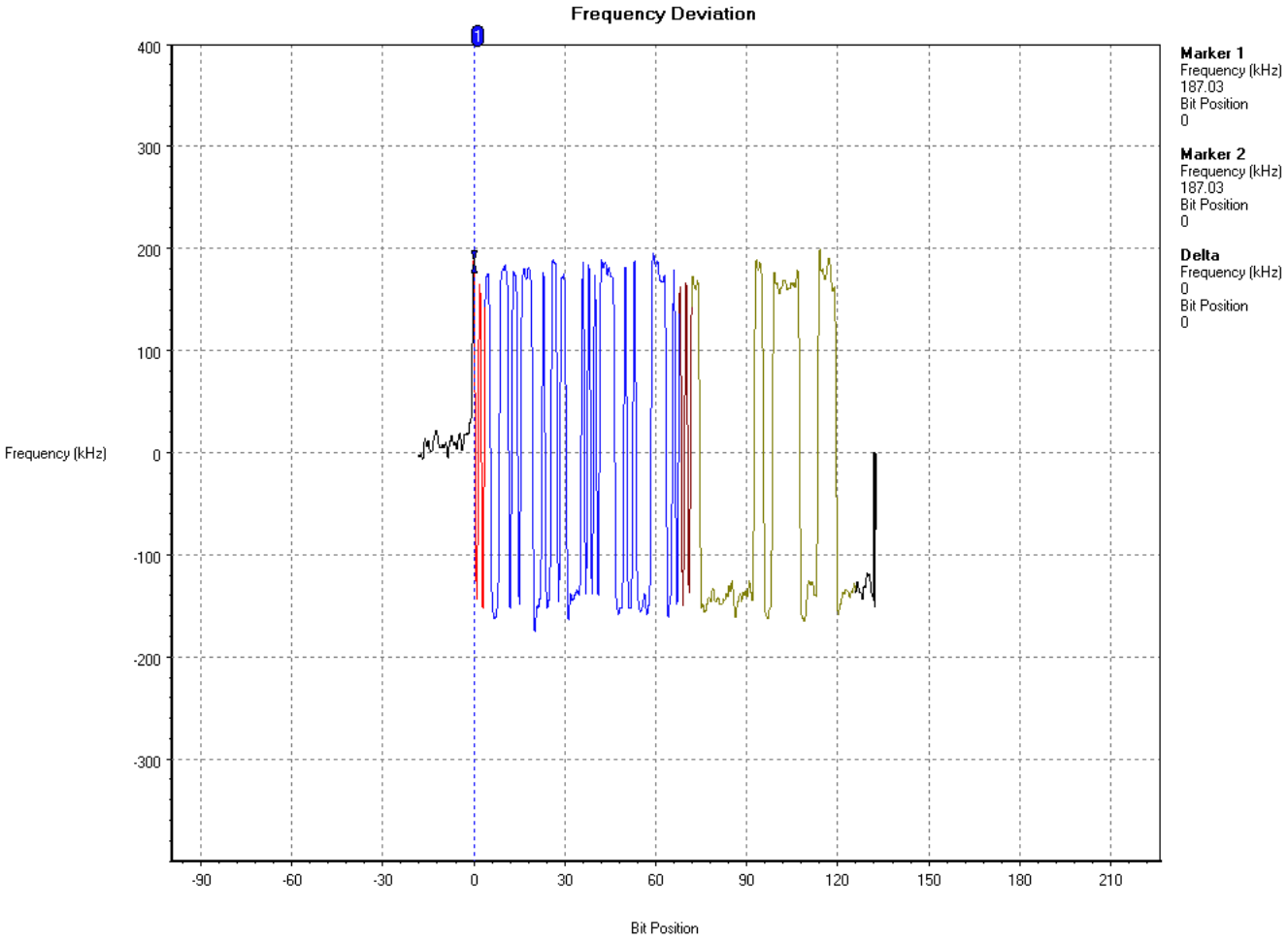


Figure 4. Frequency Offset with 10 pF//10 pF Capacitors

Table 3. System Clock Requirements

PARAMETER		MIN	TYP	MAX	UNIT
C_{REF}	External reference clock frequency	10	13	20	MHz
C_{TOL}	Frequency tolerance (over full operating temperature and aging)	–20	±15	+20	ppm
XOC_{TUNE}	Digital crystal tuning load range		8		pF
C_{OSC}	Crystal oscillator	10	13	20	MHz
C_{ESR}	Crystal serial resistance			230	Ω
C_{REF-PS}	External reference clock power swing, pk to pk	100	200	400	mV
C_{int}	Internal load capacitance		8		pF
C_{AGE}	Aging			±1	ppm/year

Table 4. Register 2: XOC_{TUNE} Tuning Load Range

BINARY VALUE	HEX VALUE	VALUE	UNIT
000 0000	0	0	pF
010 1000	28(1)	2.6	pF
111 1111	7F	8	pF

(1) Default value for RF initialization register 2.

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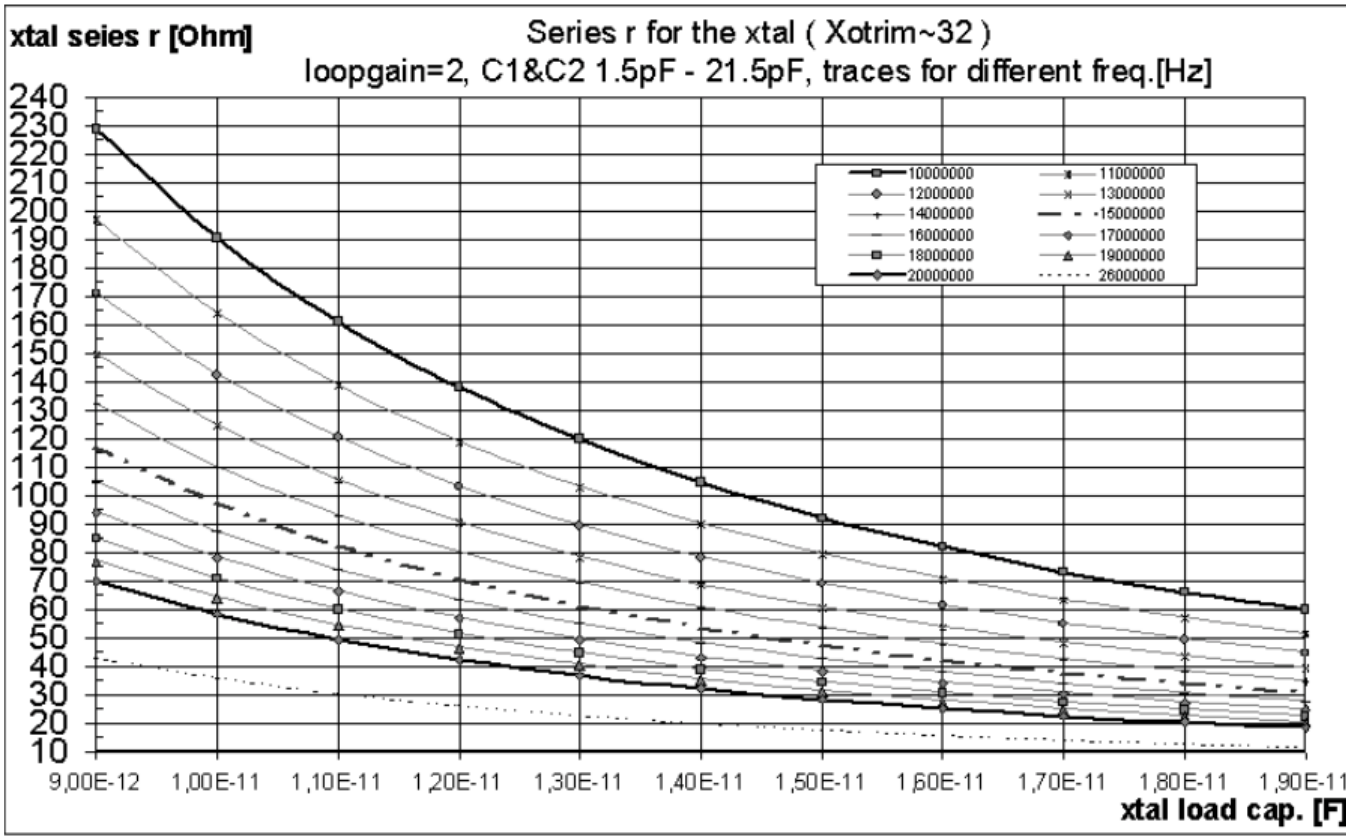


Figure 5. ESR vs Load Capacitance for the Crystal

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TYPICAL PERFORMANCE CHARACTERISTICS

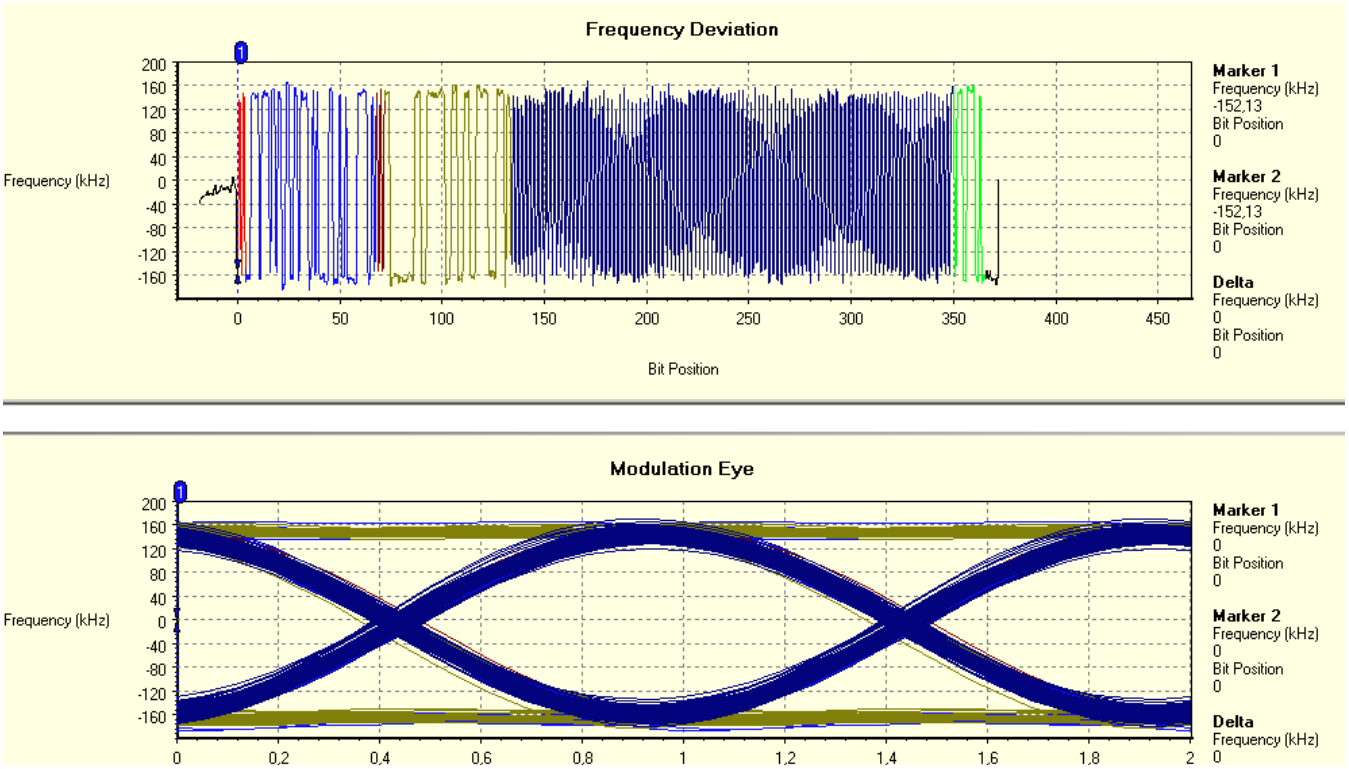


Figure 6. Modulation and Eye Diagram

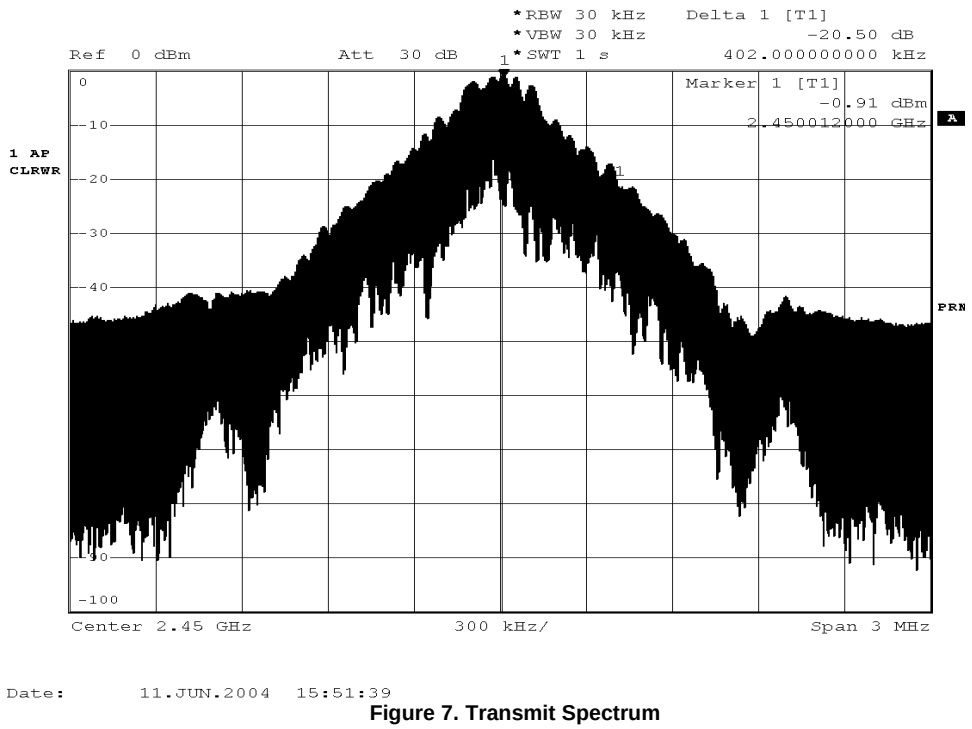


Figure 7. Transmit Spectrum

TYPICAL PERFORMANCE CHARACTERISTICS (continued)

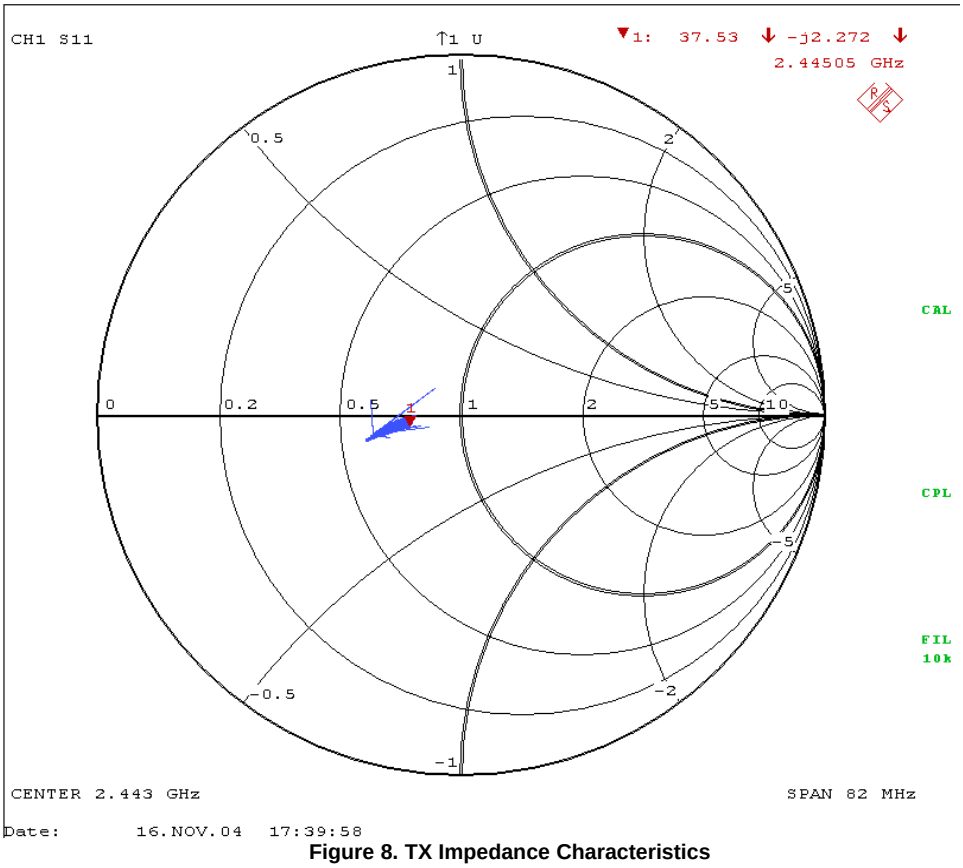


Figure 8. TX Impedance Characteristics

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TYPICAL PERFORMANCE CHARACTERISTICS (continued)

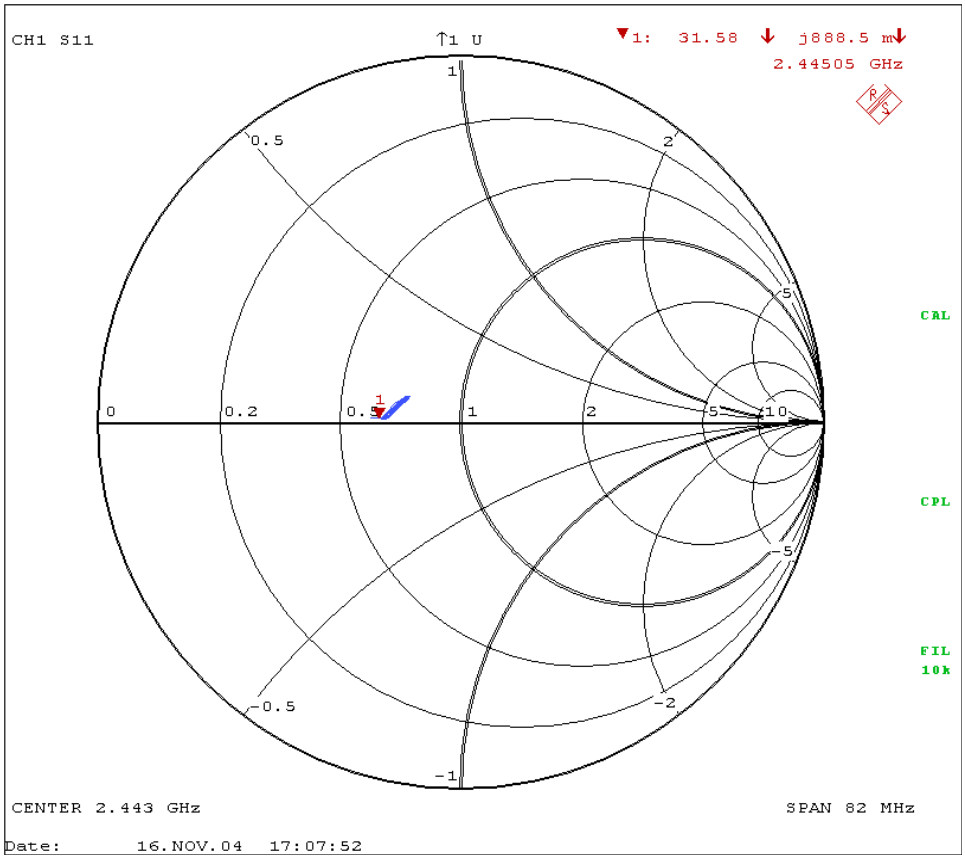


Figure 9. RX Impedance Characteristics

TYPICAL PERFORMANCE CHARACTERISTICS (continued)

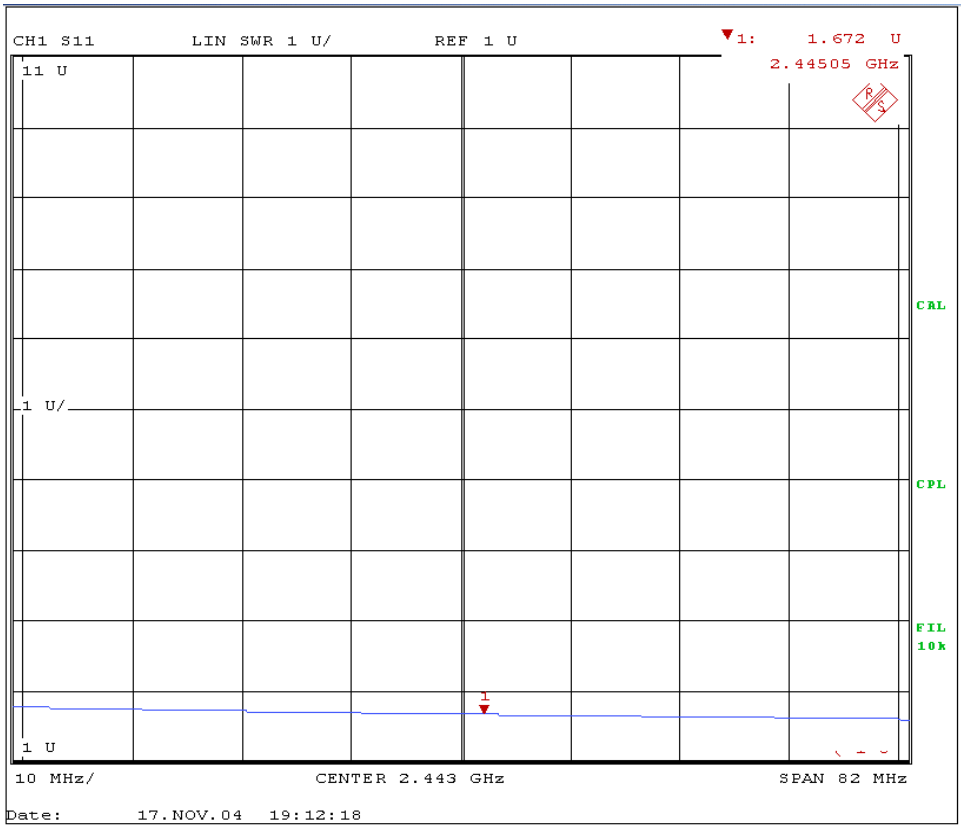


Figure 10. Transmitter Return Loss

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FUNCTIONAL DESCRIPTION

The circuitry of the LMX5252 (see FUNCTIONAL BLOCK DIAGRAM) utilizes a heterodyne receiver architecture with a low intermediate frequency (2 MHz) such that the intermediate frequency filters can be integrated on chip. The receiver consists of a low-noise amplifier (LNA) followed by two mixers. The intermediate frequency signal processing blocks consist of a poly-phase bandpass filter (BPF), two hard-limiters (LIM), a frequency discriminator (DET), and a post-detection filter (PDF). The received signal level is detected by a received signal strength indicator (RSSI).

The received frequency equals the local oscillator frequency (fLO) plus the intermediate frequency (fIF):

fRF = fLO + fIF (supradyne).

The LMX5252 is able to operate with multiple reference frequencies between 10 and 20 MHz. Simulations to ensure performance are done with 13.0 MHz, 26.0 MHz (used by GSM and WCDMA platforms in Europe), and 19.2 MHz. To operate with multiple reference frequencies, the LMX5252 contains a fractional-N delta-sigma synthesizer. The synthesizer consists of a phase detector, a charge pump, an (off-chip) loop-filter, an RF-frequency divider, and a voltage controlled oscillator (VCO).

The transmitter utilizes IQ-modulation with bit-stream data that is gaussian filtered. Other blocks included in the transmitter are a VCO buffer and a power amplifier (PA).

SYSTEM INTERACTION

For complete operation, the LMX5252 must be connected with a Bluetooth baseband controller (e.g., LMX5100) or to a device that can emulate the baseband functionality. The baseband function is to read and write to the internal registers in the radio chip. These registers are used for setting the frequency, tuning, and control. The communication between the baseband controller and the radio chip is performed via the serial interface. The LMX5252 also requires an external antenna. The antenna must be connected through a 50 ohm interface. The power supply is divided externally into four parts: two for the RF blocks (RF and VCO), one for the IF blocks, and one for the low frequency and digital blocks. Each of the supplies must be low frequency decoupled for maximum performance.

RECEIVER FRONT-END

The receiver front-end consists of a low-noise amplifier (LNA) followed by two mixers and two low-pass filters for the I- and Q-channels.

The intermediate frequency (IF) part of the receiver front end consists of two IF amplifiers that receive input signals from the mixers, delivering balanced I- and Q-signals to the poly-phase bandpass filter. The poly-phase bandpass filter is directly followed by two hard-limiters that together generate an AD-converted RSSI signal.

Poly-Phase Bandpass Filter

The purpose of the IF bandpass filter is to reject noise and spurious (mainly adjacent channel) interference that would otherwise enter the hard limiting stage. In addition, it takes care of the image rejection.

The bandpass filter uses both the I- and Q-signals from the mixers. The out-of-band suppression should be higher than 40 dB (f<1 MHz, F>3 MHz). The bandpass filter is tuned over process spread and temperature variations by the autotuner circuitry. A 5th order Butterworth filter is used

Hard-Limiter and RSSI

The I- and Q-outputs of the bandpass filter are each followed by a hard-limiter. The hard-limiter has its own reference current. The RSSI (Received Signal Strength Indicator) measures the level of the RF input signal.

The RSSI is generated by piece-wise linear approximation of the level of the RF signal. The RSSI has a mV/dB scale, and an analog-to-digital converter for processing by the baseband circuit. The input RF power is converted to a 5- bit value. The RSSI value is then proportional to the input power (in dBm).

The digital output from the ADC is sampled on the BPKTCTL signal low-to-high transition.

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RECEIVER BACK-END

The hard-limiters are followed by a two frequency discriminators. The I-frequency discriminator uses the 90× phase shifted signal from the Q-path, while the Q-discriminator uses the 90× phase-shifted signal from the I-path. A polyphase bandpass filter performs the required phase shifting. The output signals of the I- and Q-discriminator are substracted and filtered by a low-pass filter. An equalizer is added to improve the eye-pattern for 101010 patterns.

After equalization, a dynamic AFC (automatic frequency offset compensation) circuit and slicer extract the RX_DATA from the analog data pattern. It is expected that the Eb/No of the demodulator is approximately 17 dB.

Frequency Discriminator

The frequency discriminator gets its input signals from the limiter. A defined signal level (independent of the power supply voltage) is needed to obtain the input signal. Both inputs of the frequency discriminator have limiting circuits to optimize performance. The bandpass filter in the frequency discriminator is tuned by the autotuning circuitry.

Post-Detection Filter and Equalizers

The output signals of the FM discriminator first go through a post-detection filter and then through an equalizer. Both the post-detection filter and equalizer are tuned to the proper frequency by the autotuning circuitry. The post-detection filter is a low-pass filter intended to suppress all remaining spurious signals, such as the second harmonic (4 MHz) from the FM detector and noise generated after the limiter.

The post-detection filter also helps for attenuating the first adjacent channel signal. The equalizer improves the eye opening for 101010 patterns. The post-detection filter is a third order Butterworth filter.

AUTOTUNING CIRCUITRY

The autotuning circuitry is used for tuning the bandpass filter, the detector, the post-detection filter, the equalizer, and the transmit filters for process and temperature variations. The circuit also includes an offset compensation for the FM detector.

SYNTHESIZER

The LMX5252 features a fractional-N delta-sigma (DS) synthesizer that operates using an external reference frequency in the range of 10 to 20 MHz or, alternatively, up to 40 MHz.

The synthesizer consists of a phase-frequency detector, a charge pump, a low-pass loop filter, a programmable frequency divider, a voltage-controlled oscillator (VCO), a delta-sigma modulator, and a lookup table.

The frequency divider consists of a divide-by-2 circuit (divides the 5 GHz signal from the VCO down to 2.5 GHz), a divide-by-8-or-9 divider, and a digital modulus control. The delta-sigma modulator controls the division ratio and also generates an input channel value to the lookup table.

Phase-Frequency Detector

The phase-frequency detector is a 5-state phase-detector. It responds only to transitions, hence phase-error is independent of input waveform duty cycle or amplitude variations. Loop lockup occurs when all the negative transitions on the inputs, F_REF and F_MOD, coincide. Both outputs (i.e., Up and Down) then remain high. This is equal to the zero error mode. The phase-frequency detector input frequency range is between 10 and 20 MHz. The phase-frequency detector has the option of being turned off such that the PLL can be opened. The enabling/disabling of the phase detector operation is performed by the control signal PHD_ON. This mode is not actively used in the LMX5252.

TRANSMITTER CIRCUITRY

The transmitter consists of ROM tables, two Digital to Analog (DA) converters, two low-pass filters, IQ mixers, and a power amplifier (PA).

The ROM tables generate a digital IQ signal based on the transmit data. The output of the ROM tables is inserted into IQ-DA converters and filtered through two low-pass filters. The two signal components are mixed up to 2.5 GHz by the TX mixers and added together before being inserted into the transmit PA.

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IQ-DA Converters and TX Mixers

The ROM output signals drive an I- and a Q-DA converter. Two Butterworth low-pass filters filter the DA output signals. The 6 MHz clock for the DA converters and the logic circuitry around the ROM tables are derived from the autotuner.

The TX mixers mix the balanced I- and Q-signals up to 2.4- 2.5 GHz. The output signals of the I- and Q-mixers are summed.

LOW FREQUENCY CIRCUITRY

The low frequency circuitry includes an adjustable crystal oscillator (XO), an adjustable low power oscillator (LPO), a power-on reset (POR) block, and an off-chip reset input. For generation of the system clock, a 10-20 MHz crystal or up to a 40 MHz external reference clock input can be used.

For operation in low power modes, the low frequency circuitry generates a 3.2 kHz clock, synthesized from a 32.768 kHz or 32.0 kHz signal. The source can be either a reference clock or crystal signal input. Alternatively, the main system clock can be used.

DIGITAL CIRCUITRY

The digital functions of the LMX5252 provide I- and Q-signal generation in the transmitter, baseband interface control, filter tuning, fractional XO and PLL frequency division, and power-up control for all analog blocks. The digital circuitry also allows for programming of the analog blocks in order to compensate for process variations. By using an external voltage reference, the serial interface automatically adjusts the logic voltage levels to different baseband controllers.

The logic is contained in the Control Logic and Serial Interface and the IQROM blocks. Scan testing is used for all logic.

CRYSTAL OSCILLATOR

The oscillator should be as accurate as possible. If the LMX5252 is used in an application that already uses an XTAL oscillator, the oscillator circuitry will act as buffer to an AC coupled via 10 pF to a small signal (100 to 400 mVp). Alternatively, via a 20 kΩ resistor in series with 10 pF for an externally applied CMOS (square-wave) signal into pin XO_P.

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APPLICATION INFORMATION

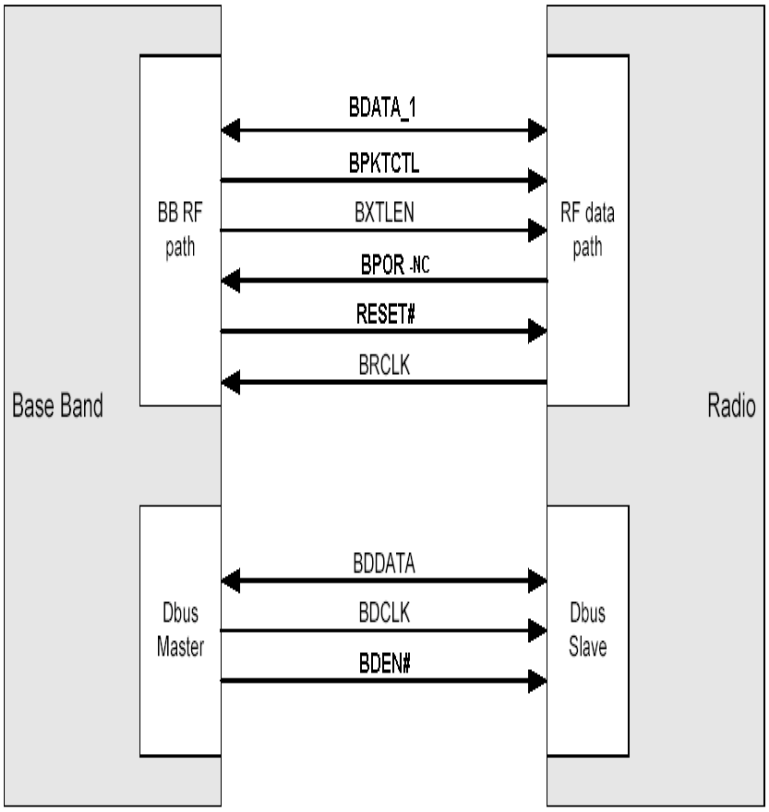


Figure 11. Base Band RF Interface

BDATA_1: Transmit/receive Bluetooth data and sync signal for transmit *interface to RFDATA*.

The RFDATA signal is the multiplexed Bluetooth data receive and transmit signal. The data is provided at a bit rate of 1 Mbit/s with 12× oversampling, synchronized to the 12 MHz BBCLK. The RFDATA signal is a dedicated RF interface pin. This signal is driven to a logic high after reset.

BPKTCTL: Access code indication from baseband controller. In transmit mode this controls the transmitter state, high = TX ON. In receive mode this controls the filter bandwidth, high = narrow, low = wide *interface to BTSEQ*, signals indicate internal states of the Bluetooth sequencer, which are used for interfacing to some external devices.

BXTLEN: BRCLK enable. System clock enable signal (active high) *interface to RFCE*. The RFCE signal is the chip enable to the radio chip. When RFCE is high, RF chip power is controlled by its power control registers. When RFCE is low, the RF chip is powered-down. However, the serial interface is operational and the CP3000 device can access the RF chip internal registers. The RFCE signal is an alternate function of a general-purpose I/O pin. At reset, this pin is in TRI-STATE mode. Software must enable the alternate function of the pin to give control over this signal to the RF interface. During Bluetooth power-down phases, the CP3000 device provides a mechanism to reduce the power consumption of an external RF chip by driving the RFCE signal of the RF interface to a logic low level. This feature is available when the Power Management Module of the CP3000 device has enabled the Hardware Clock Control mechanism.

BPOR: Reset signal to baseband controller interface to RESET, Chip general reset with internal pull-down. NC for normal operation.

RESET#: External reset (active low) to RF chip from baseband controller

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BRCLK: Buffered system clock output. Pin36 = high then same as crystal. Pin 36 = low then divide by 2 output, *interface to the X1CKI/BBCLK,* is the input signal for the 12- MHz clock signal. The radio chip uses this signal internally as the 12× oversampling clock and provides it externally to the CP3000 device for use as the Main Clock. Some CP3000 devices have a separate CLKIN pin for receiving an external clock.

BDDATA; I/O DBUS data interface to SDAT. The SDAT signal is multiplexed serial receive and transmit data between the radio chip and the CP3000 device. The SDAT signal is an alternate function of a general-purpose I/O pin. At reset, this pin is in TRI-STATE mode. Software must enable the alternate function of the pin to give control over this signal to the RF interface.

BDCLK: DBUS clock. Maximum 4 MHz *interfaces to SCLK*. The SCLK signal is the serial interface shift clock output. The CP3000 device always acts as the master of the serial interface and therefore always provides the shift clock. The SCLK signal is an alternate function of a general-purpose I/O pin. At reset, this pin is in TRI-STATE mode. Software must enable the alternate function of the pin to give control over this signal to the RF interface.

BDEN#: DBUS enable (active low). Latch enable, data latched from low to High, *interface to SLE*. The SLE pin is the serial load enable output of the serial interface of the CP3000 device. During write operations (to the radio chip registers), the data received by the shift register of the radio chip is copied into the address register on the next rising edge of SCLK after the SLE signal goes high. During read operations (read from the registers), the radio chip releases the SDAT line on the next rising edge of SCLK after the SLE signal goes high. At reset, this pin is in TRI-STATE mode. Software must enable the alternate function of the pin to give control over this signal to the RF interface.

PROGRAMMING DESCRIPTION

RADIO-BASEBAND INTERFACE

The radio-baseband (RF-BB) interface is comprised of eight signal pins according to the BlueRF specification. However, in the LMX5252, two additional pins are present. These pins are BPOR and B3k2. BPOR is used for power-on reset of the baseband. B3k2 is a clock output from the radio supplying a 3.2 kHz reference clock to the baseband for low power mode operation.

SERIAL INTERFACE TIMING

Table 5. Serial Interface Timing

PARAMETER		CONDITION	MIN	TYP	MAX	UNIT
t_{CS}	Data to clock setup time	See Figure 4		10		ns
t_{CH}	Data to clock hold time			1		ns
t_{CWH}	Clock pulse width high			20		ns
t_{CWL}	Clock pulse width low			20		ns
t_{ES}	Clock to enable setup time			5		ns
t_{CES}	Enable to clock setup time			5		ns
t_{EWH}	Enable pulse width high			200		ns
t_{EWL}	Enable pulse width low			2500		ns

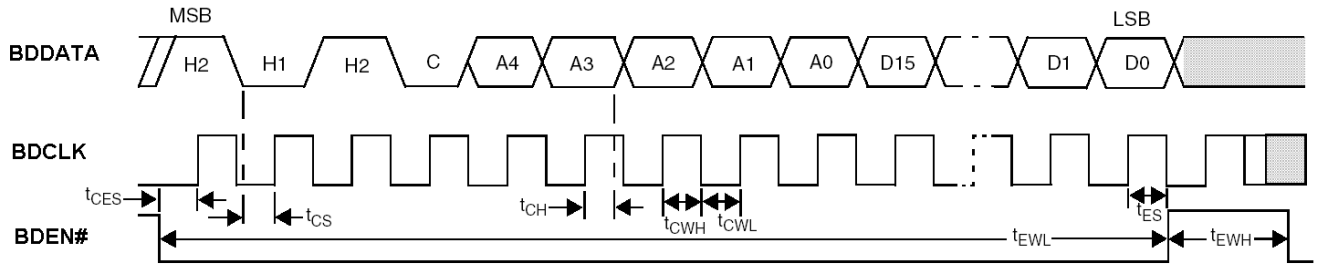


Figure 12. Serial Port Write Timing Diagram

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ACCESSING THE REGISTERS

The registers in the radio are accessed over the DBUS (see Table 2).

Table 6. Radio Registers

FIELD	NO. OF BITS	COMMENT
Device Address	3	Radio is allocated binary device address 101.
Read/Write	1	Driving this bit high indicates a read operation.
Register Address	5	
Data	16	

When accessing a 32-bit register the user must write to the same register twice. The highest bits ([31:16]) are accessed first and on the second write, the lowest bits ([15:0]) are accessed. The time in-between these two accesses must be at least two clock cycles. In the case of a 4 MHz clock, the minimum time would be 500 ns.

16-Bit Register

When reading a 16-bit register, the value of the register is read back. If a value of 0x0063 is written, 0x0063 is read back.

32-Bit Register

The value read from a 32-bit register is not the actual register value, but a counter value. The value that the user receives when reading a 32-bit register depends on read/ write order. If the highest bits are written first, 0x0000 is read back. If the lowest bits are written first, 0x0001 is read back. If the user writes two consecutive times to the register, 0x0001 is always read back. The read back of a 32-bit WORD is independent of data written to the register.

Example 1
Writing 0xFFFF DC04 to register 10.
BDDATA 101 0 01010 1111111111111111
BDDATA 101 0 01010 1101110000000100
Reading register 10.
BDDATA 101 1 01010 and following value is received: 0000000000000001

Example 2
Writing 0xFFFF DC04 to register 10 when doing read back between the writing.
BDDATA 101 0 01010 1111111111111111
BDDATA 101 1 01010 and following value is received: 0000000000000000
BDDATA 101 0 01010 1101110000000100
BDDATA 101 1 01010 and following value is received: 00000000000000011

The order for accessing the registers is from high to low: 17, 15, 14, 12, 11, 10, 9, 8, 7, 6, 5, 4, 2, and 1. These registers need to be written to during the initialization of the radio. After initialization the radio is ready to transmit or receive. The radio receives and transmits on the positive edge of the BDCLK. Figure 13 and Figure 14 show the timing for register writing and reading.

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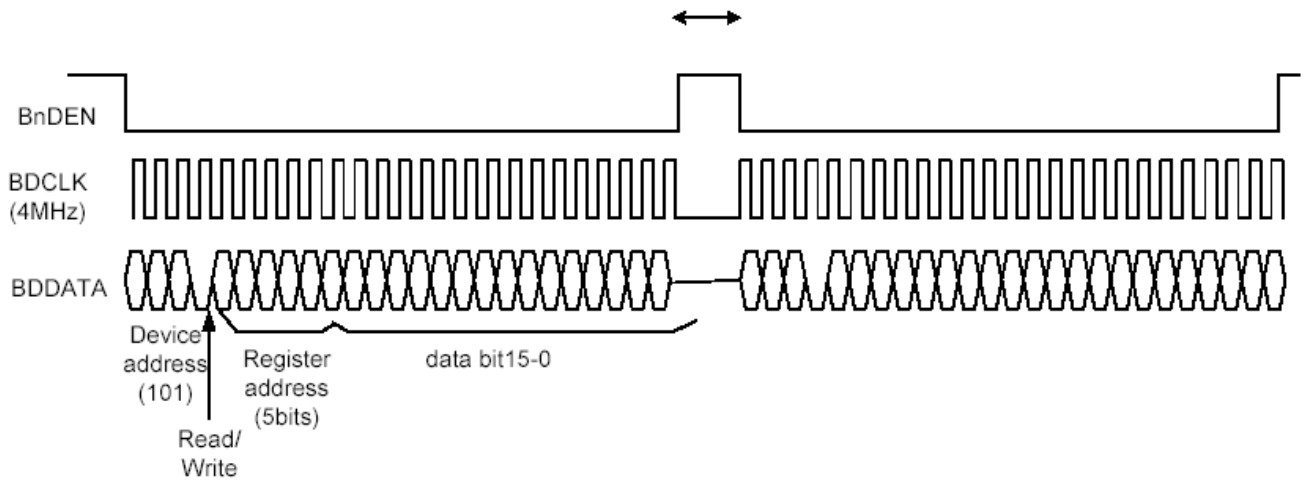


Figure 13. 32-Bit Register Write Timing

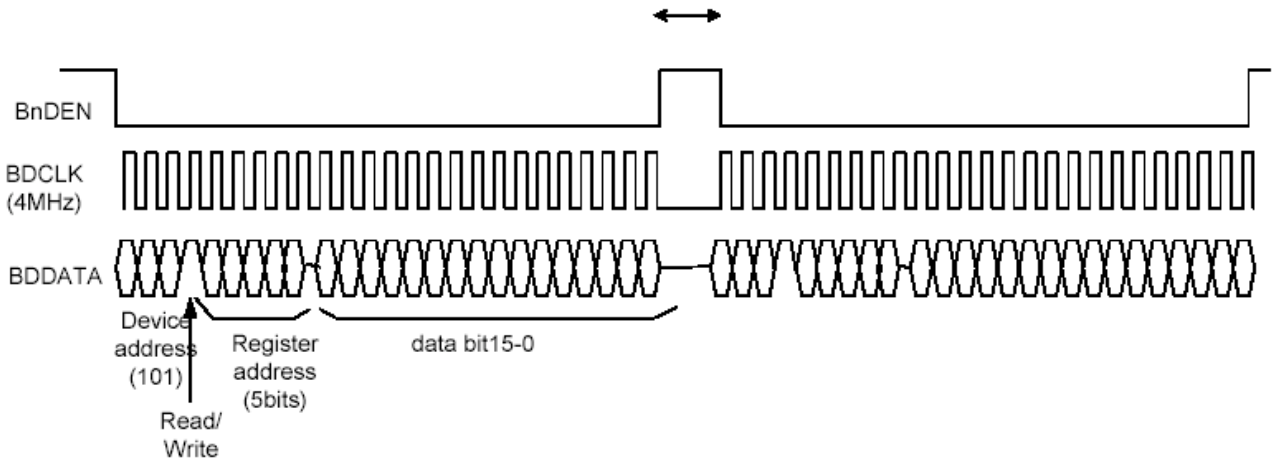


Figure 14. 32-Bit Register Read Timing

POWER-UP MODE, STATE MACHINE

When the LMX5252 is powered up, it enters a power-up mode and the power-up sequence is started. After that, the LMX5252 performs a controlled reset of the baseband (see Figure 15 and Figure 16). The LMX5252 states are described in the following paragraphs.

Off: When the LMX5252 enters Off mode, all configuration data is lost. In this state, the LMX5252 also drives BPOR low.

Power-up: When the power supply is on and the RESET# is high, the LMX5252 starts up the crystal oscillator and enters Power-up mode. After the crystal oscillator (XO) is settled, the LMX5252 sends four clock cycles on the BRCLK before driving BPOR high.

RF init: The baseband now drives BXTLEN high and takes control of the XO. The baseband performs all the needed initialization (i.e., writing the registers in the radio, such as XO trim).

Idle: The baseband drives BDATA_1 low when the initialization is ready. The LMX5252 is now ready to start transmitting, receiving, or to enter Sleep mode.

Sleep: The LMX5252 can be forced into Sleep mode at any time by driving BXTLEN low. All configuration settings are kept, only the Bluetooth low power clock is running (B3k2).

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Wait XTL: When BXTLEN goes high, the crystal oscillator becomes operational. When it is stable, the LMX5252 enters Idle mode and outputs the BRCLK for the baseband.

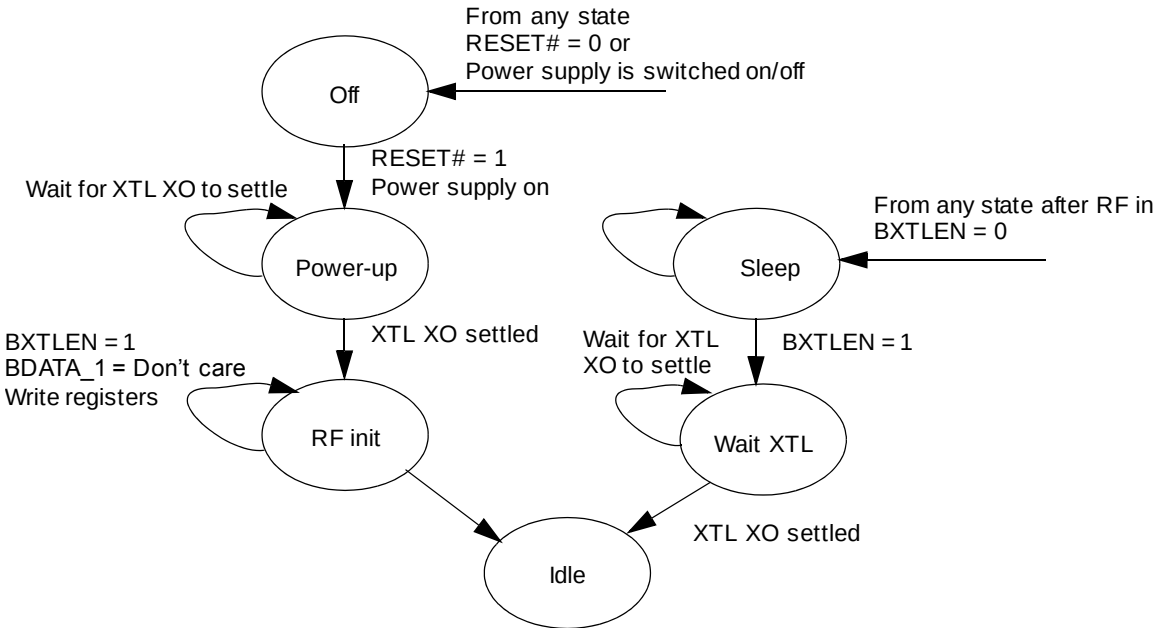


Figure 15. Power-Up Sequence

TRANSMIT MODE STATE MACHINE

LMX5252 Radio can only initiate a transmit sequence from the idle state mode, see Figure 16.

Idle: To initiate the transmit mode, the baseband needs to write a new channel number to the radio. This write command enables the PLL counter. (The counter value is set in register 1 bit(7:0)

Wait data: The PLL counter starts to count down and when it reaches zero the PLL is enabled. LMX5252 then waits for the TX clock synchronization on BDATA_1.

Data: Synchronization is done; LMX5252 is in this state until BPKTCTL goes high.

TX power up: When the BPKTCTL is high the complete transmit path is powered up. Now LMX5252 is transmitting a carrier and is waiting for TX data on BDATA_1.

TX data: The transmit path is powered down by BPKTCTL going low. Note that the synthesizer is still active.

The synthesizer is active during the complete transmit sequence until LMX5252 is in idle state.

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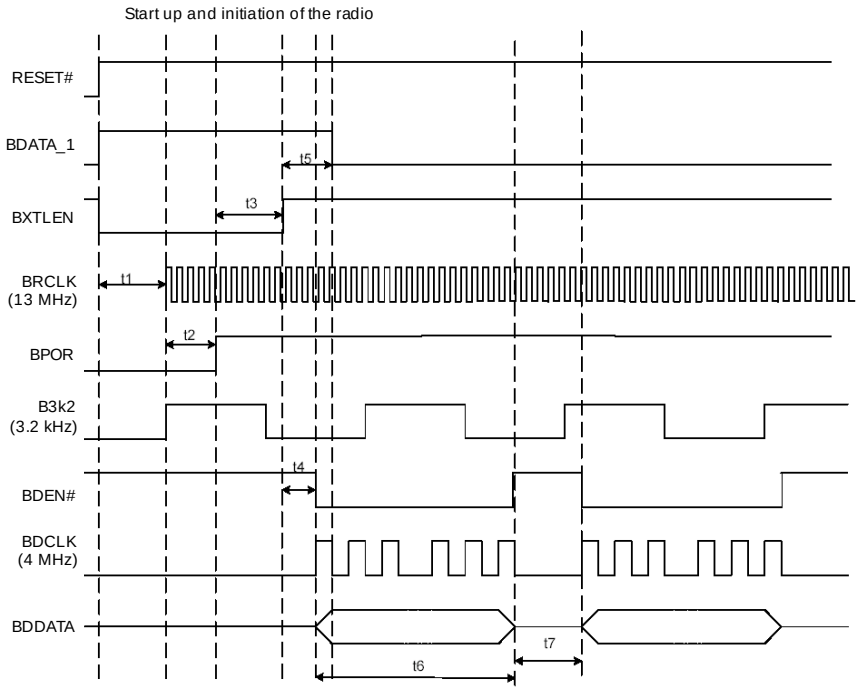


Figure 16. Power-up Timing Diagram

Table 7. Start Up Timing

PARAMETER	TIME	COMMENT
t1	20 ms	Start up time for the crystal.
t2	350 ns for 13 MHz clock	BPOR to the baseband will go high after 4.5 clock cycles.
t3		Depends of the baseband when it is ready to set BXTLEN high after receiving BPOR from the radio.
t4		Depends of the baseband how long time after BXTLEN goes high it is ready to set BnDEN low.
t5		Is set by the baseband; the radio is not dependent on it at all.
t6	6.25 µs	26 (4 MHz) clock cycles are needed to access/doing register writing.
t7	Minimum 500 ns	At least 2 clock cycles are needed in between accessing two registers.

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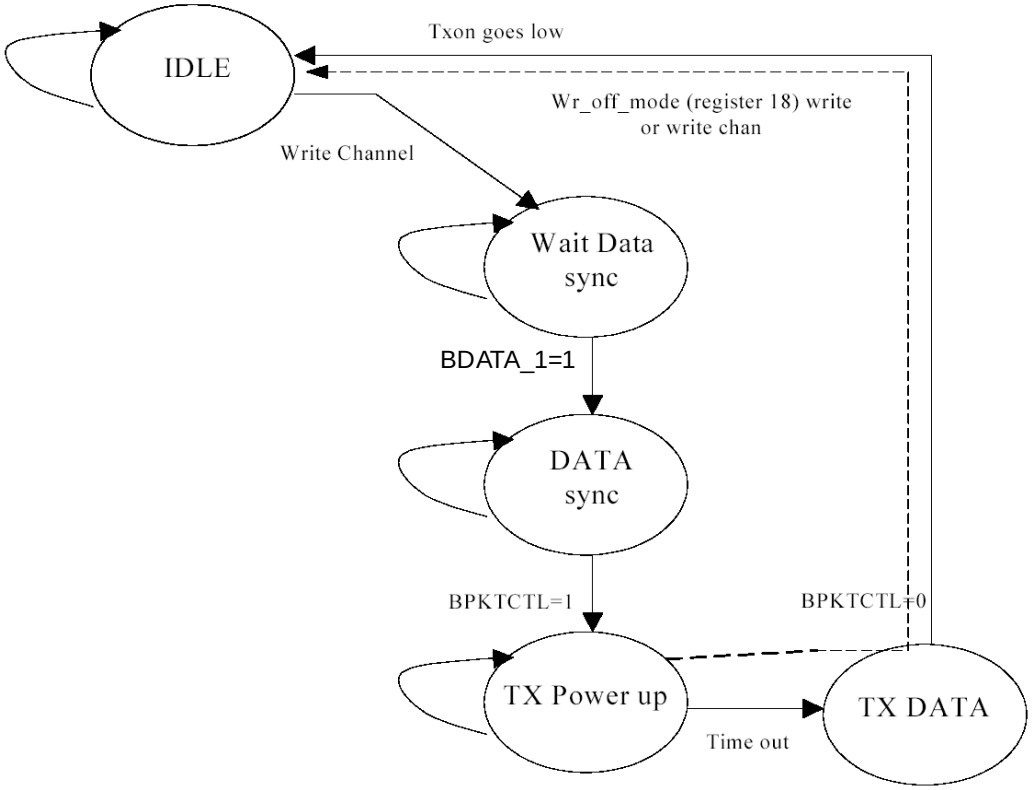


Figure 17. Tx-Mode Sequence

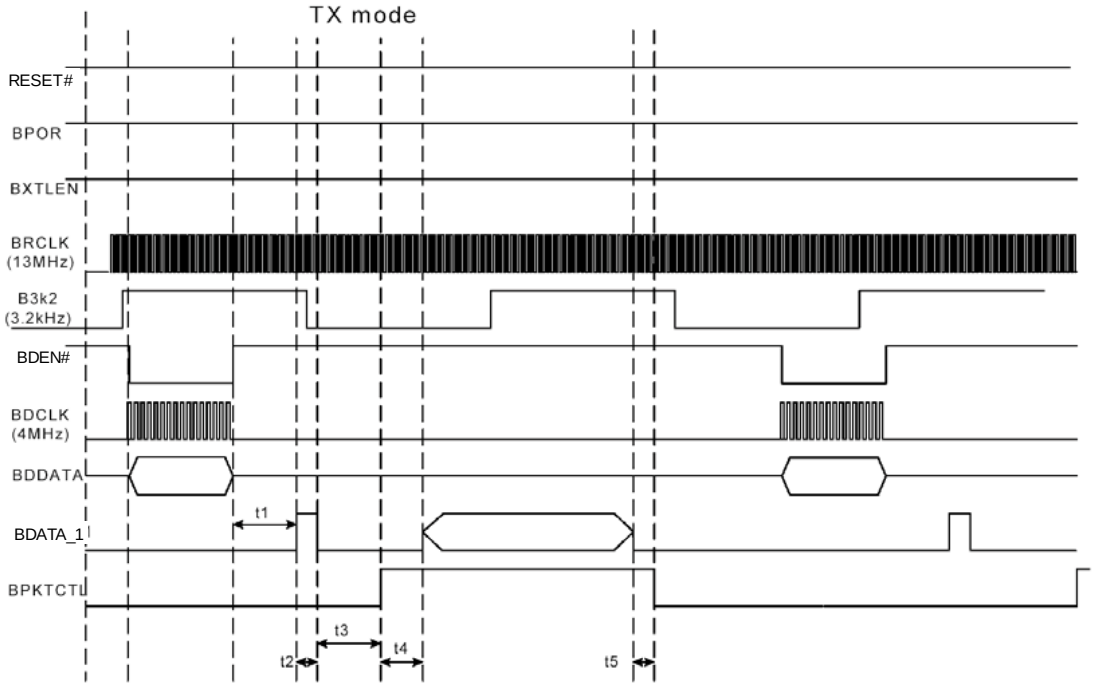


Figure 18. Tx-Mode Timing Diagram

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PARAMETER	TIME	MEASURED TIME	COMMENT
t1			The radio is ready for transmit mode as soon as the frequency is written. After that LMX5252 is just waiting for the synchronization pulse.
t2	1 µs	1 µs	Synchronization pulse ≥ 0.3 µs.
t3		109 µs	Is set by the baseband.
t4	Need to optimized	86 µs	Time between BPKTCTL goes high and data is available on BDATA1.
			TX is turned on when BPKTCTL goes high, the PA is turned on x µs after that. x is set by register 17, (bit 15:8).
t5	Need to optimized		Time between no data on BDATA_1 and BPKTCTL goes low.
			The Pa is turned off when BPKTCTL goes low the rest of the TX path turns off x µs after the PA. x is set by register 17, (bit 7:0).

RECEIVE MODE STATE MACHINE

LMX5252 Radio can only initiate a receive sequence from the idle state, see Figure 19.

Idle: To enter receive mode the baseband needs to write a new channel number to the radio. This write command enables the PLL counter. This counter is set in register 1 and sets the settling time for the receive path.

RX PLL: The PLL starts and the counter begins counting down (1ìs/bit) when BnDEN goes high.

RX Wide Filt: When the counter reaches the value 0 the receive path is powered up and begins detecting the incoming data using the wide tracking filter.

RX Narrow Filt: Upon detection of the access code, the baseband drives the BPKTCTL high and the radio switches to the narrow tracking filter.

After receiving the last data-bit, the baseband ends the receive sequence and puts the radio back to Idle state. Both the RX path and the PLL are powered down. LMX5252 now releases BDATA_1 to be used by the baseband.

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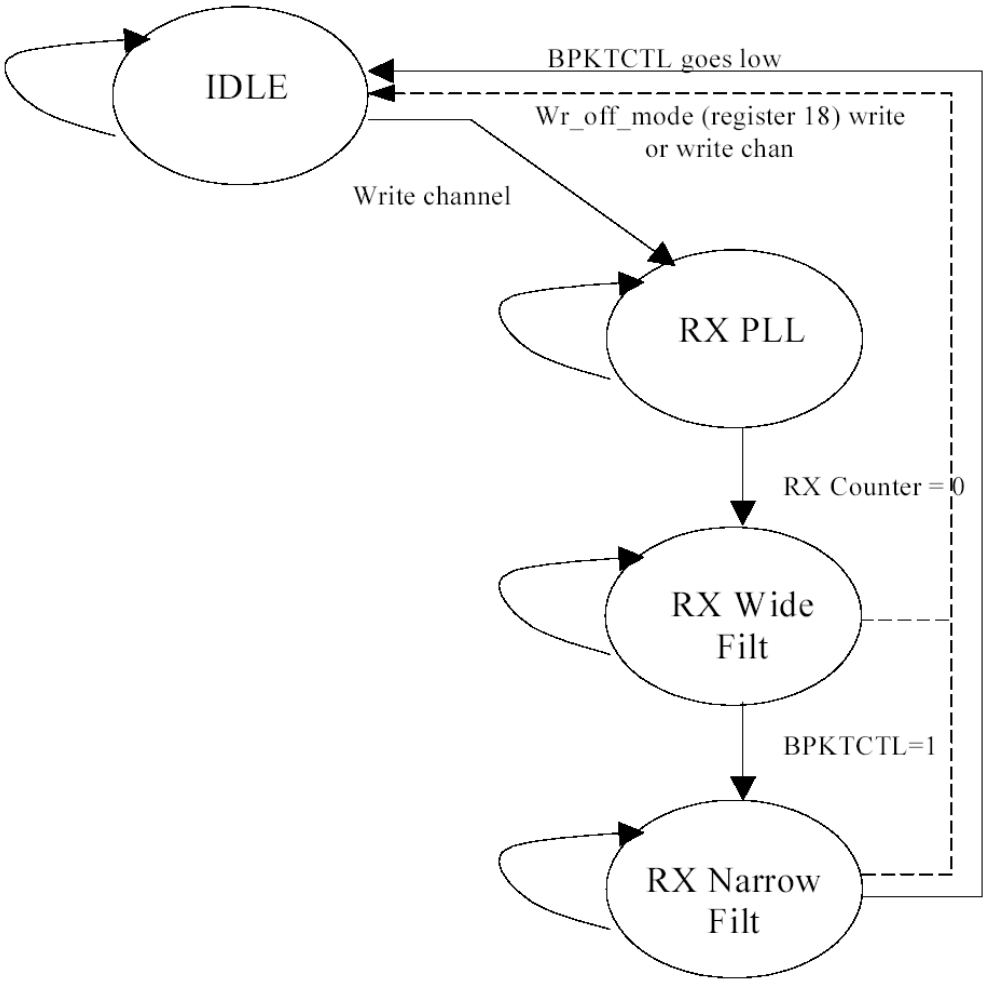


Figure 19. Rx-Mode Sequence

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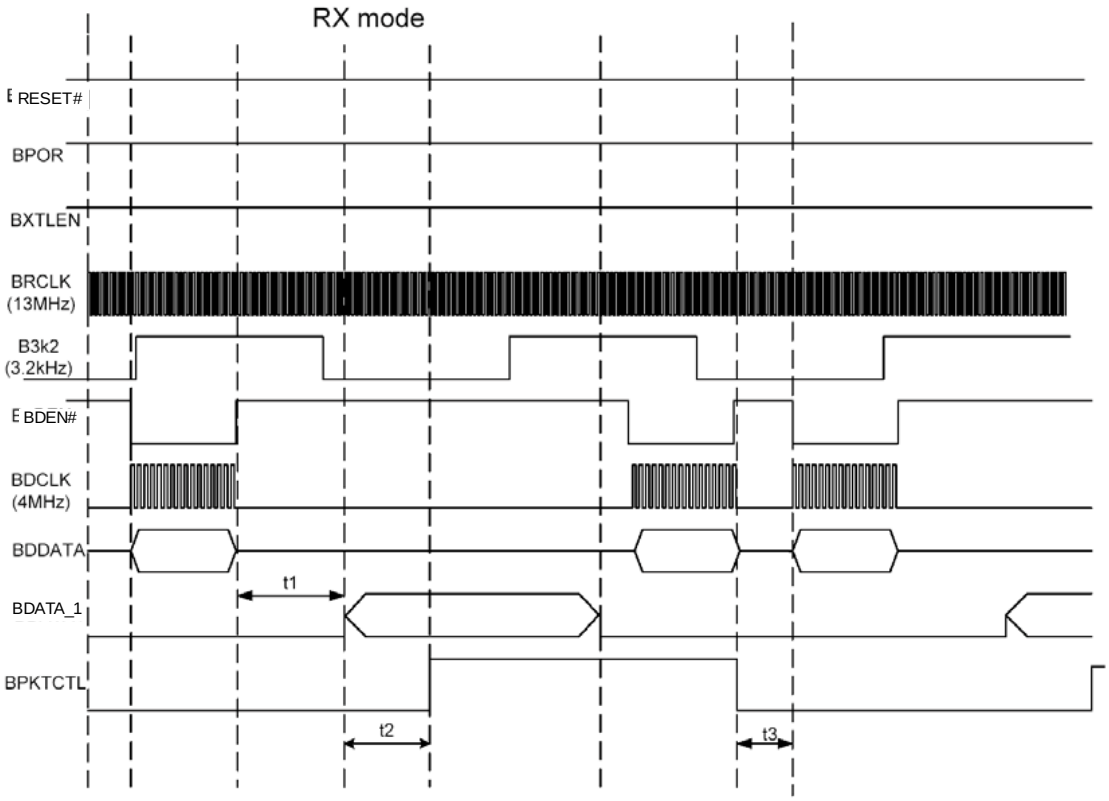


Figure 20. Rx-Mode Timing Diagram

PARAMETER	TIME	MEASURED TIME	COMMENT
t1	120 µs	120 µs	Time between when BnDEN goes high and when the radio puts data on BDATA1.
t2			Depends on when the baseband has detected the access code. The LMX5252 requires that BPKTCTL goes high for at least 1 is after BDATA_1 is done to switch off RX path.
t3		11.2 µs	Time between register writing for switching off RX path and set new node and channel. This register writing will be implemented and used for LMX5252.

REGISTER MAPPING

Table 8 specifies the different registers in the LMX5252 Read or Write status, the address and value at power-up, and programmed value. Some of the trim registers have specific values and are indicated by a note in the table. Values programmed after startup are 12MHz clock source.

Table 8. Register Setup(1)

Register Address (Decimal)	Register Name	Width (Bits)	R/Wb	Power-Up Value (Hex)	Program Value (Hex)	Program Value (Binary)
0	RF Channel (2)	16	W, R	0005	N/A	N/A
1	SyntRxOnCounter(3)	16	W, R	FFFF	5A00	0101 1010 0000 0000
2	XO Trim	16	W, R	0000	0028	0000 0000 0010 1000
3	RSSI	16	R	Undefined	NA	NA

(1) Two words needs to be written consecutive to the same address.
(2) Register 0 must be updated every frame.
(3) Register 1, 2, 4-12, 14, 15, and 17 must be updated after power-up.

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Table 8. Register Setup(1) (continued)

Register Address (Decimal)	Register Name	Width (Bits)	R/Wb	Power-Up Value (Hex)	Program Value (Hex)	Program Value (Binary)
4	Trim (1)(3)(4)	32	W, Wc	0037 0000	003C D400	0000 0000 0011 1100 1101 0100 0000 0000
5	Control (3)	16	W, R	0050	4844	0100 1000 0100 0100
6	BlockOn(1)(3) (5)	32	W, Wc	0000 0040	0080 0060	0000 0000 1000 0000 0000 0000 0110 000
7	Enable(3)	16	W, R	0007	001F	0000 0000 0001 1111
8	Power Control (3)	16	W, R	001F	0016	0000 0000 0001 0110
9	Frequency Reference(1)(3) (6)	32	W, R, Wc	0013 D620	0012 4F80	0000 0000 0001 0010 0100 1111 1000 0000
10	Clock Division(1) (3)(6)	32	W, Wc	FFFF DC04	FFFF F801	1111 1111 1111 1111 1111 1000 0000 0001
11	DSMIN(1)	32	W, Wc	0000 0000	0000 0000	0000 0000 0000 0000 0000 0000 0000 0000
12	DSMOUT	32	W, R	0000	0000	0000 0000 0000 0000
13	Test pins(4)	16	W, R	FFFF	FFFF	1111 1111 1111 1111
14	LPO Division(1) (3)	32	W, Wc	0092 8EC3	00A0 8EC3	0000 0000 1010 0000 1000 1110 1100 0011
15	Auxiliary(7)(8) (9)	32	W, Wc	004A 0000	0150 A100	0000 0001 0100 1010 1110 1101 0000 0000
16	MidTiming	16	W, R	0000	0000	0000 0000 0000 0000
17	PA Counter(8)	16	W, R	FFFF	0108	0000 0001 0000 1000
18	WrOffMode	16	W	xxxx	xxxx	xxxx
30	ManufacturerCode1	16	R	E3C7	N/A	N/A
31	ManufacturerCode2(10)	16	R	6000	N/A	N/A

(4) Register 13 is only for test and does not need to be updated after power-up.
(5) In conjunction with CP3000 rev B0, B1
(6) Clock Division Ratio set for 12MHz
(7) Two words needs to be written consecutive to the same address.
(8) Register 1, 2, 4-12, 14, 15, and 17 must be updated after power-up.
(9) Register 13 is only for test and does not need to be updated after power-up.
(10) Clock Division Ratio set for 12MHz

Table 9. Selected Register Description

REGISTER	REGISTER NAME	BIT	DESCRIPTION
2	XO TRIM	6:0	Trim value for the internal capacitor load of the crystal
3	RSSI	4:0	The RSSI is read when RSSI register is accessed
4	TRIM- VCO Cal	23	VCO calibration bit
TRIM- VCO trim TRIM- CS trim TRIM- Tx bias TRIM- RGTRIMLO TRIM- RGTRIMLO		22:20 19:16 15:12 11:8 7:0	VCO frequency range trim value Current source trim value for both PA and charge pump Current source trim value for both V to I and the mixer driver The 4 bit signal controls the expectation value Spare bits
8	Power Control	4	Gain Step
	Power Control	3:0	Internal PA current timing

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APPLICATION DIAGRAM AND SCHEMATICS

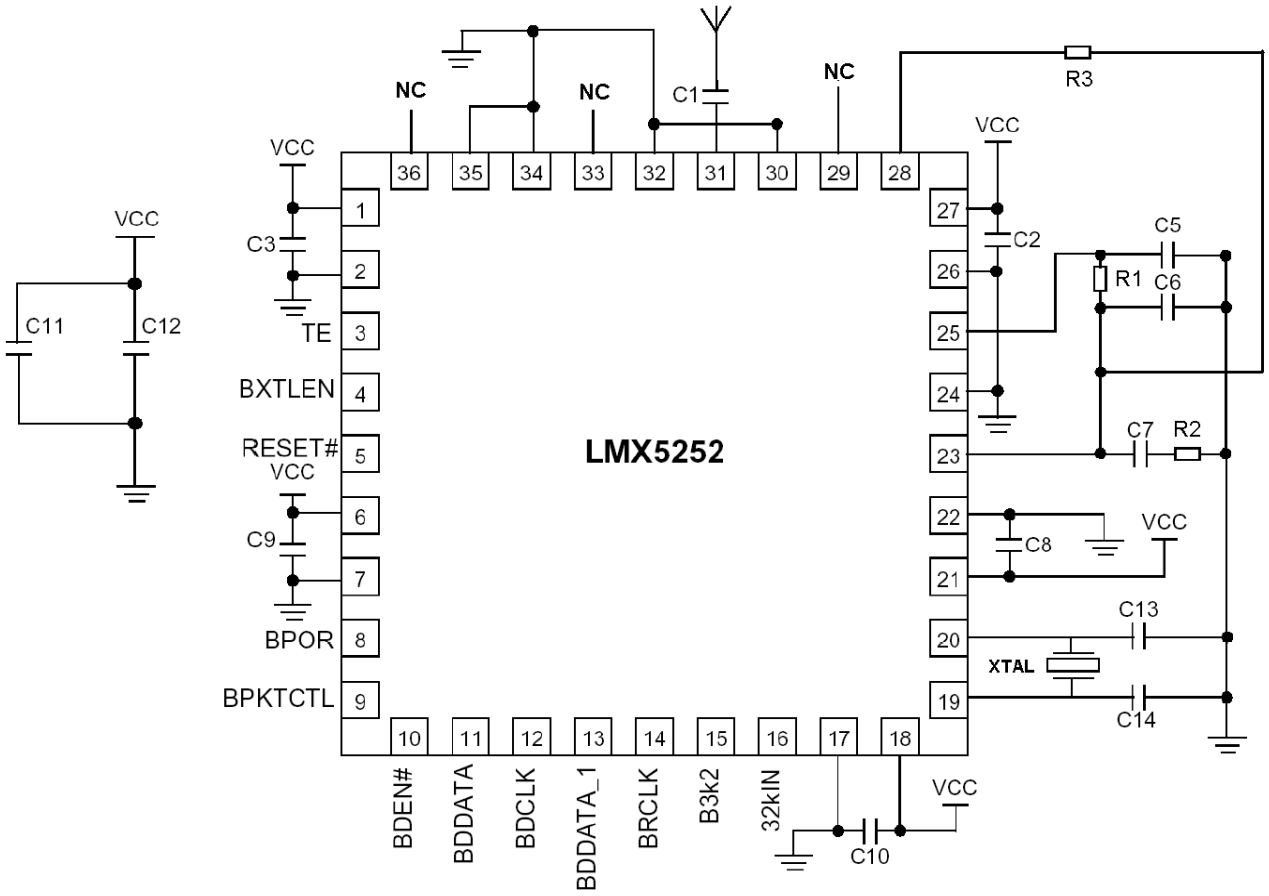


Figure 21. Application Diagram

Table 10. Component Bill of Material for 12 MHz

REFERENCE	DESCRIPTION	VALUE	TOLERANCE	SIZE
C1, C2, C3, C8. C9. C10	Ceramic Capacitor	4.7 pF	20%	402
C5	Ceramic Capacitor	39 pF	20%	402
C6	Ceramic Capacitor	220 pF	10%	402
C7	Ceramic Capacitor	2200 pF	10%	402
C11	Ceramic Capacitor	2.2 uF	20%	603
C12	Ceramic Capacitor	0.1 uF	20%	603
C13	Ceramic Capacitor	12 pF	10%	402
C14	Ceramic Capacitor	15 pF	10%	402
R1	Resistor	10 kΩ	5%	402
Crystal	12MHz			
R2	Resistor	3.3 kΩ	5%	402
R3	Resistor	NM 0Ω		402

Table 11. Component Bill of Material for 13 MHz

REFERENCE	DESCRIPTION	VALUE	TOLERANCE	SIZE
C1, C2, C3, C8. C9. C10	Ceramic Capacitor	4.7 pF	20%	0402
C5	Ceramic Capacitor	39 pF	20%	0402
C6	Ceramic Capacitor	220 pF	10%	0402
C7	Ceramic Capacitor	3300 pF	10%	0402
C11	Ceramic Capacitor	2.2 uF	20%	0603
C12	Ceramic Capacitor	0.1 uF	20%	0603
C13	Ceramic Capacitor	12 pF	10%	0402
C14	Ceramic Capacitor	15 pF	10%	0402
R1	Resistor	10 kΩ	5%	0402
Crystal	13MHz			
R2	Resistor	3.3 kΩ	5%	0402
R3	Resistor	NM 0Ω		0402

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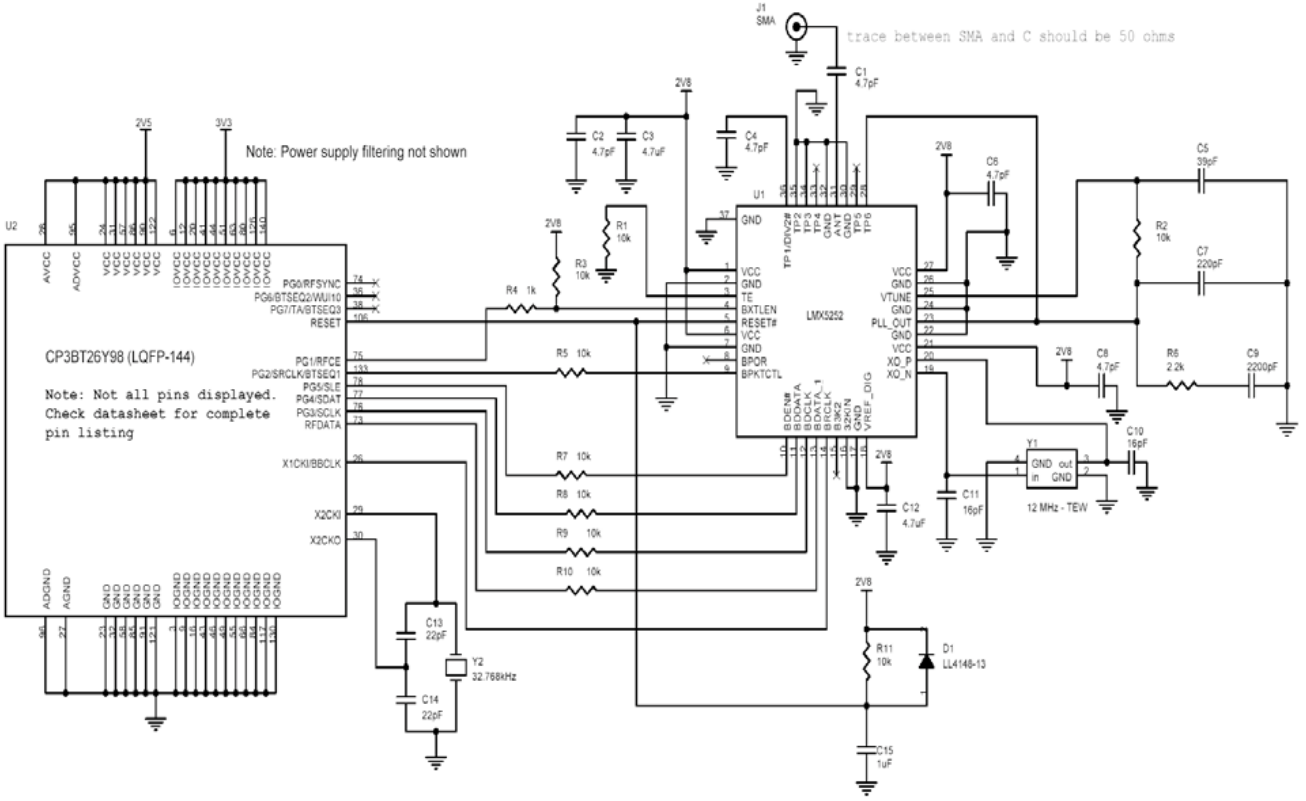


Figure 22. Reference Schematic with CP3BT26 Base Band

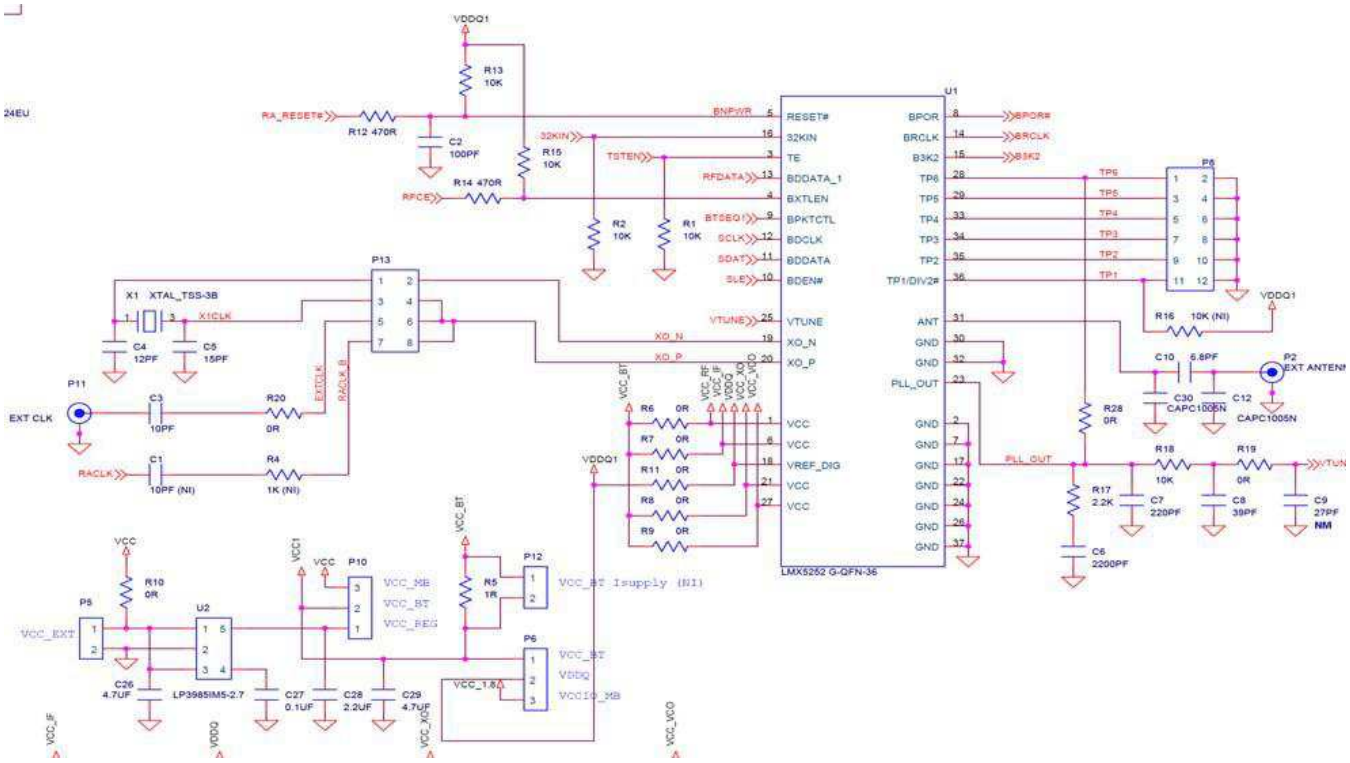


Figure 23. Tucson Reference Schematic

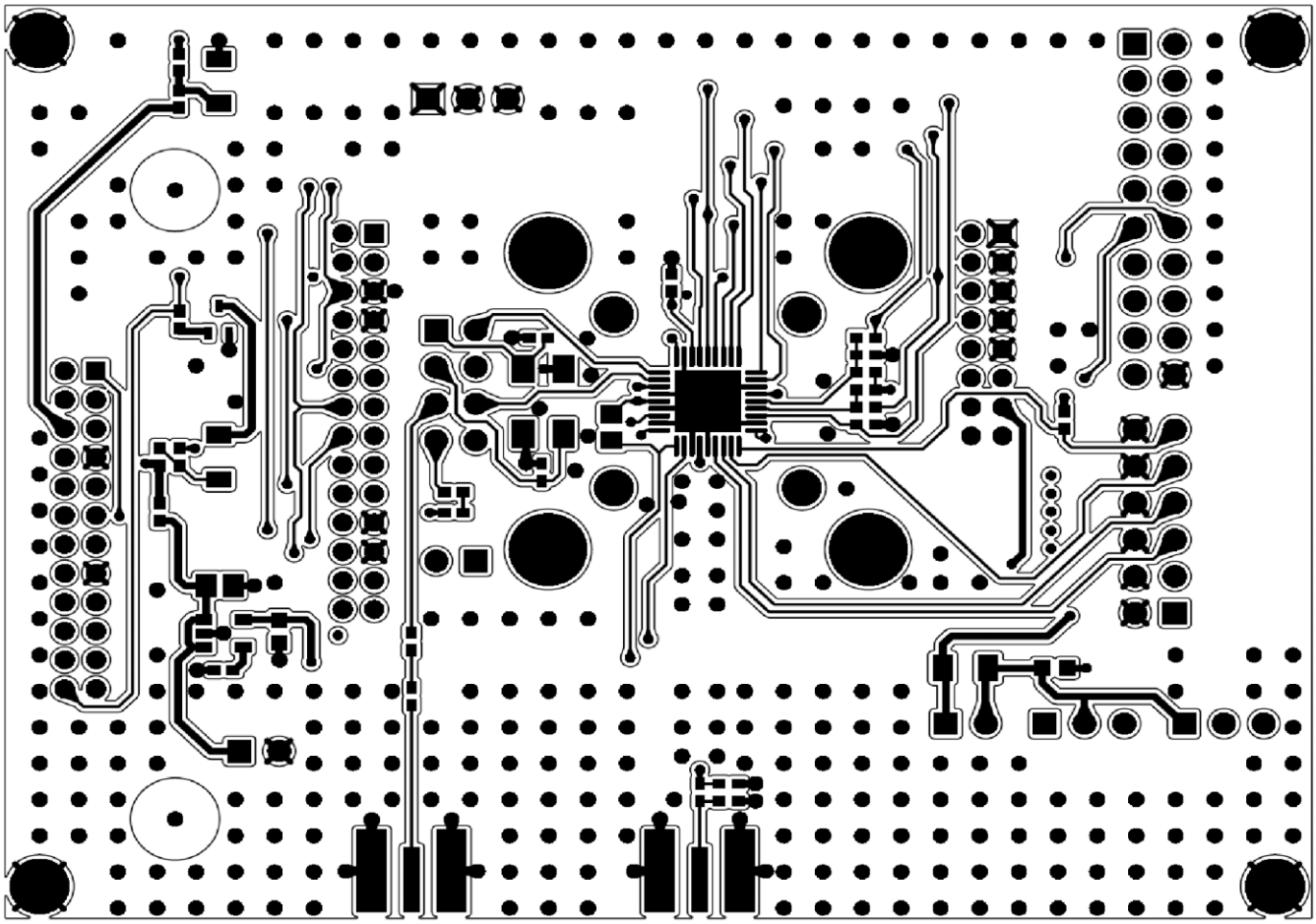


Figure 24. Tucson Reference Layout

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REVISION HISTORY

Changes from Original (December 2004) to Revision A **Page**

- Added all the revision histories that were at the end of this data sheet. 34
- Added 0.1 (April 2003) First draft of advance datasheet. 34
- Added 0.2 (June 2003) This update includes modifications to electrical specs, minor corrections, and the addition of the Physical Dimensions section. 34
- Added 0.3 (July 2003) Update of physical dimensions. Changed document status from Advance Information to Preliminary. 34
- Added 0.4 (August 2003) Updates in Tables 2, 4, 5, and 6. New subsections added to Functional Description. Addition of Programming Description section. 34
- Added 0.5 (March 2004) Updates to Application diagram, Register description, Pin description, Crystal specifications and Operating conditions 34
- Added 0.7 (May 2004) Updates to Applications Diagram, BOM, Selected register description, Register values, Electrical Specifications, and Pin descriptions 34
- Added 0.8 (July - Sept 2004) Addition of reference schematics, Base band RF interface description, typical performance characteristics and new information on crystal tuning Not released 34
- Added 1.0 (December 2004) See Table 21 on page 36 for edits to current revision. 34
- Changed to ordering information – Connections Diagram 34
- Changed B3K2 default to ground – Pin Description 34
- Changed to Tx/Rx impedance, synthesizer lock time, output power, 2nd & 3rd Harmonics, lead soldering temperature, humidity of operation, absolute maximum input power – Electrical Specifications 34
- Added Tx/Rx impedance plots – Typical Performance Characteristics 34
- Added to reg 15 – Register Map 34
- Added Update to loop filter values and new schematic and layout added – Application Diagram Schematics 34

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PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
LMX5252LQ/NOPB	ACTIVE	WQFN	NJJ	36	250	Green (RoHS & no Sb/Br)	CU SN	Level-3-260C-168 HR	-40 to 85	X5252LQ	Samples
LMX5252LQX/NOPB	ACTIVE	WQFN	NJJ	36		TBD	Call TI	Call TI	-40 to 85	X5252LQ	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

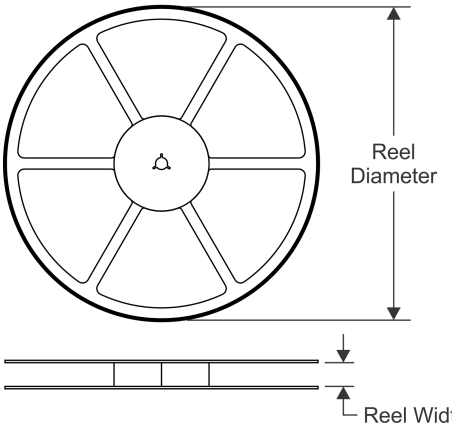
(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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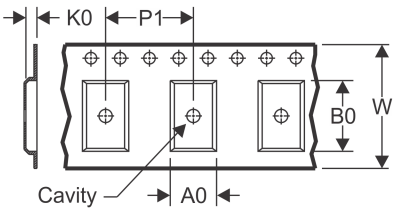
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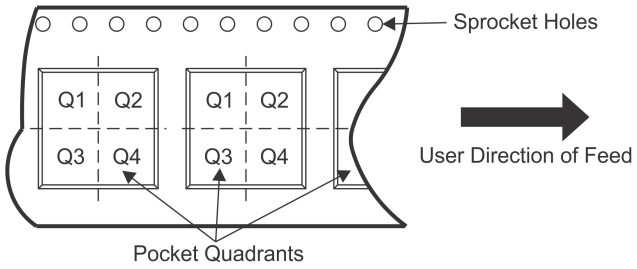


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

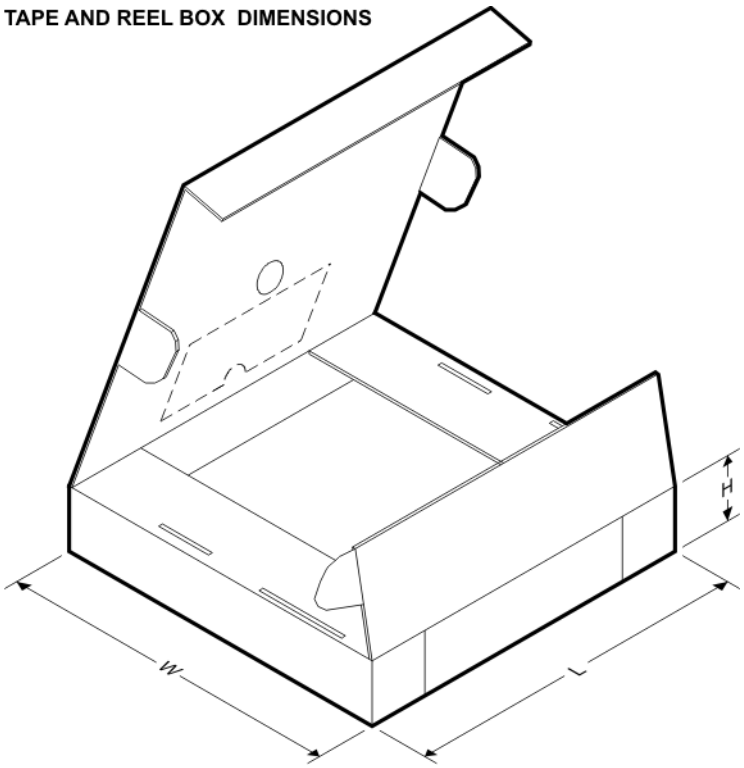
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
LMX5252LQ/NOPB	WQFN	NJJ	36	250	178.0	16.4	6.3	6.3	1.5	12.0	16.0	Q1

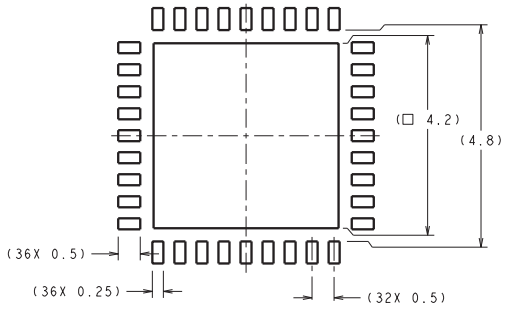
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

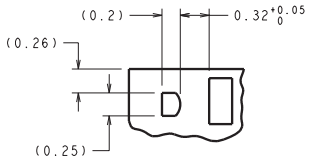
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
LMX5252LQ/NOPB	WQFN	NJJ	36	250	213.0	191.0	55.0

NJJ0036B

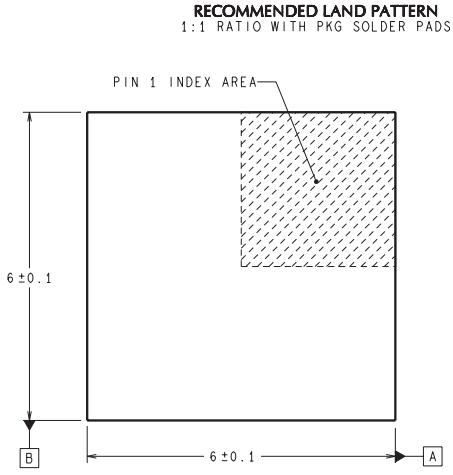


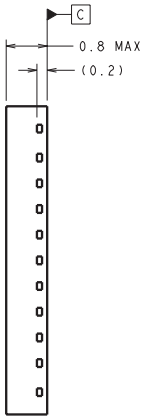
RECOMMENDED LAND PATTERN
1:1 RATIO WITH PKG SOLDER PADS

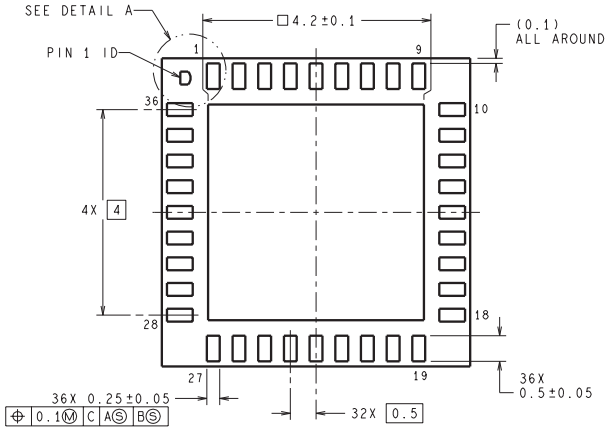
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DETAIL A







LQA36B (Rev A)

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