LMV881 23 MHz Low Power CMOS EMI Hardened Operational Amplifier with 1.8V Logic Shutdown

Check for Samples: LMV881

FEATURES

- **Unless Otherwise Noted, Typical Values at T_A = 25°C, V^+ = 3.3V**
- **Supply Voltage 2.7V to 5.5V**
- **Supply Current 1.65 mA**
- **Shutdown Current 200 pA**
- **Input Offset Voltage 1 mV Max**
- **Input Bias Current 0.1 pA**
- **GBW 23 MHz**
- **EMIRR at 1.8 GHz 105 dB**
- **Input Noise Voltage at 1 kHz 9 nV/√Hz**
- **Slew Rate 12 V/µs**
- **Output Voltage Swing Rail-to-Rail**
- **Output Current Drive 70 mA**
- **Operating Ambient Temperature Range −40°C to 125°C**
- **Space Saving Micro-UQFN Package 1.5 x 1.0 x 0.5 mm**

APPLICATIONS

- **Weight Scale Systems**
- **Filters/Buffers**
- **Medical Diagnosis Equipment**

DESCRIPTION

The LMV881 is a low power CMOS input operational amplifier that provides low input bias currents, a rail to rail output with high output drive capability and a wide temperature range of −40°C to +125°C. Additionally, the LMV881 is EMI hardened to minimize sensitivity to external interference.

The LMV881 has a maximum input offset voltage of 1 mV with an input common-mode voltage range that includes ground. Over an operating supply range from 2.7V to 5.5V, the LMV881 provides a typical PSRR of 110dB and a CMRR of 110dB. This makes the LMV881 ideal for EMI sensitive applications as well as exceptional performance as a robust general purpose part.

The unity gain stable LMV881 features 23 MHz of bandwidth while consuming only 1.65 mA of current. This device also maintains stability for capacitive loads as large as 200 pF.

Typical Application

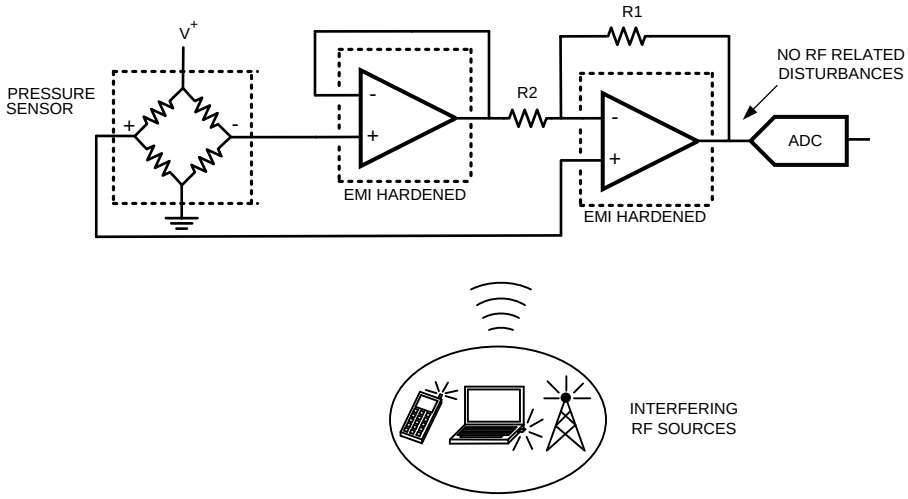

Figure 1. EMI Hardened Sensor Application

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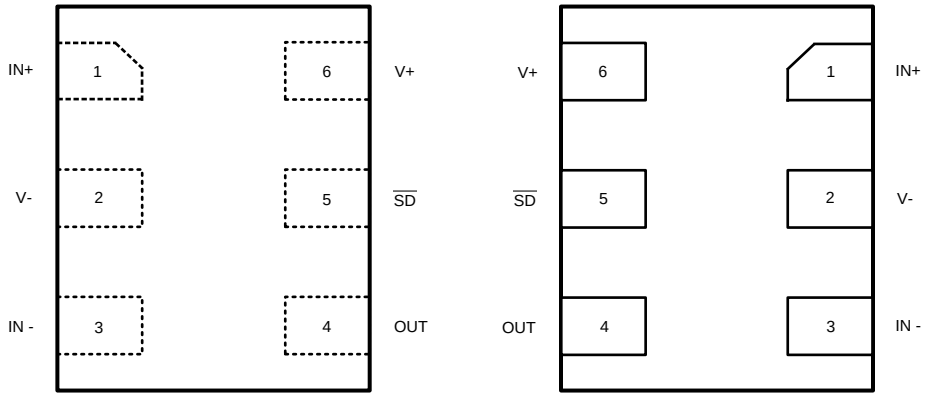
DESCRIPTION (CONTINUED)

LMV881 offers a shutdown pin that can be used to disable the device and reduce the supply current to sub-nanoamp levels. During shutdown, the output is hard-clamped to V- to provide a known output state. The shutdown input thresholds are set for 1.8V logic, regardless of the amplifiers supply voltage. This eliminates the need for additional logic level shifting circuitry or translators.

The LMV881 is offered in the space saving 6-Pin µUQFN package and provides excellent performance and economy in terms of power and space usage.

Connection Diagram



Top View **Bottom View**

6-Pad UQFN Package
See Package Number NKK0006A

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

Absolute Maximum Ratings(1) (2)

ESD Tolerance(3)	Human Body Model	2 kV
	Charge-Device Model	1 kV
	Machine Model	200V
V_{IN} Differential		± Supply Voltage
Supply Voltage ($V_S = V^+ – V^–$)		6V
Voltage at Input/Output Pins		V^+ +0.4V $V^–$ −0.4V
Storage Temperature Range		−65°C to +150°C
Junction Temperature(4)		+150°C
For soldering specifications http://www.ti.com/lit/SNOA549		

(1) Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Operating Ratings indicate conditions for which the device is intended to be functional, but specific performance is not ensured. For specifications and the test conditions, see the Electrical Characteristics Tables.
(2) If Military/Aerospace specified devices are required, please contact the Texas Instruments Sales Office/Distributors for availability and specifications.
(3) Human Body Model, applicable std. MIL-STD-883, Method 3015.7. Machine Model, applicable std. JESD22-A115-A (ESD MM std. of JEDEC) Field-Induced Charge-Device Model, applicable std. JESD22-C101-C (ESD FICDM std. of JEDEC).
(4) The maximum power dissipation is a function of $T_{J(MAX)}$, θ_{JA} and T_A. The maximum allowable power dissipation at any ambient temperature is $P_D = (T_{J(MAX)} - T_A)/ \theta_{JA}$. All numbers apply for packages soldered directly onto a PC board.

Operating Ratings(1)

Temperature Range(2)		−40°C to +125°C
Supply Voltage ($V_S = V^+ – V^–$)		2.7V to 5.5V
Package Thermal Resistance (θ_{JA} (2))	6-Pad µUQFN	335°C/W

(1) Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Operating Ratings indicate conditions for which the device is intended to be functional, but specific performance is not ensured. For specifications and the test conditions, see the Electrical Characteristics Tables.
(2) The maximum power dissipation is a function of $T_{J(MAX)}$, θ_{JA} and T_A. The maximum allowable power dissipation at any ambient temperature is $P_D = (T_{J(MAX)} - T_A)/ \theta_{JA}$. All numbers apply for packages soldered directly onto a PC board.

3.3V Electrical Characteristics[1]

Unless otherwise specified, all limits are specified for T_A = 25°C, V^+ = 3.3V, V^- = 0V, V_{CM} = V^+/2, and R_L =10 kΩ to V^+/2. **Boldface** limits apply at the temperature extremes.

Parameter		Test Conditions	Min[2]	Typ[3]	Max[2]	Units
V_{OS}	Input Offset Voltage[4]			±273	±1000 **±1260**	µV
TCV_{OS}	Input Offset Voltage Temperature Drift[5]			±0.7	±2.6	µV/°C
I_B	Input Bias Current[5]			0.1	30 **500**	pA
I_{OS}	Input Offset Current			1		pA
CMRR	Common-Mode Rejection Ratio[4]	0.2V ≤ V_{CM} ≤ V^+ - 1.2V	77 **76**	93		dB
PSRR	Power Supply Rejection Ratio[4]	2.7V ≤ V^+ ≤ 5.5V, V_{OUT} = 1V	79 **78**	95		dB
EMIRR	EMI Rejection Ratio, IN+ and IN−[6]	V_{RF_PEAK} = 100 mV_P (−20 dBV_P), f = 400 MHz		70		dB
		V_{RF_PEAK} = 100 mV_P (−20 dBV_P), f = 900 MHz		80		
		V_{RF_PEAK} = 100 mV_P (−20 dBV_P), f = 1800 MHz		105		
		V_{RF_PEAK} = 100 mV_P (−20 dBV_P), f = 2400 MHz		110		
CMVR	Input Common-Mode Voltage Range	CMRR ≥ 65 dB	−0.2 **−0.1**		2.2 **2.1**	V
A_{VOL}	Large Signal Voltage Gain[7]	R_L = 2 kΩ V_{OUT} = 0.15V to 1.65V, V_{OUT} = 3.15V to 1.65V	99 **98**	110		dB
		R_L = 10 kΩ V_{OUT} = 0.1V to 1.65V, V_{OUT} = 3.2V to 1.65V	102 **101**	112		
V_{OUT}	Output Voltage Swing High	R_L = 2 kΩ to V^+/2		12	14 **18**	mV from either rail
		R_L = 10 kΩ to V^+/2		3	4 **5**	
	Output Voltage Swing Low	R_L = 2 kΩ to V^+/2		8	12 **16**	
		R_L = 10 kΩ to V^+/2		2	4 **5**	
I_{OUT}	Output Short Circuit Current	Sourcing, V_{OUT} = V_{CM}, V_{IN} = 100 mV	61 **52**	70		mA
		Sinking, V_{OUT} = V_{CM}, V_{IN} = −100 mV	72 **58**	86		
R_{OUT}	Shutdown Output Resistance	V_{SDN} = 0V		8.5		Ohms
V_{OSD}	Shutdown Output Voltage	V_{SDN} = 0V, 200Ω pullup from OUT to V+		134	230	mV

(1) Electrical Table values apply only for factory testing conditions at the temperature indicated. Factory testing conditions result in very limited self-heating of the device such that T_J = T_A. No guarantee of parametric performance is indicated in the electrical tables under conditions of internal self-heating where T_J > T_A.
(2) Limits are 100% production tested at 25°C. Limits over the operating temperature range are specified through correlations using statistical quality control (SQC) method.
(3) Typical values represent the most likely parametric norm as determined at the time of characterization. Actual typical values may vary over time and will also depend on the application and configuration. The typical values are not tested and are not specified on shipped production material.
(4) The typical value is calculated by applying the absolute value transform to the distribution, then taking the statistical average of the resulting distribution.
(5) This parameter is ensured by design and/or characterization and is not tested in production.
(6) The EMI Rejection Ratio is defined as EMIRR = 20log ($V_{RF\_PEAK}/\Delta V_{OS}$).
(7) The specified limits represent the lower of the measured values for each output range condition.

3.3V Electrical Characteristics[1] (continued)

Unless otherwise specified, all limits are specified for T_A = 25°C, V^+ = 3.3V, V^- = 0V, V_{CM} = V^+/2, and R_L =10 kΩ to V^+/2. **Boldface** limits apply at the temperature extremes.

Parameter		Test Conditions	Min[2]	Typ[3]	Max[2]	Units
V_{EN}	Turn-on Voltage[8]			≥ 1	**1.5**	V
	Turn-off Voltage[8]		**0.3**	≤ 0.7		
I_S	Supply Current	Active, V_{SD} > 0.972 V		1.65	2.17 **2.75**	mA
		In Shutdown, V_{SD} < 0.676 V		200		pA
SR	Slew Rate[9]	A_V = +1, V_{OUT} = 1 V_{PP}, 10% to 90%		12		V/µs
GBW	Gain Bandwidth Product			23		MHz
Φ_m	Phase Margin			60		deg
e_n	Input Referred Voltage Noise Density	f = 1 kHz		9		nV/√Hz
		f = 100 kHz		5.3		
i_n	Input Referred Current Noise Density	f = 1 kHz		0.015		pA/√Hz
C_{IN}	Common-Mode Input Capacitance			5		pF
	Differential-Mode Input Capacitance			15		
THD+N	Total Harmonic Distortion + Noise	f = 1 kHz, A_V = 1, BW ≥ 500 kHz		0.02		%

(8) The shutdown logic levels are fixed to match 1.8V logic levels (referenced to V-), and do not change with the total power supply voltage.
(9) Number specified is the slower of positive and negative slew rates.

5V Electrical Characteristics[1]

Unless otherwise specified, all limits are specified for T_A = 25°C, V^+ = 5V, V^- = 0V, V_{CM} = V^+/2, and R_L =10 kΩ to V^+/2. **Boldface** limits apply at the temperature extremes.

Parameter		Test Conditions	Min[2]	Typ[3]	Max[2]	Units
V_{OS}	Input Offset Voltage[4]			±273	±1000 **±1260**	µV
TCV_{OS}	Input Offset Voltage Temperature Drift[5]			±0.7	±2.6	µV/°C
I_B	Input Bias Current[5]			0.1	30 **500**	pA
I_{OS}	Input Offset Current			1		pA
CMRR	Common-Mode Rejection Ratio[4]	0V ≤ V_{CM} ≤ V^+ –1.2V	79 **78**	94		dB
PSRR	Power Supply Rejection Ratio[4]	2.7V ≤ V^+ ≤ 5.5V, V_{OUT} = 1V	79 **78**	95		dB
EMIRR	EMI Rejection Ratio, IN+ and IN−[6]	V_{RF_PEAK} = 100 mV_P (−20 dBV_P), f = 400 MHz		70		dB
		V_{RF_PEAK} = 100 mV_P (−20 dBV_P), f = 900 MHz		80		
		V_{RF_PEAK} = 100 mV_P (−20 dBV_P), f = 1800 MHz		105		
		V_{RF_PEAK} = 100 mV_P (−20 dBV_P), f = 2400 MHz		110		
CMVR	Input Common-Mode Voltage Range	CMRR ≥ 65 dB	−0.2 **−0.1**		3.9 **3.8**	V
A_{VOL}	Large Signal Voltage Gain[7]	R_L = 2 kΩ V_{OUT} = 0.15V to 2.5V, V_{OUT} = 4.85V to 2.5V	102 **101**	110		dB
		R_L = 10 kΩ V_{OUT} = 0.1V to 2.5V, V_{OUT} = 4.9V to 2.5V	102 **101**	113		
V_{OUT}	Output Voltage Swing High	R_L = 2 kΩ to V^+/2		13	15 **19**	mV from either rail
		R_L = 10 kΩ to V^+/2		3	4 **5**	
	Output Voltage Swing Low	R_L = 2 kΩ to V^+/2		10	14 **18**	
		R_L = 10 kΩ to V^+/2		3	4 **5**	
I_{OUT}	Output Short Circuit Current	Sourcing, V_{OUT} = V_{CM}, V_{IN} = 100 mV	90 **86**	110		mA
		Sinking, V_{OUT} = V_{CM}, V_{IN} = −100 mV	90 **86**	110		
R_{OUT}	Shutdown Output Resistance	V_{SDN} = 0V		7		Ohms
V_{OSD}	Shutdown Output Voltage	V_{SDN} = 0V, 200Ω pullup from OUT to V+		169	260	mV

(1) Electrical Table values apply only for factory testing conditions at the temperature indicated. Factory testing conditions result in very limited self-heating of the device such that T_J = T_A. No guarantee of parametric performance is indicated in the electrical tables under conditions of internal self-heating where T_J > T_A.
(2) Limits are 100% production tested at 25°C. Limits over the operating temperature range are specified through correlations using statistical quality control (SQC) method.
(3) Typical values represent the most likely parametric norm as determined at the time of characterization. Actual typical values may vary over time and will also depend on the application and configuration. The typical values are not tested and are not specified on shipped production material.
(4) The typical value is calculated by applying the absolute value transform to the distribution, then taking the statistical average of the resulting distribution.
(5) This parameter is ensured by design and/or characterization and is not tested in production.
(6) The EMI Rejection Ratio is defined as EMIRR = 20log ($V_{RF\_PEAK}/\Delta V_{OS}$).
(7) The specified limits represent the lower of the measured values for each output range condition.

5V Electrical Characteristics[1] (continued)

Unless otherwise specified, all limits are specified for T_A = 25°C, V^+ = 5V, V^- = 0V, V_{CM} = V^+/2, and R_L =10 kΩ to V^+/2. **Boldface** limits apply at the temperature extremes.

Parameter		Test Conditions	Min[2]	Typ[3]	Max[2]	Units
V_{EN}	Turn-on Voltage[8]			≥ 1	**1.5**	V
	Turn-off Voltage[8]		**0.3**	≤ 0.7		
I_S	Supply Current	V_{SD}> 0.972 V		1.9	2.45 **2.95**	mA
		In Shutdown, V_{SD}< 0.676 V		200		pA
SR	Slew Rate[9]	A_V = +1, V_{OUT} = $2V_{PP}$, 10% to 90%		12		V/µs
GBW	Gain Bandwidth Product			23		MHz
Φ_m	Phase Margin			61		deg
e_n	Input Referred Voltage Noise Density	f = 1 kHz		9		nV/$\sqrt{Hz}$
		f = 100 kHz		5.5		
i_n	Input Referred Current Noise Density	f = 1 kHz		0.015		pA/$\sqrt{Hz}$
C_{IN}	Common-Mode Input Capacitance			5		pF
	Differential-Input Capacitance			15		
THD+N	Total Harmonic Distortion + Noise	f = 1 kHz, A_V= 1, BW ≥ 500 kHz		0.02		%

(8) The shutdown logic levels are fixed to match 1.8V logic levels (referenced to V-), and do not change with the total power supply voltage.
(9) Number specified is the slower of positive and negative slew rates.

Typical Performance Characteristics

At T_A = 25°C, V^+ = 5V, V^- = 0V, V_{CM} = V^+/2, and R_L =10 kΩ to V^+/2, unless otherwise specified.

Input Bias Current vs. V_{CM} at 25°C

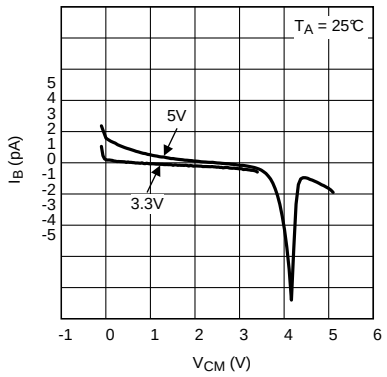


Figure 2.

Input Bias Current vs. V_{CM} at 85°C

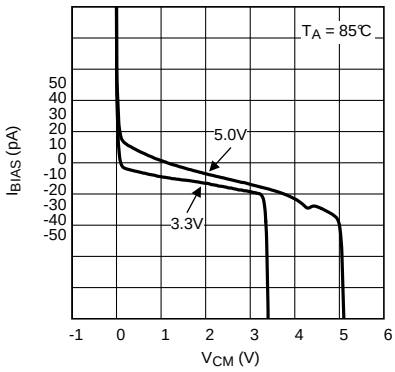


Figure 3.

Input Bias Current vs. V_{CM} at 125°C

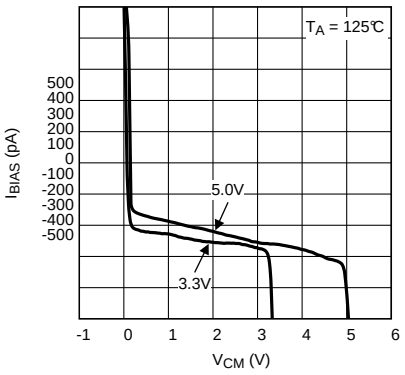


Figure 4.

Supply Current vs. Supply Voltage

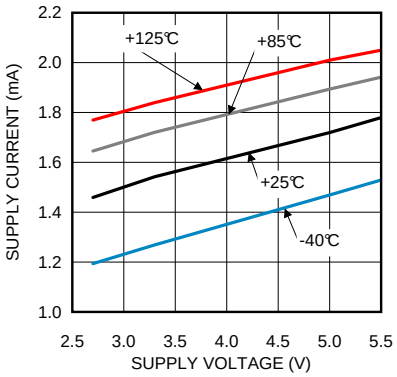


Figure 5.

Output Swing High vs. Supply Voltage R_L = 2 kΩ

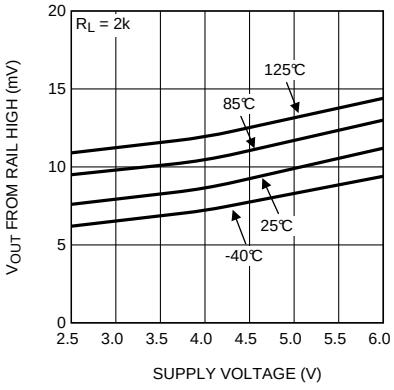


Figure 6.

Output Swing High vs. Supply Voltage R_L = 10 kΩ

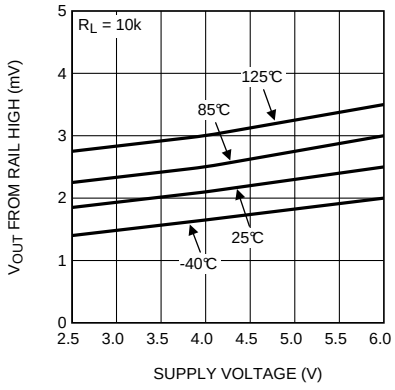


Figure 7.

Typical Performance Characteristics (continued)

At T_A = 25°C, V^+ = 5V, V^- = 0V, V_{CM} = V^+/2, and R_L =10 kΩ to V^+/2, unless otherwise specified.

Output Swing Low vs. Supply Voltage R_L = 2 kΩ

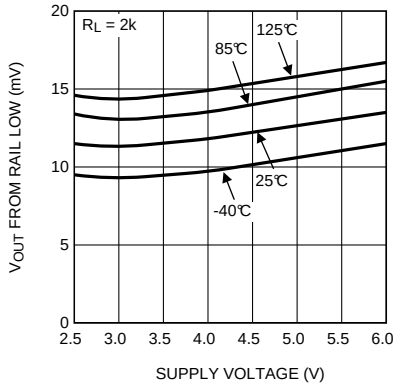


Figure 8.

Output Swing Low vs. Supply Voltage R_L = 10 kΩ

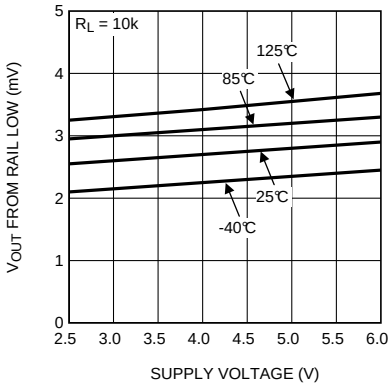


Figure 9.

Output Voltage Swing vs. Load Current at 3.3V

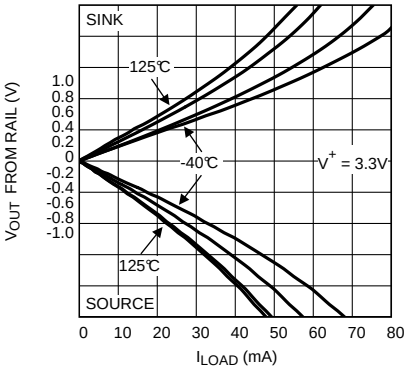


Figure 10.

Output Voltage Swing vs. Load Current at 5V

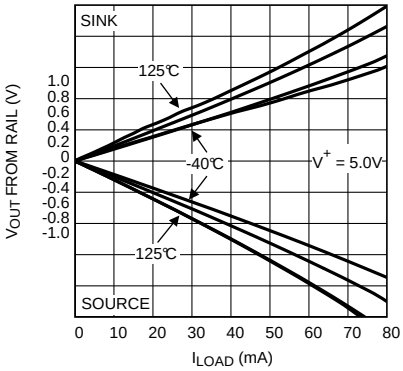


Figure 11.

Open Loop Gain vs. Capacitive Load at 3.3V

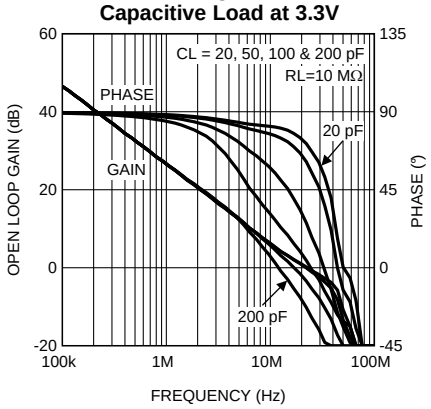


Figure 12.

Open Loop Gain vs. Capacitive Load at 5V

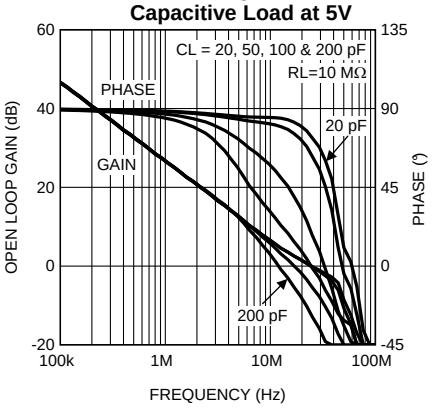


Figure 13.

Typical Performance Characteristics (continued)

At T_A = 25°C, V^+ = 5V, V^- = 0V, V_{CM} = V^+/2, and R_L =10 kΩ to V^+/2, unless otherwise specified.

PSRR vs. Frequency

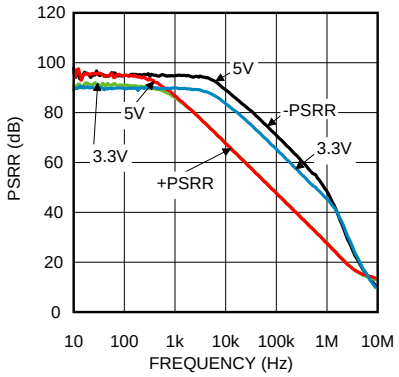


Figure 14.

CMRR vs. Frequency

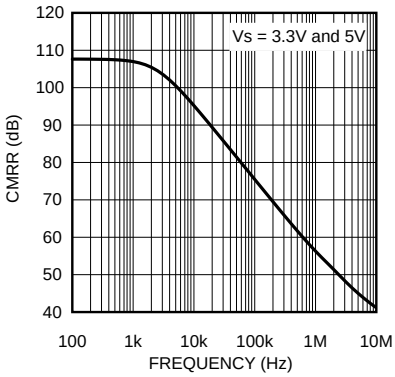


Figure 15.

Large Signal Step Response at V_S = 3.3V

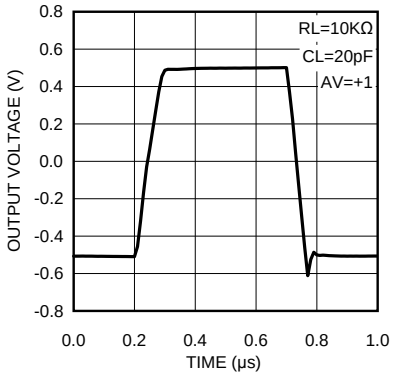


Figure 16.

Large Signal Step Response at V_S = 5V

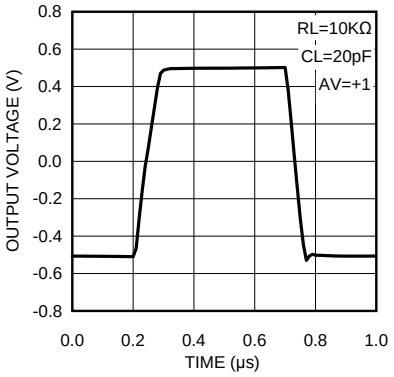


Figure 17.

Turn-on Time vs Supply Voltage

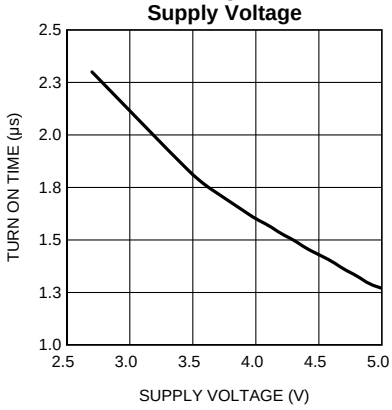


Figure 18.

Slew Rate vs. Supply Voltage

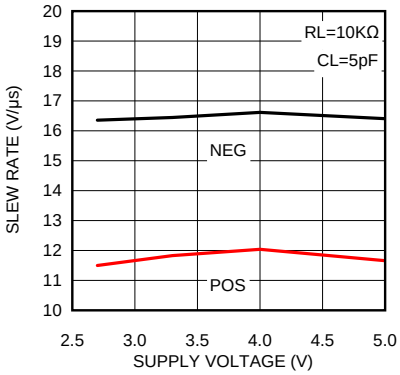


Figure 19.

Typical Performance Characteristics (continued)

At T_A = 25°C, V^+ = 5V, V^- = 0V, V_{CM} = V^+/2, and R_L =10 kΩ to V^+/2, unless otherwise specified.

Input Voltage Noise vs. Frequency

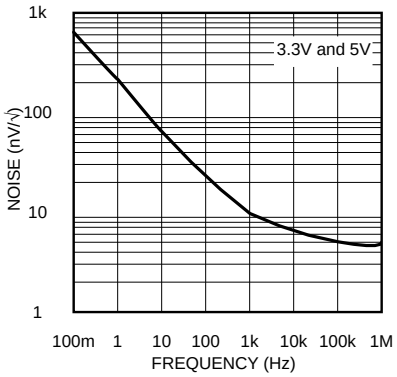


Figure 20.

THD+N vs. Frequency

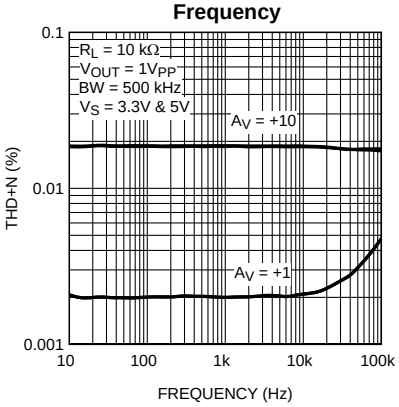


Figure 21.

THD+N vs. Amplitude

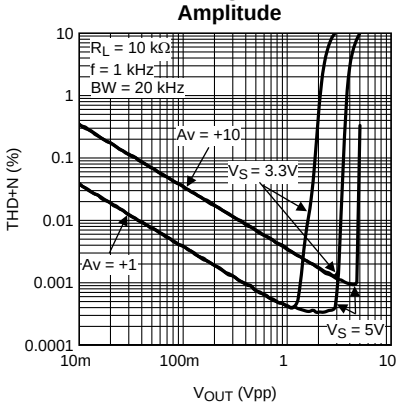


Figure 22.

EMIRR IN+ vs. Power at 400 MHz

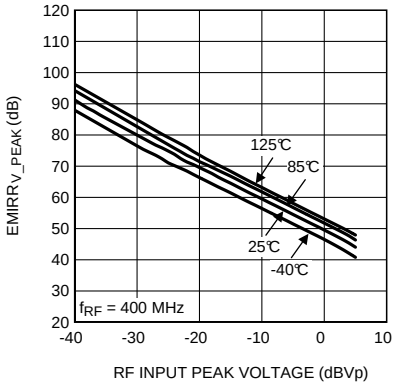


Figure 23.

EMIRR IN+ vs. Power at 900 MHz

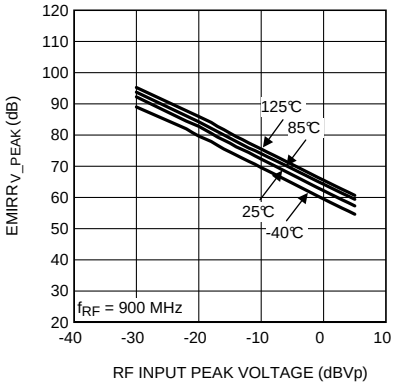


Figure 24.

EMIRR IN+ vs. Power at 1800 MHz

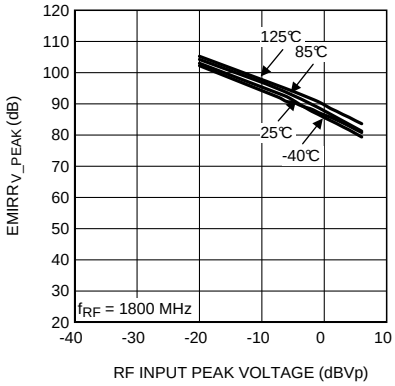


Figure 25.

Typical Performance Characteristics (continued)

At T_A = 25°C, V^+ = 5V, V^- = 0V, V_{CM} = V^+/2, and R_L =10 kΩ to V^+/2, unless otherwise specified.

EMIRR IN+ vs. Power at 2400 MHz

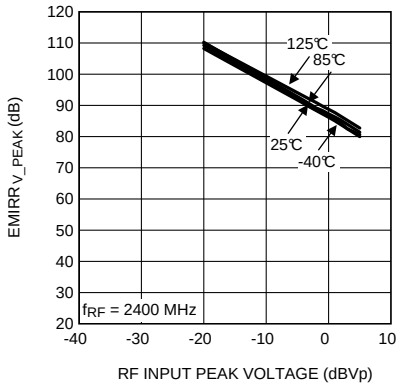


Figure 26.

EMIRR IN+ vs. Frequency

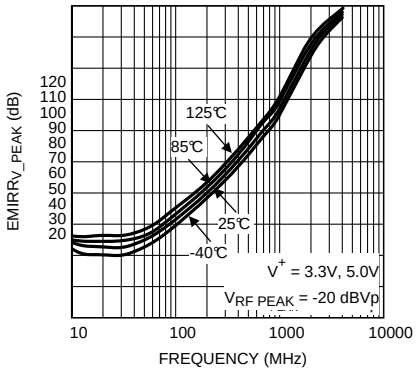


Figure 27.

APPLICATION INFORMATION

INTRODUCTION

The LMV881 is an operational amplifier with low offset, low noise and a high current rail-to-rail output. These specifications make the LMV881 great choices for medical and instrumentation applications such as diagnosis equipment and power line monitors. The low supply current and 1.8V shutdown logic is perfect for battery powered equipment. The small package make this device a perfect choice for portable electronics.

Additionally, the EMI hardening makes the LMV881 a must for applications that are exposed to Radio Frequency (RF) signals such as the signals transmitted by mobile phones or wireless computer peripherals. The LMV881 will effectively reduce disturbances caused by RF signals to a level that will be hardly noticeable. This again reduces the need for additional filtering and shielding. Using this EMI resistant op amp will thus reduce the number of components and space needed for applications that are affected by EMI, and will help applications, not yet identified as possible EMI sensitive, to be more robust for EMI.

SHUTDOWN MODE

To conserve battery life in portable applications, the LMV881 can be disabled when the shutdown pin voltage is pulled low. The shutdown pin is designed for 1.8V logic levels, with thresholds independent of total supply voltage.

In shutdown mode, the amplifier is disabled and the output is hard-clamped by an internal MOSFET to V− to provide a known output state. Care must be taken not to exceed the maximum output sinking current (specified in the electrical table) during shutdown.

The shutdown pin input thresholds are referenced to the V- pin, and may need to be level shifted in split supply applications. Continuous voltages between 0.9V and 1.1V on the shutdown pins should be avoided to prevent excessive supply current draw due to internal shoot-through currents.

The shutdown pin cannot be left unconnected. In case shut down operation is not needed, the shutdown pin should be connected to V+ for normal operation. Leaving the shutdown pin floating will result in an undefined operation modes, either shutdown or active, or even oscillating between the two modes.

INPUT CHARACTERISTICS

The input common mode voltage range of the LMV881 includes ground, and can even sense well below ground. The CMRR level does not degrade for input levels up to 1.2V below the positive supply voltage. For a supply voltage of 5V, the maximum voltage that should be applied to the input for best CMRR performance is thus 3.8V.

When not configured as unity gain, this input limitation will usually not degrade the effective signal range. The output is rail-to-rail and therefore will introduce no limitations to the signal range.

The typical offset is only 70 µV and the TCV_{OS} is 0.7 µV/°C, placing the specifications close to that of precision op amps.

INPUT CAPACITANCE

The LMV881's input capacitance is larger than most typical op-amps due to the internal EMIRR circuitry. The differential mode capacitance (capacitance between the two input pins) is about 15pF. The common mode capacitance (“stray” input capacitance) is about 5pF on each input pin to the supplies. This extra input capacitance will cause peaking to occur with source impedances above 10KΩ. The effect of source resistance on the peaking is shown in Figure 28 below, where the source resistance is effectively the value of R_F.

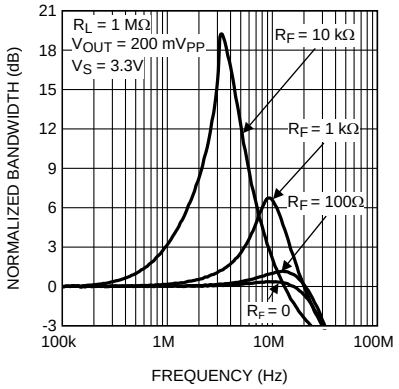


Figure 28. Effect of Source Resistance on Peaking

The 15pF differential mode capacitance mostly cancels due to the feedback bootstrapping effect at lower frequencies, but there still remains about 8pF of equivalent capacitance on each pin as seen by the circuit. The designer should be aware of this capacitance and make the appropriate adjustments to their circuit.

OUTPUT CHARACTERISTICS

During shutdown, the output is hard-clamped to V- with a resistance of just a few ohms.

In normal operation, the output is rail-to-rail. When loading the output with a 10 kΩ resistor the maximum swing of the output is typically 3 mV from the positive and negative rail.

The output of the LMV881 can typically drive peak currents up to 70 mA at 3.3V, and even up to 110 mA at 5V. However, power dissipation in small packages can become an issue at high drive currents.

The LMV881 can be connected as a non-inverting unity gain amplifier (“buffer”). This configuration is the most sensitive to capacitive loading. The combination of a capacitive load placed at the output of an amplifier along with the amplifier’s output impedance creates a phase lag, which reduces the phase margin of the amplifier. If the phase margin is significantly reduced, the response will be under damped which causes peaking in the transfer and, when there is too much peaking, the op amp might start oscillating.

The LMV881 can directly drive capacitive loads up to 200 pF without any stability issues. In order to drive heavier capacitive loads, an isolation resistor, R_{ISO}, should be used, as shown in Figure 29. By using this isolation resistor, the capacitive load is isolated from the amplifier’s output, and hence, the pole caused by C_L is no longer in the feedback loop. The larger the value of R_{ISO}, the more stable the amplifier will be. If the value of R_{ISO} is sufficiently large, the feedback loop will be stable, independent of the value of C_L. However, larger values of R_{ISO} result in reduced output swing and reduced output current drive.

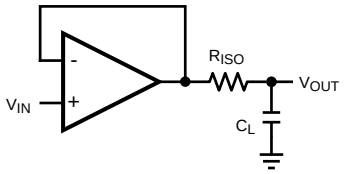


Figure 29. Isolating Capacitive Load

A resistor value of around 50Ω would be sufficient. As an example some values are given in the following table, for 5V and an open loop gain of 111 dB.

C_{LOAD}	R_{ISO}
300 pF	62Ω
400 pF	55Ω
500 pF	50Ω

When increasing the closed-loop gain the capacitive load can be increased even further. With a closed loop gain of 2 and a 27Ω isolation resistor, the load can be 1 nF

EMIRR

With the increase of RF transmitting devices in the world, the electromagnetic interference (EMI) between those devices and other equipment becomes a bigger challenge. The LMV881 is a EMI hardened op amp which is specifically designed to overcome electromagnetic interference. Along with EMI hardened op amps, the EMIRR parameter is introduced to unambiguously specify the EMI performance of an op amp. This section presents an overview of EMIRR. A detailed description on this specification for EMI hardened op amps can be found in Application Note AN-1698.

The dimensions of an op amp IC are relatively small compared to the wavelength of the disturbing RF signals. As a result, the op amp itself will hardly receive any disturbances. The RF signals interfering with the op amp are dominantly received by the PCB and wiring connected to the op amp. The received RF signals on the pins of the op amp can be represented by voltages and currents. This representation significantly simplifies the unambiguous measurement and specification of the EMI performance of an op amp.

RF signals interfere with op amps via the non-linearity of the op amp circuitry. This non-linearity results in the detection of the so called out-of-band signals. The obtained effect is that the amplitude modulation of the out-of-band signal is downconverted into the base band. This base band can easily overlap with the band of the op amp circuit. As an example Figure 30 depicts a typical output signal of a unity-gain connected op amp in the presence of an interfering RF signal. Clearly the output voltage varies in the rhythm of the on-off keying of the RF carrier.

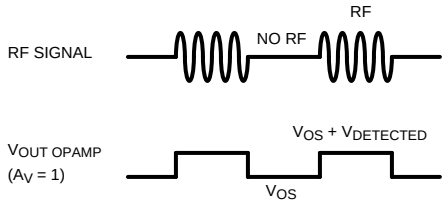


Figure 30. Offset Voltage Variation Due to an Interfering RF Signal

EMIRR Definition

To identify EMI hardened op amps, a parameter is needed that quantitatively describes the EMI performance of op amps. A quantitative measure enables the comparison and the ranking of op amps on their EMI robustness. Therefore the EMI Rejection Ratio (EMIRR) is introduced. This parameter describes the resulting input-referred offset voltage shift of an op amp as a result of an applied RF carrier (interference) with a certain frequency and level. The definition of EMIRR is given by:

$$EMIRR_{V_{RF\_PEAK}} = 20 \log \left(\frac{V_{RF\_PEAK}}{\Delta V_{OS}} \right)$$

where

- V_{RF_PEAK} is the amplitude of the applied un-modulated RF signal (V)
- ΔV_{OS} is the resulting input-referred offset voltage shift (V) (1)

The offset voltage depends quadratically on the applied RF level, and therefore, the RF level at which the EMIRR is determined should be specified. The standard level for the RF signal is 100 mV_P. Application Note AN-1698 addresses the conversion of an EMIRR measured for an other signal level than 100 mV_P. The interpretation of the EMIRR parameter is straightforward. When two op amps have EMIRRs which differ by 20 dB, the resulting error signals when used in identical configurations, differs by 20 dB as well. So, the higher the EMIRR, the more robust the op amp.

Coupling an RF Signal to the IN+ Pin

Each of the op amp pins can be tested separately on EMIRR. In this section the measurements on the IN+ pin (which, based on symmetry considerations, also apply to the IN- pin) are discussed. In Application Note AN-1698 the other pins of the op amp are treated as well. For testing the IN+ pin the op amp is connected in the unity gain configuration. Applying the RF signal is straightforward as it can be connected directly to the IN+ pin. As a result the RF signal path has a minimum of components that might affect the RF signal level at the pin. The circuit diagram is shown in Figure 31. The PCB trace from RF_{IN} to the IN+ pin should be a 50Ω stripline in order to match the RF impedance of the cabling and the RF generator. On the PCB a 50Ω termination is used. This 50Ω resistor is also used to set the bias level of the IN+ pin to ground level.

For determining the EMIRR, two measurements are needed: one is measuring the DC output level when the RF signal is off; and the other is measuring the DC output level when the RF signal is switched on. The difference of the two DC levels is the output voltage shift as a result of the RF signal. As the op amp is in the unity gain configuration, the input referred offset voltage shift corresponds one-to-one to the measured output voltage shift.

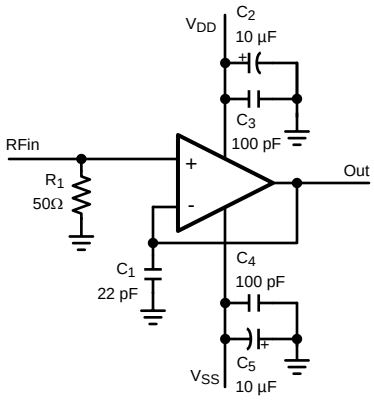


Figure 31. Circuit for Coupling the RF Signal to IN+

Cell Phone Call

The effect of electromagnetic interference is demonstrated in a setup where a cell phone interferes with a pressure sensor application. The application is show in Figure 33.

This application needs two op amps. The op amp configured as a buffer and connected at the negative output of the pressure sensor prevents the loading of the bridge by resistor R2. The buffer also prevents the resistors of the sensor from affecting the gain of the following gain stage. The op amps are placed in a single supply configuration.

The experiment is performed on two different op amps: a typical standard op amp and the LMV881 EMI hardened op amp. A cell phone is placed on a fixed position a couple of centimeters from the op amps in the sensor circuit.

When the cell phone is called, the PCB and wiring connected to the op amps receive the RF signal. Subsequently, the op amps detect the RF voltages and currents that end up at their pins. The resulting effect on the output of the second op amp is shown in Figure 32.

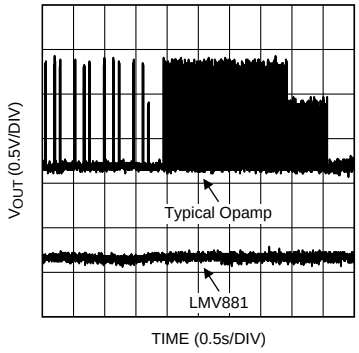


Figure 32. Comparing EMI Robustness

The difference between the two types of op amps is clearly visible. The typical standard op amp has an output shift (disturbed signal) larger than 1V as a result of the RF signal transmitted by the cell phone. The LMV881 EMI hardened op amp does not show any significant disturbances. This means that the RF signal will not disturb the signal entering the ADC when using the LMV881.

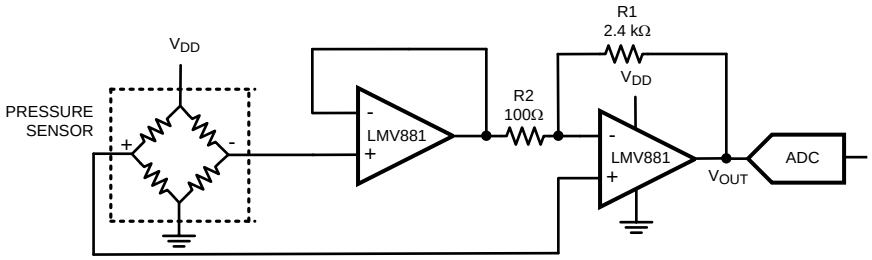


Figure 33. Pressure Sensor Application

DECOUPLING AND LAYOUT

Care must be given when creating a board layout for the op amp. For decoupling the supply lines it is suggested that 10 nF capacitors be placed as close as possible to the op amp. For single supply, place a capacitor between V^+ and V^-. For dual supplies, place one capacitor between V^+ and the board ground, and a second capacitor between ground and V^-.

Even with the LMV881 inherent hardening against EMI, it is still recommended to keep the input traces short and as far as possible from RF sources. Then the RF signals entering the chip are as low as possible and the remaining EMI can be almost, completely eliminated in the chip by the EMI reducing features of the LMV881 . Most of the EMI will be shunted out to the supply pins, so the supply pins should have bypassing and grounding suitable well up into the gigahertz range. A small 100pF RF grade capacitor directly from the supply pin to the nearest suitable RF ground is recommended.

LOAD CELL SENSOR APPLICATION

The LMV881 can be used for weight measuring system applications which use a load cell sensor. Examples of such systems are: bathroom weight scales, industrial weight scales and weight measurement devices on moving equipment such as forklift trucks.

The following example describes a typical load cell sensor application that can be used as a starting point for many different types of sensors and applications. Applications in environments where EMI may appear would especially benefit from the EMIRR performance of the LMV881 .

Load Cell Characteristics

The load cell used in this example is a Wheatstone bridge. The value of the resistors in the bridge changes when pressure is applied to the sensor. This change of the resistor values will result in a differential output voltage depending on the sensitivity of the sensor, the used supply voltage and the applied pressure. The difference between the output at full scale pressure and the output at zero pressure is defined as the span of the load cell. A typical value for the span is 10 mV/V.

The circuit configuration should be chosen such that loading of the sensor is prevented. Loading of the resistor bridge due to the circuit following the sensor, could result in incorrect output voltages of the sensor.

Load Cell Example

Figure 34 shows a typical schematic for a load cell application. It uses a single supply and has an adjustment for both positive and negative offset of the load cell. An ADC converts the amplified signal to a digital signal.

The op amps A1 and A2 are configured as buffers, and are connected at both the positive and the negative output of the load cell. This is to prevent the loading of the resistor bridge in the sensor by the resistors configuring the differential op amp circuit (op amp A4). The buffers also prevent the resistors of the sensor from affecting the gain of the following gain stage. The third buffer (A3) is used to create a reference voltage, to correct for the offset in the system.

Given the differential output voltage V_{SENSE} of the load cell the output signal of this op amp configuration, V_{OUT}, equals:

$$V_{OUT} = \frac{R3}{R1} \times V_{SENSE} + \left(\frac{R3}{R5} + 1\right) \times V_{REF} - \frac{R3}{R5} \times V_{DD} \quad (2)$$

To align the pressure range with the full range of an ADC the correct gain needs to be set. To calculate the correct gain, the power supply voltage and the span of the load cell are needed. For this example a power supply of 5V is used and the span of the sensor, in this case a 125 kg sensor, is 100 mV. With the configuration as shown in Figure 34, this signal is covering almost the full input range of the ADC. With no weight on the load cell, the output of the sensor and the op amp A4 will be close to 0V. With the full weight on the load cell, the output of the sensor is 100 mV, and will be amplified with the gain from the configuration. In the case of the configuration of Figure 34 the gain is R3/R1 = 5 kΩ/100Ω = 50. This will result in a maximum output of 100 mV x 50 = 5V, which covers the full range of the ADC.

For further processing the digital signal can be processed by a microprocessor following the ADC, this can be used to display or log the weight on the load cell. To get a resolution of 0.5 kg, the LSB of the ADC should be smaller then 0.5 kg/125 kg = 1/1000. A 12-bit ADC would be sufficient as this gives 4096 steps. A 12-bit ADC such as the two channel 12-bit ADC122S021 can be used for this application.

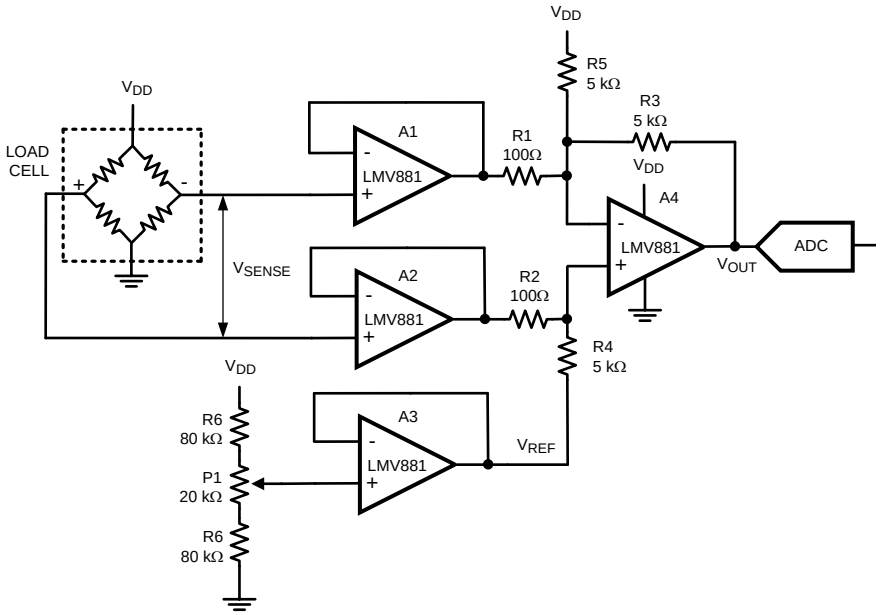


Figure 34. Load Cell Application

EVALUATION BOARD

The LMV881 has a multi-function evaluation board available for ease of bench testing and prototyping. The board has a separate users guide that describes the various configurations. The boards can be ordered through the web or through your local representative.

Device	Package	Evaluation Board Part Number
LMV881	µUQFN	LMV881EVAL

REVISION HISTORY

Changes from Revision A (May 2013) to Revision B	Page
• Changed layout of National Data Sheet to TI format	19

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
LMV881LE/NOPB	ACTIVE	USON	NKK	6	1000	Green (RoHS & no Sb/Br)	SN	Level-1-260C-UNLIM	-40 to 125		Samples
LMV881LEE/NOPB	ACTIVE	USON	NKK	6	250	Green (RoHS & no Sb/Br)	SN	Level-1-260C-UNLIM	-40 to 125		Samples
LMV881LEX/NOPB	ACTIVE	USON	NKK	6	3000	Green (RoHS & no Sb/Br)	SN	Level-1-260C-UNLIM	-40 to 125		Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

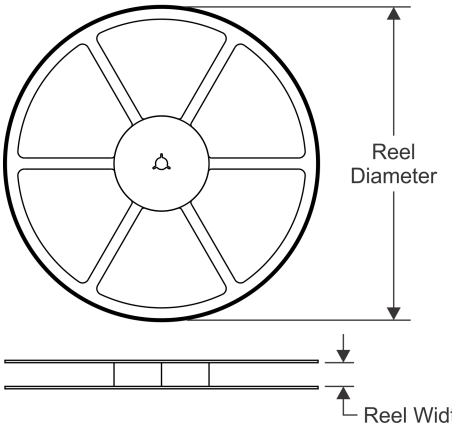
(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

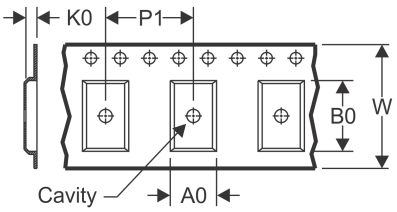
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

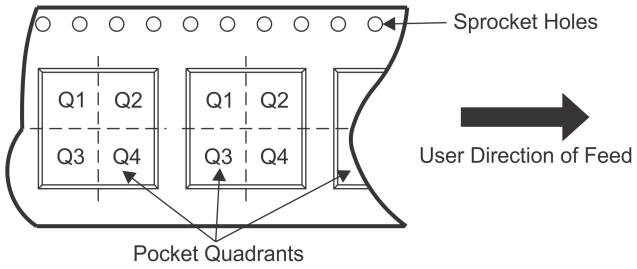


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

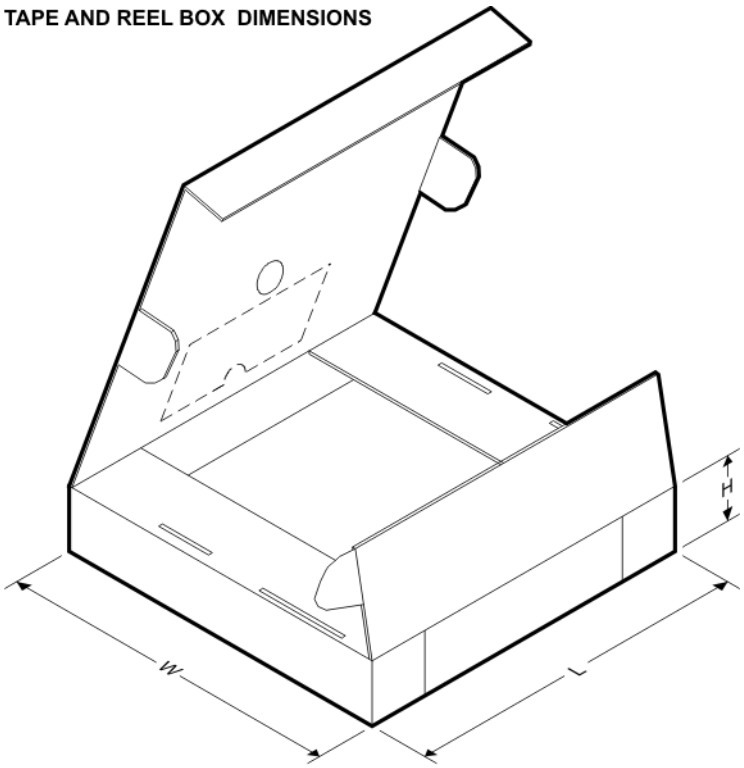
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
LMV881LE/NOPB	USON	NKK	6	1000	180.0	9.5	1.15	1.6	0.75	4.0	8.0	Q1
LMV881LEE/NOPB	USON	NKK	6	250	180.0	9.5	1.15	1.6	0.75	4.0	8.0	Q1
LMV881LEX/NOPB	USON	NKK	6	3000	180.0	9.5	1.15	1.6	0.75	4.0	8.0	Q1

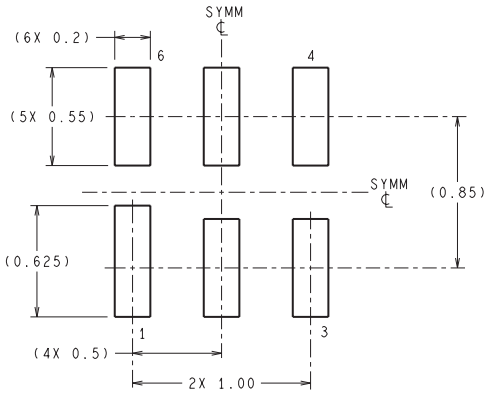
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

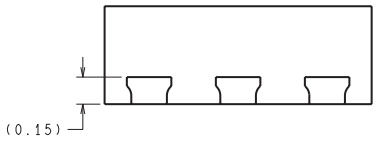
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
LMV881LE/NOPB	USON	NKK	6	1000	184.0	184.0	19.0
LMV881LEE/NOPB	USON	NKK	6	250	184.0	184.0	19.0
LMV881LEX/NOPB	USON	NKK	6	3000	184.0	184.0	19.0

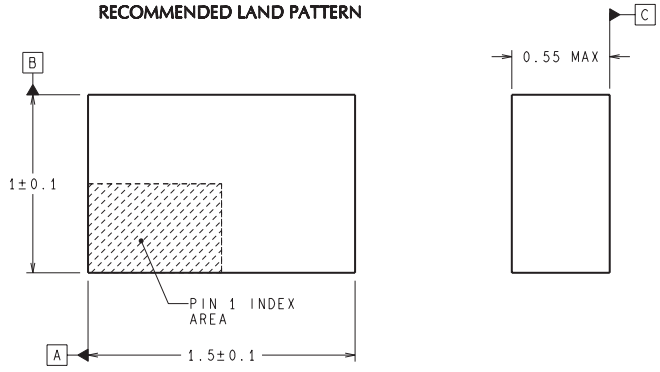
NKK0006A



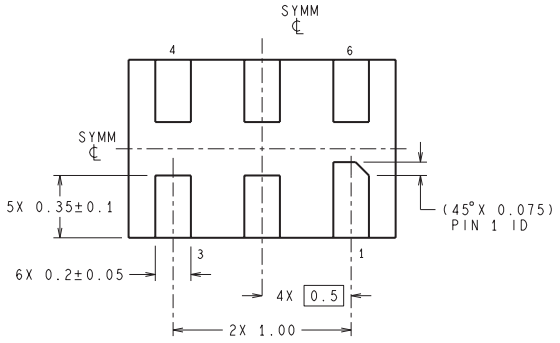
RECOMMENDED LAND PATTERN

DIMENSIONS ARE IN MILIMETERS
DIMENSIONS IN () FOR REFERENCE ONLY





TOP SIDE OF PACKAGE



BOTTOM SIDE OF PACKAGE

LEH06A (Rev A)

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