LMV712-N, LMV712-N-Q1 Low Power, Low Noise, High Output, RRIO Dual Operational Amplifier with Independent Shutdown

Check for Samples: LMV712-N, LMV712-N-Q1

FEATURES

- **(Typical Unless Otherwise Noted)**
- **LMV712-N is available in Automotive AEC-Q100 Grade 1 version**
- **5MHz GBP**
- **Slew Rate 5V/µs**
- **Low Noise 20nV/√Hz**
- **Supply Current 1.22mA/Channel**
- **V_{OS}< 3mV Max**
- **Ensured 2.7V and 5V Specifications**
- **Temperature Range -40°C to 125°C**
- **Rail-to-Rail Inputs and Outputs**
- **Unity Gain Stable**
- **Small Package: 10-Pin WSON, 10-Pin VSSOP and 10-Bump DSBGA**
- **1.5µA Shutdown I_{CC}**
- **2.2µs Turn On**

APPLICATIONS

- **Power Amplifier Control Loop**
- **Cellular Phones**
- **Portable Equipment**
- **Wireless LAN**
- **Radio Systems**
- **Cordless Phones**

DESCRIPTION

The LMV712-N duals are high performance BiCMOS operational amplifiers intended for applications requiring Rail-to-Rail inputs combined with speed and low noise. They offer a bandwidth of 5MHz and a slew rate of 5 V/µs and can handle capacitive loads of up to 200pF without oscillation.

The LMV712-N is ensured to operate from 2.7V to 5.5V and offers two independent shutdown pins. This feature allows disabling of each device separately and reduces the supply current to less than 1µA typical. The output voltage rapidly ramps up smoothly with no glitch as the amplifier comes out of the shutdown mode.

The LMV712-N with the shutdown feature is offered in space saving 10-Bump DSBGA and 10-Pin WSON packages. It is also offered in 10-Pin VSSOP package. These packages are designed to meet the demands of small size, low power, and low cost required by cellular phones and similar battery operated portable electronics.

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Typical Application Circuit

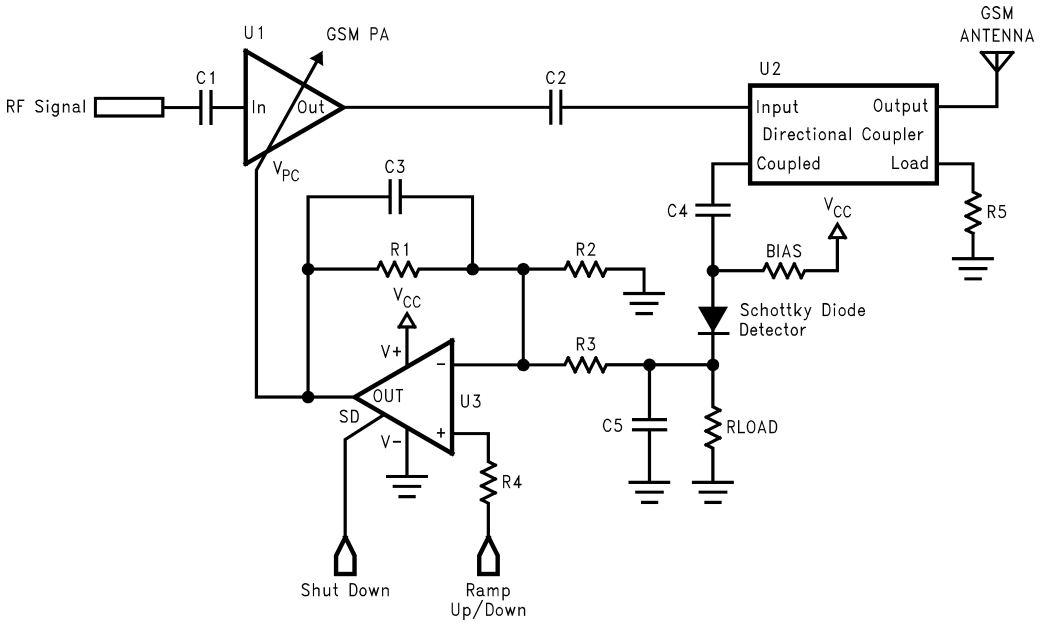

Figure 1. P.A. Control Loop

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

Absolute Maximum Ratings (1)(2)

ESD Tolerance (3)	
Human Body Model	1.5kV
Machine Model	150V
Differential Input Voltage	±Supply Voltage
Voltage at Input/Output Pin	(V^+) +0.4V to (V^-) −0.4V
Supply Voltage $(V^+ - V^-)$	6V
Output Short Circuit V^+	(4)
Output Short Circuit V^-	(4)
Current at Input Pin	±10mA
Current at Output Pin	±50mA
Storage Temp Range	−65°C to 150°C
Junction Temperature T_{JMAX} (5)	150°C
Soldering specification for WSON SnPb:	
Infrared or Convection (20sec)	235°C
Soldering specification for all other packages:	
see product folder at www.ti.com and	
http://www.ti.com/lit/SNOA549	

(1) *Absolute Maximum Ratings* indicate limits beyond which damage to the device may occur. *Operating Ratings* indicate conditions for which the device is intended to be functional, but specific performance is not ensured. For ensured specifications and the test conditions, see the *Electrical Characteristics*.

(2) **If Military/Aerospace specified devices are required, please contact the Texas Instruments Sales Office / Distributors for availability and specifications.**

(3) Human Body Model, applicable std. MIL-STD-883, Method 3015.7. Machine Model, applicable std. JESD22-A115-A (ESD MM std. of JEDEC)Field-Induced Charge-Device Model, applicable std. JESD22-C101-C (ESD FICDM std. of JEDEC).

(4) Shorting circuit output to either V^+ or V^- will adversely affect reliability.

(5) The maximum power dissipation is a function of $T_{J(MAX)}$, θ_{JA}. The maximum allowable power dissipation at any ambient temperature is $P_D = (T_{J(MAX)} - T_A)/ \theta_{JA}$. All numbers apply for packages soldered directly onto a PC Board.

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Recommended Operating Conditions (1)

Supply Voltage	2.7V to 5.5V
Temperature Range	
LMV712	−40°C ≤ T_J ≤ 85°C
LMV712-Q1	−40°C ≤ T_J ≤ 125°C
Thermal Resistance	
10-Pin VSSOP	235°C/W
10-Pin WSON	53.4°C/W
10-Bump DSBGA	196°C/W

(1) *Absolute Maximum Ratings* indicate limits beyond which damage to the device may occur. *Operating Ratings* indicate conditions for which the device is intended to be functional, but specific performance is not ensured. For ensured specifications and the test conditions, see the *Electrical Characteristics*.

2.7V Electrical Characteristics

Unless otherwise specified, all limits ensured for V^+ = 2.7V, V^- = 0V, V_{CM} = 1.35V and T_A = 25°C and R_L > 1MΩ. **Boldface** limits apply at the temperature extremes (−40°C ≤T J ≤85°C for LMV712 and −40°C ≤T J ≤125°C for LMV712-Q1).

Symbol	Parameter	Condition		Min (1)	Typ (2)	Max (1)	Units
V_{OS}	Input Offset Voltage	V_{CM} = 0.85V and V_{CM} = 1.85V	VSSOP WSON		0.4	3 **3.2**	mV
			DSBGA		3	7 **9**	
I_B	Input Bias Current	LMV712			5.5	115 **130**	pA
		LMV712-Q1			5.5	**3740**	
CMRR	Common Mode Rejection Ratio	0V ≤ V_{CM} ≤ 2.7V		50 **45**	75		dB
PSRR	Power Supply Rejection Ratio	2.7V ≤ V^+ ≤ 5V, V_{CM} = 0.85V		70 **68**	90		dB
		2.7V ≤ V^+ ≤ 5V, V_{CM} = 1.85V		70 **68**	90		dB
CMVR	Common Mode Voltage Range	For CMRR ≥ 50dB			−0.3	−0.2	V
				2.9	3		
I_{SC}	Output Short Circuit Current	Sourcing V_O = 0V		15 **12**	25		mA
		Sinking V_O = 2.7V		25 **22**	50		mA
V_O	Output Swing	R_L = 10kΩ to 1.35V		2.62 **2.60**	2.68		V
					0.01	0.12 **0.15**	V
		R_L = 600Ω to 1.35V		2.52 **2.50**	2.55		V
					0.05	0.23 **0.30**	V
V_O(SD)	Output Voltage in Shutdown				10	200	mV
I_S	Supply Current per Channel	On Mode			1.22	1.7 **1.9**	mA
		Shutdown Mode			0.12	1.5 **2.0**	uA

(1) All limits are ensured by testing or statistical analysis.
(2) Typical values represent the most likely parametric norm as determined at the time of characterization. Actual typical values may vary over time and will also depend on the application and configuration. The typical values are not tested and are not ensured on shipped production material.

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2.7V Electrical Characteristics (continued)

Unless otherwise specified, all limits ensured for V^+ = 2.7V, V^- = 0V, V_{CM} = 1.35V and T_A = 25°C and R_L > 1MΩ. **Boldface** limits apply at the temperature extremes (−40°C ≤T J ≤85°C for LMV712 and −40°C ≤T J ≤125°C for LMV712-Q1).

Symbol	Parameter	Condition	Min (1)	Typ (2)	Max (1)	Units
A_{VOL}	Large Signal Voltage Gain	Sourcing R_L = 10kΩ V_O = 1.35V to 2.3V LMV712	80 **76**	115		dB
		LMV712-Q1	**69**	115		
		Sinking R_L = 10kΩ V_O = 0.4V to 1.35V LMV712	80 **76**	113		dB
		LMV712-Q1	**69**	113		
		Sourcing R_L = 600Ω V_O = 1.35V to 2.2V LMV712	80 **76**	97		dB
		LMV712-Q1	**64**	97		
		Sinking R_L = 600Ω V_O = 0.5V to 1.35V LMV712	80 **76**	100		dB
		LMV712-Q1	**62**	100		
V_{SD}	Shutdown Pin Voltage Range	On Mode	2.4 to 2.7	2.0 to 2.7		V
		Shutdown Mode	0 to 0.8	0 to 1		V
GBWP	Gain-Bandwidth Product			5		MHz
SR	Slew Rate	(3)		5		V/µs
φ_m	Phase Margin			60		Deg
e_n	Input Referred Voltage Noise	f = 1kHz		20		nV/√Hz
T_{ON}	Turn-On Time from Shutdown			2.2	4 **4.6**	µs
	Turn-On Time from Shutdown	DSBGA	6 **8**			µs

(3) Number specified is the slower of the positive and negative slew rates.

5V Electrical Characteristics

Unless otherwise specified, all limits ensured for V^+ = 5V, V^- = 0V, V_{CM} = 2.5V and T_A = 25°C and R_L > 1MΩ. **Boldface** limits apply at the temperature extremes.

Symbol	Parameter	Condition		Min (1)	Typ (2)	Max (1)	Units
V_{OS}	Input Offset Voltage	V_{CM} = 0.85V and V_{CM} = 1.85V	VSSOP WSON		0.4	3 **3.2**	mV
			DSBGA		3	7 **9**	
I_B	Input Bias Current	LMV712			5.5	115 **130**	pA
		LMV712-Q1				**3600**	
CMRR	Common Mode Rejection Ratio	0V ≤ V_{CM} ≤ 5V		50 **45**	80		dB

(1) All limits are ensured by testing or statistical analysis.
(2) Typical values represent the most likely parametric norm as determined at the time of characterization. Actual typical values may vary over time and will also depend on the application and configuration. The typical values are not tested and are not ensured on shipped production material.

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5V Electrical Characteristics (continued)

Unless otherwise specified, all limits ensured for V^+ = 5V, V^- = 0V, V_{CM} = 2.5V and T_A = 25°C and R_L > 1MΩ. **Boldface** limits apply at the temperature extremes.

Symbol	Parameter	Condition	Min (1)	Typ (2)	Max (1)	Units
PSRR	Power Supply Rejection Ratio	2.7V ≤ V^+ ≤ 5V, V_{CM} = 0.85V	70 **68**	90		dB
		2.7V ≤ V^+ ≤ 5V, V_{CM} = 1.85V	70 **68**	90		dB
CMVR	Common Mode Voltage Range	For CMRR ≥ 50dB		−0.3	−0.2	V
			5.2	5.3		V
I_{SC}	Output Short Circuit Current	Sourcing V_O = 0V	20 **18**	35		mA
		Sinking V_O = 5V	25 **21**	50		mA
V_O	Output Swing	R_L = 10kΩ to 2.5V	4.92 **4.90**	4.98		V
				0.01	0.12 **0.15**	V
		R_L = 600Ω to 2.5V	4.82 **4.80**	4.85		V
				0.05	0.23 **0.30**	V
V_O(SD)	Output Voltage in Shutdown			10	200	mV
I_S	Supply Current per Channel	On Mode		1.17	1.7 **1.9**	mA
		Shutdown Mode		0.12	1.5 **2.0**	uA
A_{VOL}	Large Signal Voltage Gain	Sourcing R_L = 10kΩ V_O = 2.5V to 4.6V LMV712	80 **76**	130		dB
		LMV712-Q1	**69**	130		
		Sinking R_L = 10kΩ V_O = 0.4V to 2.5V LMV712	80 **76**	130		dB
		LMV712-Q1	**69**	130		
		Sourcing R_L = 600Ω V_O = 2.5V to 4.6V LMV712	80 **76**	110		dB
		LMV712-Q1	**69**	110		
		Sinking R_L = 600Ω V_O = 0.4V to 2.5V LMV712	80 **76**	107		dB
		LMV712-Q1	**69**	107		
V_{SD}	Shutdown Pin Voltage Range	On Mode	4.5 to 5	3.5 to 5		V
		Shutdown Mode	0 to 0.8	0 to 1.5		V
GBWP	Gain-Bandwidth Product			5		MHz
SR	Slew Rate	(3)		5		V/µs
φ_m	Phase Margin			60		Deg
e_n	Input Referred Voltage Noise	f = 1kHz		20		nV/√Hz

(3) Number specified is the slower of the positive and negative slew rates.

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5V Electrical Characteristics (continued)

Unless otherwise specified, all limits ensured for V^+ = 5V, V^- = 0V, V_{CM} = 2.5V and T_A = 25°C and R_L > 1MΩ. **Boldface** limits apply at the temperature extremes.

Symbol	Parameter	Condition	Min (1)	Typ (2)	Max (1)	Units
T_{ON}	Turn-On Time for Shutdown			1.6	4 **4.6**	µs
	Turn-On Time for Shutdown	DSBGA	6 **8**			µs

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Typical Performance Characteristics

Unless otherwise specified, V_S = +5V, single supply, T_A = 25°C.

Supply Current Per Channel vs. Supply Voltage

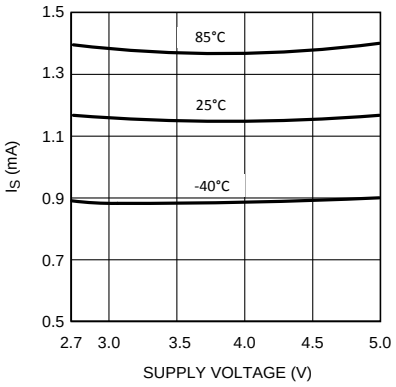

Figure 2.

Supply Current vs. Supply Voltage (Shutdown)

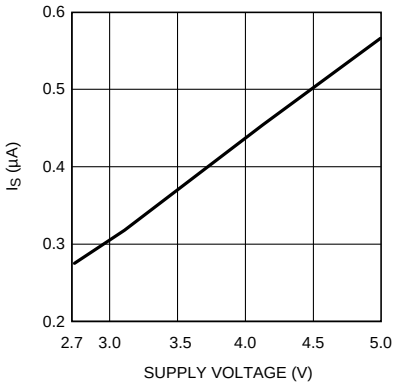

Figure 3.

V_{OS} vs. V_{CM}

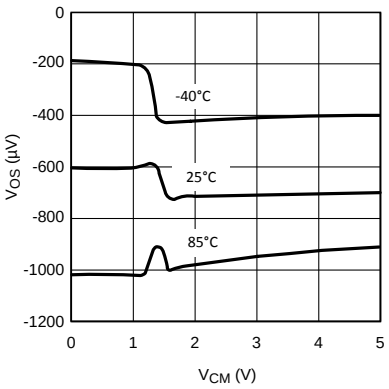

Figure 4.

I_B vs. V_{CM} Over Temp

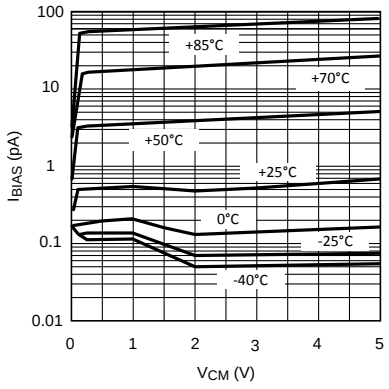

Figure 5.

Output Positive Swing vs. Supply Voltage, R_L = 600Ω

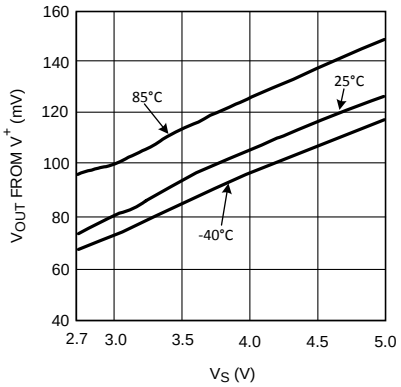

Figure 6.

Output Negative Swing vs. Supply Voltage, R_L = 600Ω

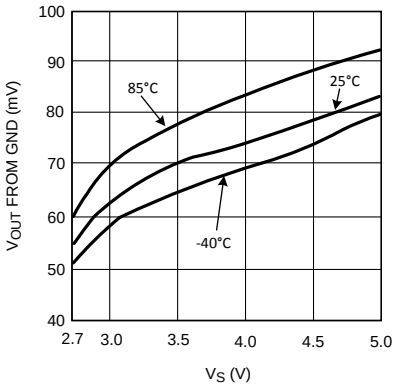

Figure 7.

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Typical Performance Characteristics (continued)

Unless otherwise specified, V_S = +5V, single supply, T_A = 25°C.

Sourcing Current vs. Output Voltage, V_S = 2.7V

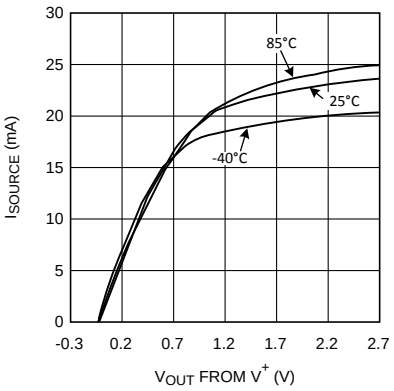

Figure 8.

Sourcing Current vs. Output Voltage, V_S = 5V

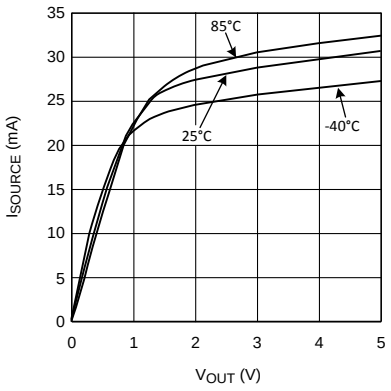

Figure 9.

Sinking Current vs. Output Voltage, V_S = 2.7V

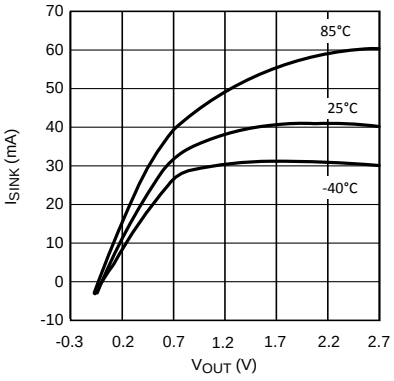

Figure 10.

Sinking Current vs. Output Voltage, V_S = 5V

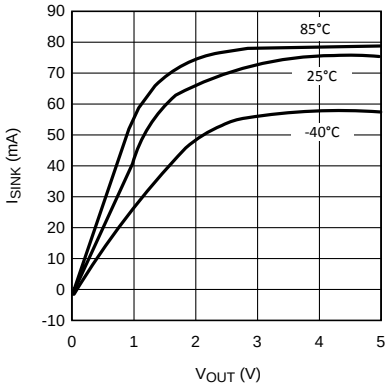

Figure 11.

PSRR vs. Frequency V_S = 2.7V

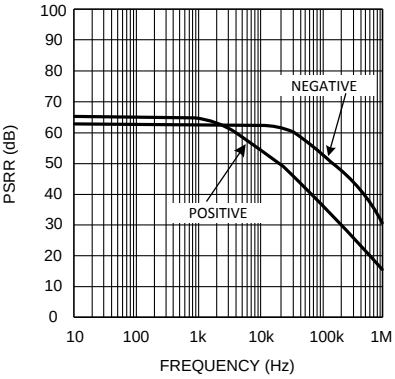

Figure 12.

PSRR vs. Frequency V_S = 5V

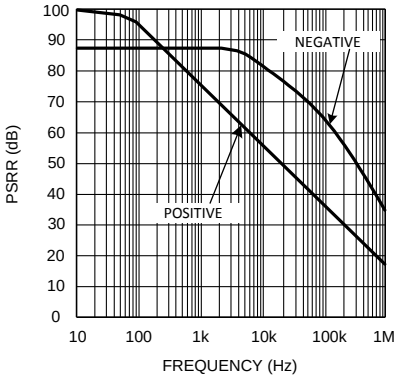

Figure 13.

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Typical Performance Characteristics (continued)

Unless otherwise specified, V_S = +5V, single supply, T_A = 25°C.

CMRR vs. Frequency

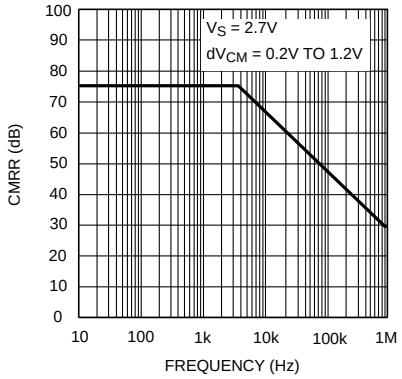

Figure 14.

CMRR vs. Frequency

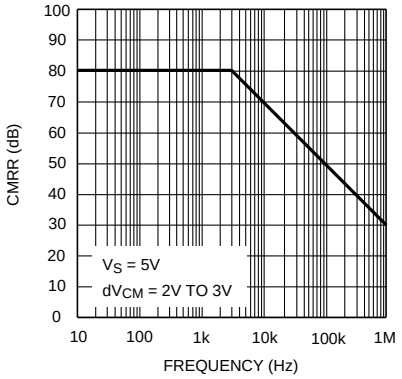

Figure 15.

Open Loop Frequency Response vs. R_L

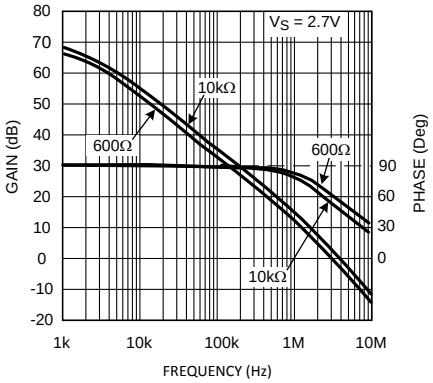

Figure 16.

Open Loop Frequency Response vs. R_L

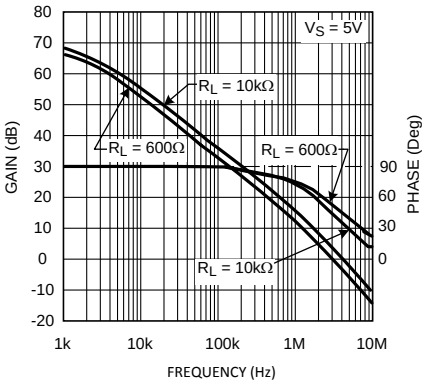

Figure 17.

Open Loop Frequency Response vs. C_L

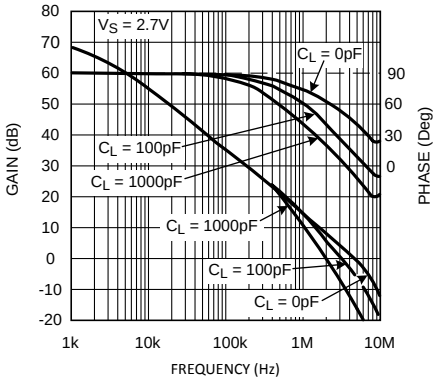

Figure 18.

Open Loop Frequency Response vs. C_L

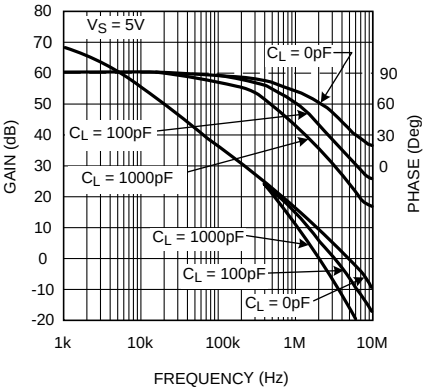

Figure 19.

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Typical Performance Characteristics (continued)

Unless otherwise specified, V_S = +5V, single supply, T_A = 25°C.

Voltage Noise vs. Frequency

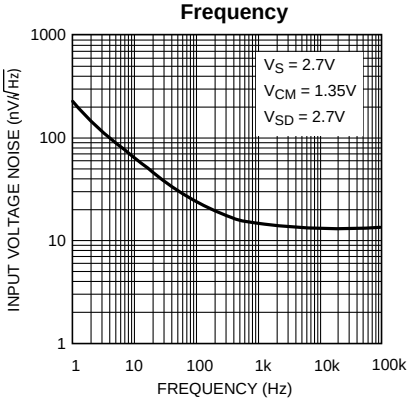

Figure 20.

Voltage Noise vs. Frequency

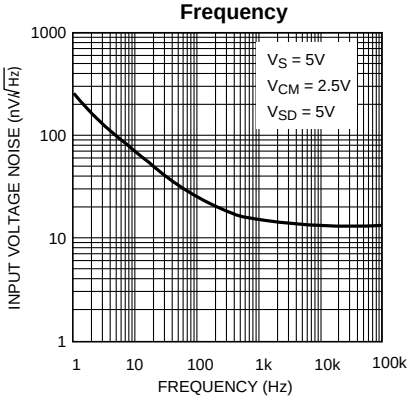

Figure 21.

Non-Inverting Large Signal Pulse Response, V_S = 2.7V

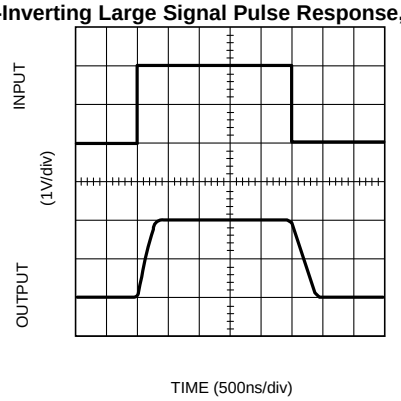

Figure 22.

Non-Inverting Large Signal Pulse Response, V_S = 5V

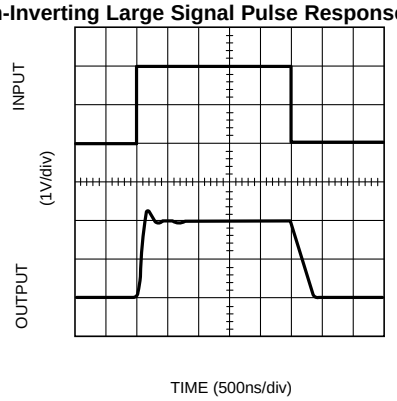

Figure 23.

Non-Inverting Small Signal Pulse Response, V_S = 2.7V

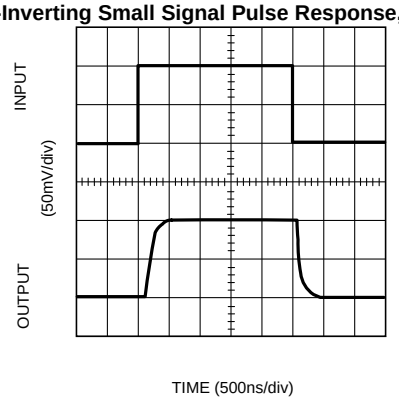

Figure 24.

Non-Inverting Small Signal Pulse Response, V_S = 5V

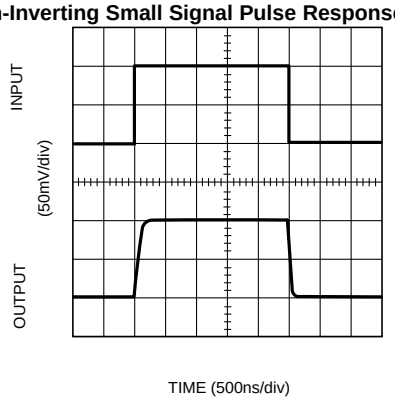

Figure 25.

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Typical Performance Characteristics (continued)

Unless otherwise specified, V_S = +5V, single supply, T_A = 25°C.

Inverting Large Signal Pulse Response, V_S = 2.7V

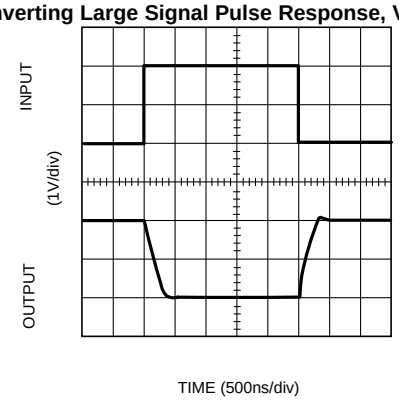

Figure 26.

Inverting Large Signal Pulse Response, V_S = 5V

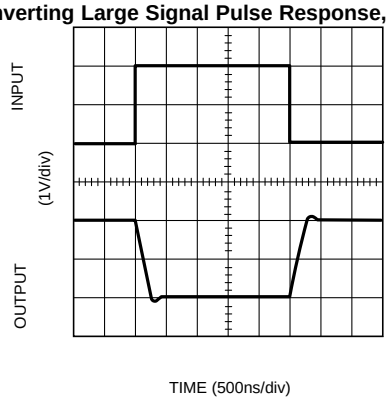

Figure 27.

Inverting Small Signal Pulse Response, V_S = 2.7V

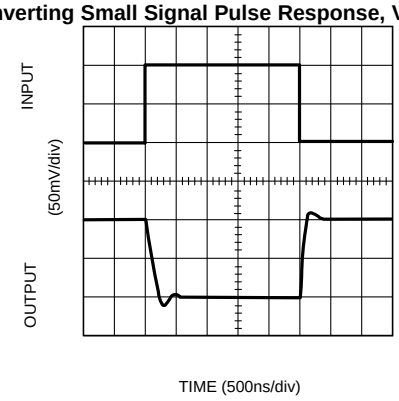

Figure 28.

Inverting Small Signal Pulse Response V_S = 5V

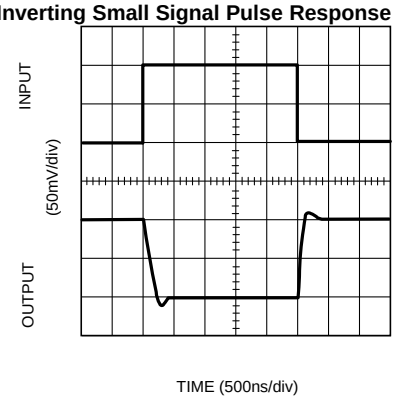

Figure 29.

Turn on Time Response V_S = 5V

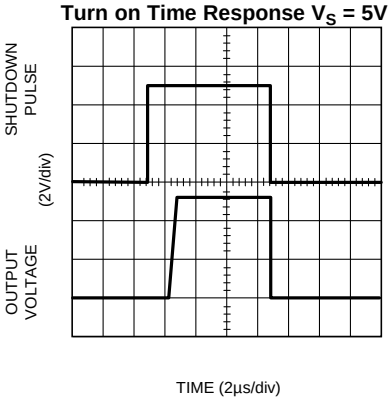

Figure 30.

Input Common Mode Capacitance vs. V_{CM} V_S = 5V

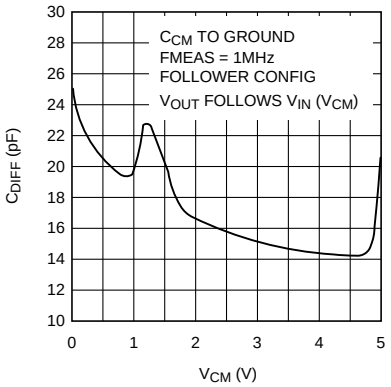

Figure 31.

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APPLICATION INFORMATION

Theory Of Operation

The LMV712-N dual op amp is derived from the LMV711 single op amp. Figure 32 contains a simplified schematic of one channel of the LMV712-N.

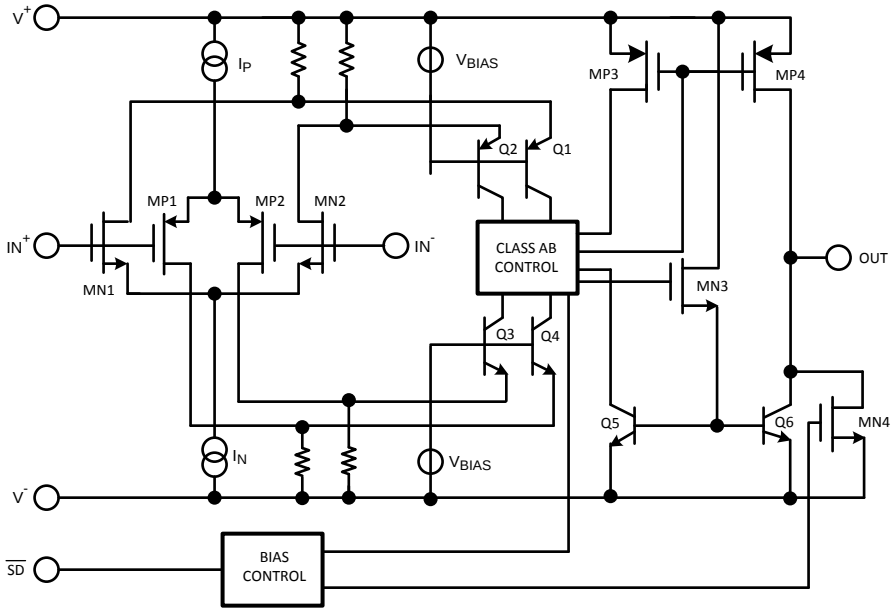

Figure 32.

Rail-to-Rail input is achieved by using in parallel, one NMOS differential pair (MN1 and MN2) and one PMOS differential pair (MP1 and MP2). When the common mode input voltage (V_{CM}) is near V^+, the NMOS pair is on and the PMOS pair is off. When V_{CM} is near V^-, the NMOS pair is off and the PMOS pair is on. When V_{CM} is between V^+ and V^-, internal logic decides how much current each differential pair will get. This special logic ensures stable and low distortion amplifier operation within the entire common mode voltage range.

Because both input stages have their own offset voltage (V_{OS}) characteristic, the offset voltage of the LMV712-N becomes a function of V_{CM}. V_{OS} has a crossover point at 1.4V above V^-. Refer to the "V_{OS} vs. V_{CM}" curve in the Typical Performance Characteristics section. Caution should be taken in situations where input signal amplitude is comparable to V_{OS} value and/or the design requires high accuracy. In these situations, it is necessary for the input signal to avoid the crossover point.

The current coming out of the input differential pairs gets mirrored through two folded cascode stages (Q1, Q2, Q3, Q4) into the "class AB control" block. This circuitry generates voltage gain, defines the op amp's dominant pole and limits the maximum current flowing at the output stage. MN3 introduces a voltage level shift and acts as a high impedance to low impedance buffer.

The output stage is composed of a PMOS and a NPN transistor in a common source/emitter configuration, delivering a rail-to-rail output excursion.

The MN4 transistor ensures that the LMV712-N output remains near V^- when the amplifier is in shutdown mode.

Shutdown Pin

The LMV712-N offers independent shutdown pins for the dual amplifiers. When the shutdown pin is tied low, the respective amplifier shuts down and the supply current is reduced to less than 1µA. In shutdown mode, the amplifier's output level stays at V^-. In a 2.7V operation, when a voltage between 1.5V to 2.7V is applied to the shutdown pin, the amplifier is enabled. As the amplifier is coming out of the shutdown mode, the output waveform ramps up without any glitch. This is demonstrated in Figure 33.

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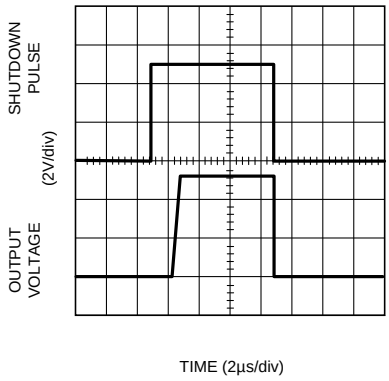

Figure 33.

A glitch-free output waveform is highly desirable in many applications, one of which is power amplifier control loops. In this application, the LMV712-N is used to drive the power amplifier's power control. If the LMV712-N did not have a smooth output ramp during turn on, it would directly cause the power amplifier to produce a glitch at its output. This adversely affects the performance of the system.

To enable the amplifier, the shutdown pin must be pulled high. It should not be left floating in the event that any leakage current may inadvertently turn off the amplifier.

Printed Circuit Board Consideration

To properly bypass the power supply, several locations on a printed circuit board need to be considered. A 6.8µF or greater tantalum capacitor should be placed at the point where the power supply for the amplifier is introduced onto the board. Another 0.1µF ceramic capacitor should be placed as close as possible to the power supply pin of the amplifier. If the amplifier is operated in a single power supply, only the V^+ pin needs to be bypassed with a 0.1µF capacitor. If the amplifier is operated in a dual power supply, both V^+ and V^- pins need to be bypassed.

It is good practice to use a ground plane on a printed circuit board to provide all components with a low inductive ground connection.

Surface mount components in 0805 size or smaller are recommended in the LMV712-N application circuits. Designers can take advantage of the DSBGA, VSSOP and WSON miniature sizes to condense board layout in order to save space and reduce stray capacitance.

Capacitive Load Tolerance

The LMV712-N can directly drive 200pF in unity-gain without oscillation. The unity-gain follower is the most sensitive configuration to capacitive loading. Direct capacitive loading reduces the phase margin of amplifiers. The combination of the amplifier's output impedance and the capacitive load induces phase lag. This results in either an under-damped pulse response or oscillation. To drive a heavier capacitive load, Figure 34 can be used.

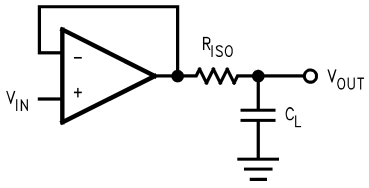

Figure 34.

In Figure 34, the isolation resistor R_{ISO} and the load capacitor C_L form a pole to increase stability by adding more phase margin to the overall system. The desired performance depends on the value of R_{ISO}. The bigger the R_{ISO} resistor value, the more stable V_{OUT} will be. But the DC accuracy is degraded when the R_{ISO} gets bigger. If there were a load resistor in Figure 34, the output voltage would be divided by R_{ISO} and the load resistor.

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The circuit in Figure 35 is an improvement to the one in Figure 34 because it provides DC accuracy as well as AC stability. In this circuit, R_F provides the DC accuracy by using feed-forward techniques to connect V_{IN} to R_L. C_F and R_{ISO} serve to counteract the loss of phase margin by feeding the high frequency component of the output signal back to the amplifier's inverting input, thereby preserving phase margin in the overall feedback loop. Increased capacitive drive is possible by increasing the value of C_F. This in turn will slow down the pulse response.

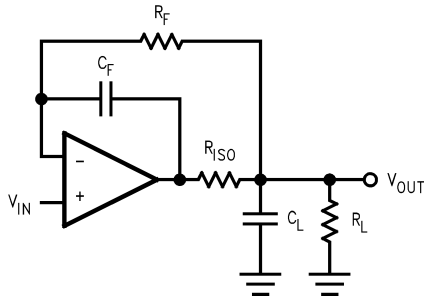

Figure 35.

Latchup

CMOS devices tend to be susceptible to latchup due to their internal parasitic SCR (silicon controlled rectifier) effects. The input and output pins look similar to the gate of the SCR. There is a minimum current required to trigger the SCR gate lead. The LMV712-N is designed to withstand 150mA surge current on all the pins. Some resistive method should be used to isolate any capacitance from supplying excess current to the pins. In addition, like an SCR, there is a minimum holding current for any latchup mode. Limiting current to the supply pins will also inhibit latchup susceptibility.

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CONNECTION DIAGRAMS

*Connect thermal pad to V^- or leave floating

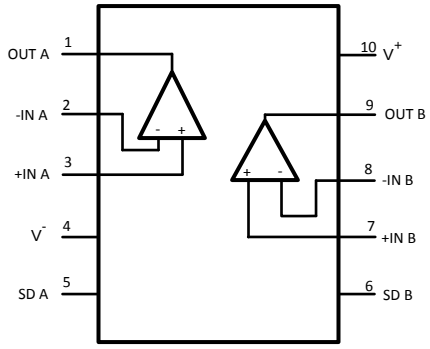

Figure 36. 10-Pin VSSOP (Top View)

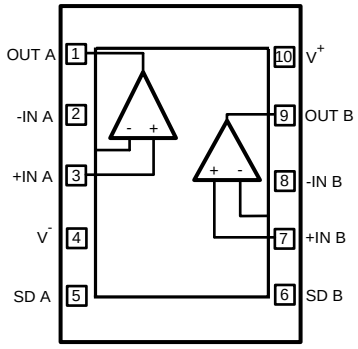

Figure 37. 10-Pin WSON (Top View)

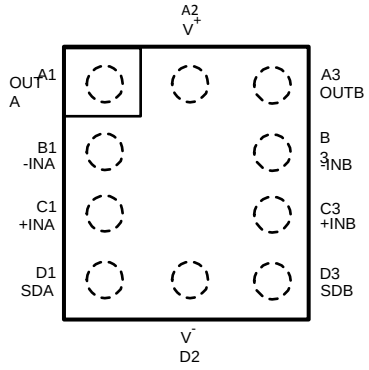

Figure 38. 10-Bump DSBGA (Top View)

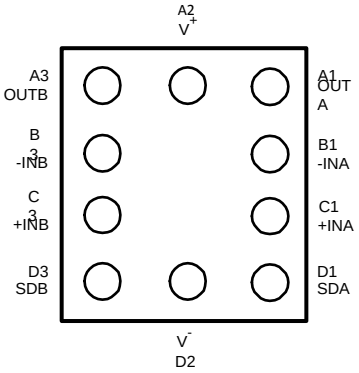

Figure 39. 10-Bump DSBGA (Bottom View)

REVISION HISTORY

Changes from Revision H (Feb 2013) to Revision I	Page
• Added Q1 part	1

Changes from Revision G (February 2013) to Revision H	Page
• Changed layout of National Data Sheet to TI format	15

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PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
LMV712LD/NOPB	ACTIVE	WSON	NGY	10	1000	Green (RoHS & no Sb/Br)	CU SN	Level-3-260C-168 HR	-40 to 85	A62	Samples
LMV712LDX/NOPB	ACTIVE	WSON	NGY	10	4500	Green (RoHS & no Sb/Br)	CU SN	Level-3-260C-168 HR	-40 to 85	A62	Samples
LMV712MM	NRND	VSSOP	DGS	10	1000	TBD	Call TI	Call TI	-40 to 85	A61	
LMV712MM/NOPB	ACTIVE	VSSOP	DGS	10	1000	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 85	A61	Samples
LMV712MMX	NRND	VSSOP	DGS	10		TBD	Call TI	Call TI	-40 to 85	A61	
LMV712MMX/NOPB	ACTIVE	VSSOP	DGS	10	3500	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 85	A61	Samples
LMV712Q1MM/NOPB	ACTIVE	VSSOP	DGS	10	1000	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 125	AUA	Samples
LMV712Q1MMX/NOPB	ACTIVE	VSSOP	DGS	10	3500	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 125	AUA	Samples
LMV712TL/NOPB	ACTIVE	DSBGA	YPA	10	250	Green (RoHS & no Sb/Br)	SNAGCU	Level-1-260C-UNLIM	-40 to 85	AU2A	Samples
LMV712TLX/NOPB	ACTIVE	DSBGA	YPA	10	3000	Green (RoHS & no Sb/Br)	SNAGCU	Level-1-260C-UNLIM	-40 to 85	AU2A	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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OTHER QUALIFIED VERSIONS OF LMV712-N, LMV712-N-Q1 :

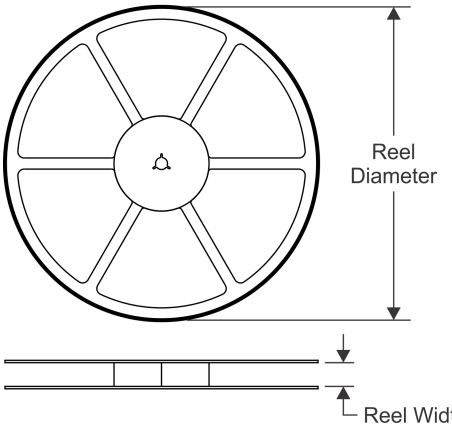
- Catalog: LMV712-N
- Automotive: LMV712-N-Q1

NOTE: Qualified Version Definitions:

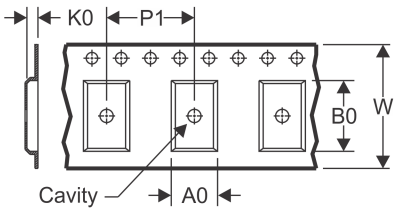
- Catalog - TI's standard catalog product
- Automotive - Q100 devices qualified for high-reliability automotive applications targeting zero defects

TAPE AND REEL INFORMATION

REEL DIMENSIONS

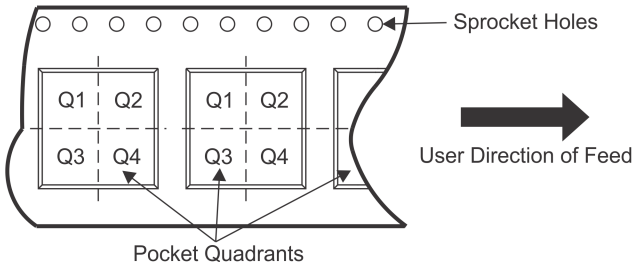


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

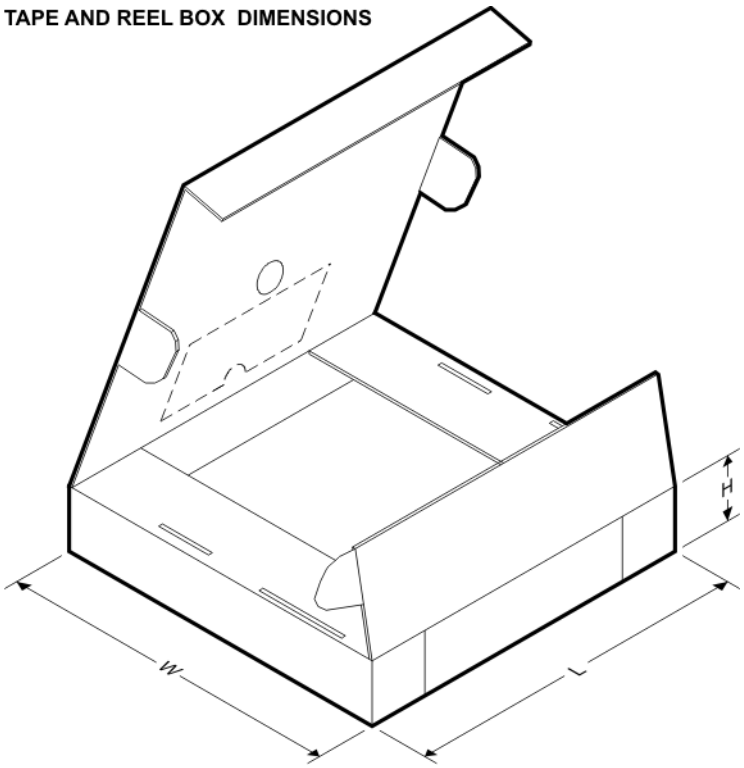
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
LMV712LD/NOPB	WSON	NGY	10	1000	178.0	12.4	3.3	3.3	1.0	8.0	12.0	Q1
LMV712LDX/NOPB	WSON	NGY	10	4500	330.0	12.4	3.3	3.3	1.0	8.0	12.0	Q1
LMV712MM	VSSOP	DGS	10	1000	178.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
LMV712MM/NOPB	VSSOP	DGS	10	1000	178.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
LMV712MMX/NOPB	VSSOP	DGS	10	3500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
LMV712Q1MM/NOPB	VSSOP	DGS	10	1000	178.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
LMV712Q1MMX/NOPB	VSSOP	DGS	10	3500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
LMV712TL/NOPB	DSBGA	YPA	10	250	178.0	8.4	1.68	2.13	0.76	4.0	8.0	Q1
LMV712TLX/NOPB	DSBGA	YPA	10	3000	178.0	8.4	1.68	2.13	0.76	4.0	8.0	Q1

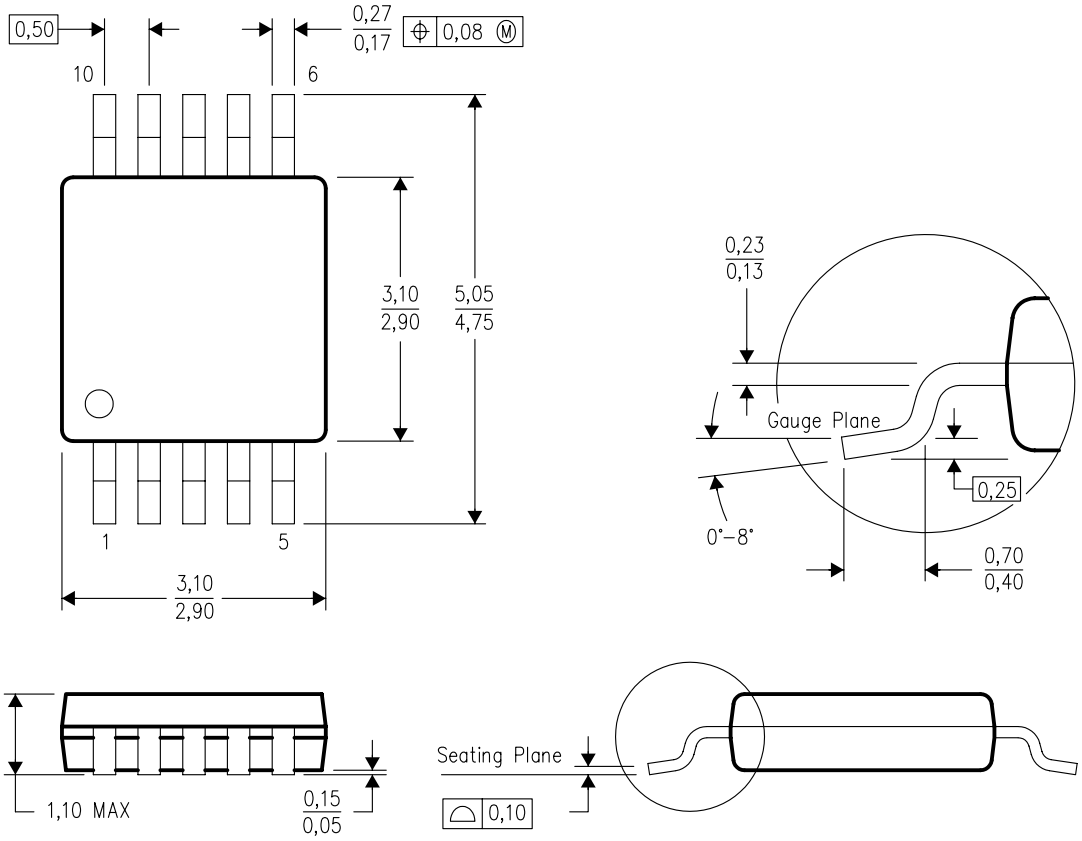
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
LMV712LD/NOPB	WSON	NGY	10	1000	213.0	191.0	55.0
LMV712LDX/NOPB	WSON	NGY	10	4500	367.0	367.0	35.0
LMV712MM	VSSOP	DGS	10	1000	210.0	185.0	35.0
LMV712MM/NOPB	VSSOP	DGS	10	1000	210.0	185.0	35.0
LMV712MMX/NOPB	VSSOP	DGS	10	3500	367.0	367.0	35.0
LMV712Q1MM/NOPB	VSSOP	DGS	10	1000	210.0	185.0	35.0
LMV712Q1MMX/NOPB	VSSOP	DGS	10	3500	367.0	367.0	35.0
LMV712TL/NOPB	DSBGA	YPA	10	250	210.0	185.0	35.0
LMV712TLX/NOPB	DSBGA	YPA	10	3000	210.0	185.0	35.0

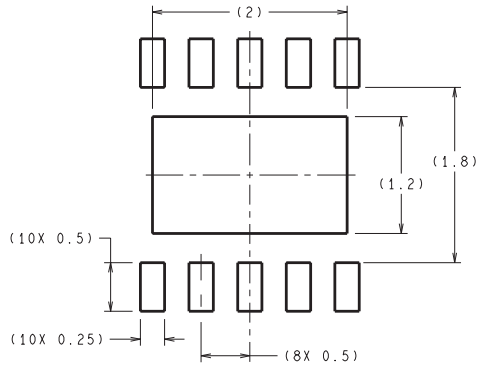
DGS (S–PDSO–G10) PLASTIC SMALL–OUTLINE PACKAGE



4073272/C 02/04

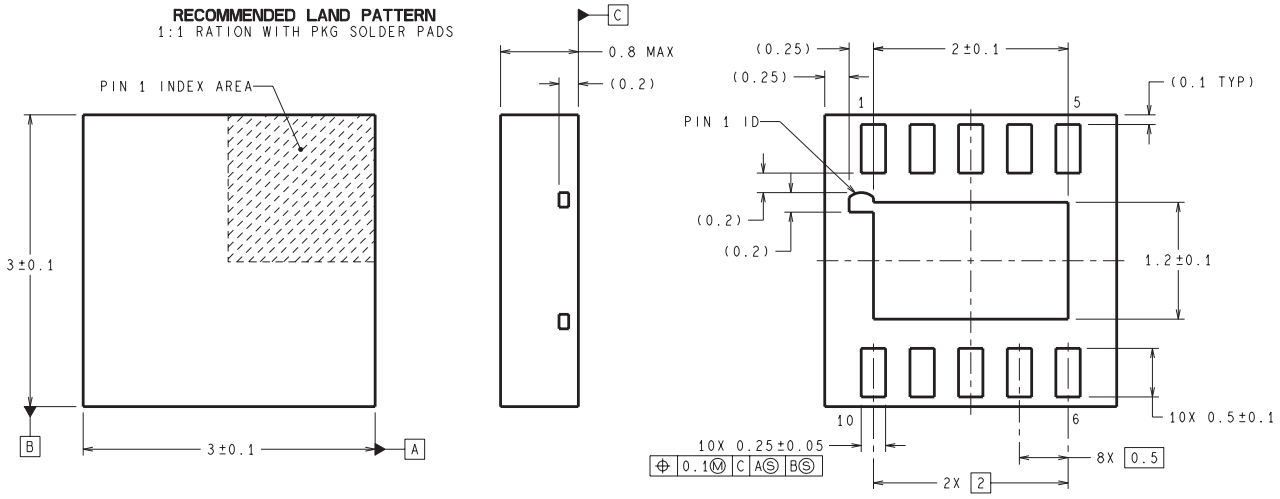
NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion.
D. Falls within JEDEC MO–187 variation BA.

NGY0010A



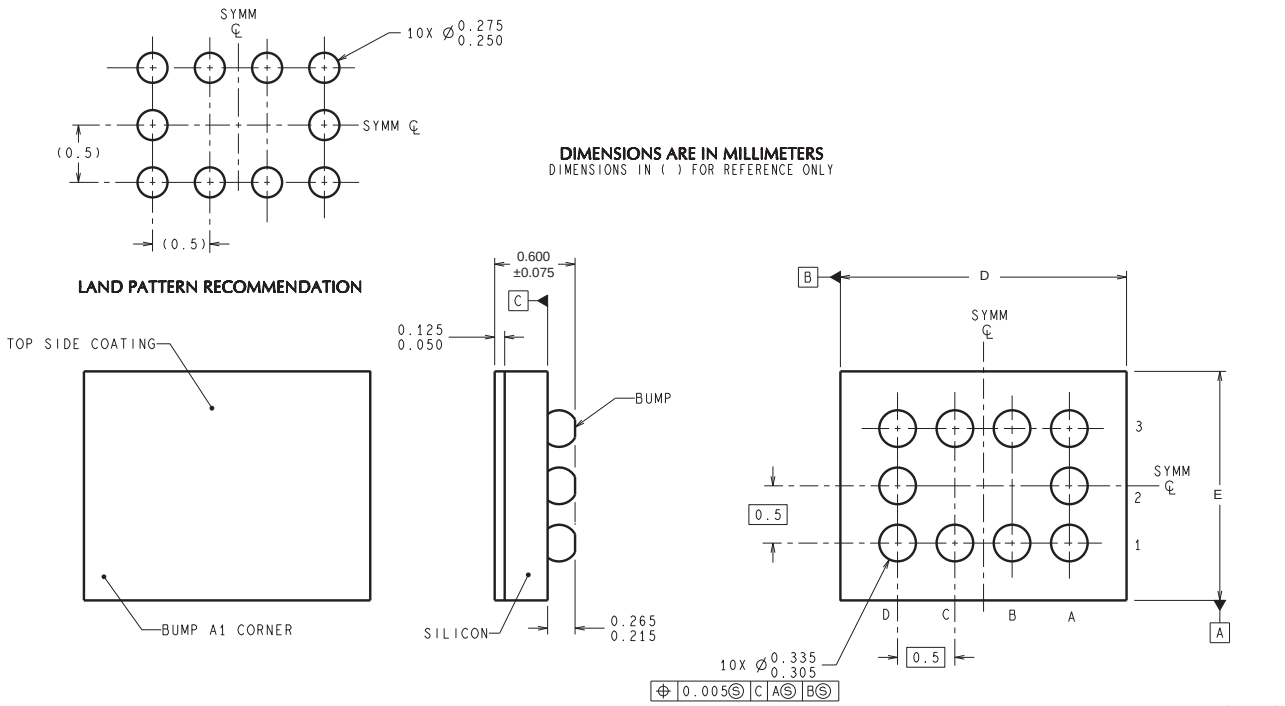
RECOMMENDED LAND PATTERN
1:1 RATION WITH PKG SOLDER PADS

DIMENSIONS ARE IN MILLIMETERS



LDA10A (Rev B)

YPA0010



D: Max = 2.048 mm, Min =1.987 mm

E: Max = 1.565 mm, Min =1.504 mm

4215069/A 12/12

NOTES: A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.
B. This drawing is subject to change without notice.

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Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265
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