# LMV321, LMV358, LMV324

# Single, Dual, Quad Low-Voltage, Rail-to-Rail Operational Amplifiers

The LMV321, LMV358, and LMV324 are CMOS single, dual, and quad low voltage operational amplifiers with rail−to−rail output swing. These amplifiers are a cost−effective solution for applications where low power consumption and space saving packages are critical. Specification tables are provided for operation from power supply voltages at 2.7 V and 5 V. Rail−to−Rail operation provides improved signal−to−noise preformance. Ultra low quiescent current makes this series of amplifiers ideal for portable, battery operated equipment. The common mode input range includes ground making the device useful for low−side current−shunt measurements. The ultra small packages allow for placement on the PCB in close proximity to the signal source thereby reducing noise pickup.

### Features

- Operation from 2.7 V to 5.0 V Single−Sided Power Supply
- LMV321 Single Available in Ultra Small 5 Pin SC70 Package
- No Output Crossover Distortion
- Industrial temperature Range: −40°C to +85°C
- Rail−to−Rail Output
- Low Quiescent Current: LMV358 Dual − 220 μA, Max per Channel
- No Output Phase−Reversal from Overdriven Input
- These are Pb−Free Devices

### Typical Applications

- Notebook Computers and PDA's
- Portable Battery−Operated Instruments
- Active Filters

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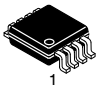
**http://onsemi.com**




**SC−70**
**CASE 419A**




**TSOP−5**
**CASE 483**




**Micro8™**
**CASE 846A**



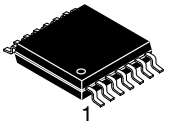

**SOIC−8**
**CASE 751**




**UDFN8**
**CASE 517AJ**




**SOIC−14**
**CASE 751A**




**TSSOP−14**
**CASE 948G**

### ORDERING AND MARKING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 12 of this data sheet.

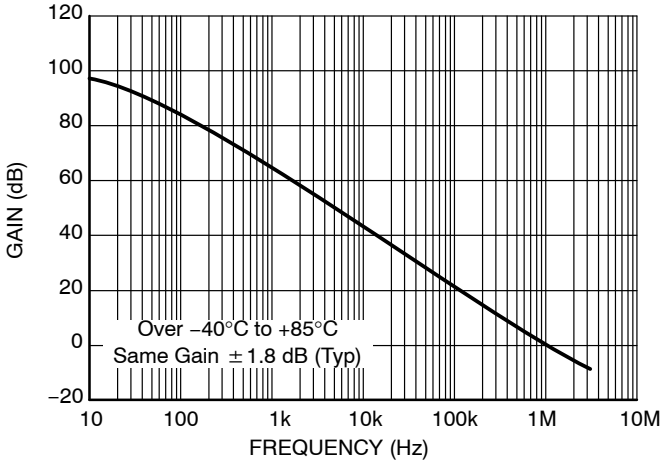



**Figure 1. Open Loop Frequency Response ($R_L$ = 2 kΩ, $T_A$ = 25°C, $V_S$ = 5 V)**

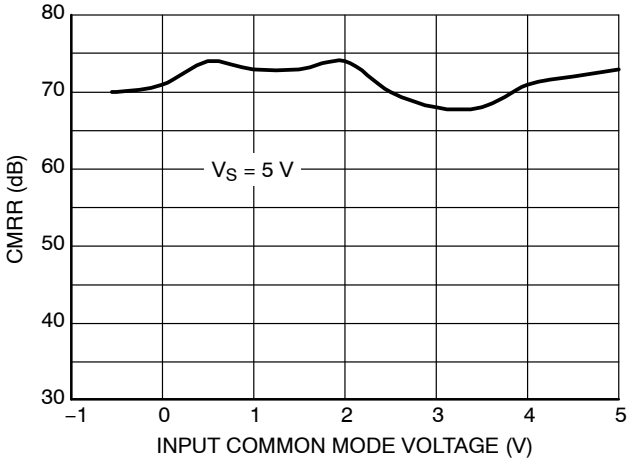
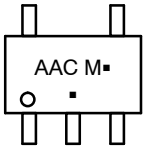



**Figure 2. CMRR vs. Input Common Mode Voltage**

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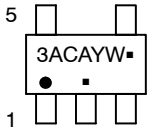
## MARKING DIAGRAMS

SC−70




AAC = Specific Device Code
M = Date Code
▪ = Pb−Free Package
(Note: Microdot may be in either location)

TSOP−5



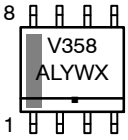

3AC = Specific Device Code
A = Assembly Location
Y = Year
W = Work Week
▪ = Pb−Free Package
(Note: Microdot may be in either location)

Micro8




V358 = Specific Device Code
A = Assembly Location
Y = Year
W = Work Week
▪ = Pb−Free Package
(Note: Microdot may be in either location)

SOIC−8



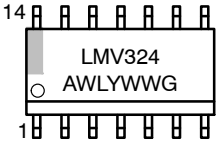

V358 = Specific Device Code
A = Assembly Location
L = Wafer Lot
Y = Year
W = Work Week
▪ = Pb−Free Package

UDFN8



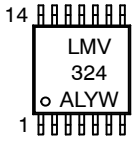

AC = Specific Device Code
M = Date Code
▪ = Pb−Free Package

SOIC−14




LMV324 = Specific Device Code
A = Assembly Location
WL = Wafer Lot
Y = Year
WW = Work Week
G = Pb−Free Package

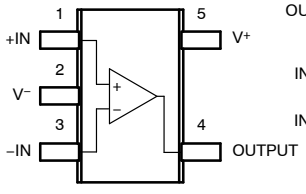
TSSOP−14




LMV324 = Specific Device Code
A = Assembly Location
L = Wafer Lot
Y = Year
W = Work Week
▪ = Pb−Free Package

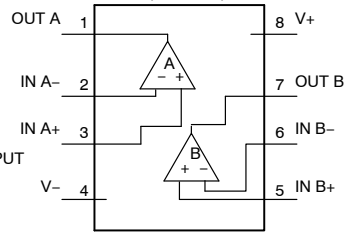
## PIN CONNECTIONS

SC70−5/TSOP−5



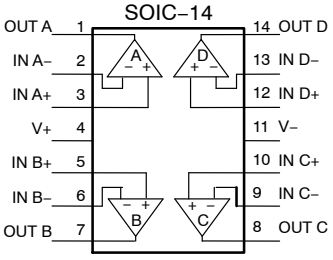

(Top View)

UDFN8/Micro8/SOIC−8



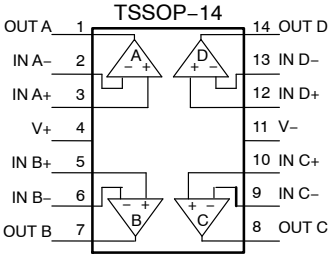

(Top View)

SOIC−14




(Top View)

TSSOP−14




(Top View)

**MAXIMUM RATINGS**

| Symbol | Rating | Value | Unit |
|---|---|---|---|
| $V_S$ | Supply Voltage (Operating Range $V_S$ = 2.7 V to 5.5 V) | 5.5 | V |
| $V_{IDR}$ | Input Differential Voltage | ± Supply Voltage | V |
| $V_{ICR}$ | Input Common Mode Voltage Range | −0.5 to (V+) + 0.5 | V |
| | Maximum Input Current | 10 | mA |
| $t_{So}$ | Output Short Circuit (Note 1) | Continuous | |
| $T_J$ | Maximum Junction Temperature (Operating Range −40°C to 85°C) | 150 | °C |
| $\theta_{JA}$ | Thermal Resistance: | | °C/W |
| | SC−70 | 280 | |
| | Micro8 | 238 | |
| | TSOP−5 | 333 | |
| | UDFN8 (1.2 mm x 1.8 mm x 0.5 mm) | 350 | |
| | SOIC−8 | 212 | |
| | SOIC−14 | 156 | |
| | TSSOP−14 | 190 | |
| $T_{stg}$ | Storage Temperature | −65 to 150 | °C |
| | Mounting Temperature (Infrared or Convection −20 sec) | 235 | °C |
| $V_{ESD}$ | ESD Tolerance<br>LMV321<br>Machine Model<br>Human Body Model<br>LMV358/324<br>Machine Model<br>Human Body Mode | <br><br>100<br>1000<br><br>100<br>2000 | V |

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

1. Continuous short−circuit operation to ground at elevated ambient temperature can result in exceeding the maximum allowed junction temperature of 150°C. Output currents in excess of 45 mA over long term may adversely affect reliability. Shorting output to either V+ or V− will adversely affect reliability.

**2.7 V DC ELECTRICAL CHARACTERISTICS** (Unless otherwise specified, all limits are guaranteed for $T_A$ = 25°C, $V^+$ = 2.7 V, $R_L$ = 1 MΩ, $V^-$ = 0 V, $V_O$ = V+/2)

| Parameter | Symbol | Condition | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| Input Offset Voltage | $V_{IO}$ | $T_A$ = −40°C to +85°C | | 1.7 | 9 | mV |
| Input Offset Voltage Average Drift | $ICV_{OS}$ | $T_A$ = −40°C to +85°C | | 5 | | μV/°C |
| Input Bias Current | $I_B$ | $T_A$ = −40°C to +85°C | | <1 | | nA |
| Input Offset Current | $I_{IO}$ | $T_A$ = −40°C to +85°C | | <1 | | nA |
| Common Mode Rejection Ratio | CMRR | 0 V ≤ $V_{CM}$ ≤ 1.7 V | 50 | 63 | | dB |
| Power Supply Rejection Ratio | PSRR | 2.7 V ≤ V+ ≤ 5 V, $V_O$ = 1 V | 50 | 60 | | dB |
| Input Common−Mode Voltage Range | $V_{CM}$ | For CMRR ≥ 50 dB | 0 to 1.7 | −0.2 to 1.9 | | V |
| Output Swing | $V_{OH}$ | $R_L$ = 10 kΩ to 1.35 V | $V_{CC}$ − 100 | $V_{CC}$ − 10 | | mV |
| | $V_{OL}$ | $R_L$ = 10 kΩ to 1.35 V (Note 2) | | 60 | 180 | mV |
| Supply Current LMV321<br>LMV358 (Both Amplifiers)<br>LMV324 (4 Amplifiers) | $I_{CC}$ | | | 80<br>140<br>260 | 185<br>340<br>680 | μA |

**2.7 V AC ELECTRICAL CHARACTERISTICS** (Unless otherwise specified, all limits are guaranteed for $T_A$ = 25°C, $V^+$ = 2.7 V, $R_L$ = 1 MΩ, $V^-$ = 0 V, $V_O$ = V+/2)

| Parameter | Symbol | Condition | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| Gain Bandwidth Product | GBWP | $C_L$ = 200 pF | | 1 | | MHz |
| Phase Margin | $\Theta_m$ | | | 60 | | ° |
| Gain Margin | $G_m$ | | | 10 | | dB |
| Input−Referred Voltage Noise | $e_n$ | f = 50 kHz | | 50 | | nV/$\sqrt{Hz}$ |

2. Guaranteed by design and/or characterization.

**5.0 V DC ELECTRICAL CHARACTERISTICS** (Unless otherwise specified, all limits are guaranteed for $T_A$ = 25°C, $V^+$ = 5.0 V, $R_L$ = 1 MΩ, $V^-$ = 0 V, $V_O$ = V+/2)

| Parameter | Symbol | Condition | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| Input Offset Voltage | $V_{IO}$ | $T_A$ = −40°C to +85°C | | 1.7 | 9 | mV |
| Input Offset Voltage Average Drift | $T_CV_{IO}$ | $T_A$ = −40°C to +85°C | | 5 | | μV/°C |
| Input Bias Current (Note 3) | $I_B$ | $T_A$ = −40°C to +85°C | | < 1 | | nA |
| Input Offset Current (Note 3) | $I_{IO}$ | $T_A$ = −40°C to +85°C | | < 1 | | nA |
| Common Mode Rejection Ratio | CMRR | 0 V ≤ $V_{CM}$ ≤ 4 V | 50 | 65 | | dB |
| Power Supply Rejection Ratio | PSRR | 2.7 V ≤ V+ ≤ 5 V, $V_O$ = 1 V, $V_{CM}$ = 1 V | 50 | 60 | | dB |
| Input Common−Mode Voltage Range | $V_{CM}$ | For CMRR ≥ 50 dB | 0 to 4 | −0.2 to 4.2 | | V |
| Large Signal Voltage Gain (Note 3) | $A_V$ | $R_L$ = 2 kΩ | 15 | 100 | | V/mV |
| | | $T_A$ = −40°C to +85°C | 10 | | | |
| Output Swing | $V_{OH}$ | $R_L$ = 2 kΩ to 2.5 V<br>$T_A$ = −40°C to +85°C | $V_{CC}$ − 300<br>$V_{CC}$ − 400 | $V_{CC}$ − 40 | | V |
| | $V_{OL}$ | $R_L$ = 2 kΩ to 2.5 V (Note 3)<br>$T_A$ = −40°C to +85°C | | 120 | 300<br>400 | mV |
| | $V_{OH}$ | $R_L$ = 10 kΩ to 2.5 V (Note 3)<br>$T_A$ = −40°C to +85°C | $V_{CC}$ − 100<br>$V_{CC}$ − 200 | | | V |
| | $V_{OL}$ | $R_L$ = 10 kΩ to 2.5 V<br>$T_A$ = −40°C to +85°C | | 65 | 180<br>280 | mV |
| Output Short Circuit Current | $I_O$ | Sourcing = $V_O$ = 0 V (Note 3)<br>Sinking = $V_O$ = 5 V (Note 3) | 10<br>10 | 60<br>160 | | mA |
| Supply Current | $I_{CC}$ | LMV321<br>$T_A$ = −40°C to +85°C | | 130 | 250<br>350 | μA |
| | | LMV358 Both Amplifiers<br>$T_A$ = −40°C to +85°C | | 210 | 440<br>615 | |
| | | LMV324 All Four Amplifiers<br>$T_A$ = −40°C to +85°C | | 410 | 830<br>1160 | |

**5.0 V AC ELECTRICAL CHARACTERISTICS** (Unless otherwise specified, all limits are guaranteed for $T_A$ = 25°C, $V^+$ = 5.0 V, $R_L$ = 1 MΩ, $V^-$ = 0 V, $V_O$ = V+/2)

| Parameter | Symbol | Condition | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| Slew Rate | $S_R$ | | | 1 | | V/μs |
| Gain Bandwidth Product | GBWP | $C_L$ = 200 pF | | 1 | | MHz |
| Phase Margin | $\Theta_m$ | | | 60 | | ° |
| Gain Margin | $G_m$ | | | 10 | | dB |
| Input−Referred Voltage Noise | $e_n$ | f = 50 kHz | | 50 | | nV/$\sqrt{Hz}$ |

3. Guaranteed by design and/or characterization.

## TYPICAL CHARACTERISTICS

($T_A$ = 25°C and $V_S$ = 5 V unless otherwise specified)

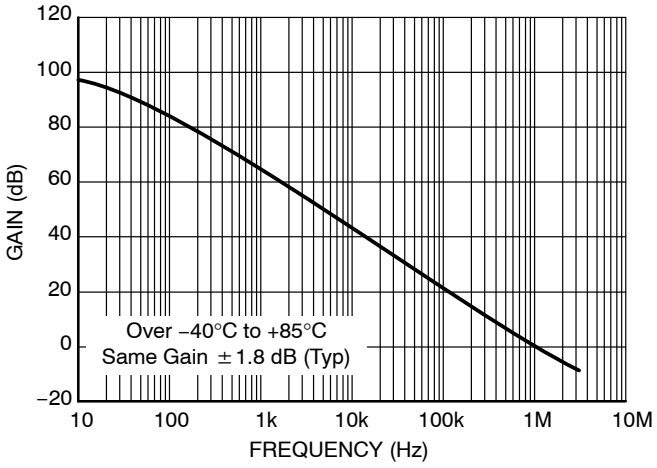



**Figure 3. Open Loop Frequency Response ($R_L$ = 2 kΩ, $T_A$ = 25°C, $V_S$ = 5 V)**

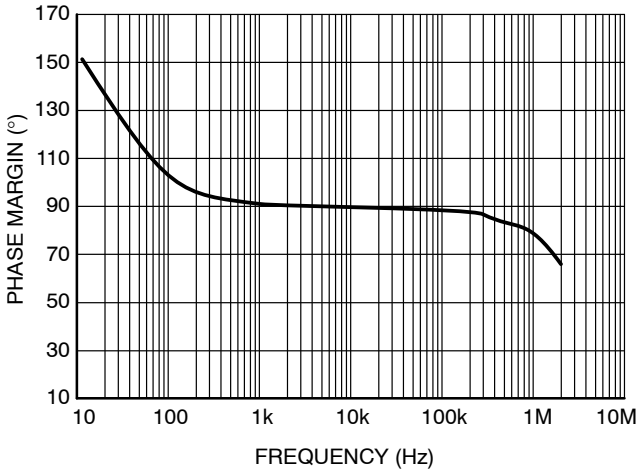



**Figure 4. Open Loop Phase Margin ($R_L$ = 2 kΩ, $T_A$ = 25°C, $V_S$ = 5 V)**

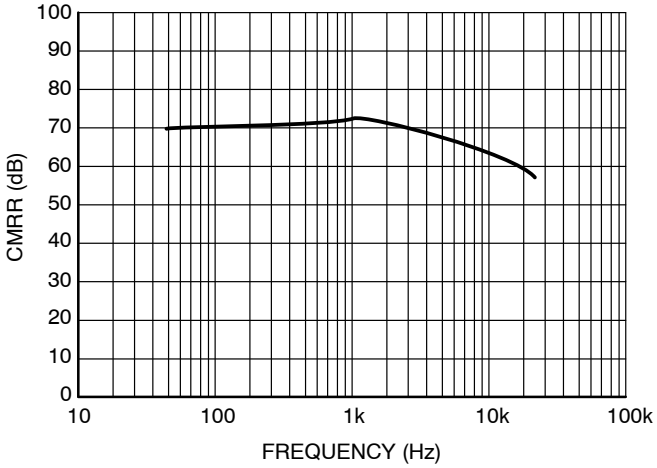



**Figure 5. CMRR vs. Frequency ($R_L$ = 5 kΩ, $V_S$ = 5 V)**

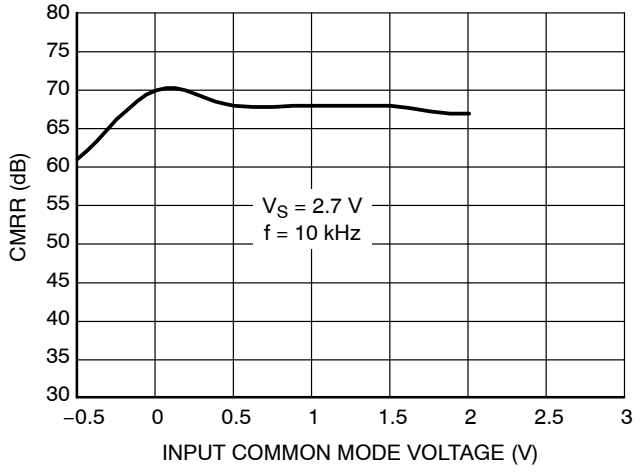



**Figure 6. CMRR vs. Input Common Mode Voltage**

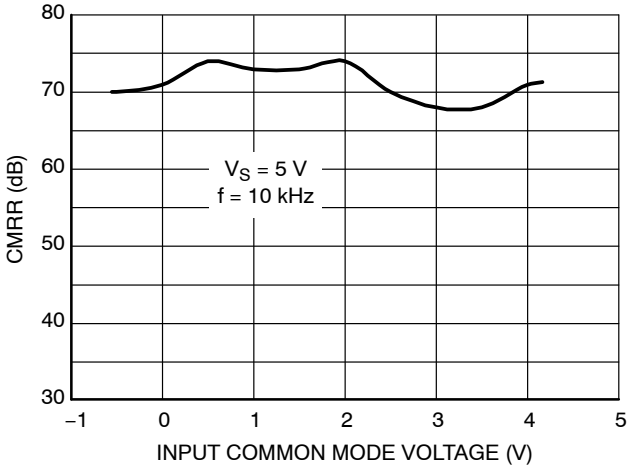



**Figure 7. CMRR vs. Input Common Mode Voltage**

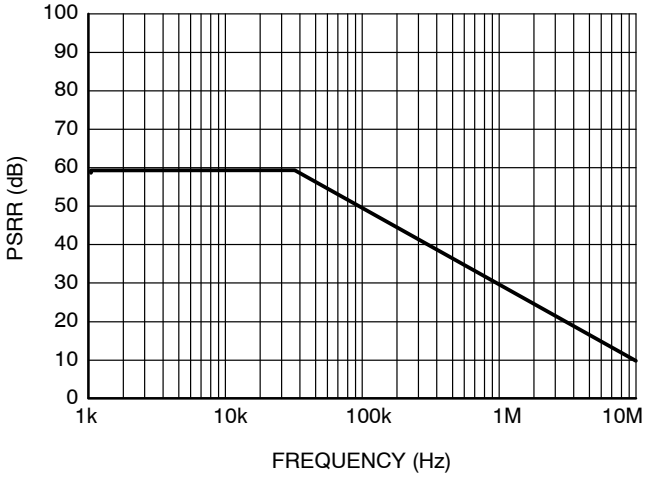



**Figure 8. PSRR vs. Frequency ($R_L$ = 5 kΩ, $V_S$ = 2.7 V, +PSRR)**

## TYPICAL CHARACTERISTICS

($T_A$ = 25°C and $V_S$ = 5 V unless otherwise specified)

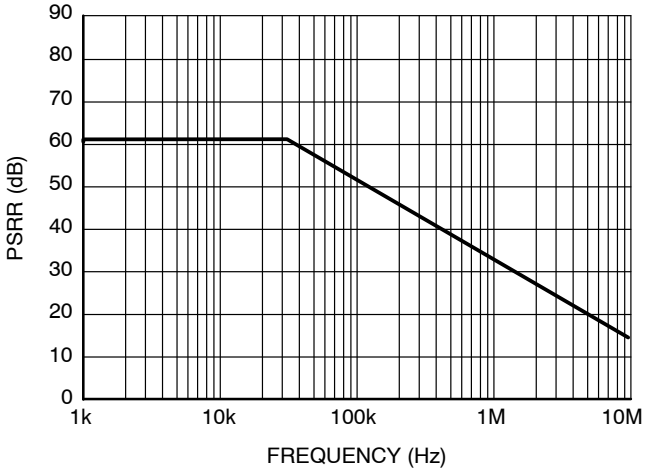



**Figure 9. PSRR vs. Frequency ($R_L$ = 5 kΩ, $V_S$ = 2.7 V, −PSRR)**

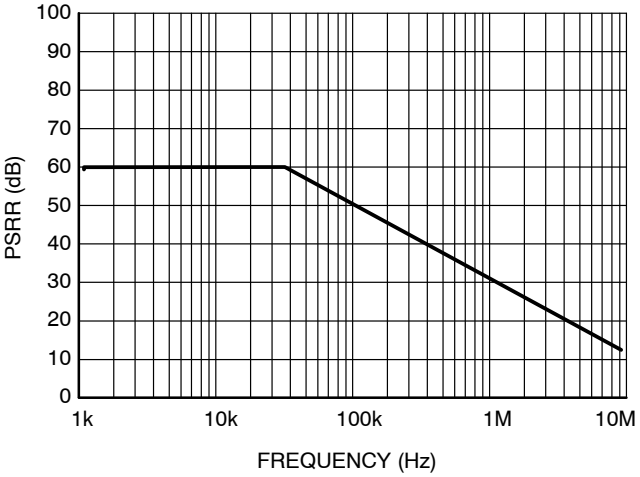



**Figure 10. PSRR vs. Frequency ($R_L$ = 5 kΩ, $V_S$ = 5 V, +PSRR)**

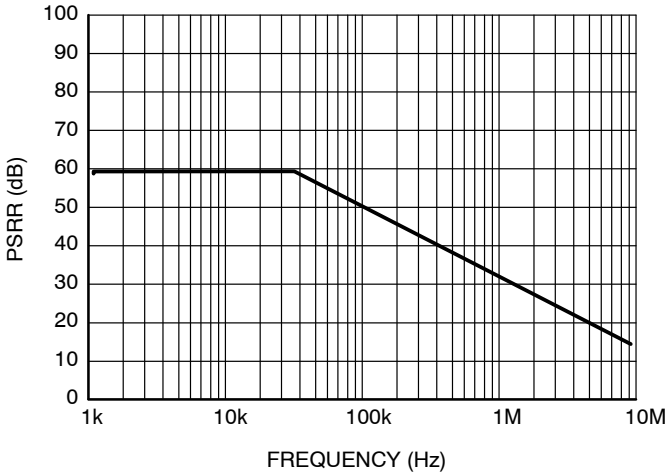



**Figure 11. PSRR vs. Frequency ($R_L$ = 5 kΩ, $V_S$ = 5 V, −PSRR)**

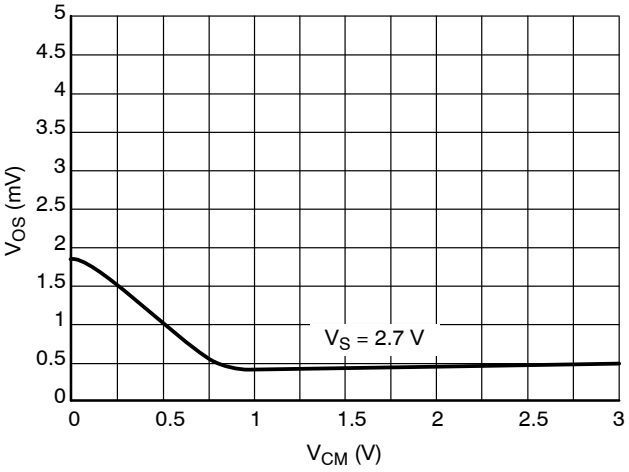



**Figure 12. $V_{OS}$ vs CMR**

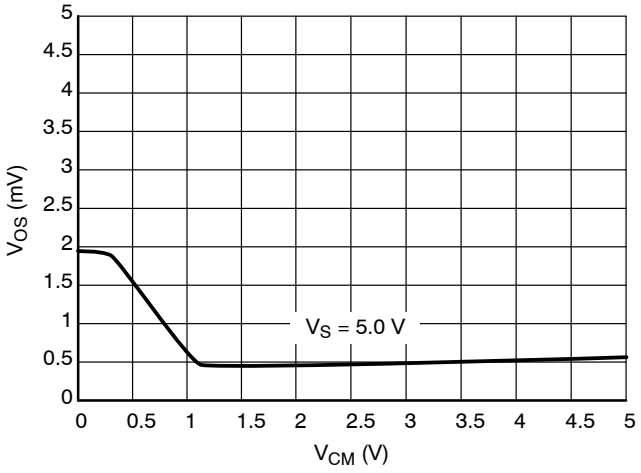



**Figure 13. $V_{OS}$ vs CMR**

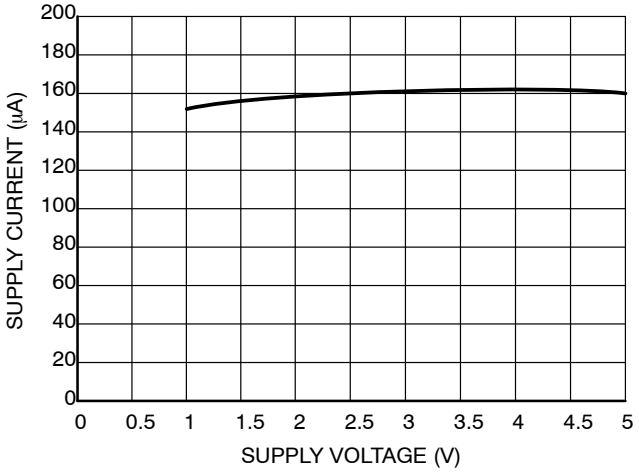



**Figure 14. Supply Current vs. Supply Voltage**

## TYPICAL CHARACTERISTICS

($T_A$ = 25°C and $V_S$ = 5 V unless otherwise specified)

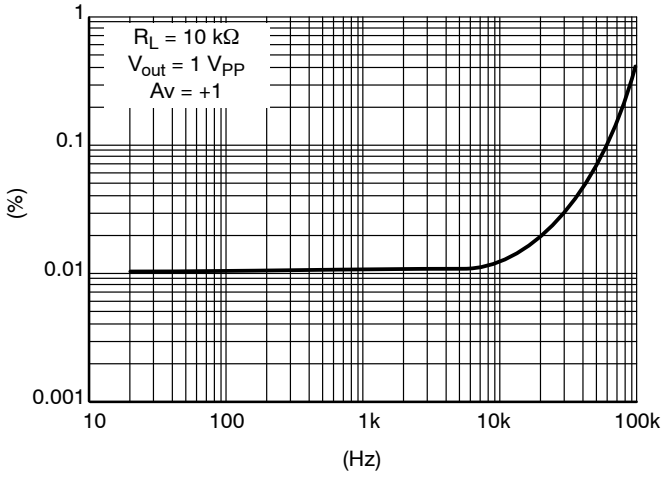



**Figure 15. THD+N vs Frequency**

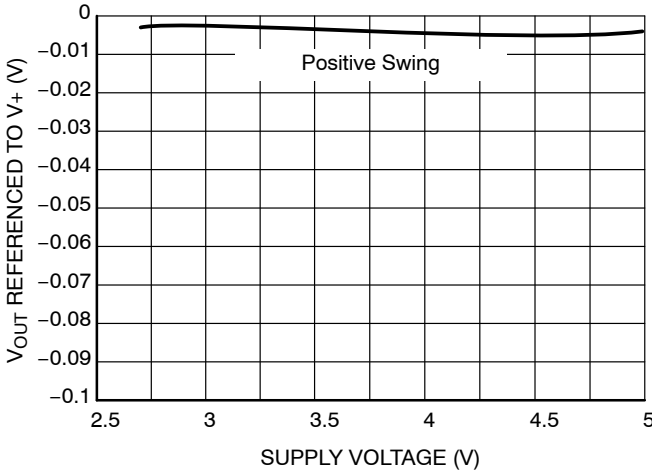



**Figure 16. Output Voltage Swing vs Supply Voltage ($R_L$ = 10k)**

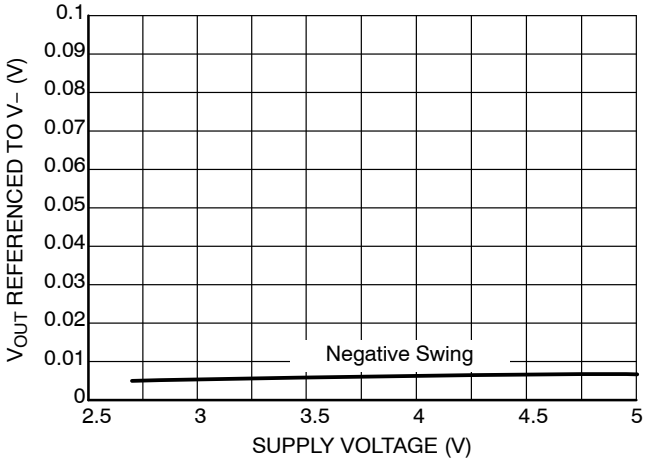



**Figure 17. Output Voltage Swing vs Supply Voltage ($R_L$ = 10k)**

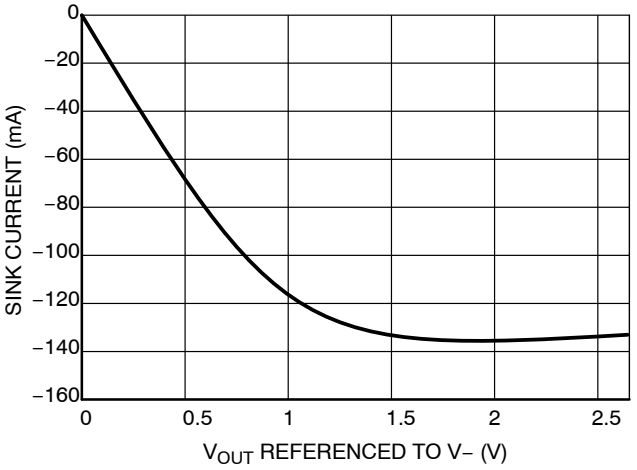



**Figure 18. Sink Current vs. Output Voltage $V_S$ = 2.7 V**

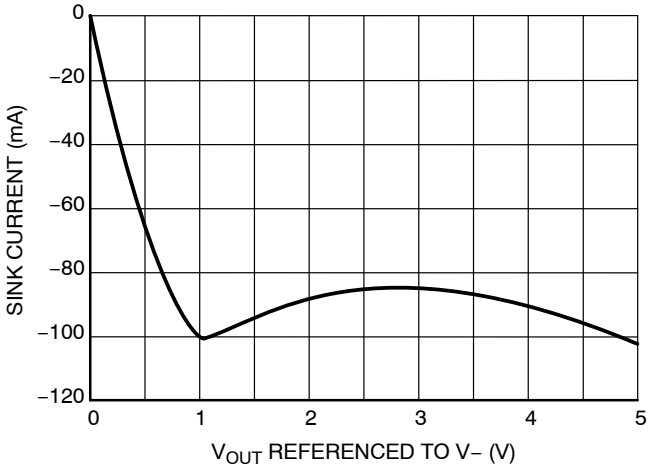



**Figure 19. Sink Current vs. Output Voltage $V_S$ = 5.0 V**

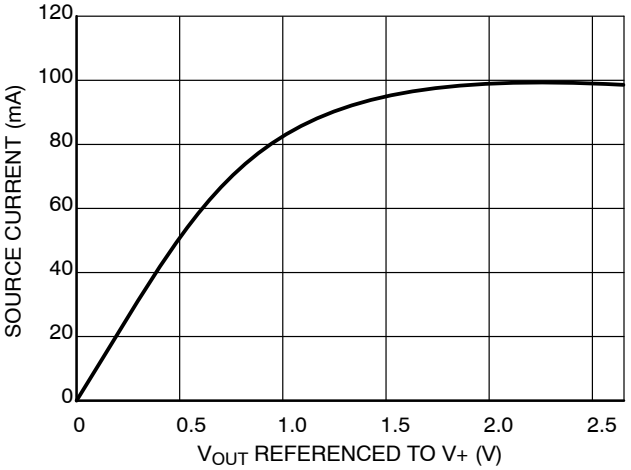



**Figure 20. Source Current vs. Output Voltage $V_S$ = 2.7 V**

## TYPICAL CHARACTERISTICS

($T_A$ = 25°C and $V_S$ = 5 V unless otherwise specified)

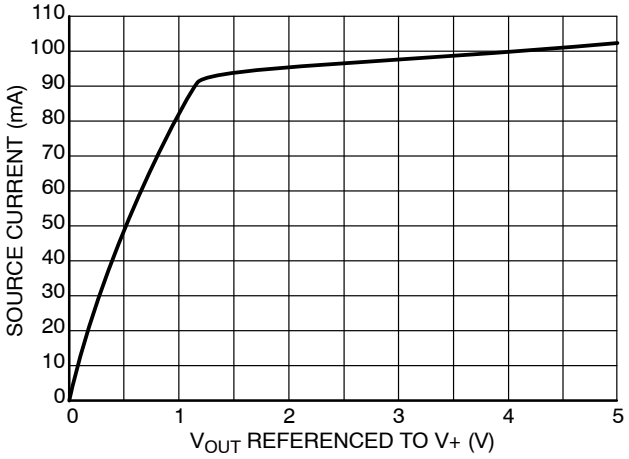



**Figure 21. Source Current vs. Output Voltage**
**$V_S$ = 5.0 V**

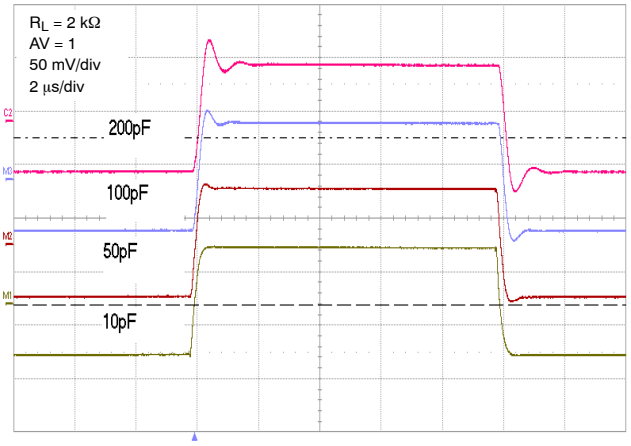



**Figure 22. Settling Time vs. Capacitive Load**

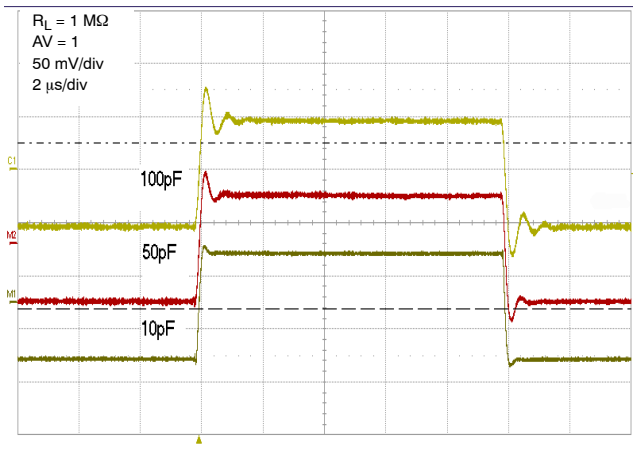



**Figure 23. Settling Time vs. Capacitive Load**

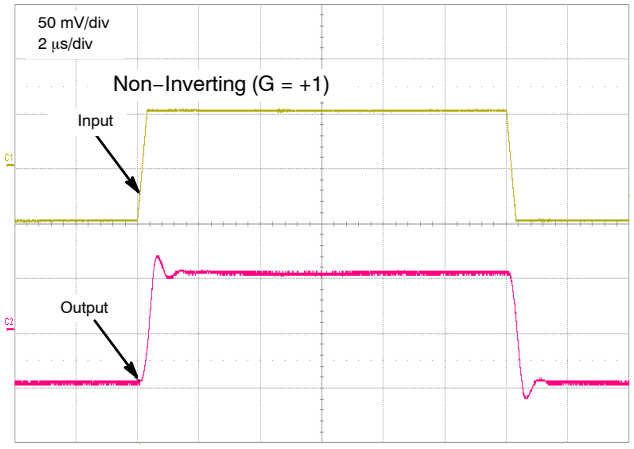



**Figure 24. Step Response − Small Signal**

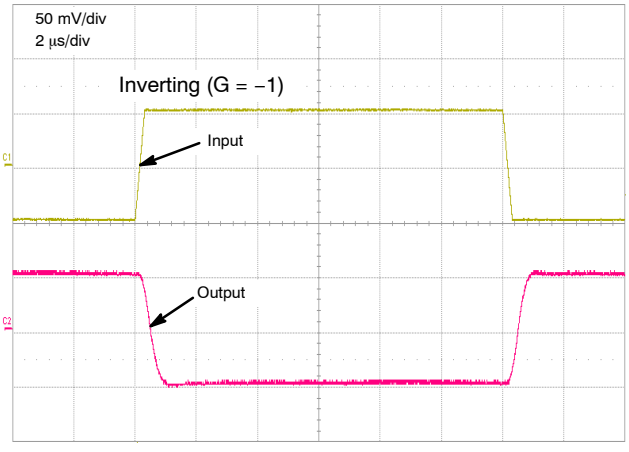



**Figure 25. Step Response − Small Signal**

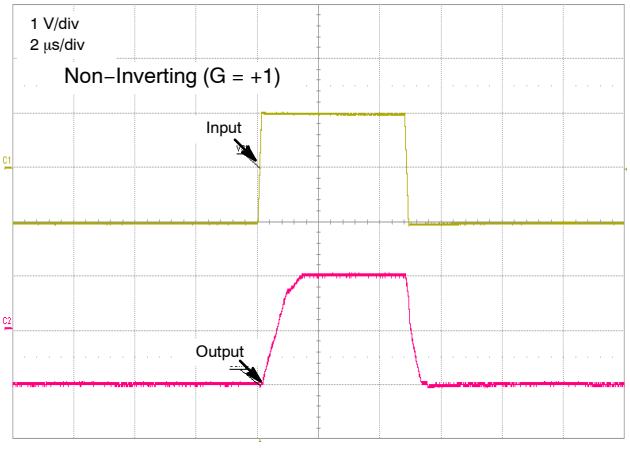



**Figure 26. Step Response − Large Signal**

## TYPICAL CHARACTERISTICS

($T_A$ = 25°C and $V_S$ = 5 V unless otherwise specified)

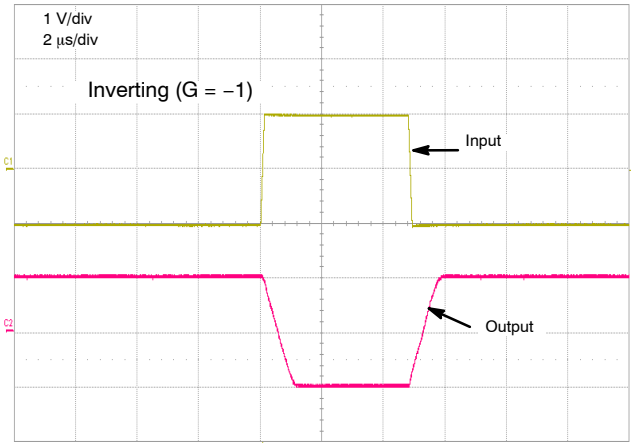



**Figure 27. Step Response − Large Signal**

## APPLICATIONS

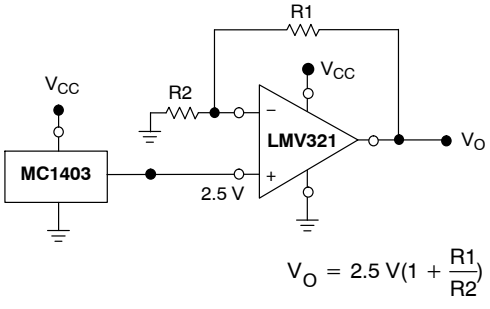



**Figure 28. Voltage Reference**

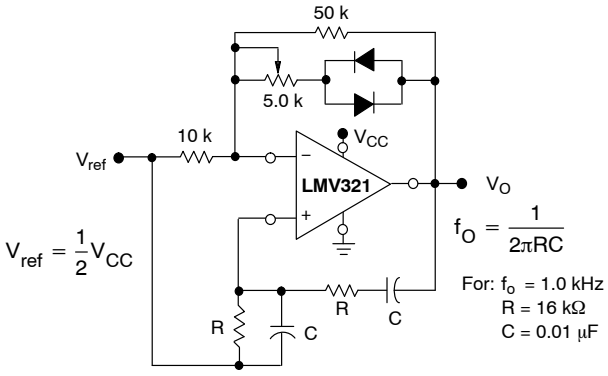
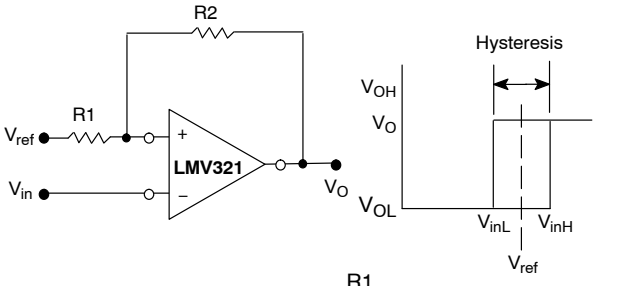



**Figure 29. Wien Bridge Oscillator**

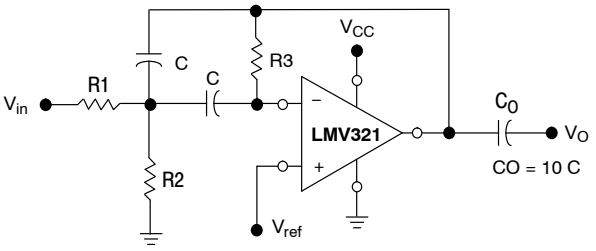



$$V_{in}L = \frac{R1}{R1 + R2} (V_{OL} - V_{ref}) + V_{ref}$$

$$V_{in}H = \frac{R1}{R1 + R2} (V_{OH} - V_{ref}) + V_{ref}$$

$$H = \frac{R1}{R1 + R2} (V_{OH} - V_{OL})$$

**Figure 30. Comparator with Hysteresis**




Given: $f_o$ = center frequency
$A(f_o)$ = gain at center frequency

Choose value $f_o$, C

Then : $R3 = \frac{Q}{\pi f_O C}$

$$R1 = \frac{R3}{2\,A(f_O)}$$

$$R2 = \frac{R1\,R3}{4Q^2\,R1 - R3}$$

For less than 10% error from operational amplifier, $((Q_O\,f_O)/BW) < 0.1$ where $f_o$ and BW are expressed in Hz. If source impedance varies, filter may be preceded with voltage follower buffer to stabilize filter parameters.

**Figure 31. Multiple Feedback Bandpass Filter**

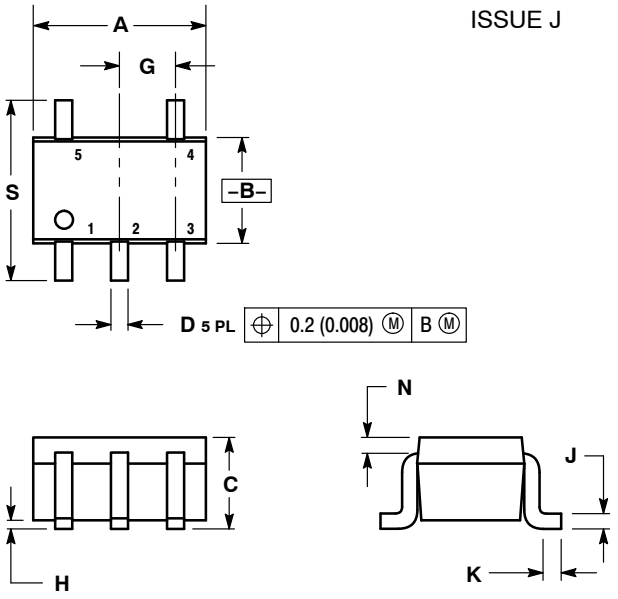
## ORDERING INFORMATION

| Order Number | Number of Channels | Specific Device Marking | Package Type | Shipping† |
|---|---|---|---|---|
| LMV321SQ3T2G | Single | AAC | SC−70 (Pb−Free) | 3000 / Tape & Reel |
| LMV321SN3T1G* | Single | 3AC | TSOP−5 (Pb−Free) | 3000 / Tape & Reel |
| LMV358DMR2G | Dual | V358 | Micro8 (Pb−Free) | 4000 / Tape & Reel |
| LMV358MUTAG | Dual | AC | UDFN8 (Pb−Free) | 3000 / Tape & Reel |
| LMV358DR2G | Dual | V358 | SOIC−8 (Pb−Free) | 2500 / Tape & Reel |
| LMV324DR2G | Quad | LMV324 | SOIC−14 (Pb−Free) | 2500 / Tape & Reel |
| LMV324DTBR2G | Quad | LMV 324 | TSSOP−14 (Pb−Free) | 2500 / Tape & Reel |

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.
*Contact factory.

## PACKAGE DIMENSIONS

**SC−88A, SOT−353, SC−70**
CASE 419A−02
ISSUE J

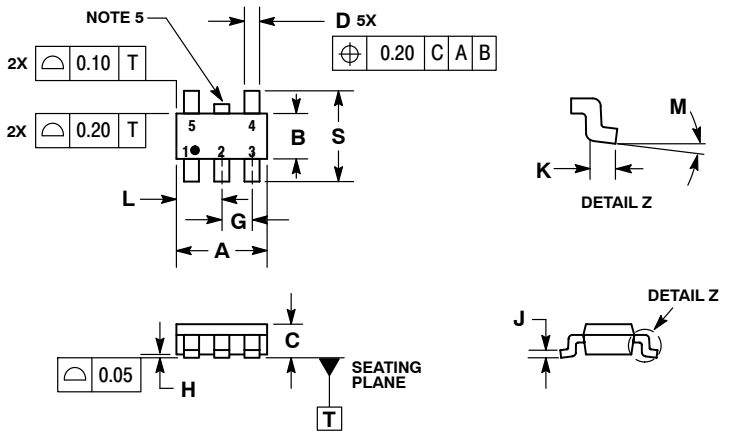



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. 419A−01 OBSOLETE. NEW STANDARD 419A−02.
4. DIMENSIONS A AND B DO NOT INCLUDE MOLD FLASH, PROTRUSIONS, OR GATE BURRS.

| | INCHES | | MILLIMETERS | |
|---|---|---|---|---|
| DIM | MIN | MAX | MIN | MAX |
| A | 0.071 | 0.087 | 1.80 | 2.20 |
| B | 0.045 | 0.053 | 1.15 | 1.35 |
| C | 0.031 | 0.043 | 0.80 | 1.10 |
| D | 0.004 | 0.012 | 0.10 | 0.30 |
| G | 0.026 BSC | | 0.65 BSC | |
| H | --- | 0.004 | --- | 0.10 |
| J | 0.004 | 0.010 | 0.10 | 0.25 |
| K | 0.004 | 0.012 | 0.10 | 0.30 |
| N | 0.008 REF | | 0.20 REF | |
| S | 0.079 | 0.087 | 2.00 | 2.20 |

## PACKAGE DIMENSIONS

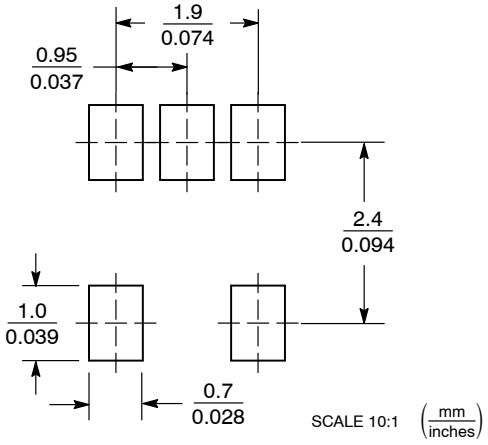
**TSOP−5**
CASE 483−02
ISSUE H




NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. MAXIMUM LEAD THICKNESS INCLUDES LEAD FINISH THICKNESS. MINIMUM LEAD THICKNESS IS THE MINIMUM THICKNESS OF BASE MATERIAL.
4. DIMENSIONS A AND B DO NOT INCLUDE MOLD FLASH, PROTRUSIONS, OR GATE BURRS.
5. OPTIONAL CONSTRUCTION: AN ADDITIONAL TRIMMED LEAD IS ALLOWED IN THIS LOCATION. TRIMMED LEAD NOT TO EXTEND MORE THAN 0.2 FROM BODY.

| | MILLIMETERS | |
|---|---|---|
| DIM | MIN | MAX |
| A | 3.00 BSC | |
| B | 1.50 BSC | |
| C | 0.90 | 1.10 |
| D | 0.25 | 0.50 |
| G | 0.95 BSC | |
| H | 0.01 | 0.10 |
| J | 0.10 | 0.26 |
| K | 0.20 | 0.60 |
| L | 1.25 | 1.55 |
| M | 0 ° | 10 ° |
| S | 2.50 | 3.00 |

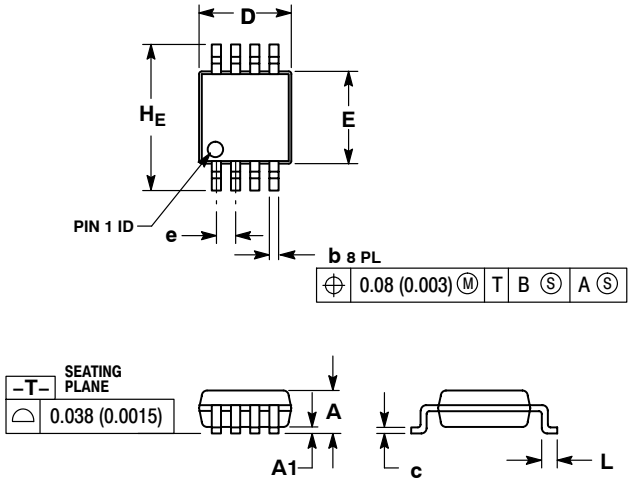
### SOLDERING FOOTPRINT*




*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

## PACKAGE DIMENSIONS

**Micro8™**
CASE 846A−02
ISSUE H



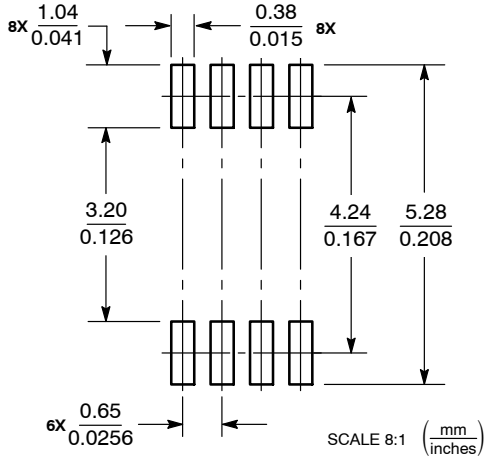




NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSION A DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS. MOLD FLASH, PROTRUSIONS OR GATE BURRS SHALL NOT EXCEED 0.15 (0.006) PER SIDE.
4. DIMENSION B DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION. INTERLEAD FLASH OR PROTRUSION SHALL NOT EXCEED 0.25 (0.010) PER SIDE.
5. 846A−01 OBSOLETE, NEW STANDARD 846A−02.

| | MILLIMETERS | | | INCHES | | |
|---|---|---|---|---|---|---|
| DIM | MIN | NOM | MAX | MIN | NOM | MAX |
| A | −− | −− | 1.10 | −− | −− | 0.043 |
| A1 | 0.05 | 0.08 | 0.15 | 0.002 | 0.003 | 0.006 |
| b | 0.25 | 0.33 | 0.40 | 0.010 | 0.013 | 0.016 |
| c | 0.13 | 0.18 | 0.23 | 0.005 | 0.007 | 0.009 |
| D | 2.90 | 3.00 | 3.10 | 0.114 | 0.118 | 0.122 |
| E | 2.90 | 3.00 | 3.10 | 0.114 | 0.118 | 0.122 |
| e | | 0.65 BSC | | | 0.026 BSC | |
| L | 0.40 | 0.55 | 0.70 | 0.016 | 0.021 | 0.028 |
| $H_E$ | 4.75 | 4.90 | 5.05 | 0.187 | 0.193 | 0.199 |

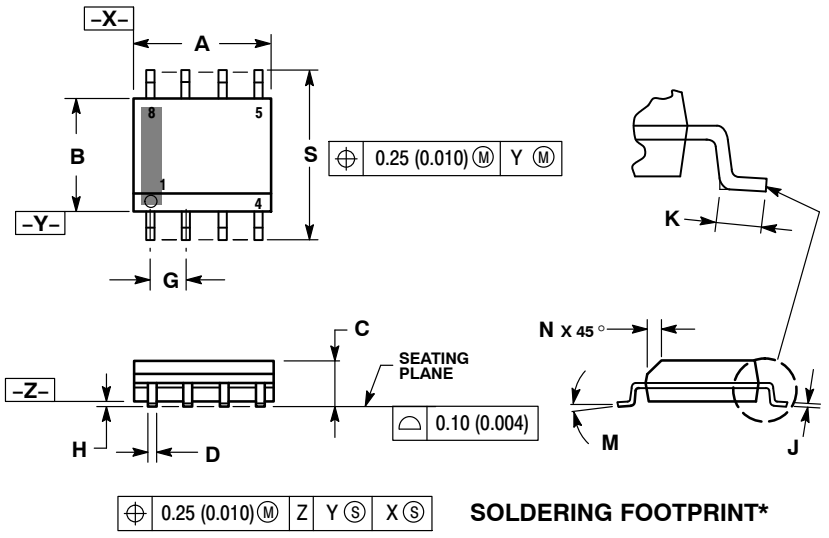
## SOLDERING FOOTPRINT*




*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

## PACKAGE DIMENSIONS

**SOIC−8 NB**
CASE 751−07
ISSUE AJ

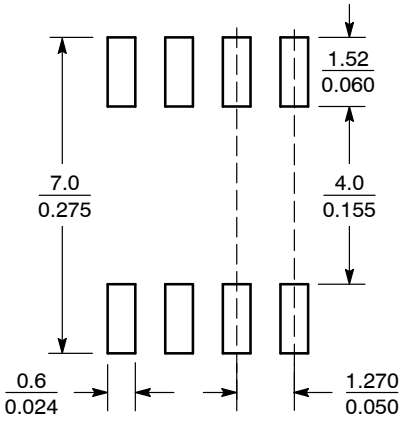



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSION A AND B DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15 (0.006) PER SIDE.
5. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.127 (0.005) TOTAL IN EXCESS OF THE D DIMENSION AT MAXIMUM MATERIAL CONDITION.
6. 751−01 THRU 751−06 ARE OBSOLETE. NEW STANDARD IS 751−07.

| | MILLIMETERS | | INCHES | |
|---|---|---|---|---|
| DIM | MIN | MAX | MIN | MAX |
| A | 4.80 | 5.00 | 0.189 | 0.197 |
| B | 3.80 | 4.00 | 0.150 | 0.157 |
| C | 1.35 | 1.75 | 0.053 | 0.069 |
| D | 0.33 | 0.51 | 0.013 | 0.020 |
| G | 1.27 BSC | | 0.050 BSC | |
| H | 0.10 | 0.25 | 0.004 | 0.010 |
| J | 0.19 | 0.25 | 0.007 | 0.010 |
| K | 0.40 | 1.27 | 0.016 | 0.050 |
| M | 0° | 8° | 0° | 8° |
| N | 0.25 | 0.50 | 0.010 | 0.020 |
| S | 5.80 | 6.20 | 0.228 | 0.244 |

0.25 (0.010) M Z Y S X S

**SOLDERING FOOTPRINT***

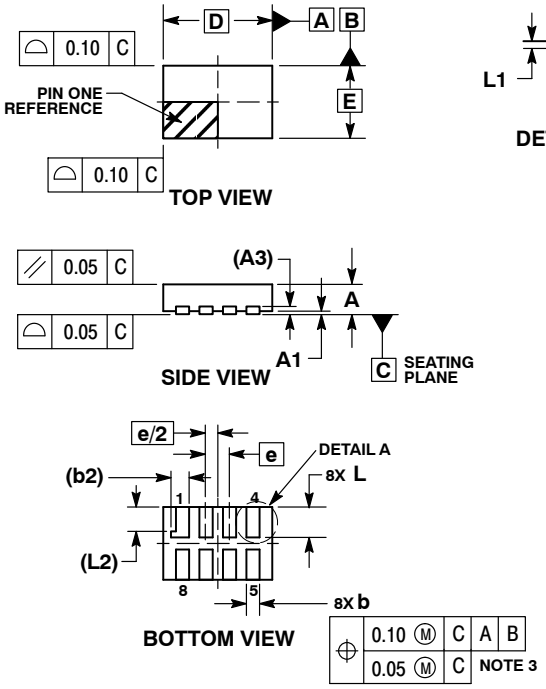



SCALE 6:1 (mm / inches)

*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

## PACKAGE DIMENSIONS

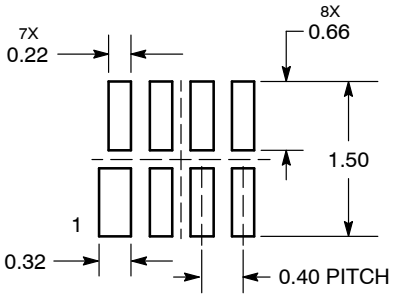
**UDFN8 1.8x1.2, 0.4P**
CASE 517AJ−01
ISSUE O




NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. DIMENSION b APPLIES TO PLATED TERMINAL AND IS MEASURED BETWEEN 0.15 AND 0.30 mm FROM TERMINAL TIP.
4. MOLD FLASH ALLOWED ON TERMINALS ALONG EDGE OF PACKAGE. FLASH MAY NOT EXCEED 0.03 ONTO BOTTOM SURFACE OF TERMINALS.
5. DETAIL A SHOWS OPTIONAL CONSTRUCTION FOR TERMINALS.

| | MILLIMETERS | |
|---|---|---|
| DIM | MIN | MAX |
| A | 0.45 | 0.55 |
| A1 | 0.00 | 0.05 |
| A3 | 0.127 REF | |
| b | 0.15 | 0.25 |
| b2 | 0.30 REF | |
| D | 1.80 BSC | |
| E | 1.20 BSC | |
| e | 0.40 BSC | |
| L | 0.45 | 0.55 |
| L1 | 0.00 | 0.03 |
| L2 | 0.40 REF | |

**MOUNTING FOOTPRINT***
**SOLDERMASK DEFINED**

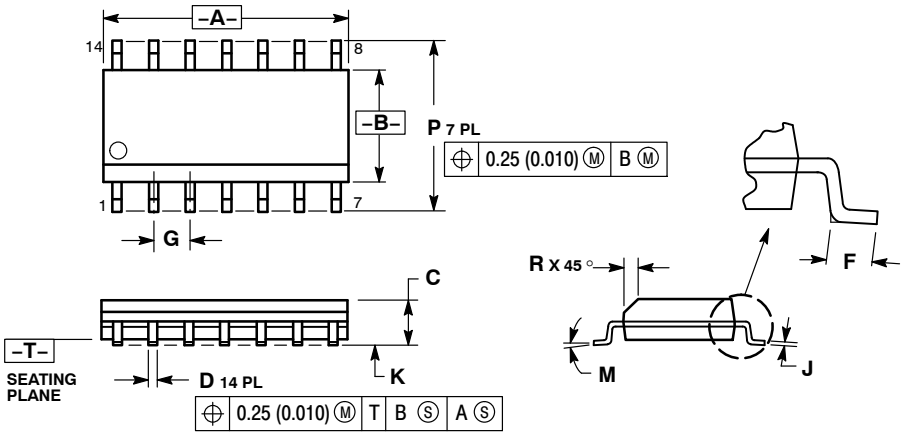



DIMENSIONS: MILLIMETERS

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## PACKAGE DIMENSIONS

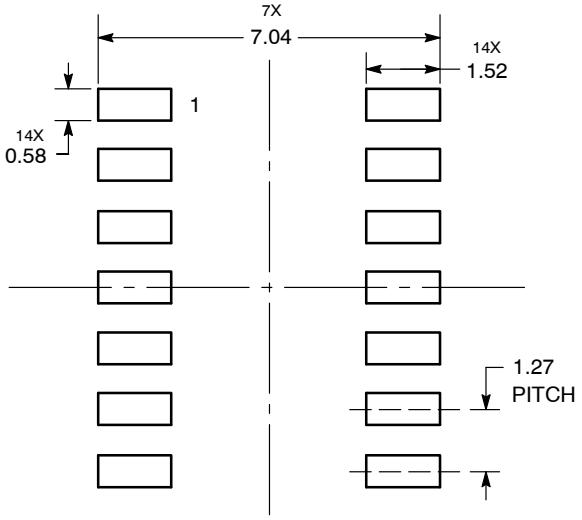
**SOIC−14**
CASE 751A−03
ISSUE J




NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSIONS A AND B DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15 (0.006) PER SIDE.
5. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.127 (0.005) TOTAL IN EXCESS OF THE D DIMENSION AT MAXIMUM MATERIAL CONDITION.

| | MILLIMETERS | | INCHES | |
|---|---|---|---|---|
| DIM | MIN | MAX | MIN | MAX |
| A | 8.55 | 8.75 | 0.337 | 0.344 |
| B | 3.80 | 4.00 | 0.150 | 0.157 |
| C | 1.35 | 1.75 | 0.054 | 0.068 |
| D | 0.35 | 0.49 | 0.014 | 0.019 |
| F | 0.40 | 1.25 | 0.016 | 0.049 |
| G | 1.27 BSC | | 0.050 BSC | |
| J | 0.19 | 0.25 | 0.008 | 0.009 |
| K | 0.10 | 0.25 | 0.004 | 0.009 |
| M | 0 ° | 7 ° | 0 ° | 7 ° |
| P | 5.80 | 6.20 | 0.228 | 0.244 |
| R | 0.25 | 0.50 | 0.010 | 0.019 |

## SOLDERING FOOTPRINT

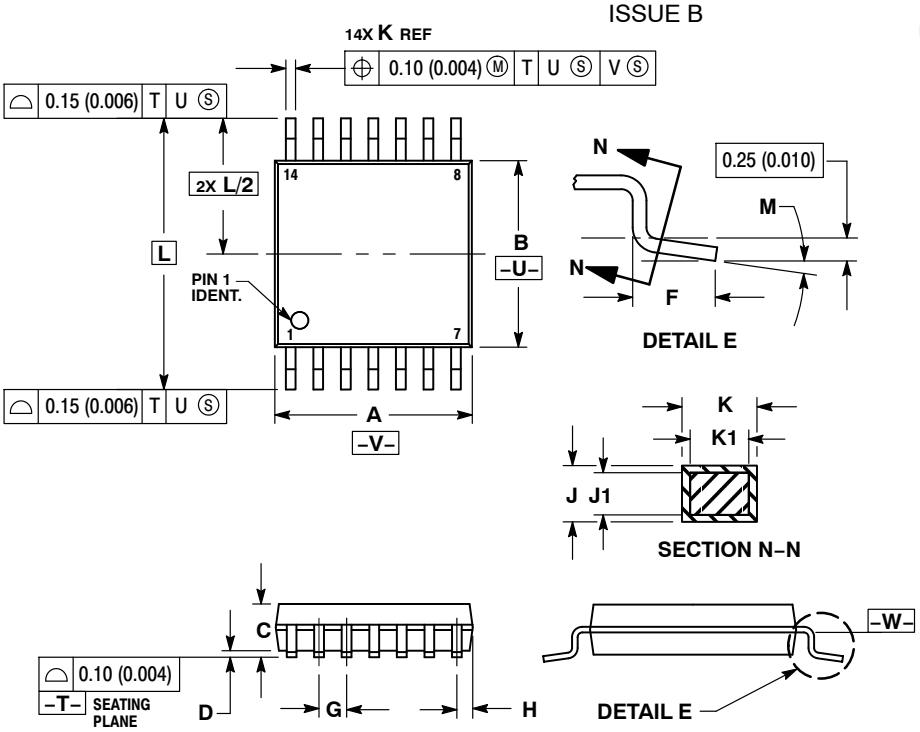



DIMENSIONS: MILLIMETERS

*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

## PACKAGE DIMENSIONS

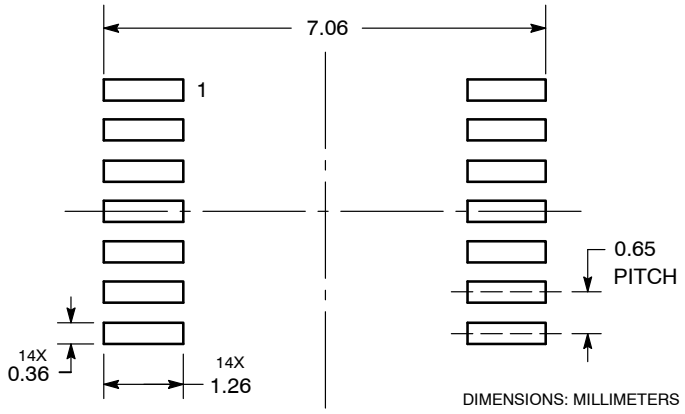
**TSSOP−14**
CASE 948G−01
ISSUE B




NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSION A DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS. MOLD FLASH OR GATE BURRS SHALL NOT EXCEED 0.15 (0.006) PER SIDE.
4. DIMENSION B DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION. INTERLEAD FLASH OR PROTRUSION SHALL NOT EXCEED 0.25 (0.010) PER SIDE.
5. DIMENSION K DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08 (0.003) TOTAL IN EXCESS OF THE K DIMENSION AT MAXIMUM MATERIAL CONDITION.
6. TERMINAL NUMBERS ARE SHOWN FOR REFERENCE ONLY.
7. DIMENSION A AND B ARE TO BE DETERMINED AT DATUM PLANE −W−.

| | MILLIMETERS | | INCHES | |
|---|---|---|---|---|
| DIM | MIN | MAX | MIN | MAX |
| A | 4.90 | 5.10 | 0.193 | 0.200 |
| B | 4.30 | 4.50 | 0.169 | 0.177 |
| C | --- | 1.20 | --- | 0.047 |
| D | 0.05 | 0.15 | 0.002 | 0.006 |
| F | 0.50 | 0.75 | 0.020 | 0.030 |
| G | 0.65 BSC | | 0.026 BSC | |
| H | 0.50 | 0.60 | 0.020 | 0.024 |
| J | 0.09 | 0.20 | 0.004 | 0.008 |
| J1 | 0.09 | 0.16 | 0.004 | 0.006 |
| K | 0.19 | 0.30 | 0.007 | 0.012 |
| K1 | 0.19 | 0.25 | 0.007 | 0.010 |
| L | 6.40 BSC | | 0.252 BSC | |
| M | 0 ° | 8 ° | 0 ° | 8 ° |

### SOLDERING FOOTPRINT*




*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

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