# LMU112
## 12 x 12-bit Parallel Multiplier

## FEATURES

- 25 ns Worst-Case Multiply Time
- Low Power CMOS Technology
- Replaces Fairchild MPY112K
- Two's Complement or Unsigned Operands
- Three-State Outputs
- Package Styles Available:
  - 48-pin PDIP
  - 52-pin PLCC, J-Lead

## DESCRIPTION

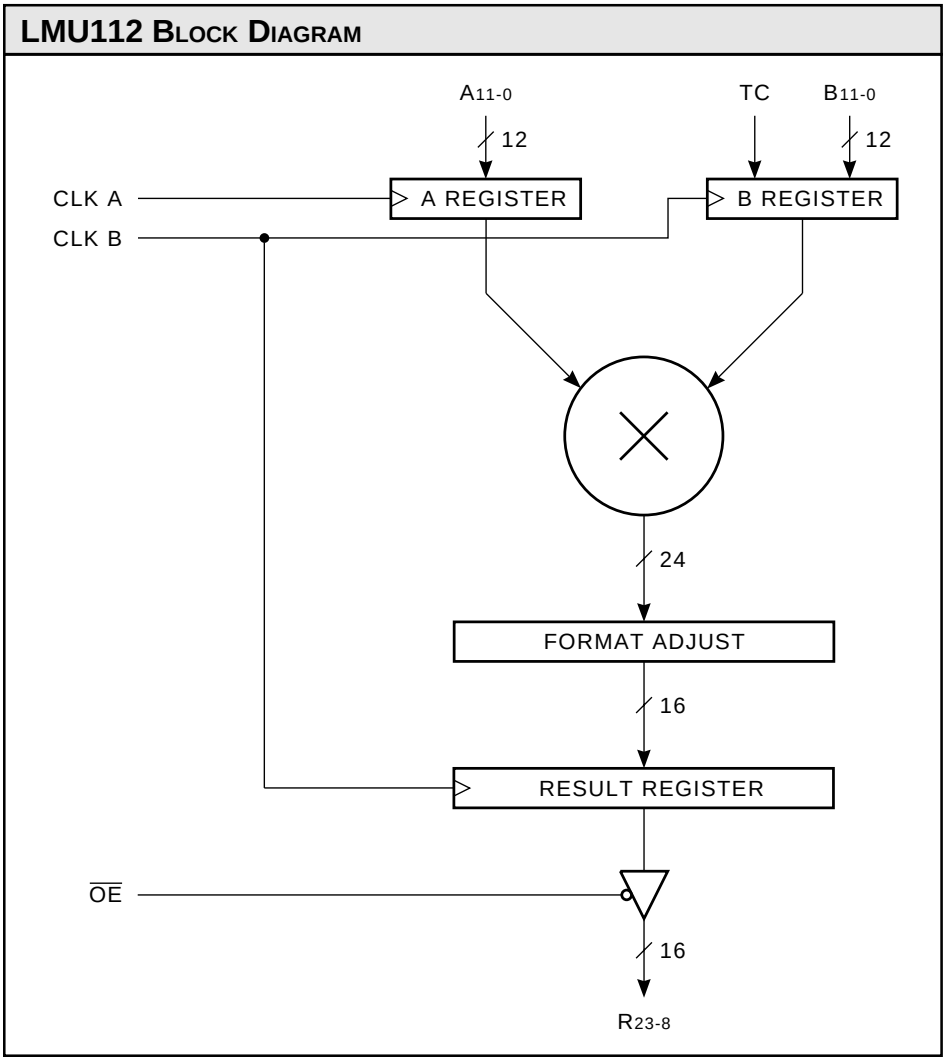
The **LMU112** is a high-speed, low power 12-bit parallel multiplier built using advanced CMOS technology. The LMU112 is pin and functionally compatible with Fairchilds's MPY112K.

The A and B input operands are loaded into their respective registers on the rising edge of the separate clock inputs (CLK A and CLK B). Two's complement or unsigned magnitude operands are accommodated via the operand control bit (TC) which is loaded along with the B operands. The operands are specified to be in two's complement format when TC is asserted and unsigned magnitude when TC is deasserted. Mixed mode operation is not allowed.

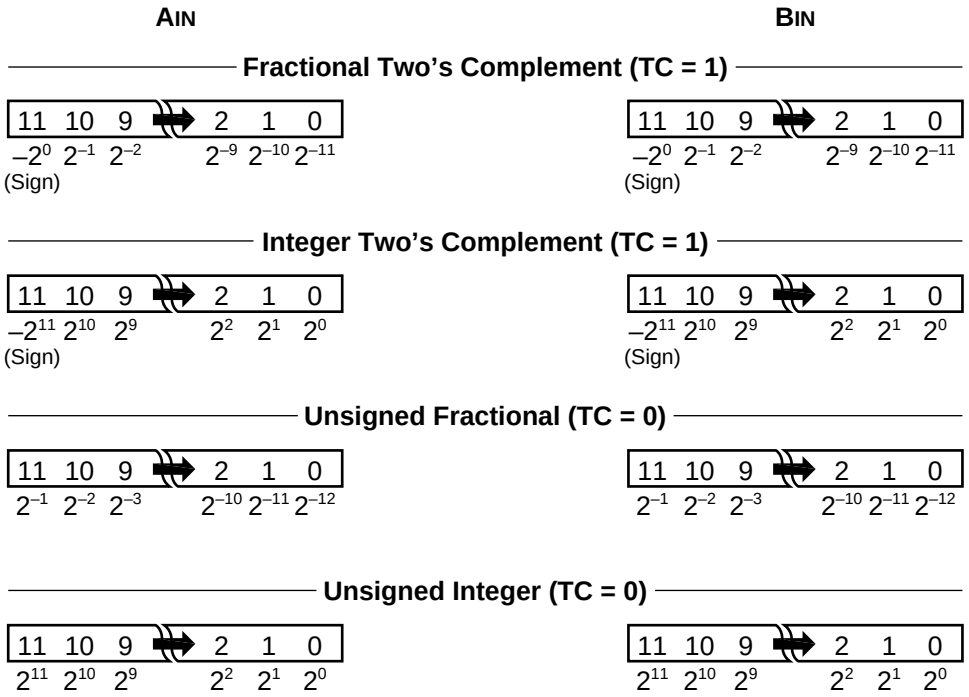
For two's complement operands, the 17 most significant bits at the output of the asynchronous multiplier array are shifted one bit position to the left. This is done to discard the redundant copy of the sign-bit, which is in the most significant bit position, and extend the bit precision by one bit. The result is then truncated to the 16 MSB's and loaded into the output register on the rising edge of CLK B.

The contents of the output register are made available via three-state buffers by asserting $\overline{OE}$. When $\overline{OE}$ is de-asserted, the outputs ($R_{23-8}$) are in the high impedance state.

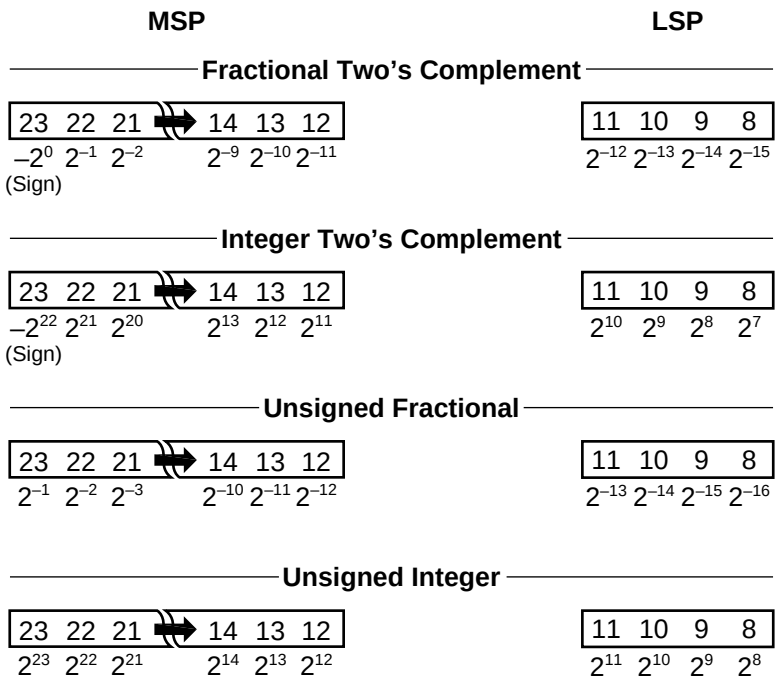
## LMU112 BLOCK DIAGRAM



## FIGURE 1A. INPUT FORMATS




## FIGURE 1B. OUTPUT FORMATS



## MAXIMUM RATINGS *Above which useful life may be impaired (Notes 1, 2, 3, 8)*

Storage temperature ..... –65°C to +150°C
Operating ambient temperature ..... –55°C to +125°C
**V**CC supply voltage with respect to ground ..... –0.5 V to +7.0 V
Input signal with respect to ground ..... –3.0 V to +7.0 V
Signal applied to high impedance output ..... –3.0 V to +7.0 V
Output current into low outputs ..... 25 mA
Latchup current ..... > 400 mA

## OPERATING CONDITIONS *To meet specified electrical and switching characteristics*

| Mode | **Temperature Range** (Ambient) | **Supply Voltage** |
|---|---|---|
| Active Operation, Commercial | 0°C to +70°C | 4.75 V ≤ **V**CC ≤ 5.25 V |
| Active Operation, Military | –55°C to +125°C | 4.50 V ≤ **V**CC ≤ 5.50 V |

## ELECTRICAL CHARACTERISTICS *Over Operating Conditions (Note 4)*

| Symbol | Parameter | Test Condition | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| **V**OH | Output High Voltage | **V**CC = Min., **I**OH = –2.0 mA | 2.4 | | | V |
| **V**OL | Output Low Voltage | **V**CC = Min., **I**OL = 8.0 mA | | | 0.5 | V |
| **V**IH | Input High Voltage | | 2.0 | | **V**CC | V |
| **V**IL | Input Low Voltage | (Note 3) | 0.0 | | 0.8 | V |
| **I**IX | Input Current | Ground ≤ **V**IN ≤ **V**CC (Note 12) | | | ±20 | µA |
| **I**OZ | Output Leakage Current | Ground ≤ **V**OUT ≤ **V**CC (Note 12) | | | ±20 | µA |
| **I**CC1 | **V**CC Current, Dynamic | (Notes 5, 6) | | 10 | 20 | mA |
| **I**CC2 | **V**CC Current, Quiescent | (Note 7) | | | 1.0 | mA |

## SWITCHING CHARACTERISTICS

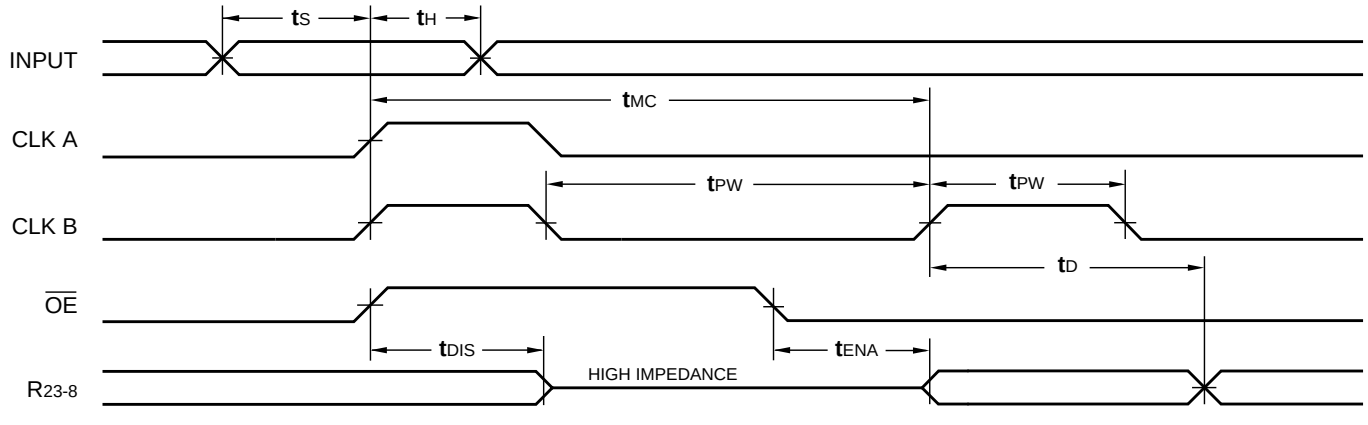
### COMMERCIAL OPERATING RANGE (0°C to +70°C) *Notes 9, 10 (ns)*

| | | LMU112– | | | | | |
|---|---|---|---|---|---|---|---|
| | | 60* | | 50 | | 25 | |
| Symbol | Parameter | Min | Max | Min | Max | Min | Max |
| $t_{MC}$ | Clocked Multiply Time | | 60 | | 50 | | 25 |
| $t_{PW}$ | Clock Pulse Width | 15 | | 15 | | 10 | |
| $t_S$ | Input Register Setup Time | 15 | | 15 | | 10 | |
| $t_H$ | Input Register Hold Time | 3 | | 3 | | 1 | |
| $t_D$ | Output Delay | | 25 | | 25 | | 20 |
| $t_{ENA}$ | Three-State Output Enable Delay (Note 11) | | 25 | | 25 | | 20 |
| $t_{DIS}$ | Three-State Output Disable Delay (Note 11) | | 25 | | 25 | | 20 |

### MILITARY OPERATING RANGE (–55°C to +125°C) *Notes 9, 10 (ns)*

| | | LMU112– | | | | | |
|---|---|---|---|---|---|---|---|
| | | 65* | | 55* | | 30* | |
| Symbol | Parameter | Min | Max | Min | Max | Min | Max |
| $t_{MC}$ | Clocked Multiply Time | | 65 | | 55 | | 30 |
| $t_{PW}$ | Clock Pulse Width | 20 | | 20 | | 12 | |
| $t_S$ | Input Register Setup Time | 15 | | 15 | | 12 | |
| $t_H$ | Input Register Hold Time | 3 | | 3 | | 3 | |
| $t_D$ | Output Delay | | 30 | | 30 | | 25 |
| $t_{ENA}$ | Three-State Output Enable Delay (Note 11) | | 30 | | 30 | | 25 |
| $t_{DIS}$ | Three-State Output Disable Delay (Note 11) | | 30 | | 30 | | 25 |

### SWITCHING WAVEFORMS




*DISCONTINUED SPEED GRADE

## NOTES

1. Maximum Ratings indicate stress specifications only. Functional operation of these products at values beyond those indicated in the Operating Conditions table is not implied. Exposure to maximum rating conditions for extended periods may affect reliability.

2. The products described by this specification include internal circuitry designed to protect the chip from damaging substrate injection currents and accumulations of static charge. Nevertheless, conventional precautions should be observed during storage, handling, and use of these circuits in order to avoid exposure to excessive electrical stress values.

3. This device provides hard clamping of transient undershoot and overshoot. Input levels below ground or above $V_{CC}$ will be clamped beginning at –0.6 V and $V_{CC}$ + 0.6 V. The device can withstand indefinite operation with inputs in the range of –0.5 V to +7.0 V. Device operation will not be adversely affected, however, input current levels will be well in excess of 100 mA.

4. Actual test conditions may vary from those designated but operation is guaranteed as specified.

5. Supply current for a given application can be accurately approximated by:

$$\frac{NCV^2F}{4}$$

where

N = total number of device outputs
C = capacitive load per output
V = supply voltage
F = clock frequency

6. Tested with all outputs changing every cycle and no load, at a 5 MHz clock rate.

7. Tested with all inputs within 0.1 V of $V_{CC}$ or Ground, no load.

8. These parameters are guaranteed but not 100% tested.

9. AC specifications are tested with input transition times less than 3 ns, output reference levels of 1.5 V (except $t_{DIS}$ test), and input levels of nominally 0 to 3.0 V. Output loading may be a resistive divider which provides for specified $I_{OH}$ and $I_{OL}$ at an output voltage of $V_{OH}$ min and $V_{OL}$ max respectively. Alternatively, a diode bridge with upper and lower current sources of $I_{OH}$ and $I_{OL}$ respectively, and a balancing voltage of 1.5 V may be used. Parasitic capacitance is 30 pF minimum, and may be distributed.

This device has high-speed outputs capable of large instantaneous current pulses and fast turn-on / turn-off times. As a result, care must be exercised in the testing of this device. The following measures are recommended:

a. A 0.1 µF ceramic capacitor should be installed between $V_{CC}$ and Ground leads as close to the Device Under Test (DUT) as possible. Similar capacitors should be installed between device $V_{CC}$ and the tester common, and device ground and tester common.

b. Ground and $V_{CC}$ supply planes must be brought directly to the DUT socket or contactor fingers.

c. Input voltages should be adjusted to compensate for inductive ground and $V_{CC}$ noise to maintain required DUT input levels relative to the DUT ground pin.

10. Each parameter is shown as a minimum or maximum value. Input requirements are specified from the point of view of the external system driving the chip. Setup time, for example, is specified as a minimum since the external system must supply at least that much time to meet the worst-case requirements of all parts. Responses from the internal circuitry are specified from the point of view of the device. Output delay, for example, is specified as a maximum since worst-case operation of any device always provides data within that time.

11. For the $t_{ENA}$ test, the transition is measured to the 1.5 V crossing point with datasheet loads. For the $t_{DIS}$ test, the transition is measured to the ±200mV level from the measured steady-state output voltage with ±10mA loads. The balancing voltage, $V_{TH}$, is set at 3.5 V for Z-to-0 and 0-to-Z tests, and set at 0 V for Z-to-1 and 1-to-Z tests.

12. These parameters are only tested at the high temperature extreme, which is the worst case for leakage current.

**FIGURE A. OUTPUT LOADING CIRCUIT**

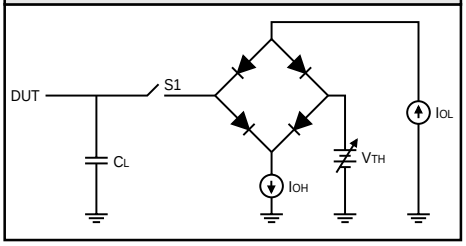
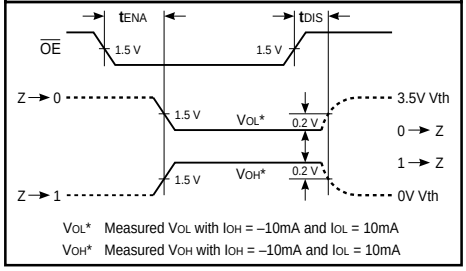
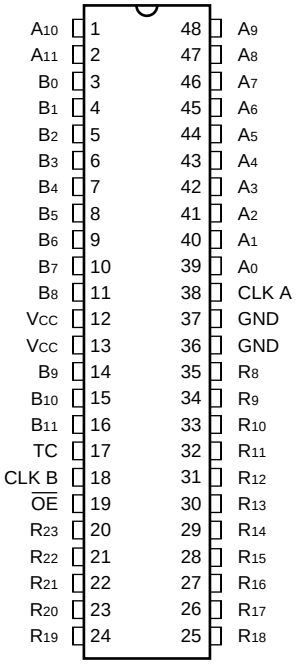



**FIGURE B. THRESHOLD LEVELS**

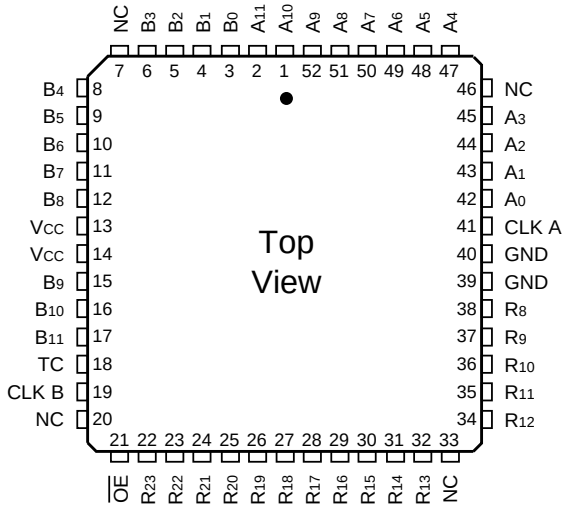


## ORDERING INFORMATION

**48-pin**




**52-pin**




| Speed | Plastic DIP (P5) | | Plastic J-Lead Chip Carrier (J5) |
|---|---|---|---|
| | **0°C to +70°C — COMMERCIAL SCREENING** | | |
| 50 ns | LMU112PC50 | | LMU112JC50 |
| 25 ns | LMU112PC25 | | LMU112JC25 |
| | **–55°C to +125°C — COMMERCIAL SCREENING** | | |
| | | | |
| | **–55°C to +125°C — MIL-STD-883 COMPLIANT** | | |
| | | | |