LMP92001 Analog System Monitor and Controller

Check for Samples: LMP92001

FEATURES

- **16 Analog Voltage Monitoring Channels**
  - **12-bit ADC with Programmable Input MUX**
  - **No Missing Codes**
  - **Total Unadjusted Error (TUE) ±0.1%**
  - **Single-Shot or Continuous Conversion Modes**
  - **Programmable Window Comparator Function**
  - **Interrupt Signal Generation for Input Out-of-Bound Condition**
- **12 Programmable Analog Voltage Outputs**
  - **Twelve 12-bit DACs**
  - **Specified Monotonic**
  - **Settling Time 8.5 µs**
  - **Simultaneous Update of All Channels to Same Value**
  - **Asynchronous Output Control Forces Rail Voltage at Output**
- **Voltage Reference**
  - **User-Selectable Source: External or Internal**
  - **Internal Reference 4.5V ±0.7%**
- **Analog Temperature Sensor**
  - **Readable via ADC Channel 17**
  - **Temperature Error ±2°C**
- **8-bit GPIO Port**
  - **Each Bit Individually Programmable**
- **I^2C-Compatible Bus**
  - **Supports Standard and Fast Modes**
  - **Bus TIMEOUT Function**
  - **Supports Block Data Transfers**

APPLICATIONS

- **RF PA Bias Monitoring and Control**
- **System Monitoring and Control**
- **Industrial Monitoring and Control**
- **Test Equipment and Instrumentation**

DESCRIPTION

The LMP92001 is a complete analog monitoring and control circuit which includes a sixteen channel 12-bit Analog to Digital Converter (ADC), twelve 12-bit Digital to Analog Converters (DACs), an internal reference, an internal temp sensor, an 8-bit GPIO port, and an I^2C-compatible interface.

The ADC can be used to monitor rail voltages, current sense amplifier outputs or sensors and includes a programmable window comparator function on six of its 16 channels to detect out-of range conditions.

The DACs can be used to control PA bias points, actuators, potentiometers, etc. When required, the outputs can be instantaneously driven to either supply rail using the output switches and the asynchronous DAC control inputs.

Both ADC and DACs can use either the internal 4.5V reference or an external reference independently.

The built-in temperature sensor is treated as the 17th analog sense input. In addition, the 8-bit GPIO port allows for the resources of the microcontroller to be further extended, providing even more flexibility.

The LMP92001 is available in a space saving 54-pin WQFN package and is operational over the full −40°C to 125°C temperature range.

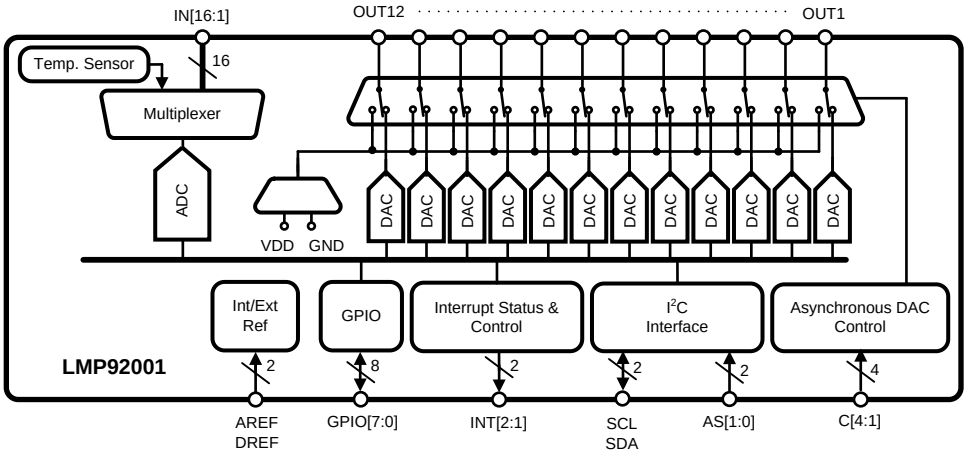
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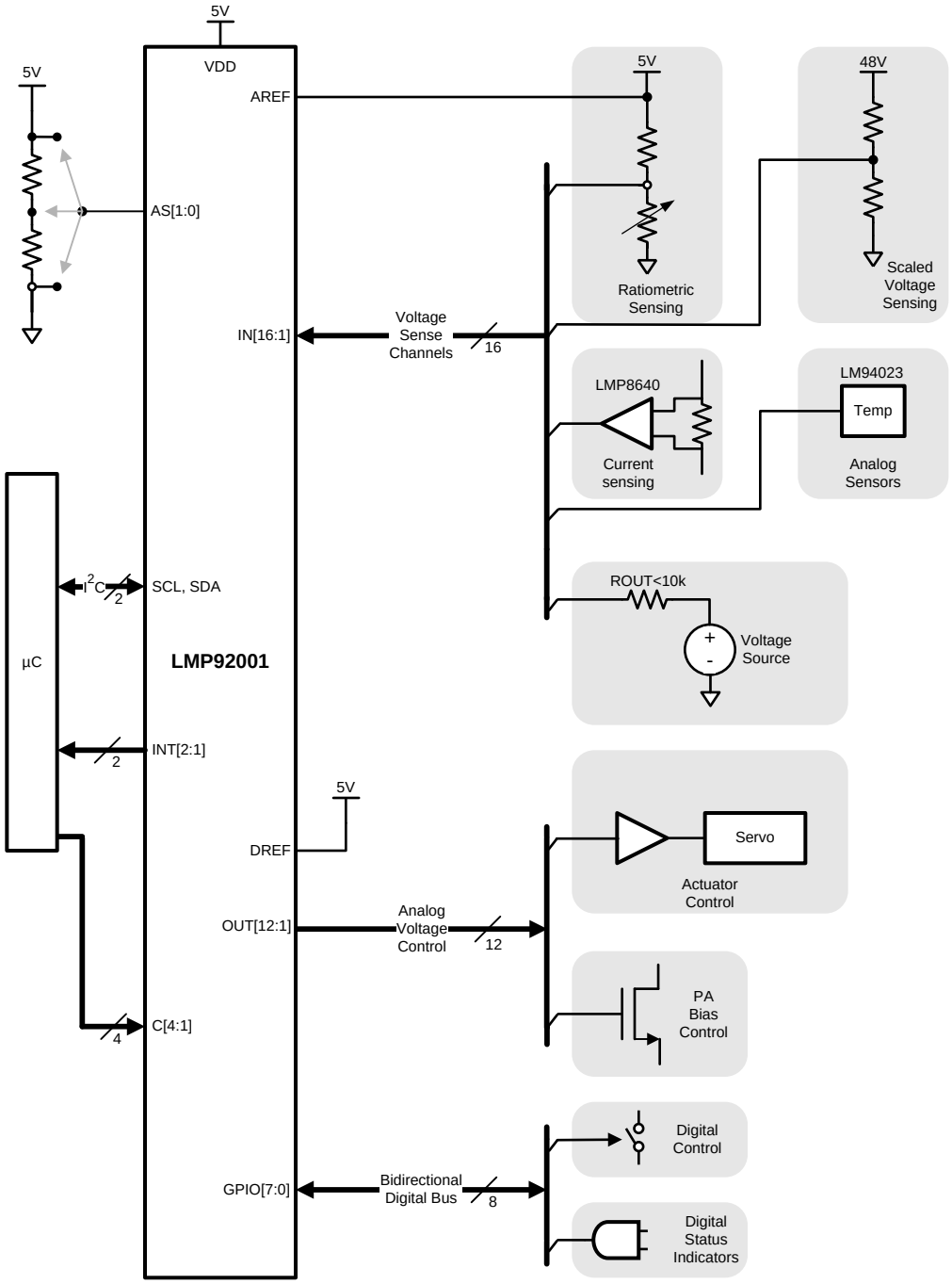
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Block Diagram



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Typical Application



Overview

The LMP92001 has a flexible, feature-rich functionality which makes it ideally suited for many analog monitoring and control applications, for example base-station PA subsystems. This device provides the analog interface between a programmable supervisor, such as a microcontroller, and an analog system whose behavior is to be monitored and controlled by the supervisor.

To facilitate analog monitoring functionality, the device contains a single 12-bit ADC fronted by a 17-input multiplexor. The 16 MUX inputs are available to the user via pins IN[16:1]. The last remaining MUX channel is reserved for the internal analog temperature sensor.

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The analog control functionality is served by twelve 12-bit voltage output DACs. Besides producing voltage corresponding to the digital input code, the DACs can be forced by the user to either rail instantaneously.

Additional digital monitoring and control can be realized via the General Purpose I/O port GPIO[7:0].

Two more blocks are present for added functionality: a local temperature sensor (already mentioned above) and an internal reference voltage generator.

17-CHANNEL ANALOG SENSE WITH 12-BIT ADC

The user can monitor up to 16 external voltages with the 12-bit ADC and its 17-channel input MUX. Typically these voltages will be generated by the analog sensors, instrumentation amplifiers, current sense amplifiers, or simply resistive dividers if high potentials need to be measured. Channel 17 of the input MUX is reserved for the internal temperature sensor, and is not available as an external input to the device.

User can program which MUX channels to enable, and whether to convert these channel inputs in sequence continuously, or in a single-shot mode. Upon completion all conversion results are stored in the internal data registers, and can be read back by the user via the I^2C-compatible interface.

Analog input channels 1-3 and 9-11 have a built-in digital window comparator function with user programmable thresholds. This function can be used to alert the supervisor microcontroller of an out-of-bound condition. The comparator function result is stored in the internal status register which is user accessible. It can also be used as the interrupt signal generator where the out of bound conditions will be reported via the INT[2:1] output pins.

Sequencing of the analog sense system is governed by the internal controller. Once enabled the MUX, the ADC, the window comparator and the interrupts perform their function without further user intervention.

PROGRAMMABLE ANALOG CONTROL VOLTAGE OUTPUTS

Twelve identical individually programmable 12-bit DAC blocks are available to generate analog voltages, which can be used to control bias conditions of external circuits, position of servos, etc.

In case simultaneous update of all outputs to the same level is needed, a single internal register is provided that effects simultaneous update of all DAC data registers.

A DAC, by definition, produces an output in the range of GND to DREF. In some systems, however, it may be desirable for the OUT pins to produce either GND or VDD, i.e., beyond DREF. This is made possible via the asynchronous DAC control inputs C[4:1]. When activated, these inputs will force the OUT pins to either rail. The choice of rail is made in the internal control register.

INTERNAL ANALOG TEMPERATURE SENSOR

An on-board analog temperature sensor is available to monitor the device's own temperature. Once enabled, the analog temperature sensor output is sampled via the MUX channel 17, and its conversion result is stored in the internal register for user read back.

INTERNAL VOLTAGE REFERENCE SOURCE

Another resource available to the user is the internal, temperature-compensated reference voltage source. By default both ADC and DACs expect reference potentials to be supplied externally. The user can choose to enable the internal reference and use it with the ADC and/or the DACs.

The internal reference source cannot drive an external load.

8-BIT GENERAL PURPOSE I/O

The GPIO port can be used to expand the microcontroller capabilities. This port is memory mapped to the internal register, which in turn is accessible via the I^2C-compatible interface. Since each bit is individually programmable as an Input or Output, the port is ideally suited for external switch control and status flag monitoring, without further burdening of microcontroller I/O resources.

I^2C-COMPATIBLE INTERFACE

The microcontroller supervisor communicates with LMP92001 via a popular I^2C-compatible 2–wire interface. This interface provides the user full access to all Data, Status and Control registers of the device.

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There are 2 address setting pins, AS[1:0], that allow the device to occupy any one of 9 possible Interface Addresses on the bus.

Block Access commands are provided to minimize the transfer overhead of larger data sets.

Connection Diagram

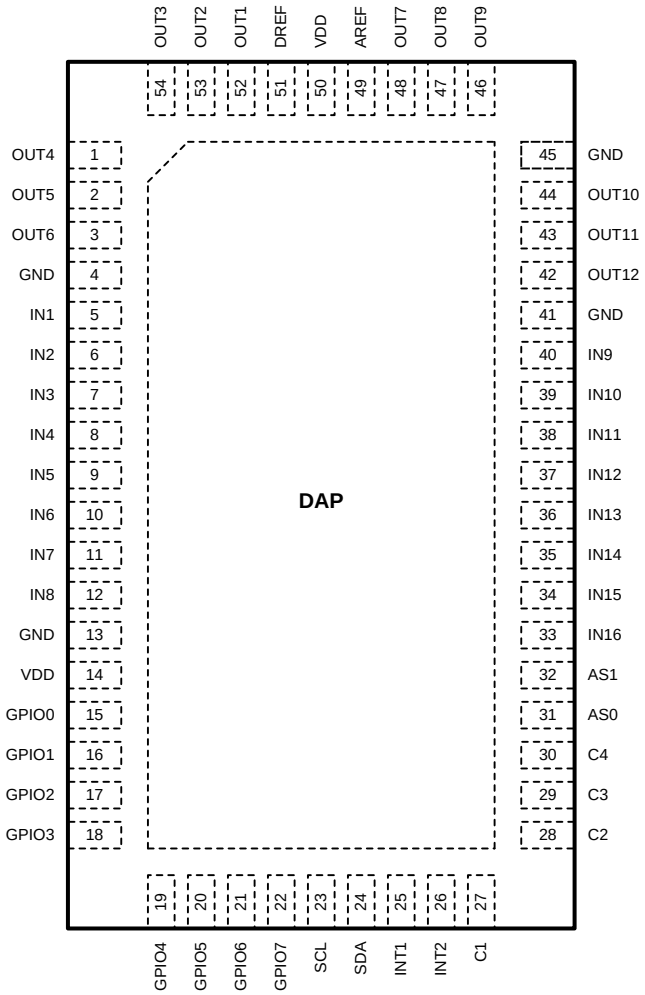
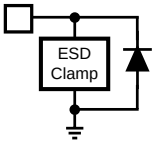
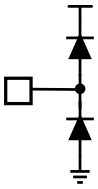
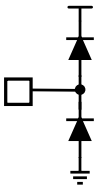
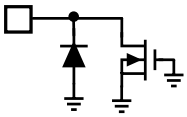
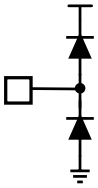


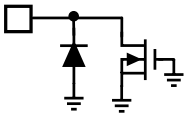
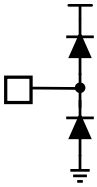
Figure 1. WQFN-54 (NJY0054A)
Top View

Pin Descriptions

Name	Pin	ESD Structures	Function
VDD	14, 50		Supply rail
GND	4, 13, 41, 45		Device Ground
IN1	5		Analog Voltage Sense Inputs
IN2	6		
IN3	7		
IN4	8		
IN5	9		
IN6	10		
IN7	11		
IN8	12		
IN9	40		
IN10	39		
IN11	38		
IN12	37		
IN13	36		
IN14	35		
IN15	34		
IN16	33		
OUT1	52		Analog Control Voltage Outputs
OUT2	53		
OUT3	54		
OUT4	1		
OUT5	2		
OUT6	3		
OUT7	48		
OUT8	47		
OUT9	46		
OUT10	44		
OUT11	43		
OUT12	42		
SCL	23		I^2C-compatible clock input
SDA	24		Bidirectional I^2C-compatible data line
AS[0:1]	31:32		I^2C-compatible Interface Address selection inputs.

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Pin Descriptions (continued)

Name	Pin	ESD Structures	Function
C[1:4]	27:30		Asynchronous DAC output control digital inputs
GPIO[0:7]	15:22		Digital I/O. CMOS Input or Open-Drain Output
INT[1:2]	25:26		Interrupt outputs. Open-Drain, active LOW
AREF	49		ADC reference
DREF	51		DAC reference

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

ABSOLUTE MAXIMUM RATINGS (1)(2)(3)

		VALUE
VDD Relative to GND		−0.3V to 6.0V
Voltage between any 2 pins (4)		6.0V
Current in or out of any pin (4)		5mA
Current through VDD or GND		78 mA, T_A = 125°C 120 mA, T_A = 105°C
Junction Temperature		+150°C
Storage Temperature Range		−65°C to +150°C
ESD Susceptibility (5)	Human Body Model	2500V
	Machine Model	250V
	Charged Device Model	1250V
For Soldering specifications: See product folder at www.ti.com and SNOA549		

(1) Absolute Maximum Ratings" indicate limits beyond which damage to the device may occur, including inoperability and degradation of device reliability and/or performance. Functional operation of the device and/or non-degradation at the Absolute Maximum Ratings or other conditions beyond those indicated in the Recommended Operating Conditions is not implied. The recommended Operating Conditions indicate conditions at which the device is functional and the device should not be operated beyond such conditions.
(2) All voltages are measured with respect to GND = 0V, unless otherwise specified.
(3) If Military/Aerospace specified devices are required, please contact the Texas Instruments Sales Office/ Distributors for availability and specifications.
(4) When the input voltage (VIN) at any pin exceeds power supplies (VIN < GND or VIN > VDD), the current at that pin must not exceed 5mA, and the voltage (VIN) at that pin relative to any other pin must not exceed 6.0V. See Pin Descriptions for additional details of input circuitry.
(5) The Human Body Model (HBM) is a 100 pF capacitor charged to the specified voltage then discharged through a 15 kΩ resistor into each pin. The Machine Model (MM) is a 200 pF capacitor charged to specified voltage then discharged directly into each pin. The Charged Device Model (CDM) is a specified circuit characterizing an ESD event that occurs when a device acquires charge through some triboelectric (frictional) or electrostatic induction process and then abruptly touches a grounded object or surface.

OPERATING CONDITIONS (1)(2)

Operating Ambient Temperature	−40°C to 125°C
VDD Voltage Range	4.5V to 5.5V
DAC Output Load C	0pF to 1500pF

(1) Absolute Maximum Ratings" indicate limits beyond which damage to the device may occur, including inoperability and degradation of device reliability and/or performance. Functional operation of the device and/or non-degradation at the Absolute Maximum Ratings or other conditions beyond those indicated in the Recommended Operating Conditions is not implied. The recommended Operating Conditions indicate conditions at which the device is functional and the device should not be operated beyond such conditions.
(2) All voltages are measured with respect to GND = 0V, unless otherwise specified.

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OPERATING CONDITIONS (1)(2) (continued)

θ_{JA}	24°C/W
θ_{JC}	2°C/W

ELECTRICAL CHARACTERISTICS

Unless otherwise noted, these specifications apply for VDD=4.75V to 5.5V, AREF=DREF=VDD, T_A=25°C. **Boldface** limits are over the temperature range of −40°C ≤ T_A ≤ 125°C unless otherwise noted. DAC input code range 48 to 4047. DAC output C_L = 200 pF unless otherwise noted.

Symbol	Parameter	Conditions	Min	Typ	Max	Units
DAC CHARACTERISTICS						
	Resolution		**12**		**12**	Bits
	Monotonicity		**12**			Bits
DNL	Differential Non-Linearity	R_L = 100k	**−0.6**		**0.6**	LSB
INL	Integral Non-Linearity	R_L = 100k	**−8**		**8**	
ZE	Zero Error	R_L = 100k			**15**	mV
ZEDRIFT	Zero Error Temperature Drift	R_L = 100k		2.0		µV/°C
FSE	Full-Scale Error	R_L = 100k	**0**		**−0.75**	%FS
GE	Gain Error	R_L = 100k	**0**		**−1**	
GEDRIFT	Gain Error Temperature Drift	R_L = 100k		11.0		ppm/° C
ZCO	Zero Code Output	I_{OUT} = 200 µA		7		mV
		I_{OUT} = 1mA		31		
FSO	Full Scale Output at code 4095	VDD = DREF = 5V, I_{OUT} = 1mA	**4.988**	4.995	**VDD**	V
I_{OS}	Output Short Circuit Current (Source) (1)	VDD = 5V, OUT = 0V, Input Code = FFFh CDAC.OFF=0 C[4:1]=HIGH		−60		mA
I_{OS}	Output Short Circuit Current (Sink) (1)	VDD = 5V, OUT = DREF, Input Code = 000h CDAC.OFF=0 C[4:1]=HIGH		70		
I_O	Continuous Output Current per Channel (to prevent damage)	T_A = 105° C			**10**	
		T_A = 125° C			**6.5**	
C_L	Load Capacitance	R_L = 2k or ∞		1500		pF
	DC Output Impedance			8		Ω
	OUT[1:12] Output Voltage when Asynchronous Output Control is activated	R_L = 100k, C[1:4] = GND, CDAC.OLVL = 1	**4.992**	VDD		V
		C[1:4] = GND, CDAC.OLVL = 0		GND	**0.6**	mV
ADC CHARACTERISTICS						
	Resolution with No Missing Codes		**11**			Bits
		−40°C ≤ T_A ≤ 105°C	**12**			
TUE	Total Unadjusted Error		**−0.1**		**0.1**	%
DNL	Differential Non-Linearity	−40°C ≤ T_A ≤ 105°C	**−0.99**		**1**	LSB
			−1.2		**1**	
INL	Integral Non-Linearity			±0.6		
OE	Offset Error		**−2.3**		**2.3**	
OEDRIFT	Offset Error Temperature Drift			0.005		LSB/°C
OEMTCH	Offset Error Match		**−1.5**		**1.5**	LSB
GE	Gain Error		**−2**		**2**	
GEDRIFT	Gain Error Temperature Drift			−0.002		LSB/°C
GEMTCH	Gain Error Match		**−1.5**		**1.5**	LSB
SNR	Signal-to-Noise Ratio			72		dB

(1) Indicates the typical internal short circuit current limit. Sustained operation at this level will lead to device damage.

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ELECTRICAL CHARACTERISTICS (continued)

Unless otherwise noted, these specifications apply for VDD=4.75V to 5.5V, AREF=DREF=VDD, T_A=25°C. **Boldface** limits are over the temperature range of −40°C ≤ T_A ≤ 125°C unless otherwise noted. DAC input code range 48 to 4047. DAC output C_L = 200 pF unless otherwise noted.

Symbol	Parameter	Conditions	Min	Typ	Max	Units
PSRR	Power Supply Rejection Ratio	Offset Error change with VDD		77		dB
		Gain Error change with VDD		73		
V_{IN}	FS Input Range				**AREF**	
I_{INA}	Input Current	In Hold or inactive			**±1**	µA
C_{INA}	Input Capacitance	In Track		33		pF
		In Hold or inactive		3		pF
REFERENCE CHARACTERISTICS						
	AREF Reference Input Range	CREF.AEXT = 1	**2.7**		**VDD**	V
	DREF Reference Input Range	CREF.DEXT = 1	**2.5**		**VDD**	V
	DREF Reference Input Resistance			10		kΩ
	DREF Input Current	DREF = 5V, CREF.DEXT = 1			**660**	µA
	AREF Peak Current	AREF = 5V CREF.DEXT = 1		2.3		mA
	AREF and DREF Reference Current in Powerdown				**1**	µA
	Internally Generated Reference Voltage		**4.47**	4.5	**4.53**	V
	AREF, DREF Output Impedance when Internal Reference Active	CREF.AEXT = 0 CREF.DEXT = 0		5		Ω
TEMPERATURE SENSOR						
	Sensor Gain			−13.45		mV/°C
	Temperature Error	−25°C to +85°C	**−2**		**2**	°C
		−45°C to +125°C	**−2.5**		**2.5**	
DIGITAL INPUT CHARACTERISTICS (AS1:AS0)						
V_{IH}	Input HIGH Voltage		**0.90x VDD**			V
V_{IM}	Input MID Voltage		**0.43 x VDD**		**0.57 x VDD**	
V_{IL}	Input LOW Voltage				**0.1 x VDD**	V
I_{IND}	Digital Input Current			±0.005	**±1**	µA
C_{IND}	Input Capacitance			4		pF
DIGITAL INPUT CHARACTERISTICS (GPIO0:GPIO7, C1:C4)						
V_{IH}	Input HIGH Voltage		**0.7 x VDD**			V
V_{IL}	Input LOW Voltage				**0.3 x VDD**	V
	Hysteresis			0.47		V
I_{IND}	Digital Input Current			±0.005	**±1**	µA
C_{IND}	Input Capacitance			4		pF
DIGITAL INPUT CHARACTERISTICS (SDA and SCL)						
V_{IH}	Input HIGH Voltage		**2.2**			V
V_{IL}	Input LOW Voltage				**1**	V
	Hysteresis			0.27		V
I_{IND}	Digital Input Current			±0.005	**±1**	µA
C_{IND}	Input Capacitance			4		pF
DIGITAL OUTPUT CHARACTERISTICS (INT and GPIO)						
V_{OL}	Output LOW Voltage	I_{OUT} = 200 µA		0.005	**0.4**	V
		I_{OUT} = 4 mA		0.16	**0.4**	V

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ELECTRICAL CHARACTERISTICS (continued)

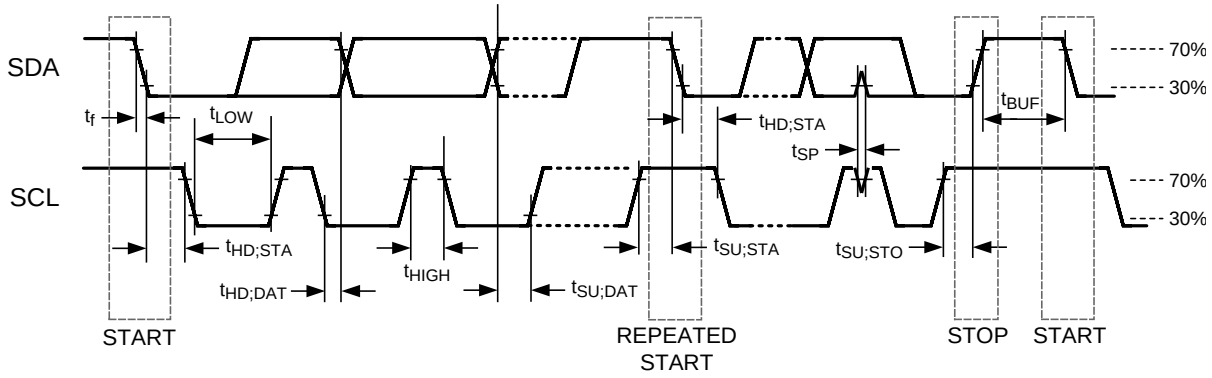
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Symbol	Parameter	Conditions	Min	Typ	Max	Units
DIGITAL OUTPUT CHARACTERISTICS (SDA)						
V_{OL}	Output LOW Voltage	I_{OUT} = 4mA		0.16	**0.4**	V
		I_{OUT} = 6mA		0.23	**0.6**	V
DIGITAL OUTPUT CHARACTERISTICS (All Outputs)						
I_{OL}	Output Leakage when HIGH	Current from the supply rail through the pullup resistor into the drain of the open-drain output device			**±1**	µA
C_{OUT}	Output Capacitance	Force 0V or VDD		4		pF
POWER SUPPLY CHARACTERISTICS						
V_{DD}	Supply Voltage Range		**4.75**	5	**5.5**	V
I_{DD}	Supply Current, converting, all blocks active	OUT[1:12] pins R_L = ∞		4	**6.5**	mA
PWR	Power Consumption, converting, all blocks active	OUT[1:12] pins R_L = ∞		25	**36**	mW
V_{POR}	Power-On Reset (2)	−40°C ≤ T_A ≤ 105°C	**1.9**		**2.4**	V
			1.85		**2.45**	
AC ELECTRICAL CHARACTERISTICS						
t_{TRACK}	ADC Track Time	Interval during which internal HOLD capacitor is connected to input signal		4.7	**5.3**	µs
t_{HOLD}	ADC Hold Time	Interval during which sampled signal is converted to digital output code		3.3	**3.8**	µs
t_s	DAC Settling Time (3)	400h to C00h code change, R_L= 2k C_L = 200 pF		6	**8.5**	µs
I^2C TIMING CHARACTERISTICS						
	I^2C Clock Frequency		**10**		**400**	kHz
t_{LOW}	Clock Low Time		**1.3**			µs
t_{HIGH}	Clock High Time		**0.6**			µs
$t_{HD;STA}$	Hold Time Repeated START condition	After this period, the first clock pulse is generated	**0.6**			µs
$t_{SU;STA}$	Set-up time for a repeated START condition		**0.6**			µs
$t_{HD;DAT}$	Data hold time (4) (5)		**0**		**900**	ns
$t_{SU;DAT}$	Data setup time		**100**			ns
t_f	SDA fall time	I_L ≤ 3mA and C_L ≤ 400 pF			**250**	ns
$t_{SU;STO}$	Set-up time for STOP condition		**0.6**			µs
t_{BUF}	Bus free time between a STOP and START condition		**1.3**			µs
C_b	SDA capacitive load				**400**	pF
t_{SP}	Pulse width of spikes that must be suppressed by the input filter				**50**	ns
t_{OUT}	SCL and SDA Timeout		**25**		**35**	ms

(2) During the power up the supply rail must ramp up beyond V_{POR} MIN for the device to acquire default state. After the supply rail has reached the nominal level, the rail can drop as low as V_{POR} MAX for the current state to be maintained.
(3) Device Specification is ensured by characterization and is not tested in production.
(4) Data hold time is measured from the falling edge of SCL, applies to data transmission and the acknowledge.
(5) Device internally provides a hold time of at least 300 ns for the SDA signal to bridge the undefined region of the falling edge of SCL.

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Figure 2. I²C Interface Timing Diagram



TYPICAL PERFORMANCE CHARACTERISTICS

ADC: DNL
VDD = 5V, AREF = 4.5V, T_A = 25°C
CREF.AEXT = 1, Single Channel Continuous Mode

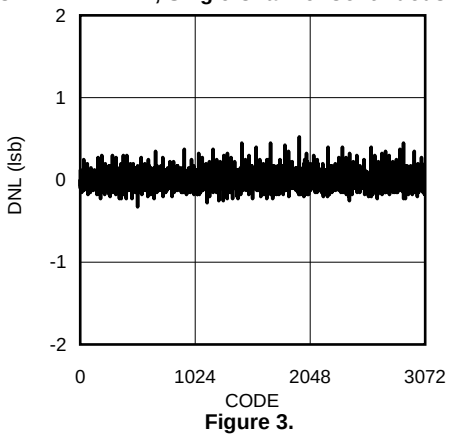


Figure 3.

ADC: INL
VDD = 5V, AREF = 4.5V, T_A = 25°C
CREF.AEXT = 1, Single Channel Continuous Mode

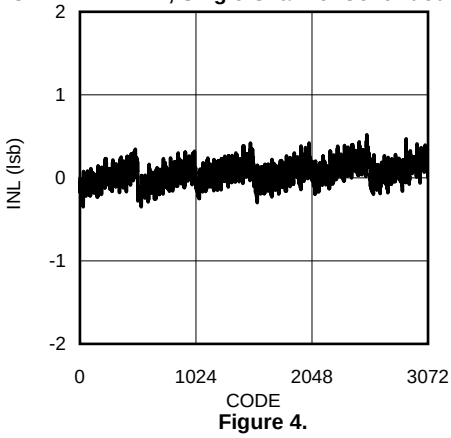


Figure 4.

DAC: DNL
VDD = 5V, DREF = 4.5V, T_A = 25°C
CREF.DEXT = 1, RL = 100kΩ

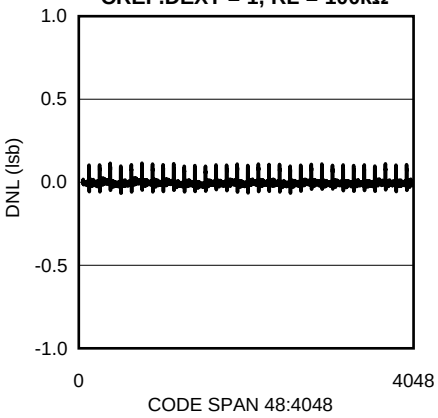


Figure 5.

DAC: INL
VDD = 5V, DREF = 4.5V, T_A = 25°C
CREF.DEXT = 1, RL = 100kΩ

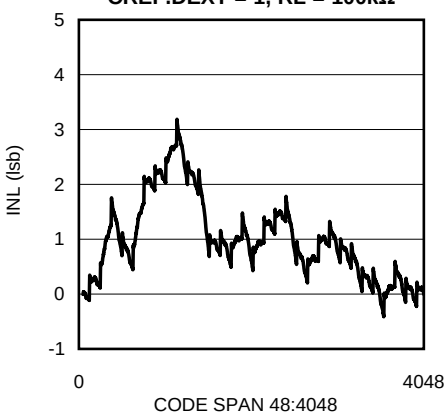


Figure 6.

ADC: DNL
vs.
Temperature
VDD = 5V, AREF = 4.5V, CREF.AEXT = 1

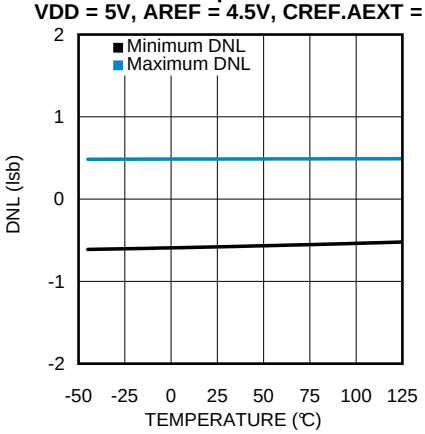


Figure 7.

ADC: INL
vs.
Temperature
VDD = 5V, AREF = 4.5V, CREF.AEXT = 1

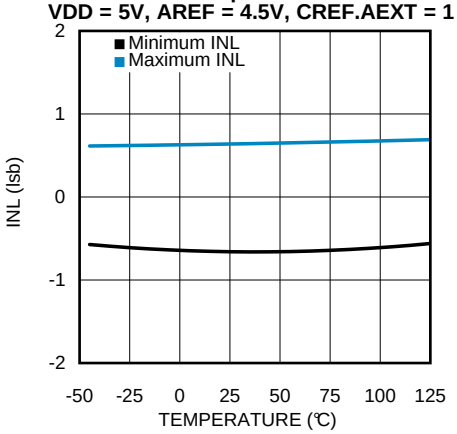


Figure 8.

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TYPICAL PERFORMANCE CHARACTERISTICS (continued)

DAC: DNL vs Temperature
VDD = 5V, DREF = 4.5V, CREF.DEXT = 1

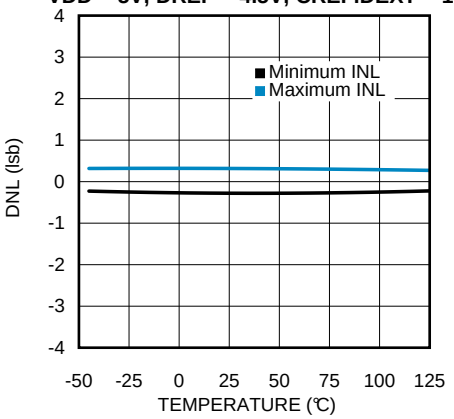


Figure 9.

DAC: INL vs Temperature
VDD = 5V, DREF = 4.5V, CREF.DEXT = 1

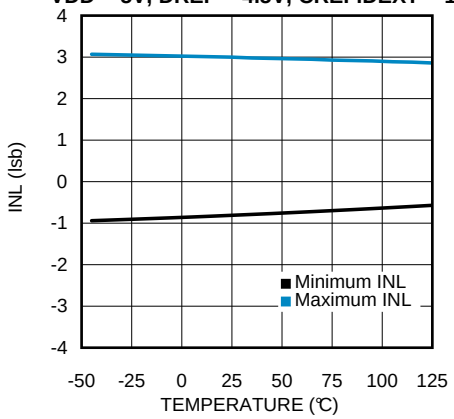


Figure 10.

OUTx Output Load Regulation
VDD = 5V, DREF = 5V,
T_A = 25°C, CREF.DEXT = 1

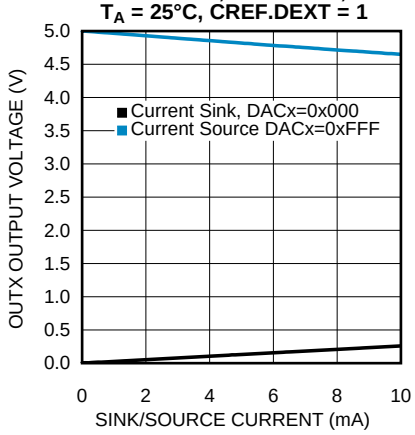


Figure 11.

Temperature Sensor Error Bounds, VDD = 5V

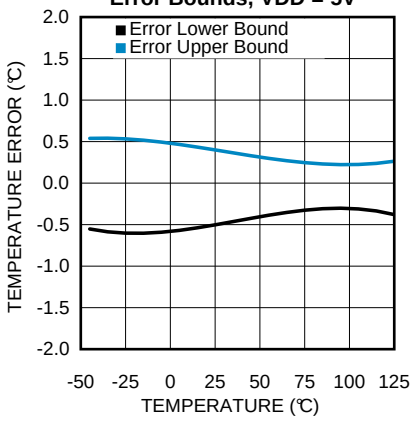


Figure 12.

Internal Reference Output Temperature Drift
VDD = 5V, CREF.AEXT = 0, CREF.DEXT = 0

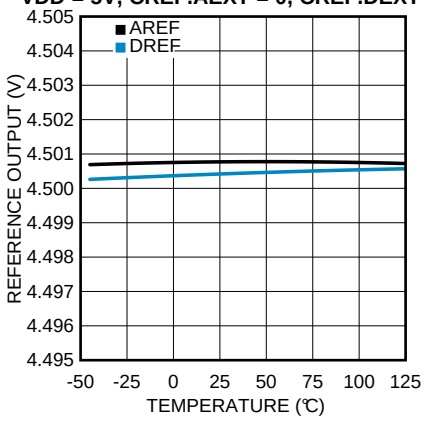


Figure 13.

REGISTER SET

RESERVED registers in the map in REGISTER MAP should not be accessed for either read or write operations as this may lead to unpredictable behavior of the device.

If writing to a RESERVED bit, user must write only 0, unless otherwise stated.

REGISTER MAP

Addr.	Name	Function	R/W	Lock
0x00		**RESERVED**		
0x01	TEST	Test Register	RW	
0x02 | 0x0D		**RESERVED**		
0x0E	ID	Company ID Register	R	
0x0F	VER	Version Register	R	
STATUS				
0x10	SGEN	Status: General	R	
0x11	SGPI	Status: GPIO	R	
0x12	SHIL	Status: over HIGH limit	R	
0x13	SLOL	Status: under LOW limit	R	
CONTROL				
0x14	CGEN	General	RW	
0x15	CDAC	DAC	RW	
0x16	CGPO	GPIO mode	RW	
0x17	CINH	INT HIGH enable	RW	Y
0x18	CINL	INT LOW enable	RW	Y
0x19	CAD1	Analog ch enable	RW	Y
0x1A	CAD2	Analog ch enable	RW	Y
0x1B	CAD3	Temp. Sens. ch enable	RW	Y
0x1C	CTRIG	Single conversion trigger	W	Y
ADC OUTPUT DATA				
0x20	ADC1	Ch1 conversion Data	R	
0x21	ADC2	Ch2 conversion Data	R	
0x22	ADC3	Ch3 conversion Data	R	
0x23	ADC4	Ch4 conversion Data	R	
0x24	ADC5	Ch5 conversion Data	R	
0x25	ADC6	Ch6 conversion Data	R	
0x26	ADC7	Ch7 conversion Data	R	
0x27	ADC8	Ch8 conversion Data	R	
0x28	ADC9	Ch9 conversion Data	R	
0x29	ADC10	Ch10 conversion Data	R	
0x2A	ADC11	Ch11 conversion Data	R	
0x2B	ADC12	Ch12 conversion Data	R	
0x2C	ADC13	Ch13 conversion Data	R	
0x2D	ADC14	Ch14 conversion Data	R	
0x2E	ADC15	Ch15 conversion Data	R	
0x2F	ADC16	Ch16 conversion Data	R	
0x30	ADC17	Temp. Sensor Data	R	
ADC WINDOW COMPARATOR LIMITS				
0x40	LIH1	ADC Ch1 HIGH limit	RW	Y

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Addr.	Name	Function	R/W	Lock
0x41	LIH2	ADC Ch2 HIGH limit	RW	Y
0x42	LIH3	ADC Ch3 HIGH limit	RW	Y
0x43	LIH9	ADC Ch9 HIGH limit	RW	Y
0x44	LIH10	ADC Ch10 HIGH limit	RW	Y
0x45	LIH11	ADC Ch11 HIGH limit	RW	Y
0x46	LIL1	ADC Ch1 LOW limit	RW	Y
0x47	LIL2	ADC Ch2 LOW limit	RW	Y
0x48	LIL3	ADC Ch3 LOW limit	RW	Y
0x49	LIL9	ADC Ch9 LOW limit	RW	Y
0x4A	LIL10	ADC Ch10 LOW limit	RW	Y
0x4B	LIL11	ADC Ch11 LOW limit	RW	Y
INTERNAL REFERENCE CONTROL				
0x66	CREF	Int. reference enable	RW	
DAC INPUT DATA				
0x80	DAC1	DAC Ch1 Input Data	RW	
0x81	DAC2	DAC Ch2 Input Data	RW	
0x82	DAC3	DAC Ch3 Input Data	RW	
0x83	DAC4	DAC Ch4 Input Data	RW	
0x84	DAC5	DAC Ch5 Input Data	RW	
0x85	DAC6	DAC Ch6 Input Data	RW	
0x86	DAC7	DAC Ch7 Input Data	RW	
0x87	DAC8	DAC Ch8 Input Data	RW	
0x88	DAC9	DAC Ch9 Input Data	RW	
0x89	DAC10	DAC Ch10 Input Data	RW	
0x8A	DAC11	DAC Ch11 Input Data	RW	
0x8B	DAC12	DAC Ch12 Input Data	RW	
0x8C | 0x8F		**RESERVED**		
0x90	DALL	All DAC Data	W	
MEMORY MAPPED BLOCK COMMANDS				
0xF0	BLK0	DAC1-12 access	RW	
0xF1	BLK1	DAC7-12 access	RW	
0xF2	BLK2	ADC1-17 access	R	
0xF3	BLK3	ADC9-17 access	R	
0xF4	BLK4	LIHx, LILx access	RW	
0xF5	BLK5	LILx access	RW	
0xF6 | 0xFF		**RESERVED**		

TEST AND INFO REGISTERS

The registers in this section do not affect the operation of the device. They are provided for user convenience and product identification.

Test Register: TEST[7:0], default = 0x00

This register can be used for verification of the I^2C-compatible bus integrity. Its contents are ignored by the device.

Company ID Register: ID[7:0], default = 0x01

Product identification register, factory set.

Device Version Register: VER[7:0], default = 0x10

Product identification register, factory set.

STATUS REGISTERS

General Status Register: SGEN[7:0], default = 0x40

Bx	Name	Function
7	BUSY	1 - while ADC is converting
6	RDYN	0 - when power up completed
5:3	-	RESERVED
2	HV	1 - if any bit in SHIL is set
1	LV	1 - if any bit in SHOL is set
0	GPI	1 - if any bit in SGPI is set

GPIO Status Register: SGPI[7:0], default = 0x**

Bx	Name	Function
7	GPI7	Indicates logic level at pin GPIO7
6	GPI6	Indicates logic level at pin GPIO6
5	GPI5	Indicates logic level at pin GPIO5
4	GPI4	Indicates logic level at pin GPIO4
3	GPI3	Indicates logic level at pin GPIO3
2	GPI2	Indicates logic level at pin GPIO2
1	GPI1	Indicates logic level at pin GPIO1
0	GPI0	Indicates logic level at pin GPIO0

High-Limit Status Register: SHIL[7:0], default = 0x00

Bx	Name	Function
7:6	-	RESERVED
5	H11	Set if ADC11 > LIH11
4	H10	Set if ADC10 >LIH10
3	H9	1 - if ADC9 > LIH9
2	H3	1 - if ADC3 > LIH3
1	H2	1 - if ADC2 > LIH2
0	H1	1 - if ADC1 > LIH1

Low-Limit Status Register: SLOL[7:0], default = 0x00

Bx	Name	Function
7:6	-	RESERVED
5	L11	1 - if ADC11 ≤ LIH11
4	L10	1 - if ADC10 ≤ LIH10
3	L9	1 - if ADC9 ≤ LIH9
2	L3	1 - if ADC3 ≤ LIH3
1	L2	1 - if ADC2 ≤ LIH2
0	L1	1 - if ADC1 ≤ LIH1

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CONTROL REGISTERS

General Configuration Register: CGEN[7:0], default = 0x00

Bx	Name	Function
7	RST	1 - RESETS all registers and self to POR value
6:3	-	RESERVED
2	TOD	1 - disable I²C-compatible TIMEOUT. See I²C-Compatible Bus Reset
1	LCK	1 - to lock registers. Lockable registers are shown in the REGISTER MAP. Once locked their contents will not be affected by the subsequent I²C-compatible bus transactions
0	STRT	1 - to start continuous conversion of all enabled ADC channels. The CGEN.LCK bit must be set for the conversion sequence to begin 0 - disable continuous ADC conversion mode

DAC Configuration Register: CDAC[7:0], default 0x03

Bx	Name	Function
7:3	-	RESERVED
2	GANG	Controls the association of analog output channels OUTx with asynchronous control inputs Cy. (See Asynchronous Output Control)
1	OLVL	1 - Cy=0 will force associated OUTx outputs to VDD 0 - Cy=0 will force associated OUTx outputs to GND
0	OFF	1 - forces all OUT[1:12] outputs to HIGH impedance state

GPIO Output Control Register: CGPO[7:0], default = 0xFF

Bx	Name	Function
7	GPO7	1 - Internal pulldown at pin GPIO7 is off
6	GPO6	1 - Internal pulldown at pin GPIO6 is off
5	GPO5	1 - Internal pulldown at pin GPIO5 is off
4	GPO4	1 - Internal pulldown at pin GPIO4 is off
3	GPO3	1 - Internal pulldown at pin GPIO3 is off
2	GPO2	1 - Internal pulldown at pin GPIO2 is off
1	GPO1	1 - Internal pulldown at pin GPIO1 is off
0	GPO0	1 - Internal pulldown at pin GPIO0 is off

INT1, INT2 High-Limit Control Register: CINH[7:0], default = 0x00

Bx	Name	Function
7	-	RESERVED
6	-	RESERVED
5	EH11	1 - Enable High limit interrupt for Ch 11
4	EH10	1 - Enable High limit interrupt for Ch 10
3	EH9	1 - Enable High limit interrupt for Ch 9
2	EH3	1 - Enable High limit interrupt for Ch 3
1	EH2	1 - Enable High limit interrupt for Ch 2
0	EH1	1 - Enable High limit interrupt for Ch 1

INT1, INT2 Low-Limit Control Register: CINL[7:0], default = 0x00

Bx	Name	Function
7	-	RESERVED
6	-	RESERVED

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Bx	Name	Function
5	EL11	1 - Enable Low limit interrupt for Ch 11
4	EL10	1 - Enable Low limit interrupt for Ch 10
3	EL9	1 - Enable Low limit interrupt for Ch 9
2	EL3	1 - Enable Low limit interrupt for Ch 3
1	EL2	1 - Enable Low limit interrupt for Ch 2
0	EL1	1 - Enable Low limit interrupt for Ch 1

ADC Conversion Enable Register 1: CAD1[7:0], default = 0x00

Bx	Name	Function
7	EN8	1 - Enable ADC input Ch 8
6	EN7	1 - Enable ADC input Ch 7
5	EN6	1 - Enable ADC input Ch 6
4	EN5	1 - Enable ADC input Ch 5
3	EN4	1 - Enable ADC input Ch 4
2	EN3	1 - Enable ADC input Ch 3
1	EN2	1 - Enable ADC input Ch 2
0	EN1	1 - Enable ADC input Ch 1

ADC Conversion Enable Register 2: CAD2[7:0], default = 0x00

Bx	Name	Function
7	EN16	1 - Enable ADC input Ch 16
6	EN15	1 - Enable ADC input Ch 15
5	EN14	1 - Enable ADC input Ch 14
4	EN13	1 - Enable ADC input Ch 13
3	EN12	1 - Enable ADC input Ch 12
2	EN11	1 - Enable ADC input Ch 11
1	EN10	1 - Enable ADC input Ch 10
0	EN9	1 - Enable ADC input Ch 9

ADC Conversion Enable Register 3: CAD3[7:0], default = 0x00

Bx	Name	Function
7:1	-	RESERVED
0	EN17	1 - Enable Temp Sensor ADC input channel

ADC One-Shot Conversion Trigger Register : CTRIG[7:0], default = 0x00

Bx	Name	Function
7:1	-	RESERVED
0	SNGL	Writing any value, when CGEN.STRT=0, will trigger Single-Shot conversion. The CGEN.LCK bit must be set for the conversion sequence to begin.

Reference Mode Register: CREF[7:0], default = 0x07

Bx	Name	Function
7:3	-	RESERVED
2	AEXT	1 - ADC external ref. enable 0 - ADC internal ref. enable
1	DEXT	1 - DAC external ref. enable 0 - DAC internal ref. enable

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Bx	Name	Function
0	-	RESERVED, must be 1

DATA REGISTERS

All registers in this section require 16-bit I^2C-compatible data transaction for both read and write operations. However, only lower 12 bits are stored. All data is assumed to be in the unsigned binary format, where the lowest value is represented by 0x000 and the highest value is represented by 0xFFF.

ADC Output Data Register: ADCx[15:0], default 0x0000

The ADCx registers, x = 1...16, contain results of the most recent ADC conversion cycle. Accessing these registers does not preempt the Analog Sense Subsystem sequencing. Enabling/Disabling of the ADC input channels via CADx registers does not affect the ADCx content.

Bx	Name	Function
15:12	-	Always 0
11:0	-	12-bit binary representing the ADC conversion result

ADC High-Limit Register: LIHx[15:0], default 0x0FFF

The LILx registers, x=1...3 and 9...11, contain the HIGH LIMIT threshold of the window comparator function of the Analog Sense Subsystem.

Bx	Name	Function
15:12	-	Always 0. Data written to this location will be discarded.
11:0	-	Window comparator upper limit.

ADC Low-Limit Register: LILx[15:0], default 0x0000

The LILx registers, x=1...3 and 9...11, contain the LOW LIMIT threshold of the window comparator function of the Analog Sense Subsystem.

Bx	Name	Function
15:12	-	Always 0. Data written to this location will be discarded.
11:0	-	Window comparator lower limit.

DAC Data Register: DACx[15:0], default 0x0000

The DACx registers, x=1...12, are input code registers. Updating the DACx register automatically updates the VOUTx of the corresponding DAC. Note that OUTx may not update due to the state of the asynchronous control inputs C[1:4]. (See Asynchronous Output Control.)

Bx	Name	Function
15:12	-	Always 0. Data written to this location will be discarded.
11:0	-	DACx input data.

Write all DAC's Data Register: DALL[15:0], default 0x0000

Writing to this register updates all DACx registers simultaneously to this value. Note that OUTx may not update due to the state of the asynchronous control inputs C[1:4].

Bx	Name	Function
15:12	-	Always 0. Data written to this location will be discarded.
11:0	-	DAC input data.

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BLOCK COMMANDS

Block access functionality is discussed in Block Access.

Name	Block Start Address	Block End Address	Block Length in Bytes	Comment
BLK0	0x80	0x8B	24	Single command access to registers DAC[1:12]
BLK1	0x86	0x8B	12	Single command access to registers DAC[7:12]
BLK2	0x20	0x30	34	Single command access to registers ADC[1:17]
BLK3	0x28	0x30	18	Single command access to registers ADC[9:17]
BLK4	0x40	0x4B	24	Single command access to all LIHx and LILx registers
BLK5	0x46	0x4B	12	Single command access to all LILx registers

APPLICATION INFORMATION

ANALOG SENSE SUBSYSTEM

The device is capable of monitoring up to 16 externally applied voltages and an internal analog temperature sensor. The system is centered around 12-bit SAR ADC fronted by a 17-input mux. Results of conversion are stored in the registers corresponding to the given input channel. The register content can be read by the supervisor via the I^2C-compatible interface.

The ADC timing signals are derived from the on-board temperature compensated oscillator, which assures the stable sampling interval.

In the applications where an instantaneous detection of the out-of-bounds condition is required the built in digital window comparator function is provided on 6 of the input channels. This window comparator is capable of triggering the external interrupts.

Sampling and Conversion

The external voltage is sampled onto the internal C_{HOLD} capacitor. The TRACK period is controlled by the internal oscillator, and its duration is t_{TRACK}. The output impedance of the sensed voltage source and the analog input capacitance C_{INA} (which is dominated by C_{HOLD} during TRACK time) limit the bandwidth of the input signal. It is recommended to limit the output resistance ROUT of the sampled voltage source to 10 kΩ to assure 12-bit accuracy of conversion.

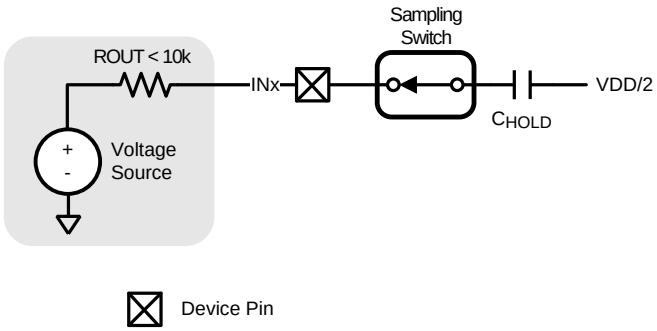


Figure 14. ADC During TRACK Period

During the HOLD period, duration of t_{HOLD}, all mux switches are in the off state, and charge captured on the hold capacitor is measured to produce an ADC output code. The resulting output code is stored in the internal register (ADCx) corresponding to the sampled analog input channel.

Typical ADC output code as a function of input voltage at device pin INx, x=1...16:

$$CODEx = INT\left(\frac{4096}{VREF} \times INx\right)$$

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In the expression above VREF is the reference voltage input to the internal ADC. VREF can be either externally applied at the AREF pin of the device, or be internally generated.

Sampling Transient

An instantaneous current will flow at the beginning of TRACK period which may lead to temporary disturbance of the input potential. This current, and resulting disturbance, will vary with the magnitude of the sampled signal and source impedance ROUT.

Channel Selection

The analog input channels are enabled by setting corresponding enable bits ENx in the control registers CAD1, CAD2, and CAD3. Enabling of the channels does not begin the conversion process.

Single-Shot and Continuous Sequencing

The ADC is in the idle state until either the Single-Shot or Continuous conversion is initiated. The channels whose corresponding ENx bit in the CAD(1|2|3) registers is set will be sampled and converted by the ADC.

Single-Shot conversion begins when the user performs a write operation (0 or 1) to CTRIG.SNGL while CGEN.STRT=0. Once the sequence is completed the ADC returns to the idle state.

Continuous conversion begins when the user sets the CGEN.STRT bit. The sequencing of events is the same as in the Single Mode. Upon completing the sequence of conversions another sequence is automatically started. This process will continue until the user clears the CGEN.STRT bit.

The operation of the Analog Sense Subsystem is further illustrated in Figure 15.

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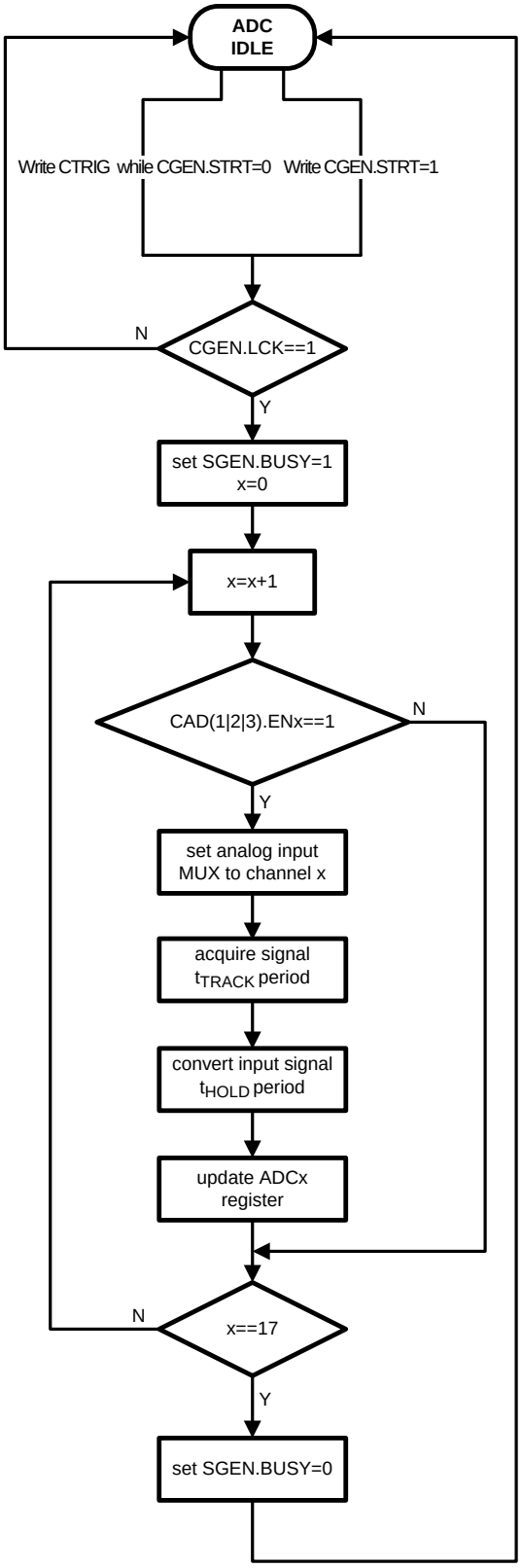


Figure 15. ADC Finite State Machine Diagram

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Reference

By default the ADC operates from the external reference voltage applied at AREF pin of the device. Due to the architecture of the ADC the DC current flowing into the AREF input is zero during conversion. However, the transient currents during the conversion can be significant.

The user can enable the internal reference generator and apply its output to the ADC VREF. This operation is described in CONTROL REGISTERS.

Window Comparator Function

The digital window comparator function is available for ADC input channels 1-3 and 9-11. This feature does not require explicit enabling, as it is always on. Comparator functional diagram is shown in Figure 16 below.

The ADC conversion result stored in ADCx register can be compared against user programmable upper and lower limits: LIHx and LILx. The comparison result is reported as a single bit value in SHIL and SLOL registers.

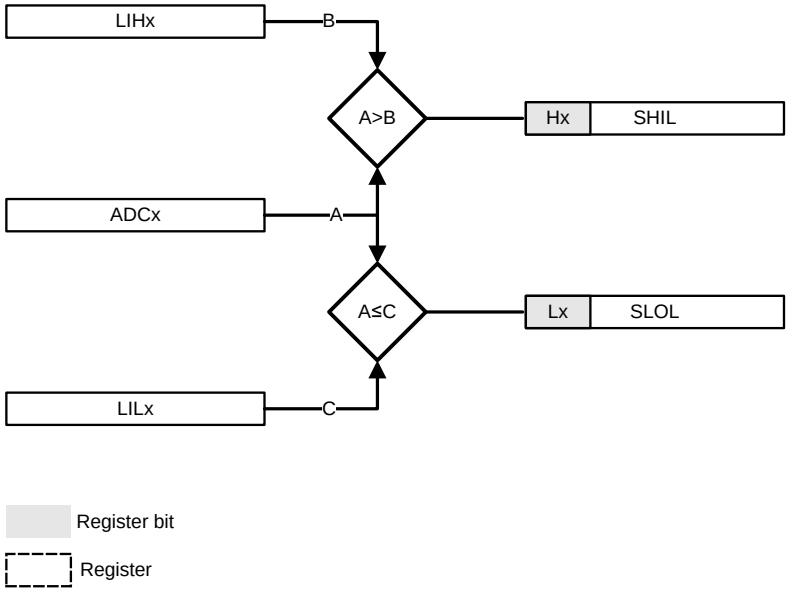


Figure 16. ADC Window Comparator Function

Interrupt Subsystem

Device outputs INT1 and INT2 report out of bounds conditions as determined by the digital window comparator. INT1 and INT2 are open collector outputs and are active LO. INT1 reports out of bound conditions at ADC channels 1-3, and INT2 reports out of bound conditions at ADC channels 9-11. Functional diagram of the interrupt system is shown in Figure 17.

Additionally, presence of any out of bound condition is reported in the SGEN register, which can be tested via the I^2C-compatible interface.

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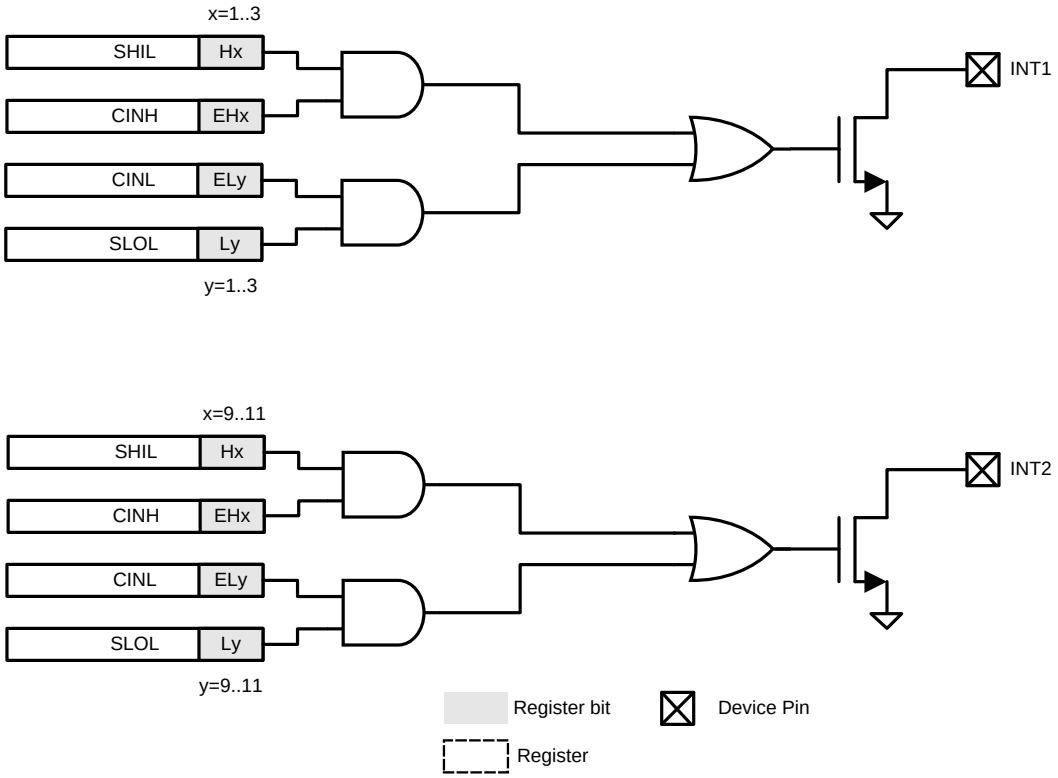


Figure 17. Interrupt System

PROGRAMMABLE ANALOG OUTPUT SUBSYSTEM

This subsystem consists of 12 identical DACs whose output is a function of user programmable registers DACx. This functionality is described in DAC Core.

There are instances where it is necessary to instantaneously "turn off" the devices downstream of OUTx output, without incurring the delay due to the I^2C-compatible data/command transfer. This functionality is described in Asynchronous Output Control.

DAC Core

The DAC core is based on a Resistive String architecture which specifies monotonicity of its transfer function. The input data is single-registered, meaning that the VOUTx of the DAC is updated as soon as the data is updated in the DACx data register at the end of the I^2C-compatible transaction.

The functional diagram of the DAC Core is shown in Figure 18.

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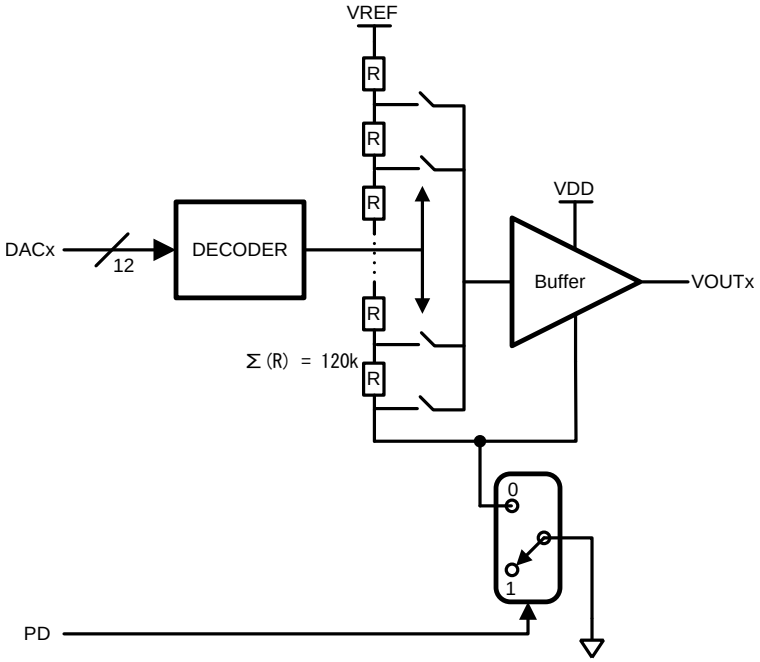


Figure 18. DAC Core

Typical DAC core output VOUTx as a function of the DACx input , x=1...12, can be expressed as:

$$VOUTx = VREF \times \frac{DACx}{4096}$$

Reference

By default the DACs operate from the external reference voltage applied at the DREF pin of the device. Given the architecture of the DAC the DC current flowing into the DREF device input pin is dependent on the number of DACs active at the given instant.

The user can enable the internal reference generator and apply its output to all DACs' VREF inputs. This operation is described in ADC/DAC VOLTAGE REFERENCE.

Asynchronous Output Control

When DACs are enabled, CDAC.OFF=0, the Cy device inputs allow the user to instantaneously disengage the VOUTx of corresponding DAC Core and force the OUTx to either rail – the rail is indicated by the CDAC.OLVL bit. Asserting either CDAC.OFF or Cy (Active LOW) will result in the corresponding DAC Core powering down.

The functional diagram of the DAC Core to OUTx signal routing is shown in Figure 19.

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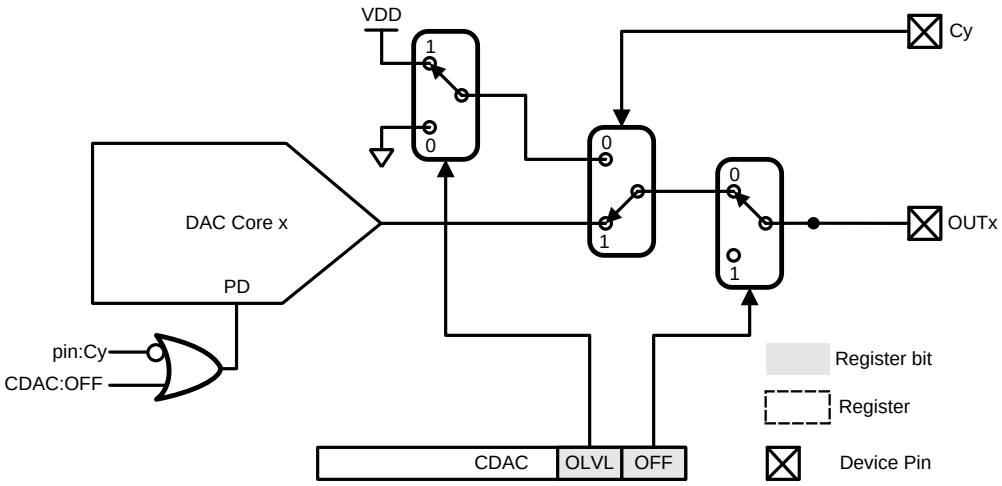


Figure 19. Asynchronous Output Control

Note that CDAC.OFF affects all OUTx, whereas Cy affects only channels assigned to it. The correspondence between Cy control inputs and OUTx outputs is governed by the CDAC.GANG bit and is outlined in Table 1.

Table 1. Cy to OUTx Assignment

Device Pin Cy	CDAC:GANG = 0	CDAC:GANG = 1
C1	OUT[1:4]	OUT[1:3]
C2	OUT[5:6]	OUT[4:6]
C3	OUT[7:8]	OUT[7:9]
C4	OUT[9:12]	OUT[10:12]

TEMPERATURE SENSOR

The output voltage of the analog temperature sensor can be sampled via ADC channel 17 input. The result of conversion is stored in the ADC17 register.

Typical ADC output code as a function of temperature:

$$CODE = INT\left(\frac{4096}{VREF} \times [2212.5 - 13.45(T - 30) - 0.005(T - 30)^2] \times 10^{-3}\right)$$

In the expression above VREF is the reference input voltage to the internal ADC.

For best temperature measurement accuracy the exposed DAP of the device should be soldered to the PCB's grounded pad, and the power dissipation of the device should be limited.

ADC/DAC VOLTAGE REFERENCE

The on-board ADC and DACs require reference voltages for their operation. By default the device is configured to accept external references applied to AREF and DREF pins respectively. In this configuration AREF and DREF can be at different potentials.

The external reference voltage sources should be bypassed to ground with capacitance appropriate for those particular sources. See example application schematic in Application Circuit Example.

The device also has a built in precision reference block which can be used to provide VREF potential to either ADC or DACs, or both at once. The internal buffers are designed to provide necessary drive to ADC and DAC blocks. The internal reference buffers are not intended to drive external loads.

When internal reference is enabled the capacitance at AREF or DREF pins should be limited to 50 pF.

The functional diagram of the reference selector is shown in Figure 20.

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NOTE

Internal reference drive must be disabled when corresponding external reference is applied; e.g., set CREF.AEXT=1 when applying external AREF.

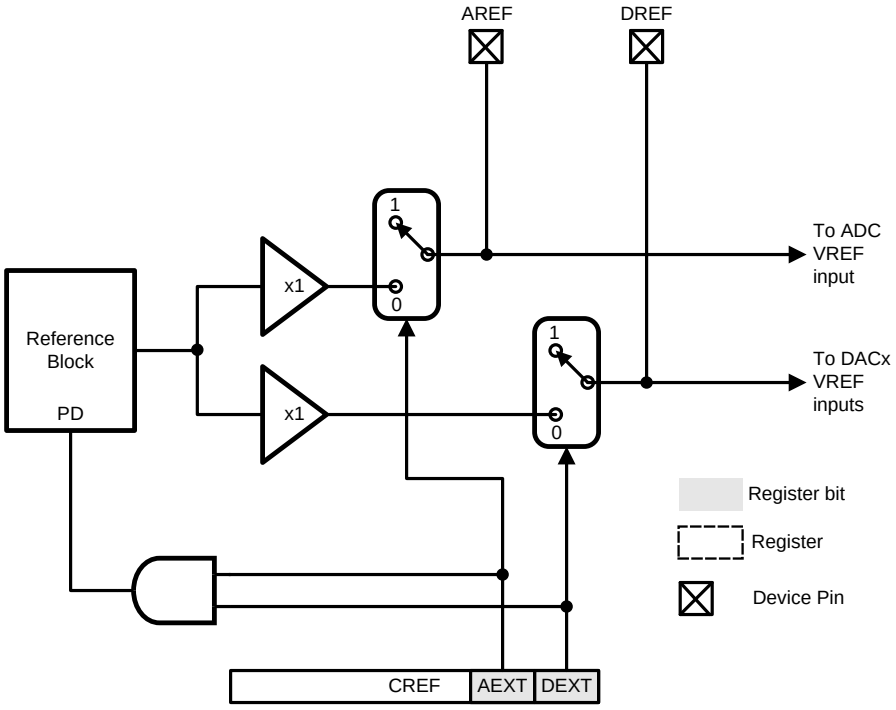


Figure 20. Reference Select Function

GENERAL PURPOSE I/O

The GPIO[7:0] port is memory mapped to registers SGPI and CGPO. Both registers are accessible through the I^2C-compatible interface.

The SGPI register content reflects at all times the digital state at the GPIOx device pins.

The CGPO register controls the individual pulldown devices at GPIOx. Together with the external pull-up resistor this realizes an “open-drain” digital output. For example, writing HIGH to CGPO:GPO0 will result in HIGH output state at pin GPIO0.

The functional diagram of the GPIO subcircuit is shown in Figure 21.

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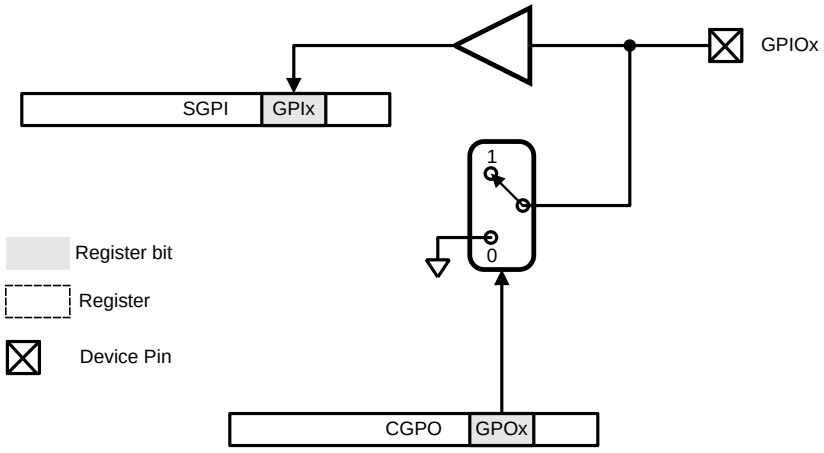


Figure 21. GPIO Functionality

SERIAL INTERFACE

The serial interface provides user access to internal CONTROL and DATA registers that govern the operation of the device. Interface functionality is compatible with I^2C "Standard" and "Fast" modes.

The device operates as the slave only.

I^2C-Compatible Protocol

Two wires, SCL and SDA, are used to carry data between master (the digital supervisor), and a slave (LMP92001). Master generates a START condition which commences all data transfers. And only the master generates the SCL signal for all transactions. However, both master and the slave can in turn be a transmitter and receiver of data.

Typical bus transaction is shown in Figure 22 below. All transactions follow the format outlined as follows:

- Master begins all transactions by generating START condition
- All transfers comprise 8-bit bytes
- First byte must contain 7-bit Slave Interface Address
- First byte is followed by a READ/WRITE bit
- All subsequent bytes contain 8-bit data
- Device, depending on the register being accessed, supports 1-byte and 2-byte transfers. Block Access commands result in multi-byte transfers
- In case of a 2-byte transfers, the byte order is always "MSB first"
- Bit order within byte is always "MSB" first"
- ACKNOWLEDGE condition follows every byte transfer – this can be generated by either Master or a Slave depending on the direction of data transfer

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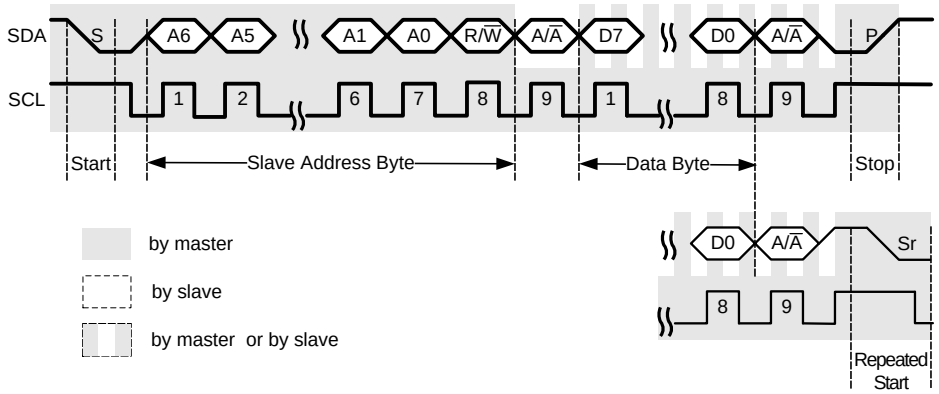


Figure 22. General I²C-Compatible Protocol

Table 2 lists all conditions defined by the I²C-compatible specification and supported by this device. All following bus descriptions will refer to the Symbols listed in the table.

Table 2. I²C-Compatible Symbol Set

Condition	Symbol	Source	Description
START	S	Master	Begins all bus transactions
STOP	P	Master	Terminates all transactions, and resets bus
ACK (Acknowledge)	A	Master/Slave	Handshaking bit (LOW)
NAK (No Acknowledge)	$\overline{A}$	Master/Slave	Handshaking bit (HIGH)
READ	R	Master	Active HIGH bit that follows immediately after the slave address sequence. Indicates that the master is initiating the slave to master data transfer
WRITE	$\overline{W}$	Master	Active LOW bit that follows immediately after the slave address sequence. Indicates that the master is initiating the master to slave data transfer
REPEATED START	Sr	Master	Generated by master, same function as the Start condition (highlights the fact that Stop condition is not strictly necessary)

Data transfers of 16-bit values are shown in Figure 23 and Figure 24 below:

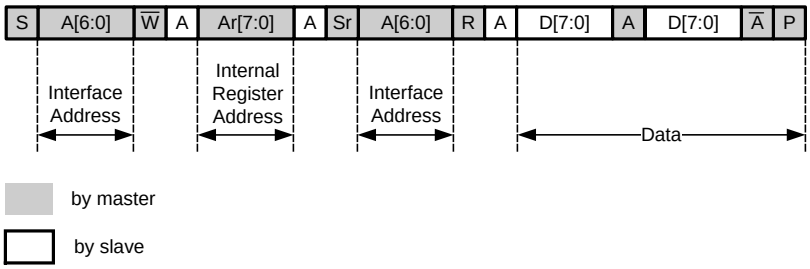


Figure 23. I²C-Compatible READ Access Protocol

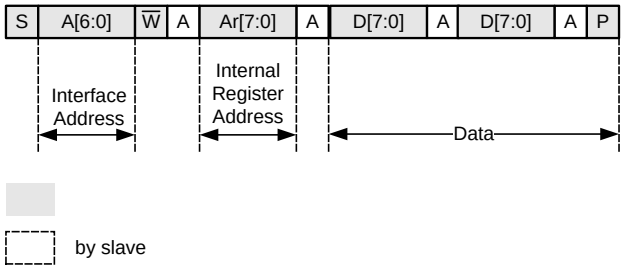


Figure 24. I²C-Compatible WRITE Access Protocol

Device Address

Interface Address of the device can be set via 2 pins: AS0 and AS1. Each address setting pin recognizes 3 levels: LOW=GND, HIGH=VDD and MID=VDD/2. All possible Interface Addresses are listed in Table 3 below:

Table 3. Interface Address Space

Device Pins		Device Interface Address [A6:A0]R/W	Equivalent HEX Address
AS1	AS0		
LOW	LOW	[0100 000]0	40
LOW	MID	[0100 001]0	42
LOW	HIGH	[0100 010]0	44
MID	LOW	[0100 011]0	46
MID	MID	[0100 100]0	48
MID	HIGH	[0100 101]0	4A
HIGH	LOW	[0100 110]0	4C
HIGH	MID	[0100 111]0	4E
HIGH	HIGH	[0101 000]0	50

The Interface Address alignment within the I²C-compatible address byte is shown in Figure 25 below:

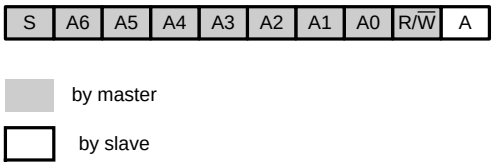


Figure 25. Interface Address Sequence within the I²C-Compatible Frame

Block Access

Block Access functionality minimizes overhead in bus transfers involving larger data sets (more than 2 bytes). Internal register addresses 0xF0 through 0xF5 are interpreted by the interface as block commands. Accessing any of these addresses initiates a multi-byte transfer which can be as long as 34 data bytes. The byte length of the transfer is dictated by the block command itself. Examples of access to internal register at address 0xF0 is shown in Figure 26 and Figure 27.

BLK0 command is issued meaning that all DACx registers accessed are accessed sequentially.

The transfer will consist of 24 bytes – 2 bytes per DACx register.

The data WRITE transfers that terminate prematurely will result in update of registers whose 16-bit words were received completely. For example, if BLK0 WRITE access is attempted, and the transfer is terminated after 3 bytes, only DAC1 register will be updated.

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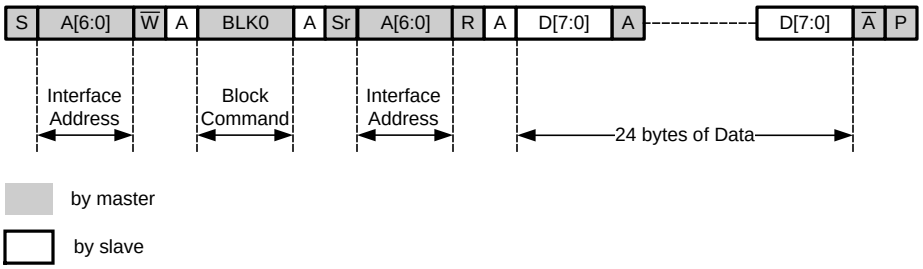


Figure 26. Block Command READ Access

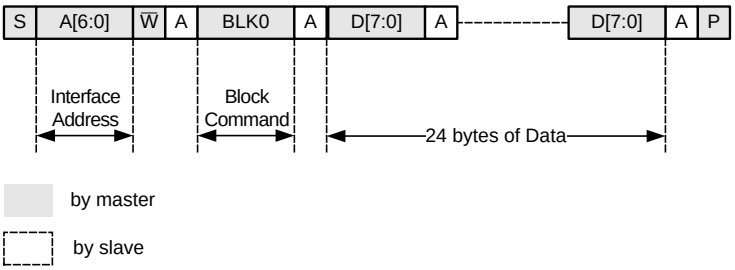


Figure 27. Block Command WRITE Access

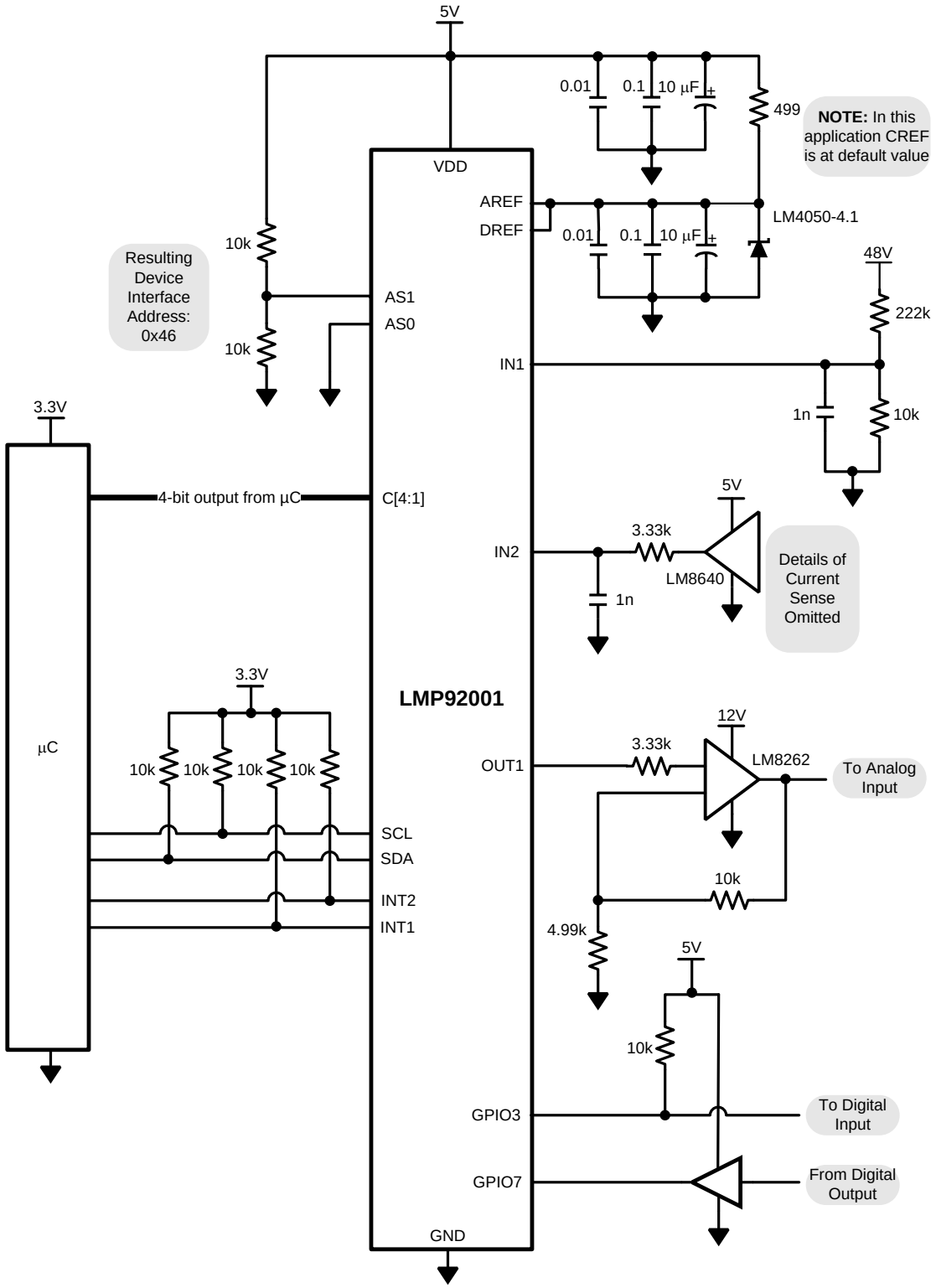
I²C-Compatible Bus Reset

In cases where Master and Slave interfaces fall out of synchronization there are 2 processes which can reset the Slave and return it to a known state:

- TIMEOUT: The device will automatically reset its interface and wait for a new START condition (by the Master) if SCL is driven LOW for duration longer than t_{OUT} (see Electrical Characteristics Table), or SDA is driven LOW by this device for duration longer than t_{OUT}. The TIMEOUT feature can be disabled by the user, see CGEN register functionality.
- When SDA is in HIGH state, the Master can issue START condition at any time. The START condition resets the Slave interface, and Slave expects to see Interface Address byte next.

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Application Circuit Example



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PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
LMP92001SQE/NOPB	ACTIVE	WQFN	NJY	54	250	Green (RoHS & no Sb/Br)	SN	Level-3-260C-168 HR	-45 to 125	LMP92001SQ	Samples
LMP92001SQX/NOPB	ACTIVE	WQFN	NJY	54	2000	Green (RoHS & no Sb/Br)	SN	Level-3-260C-168 HR	-45 to 125	LMP92001SQ	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

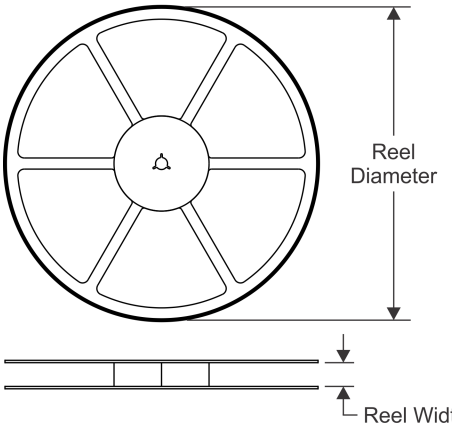
(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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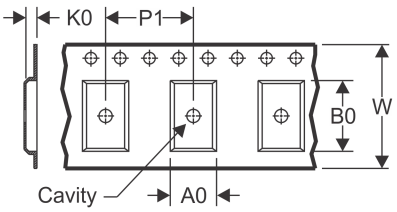
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TAPE AND REEL INFORMATION

REEL DIMENSIONS

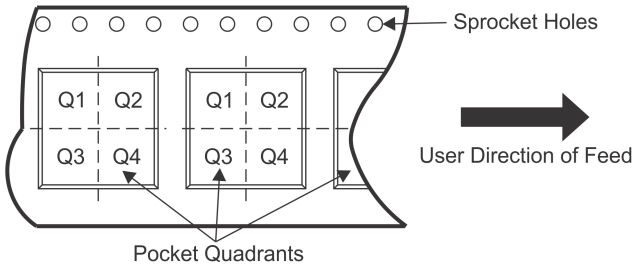


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

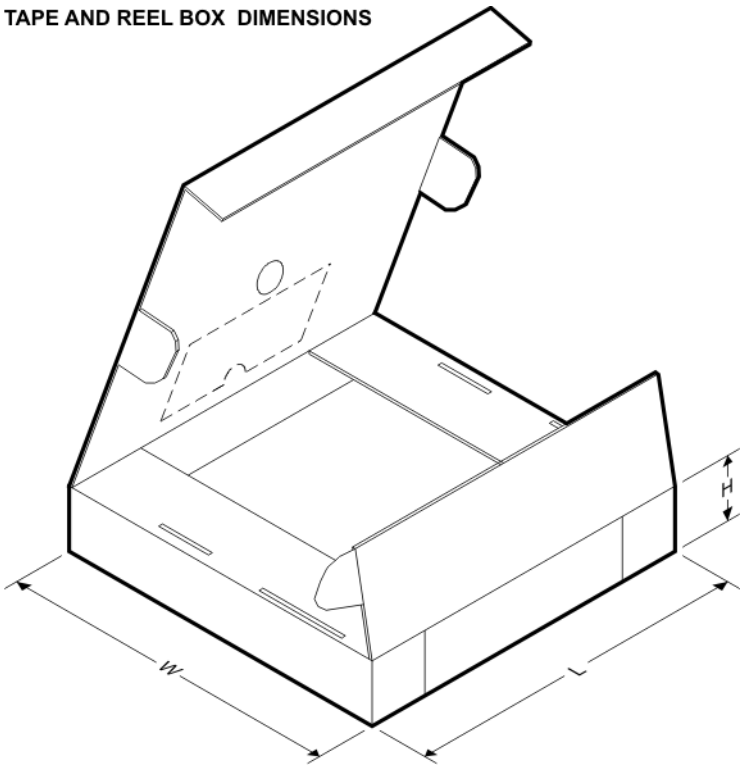
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

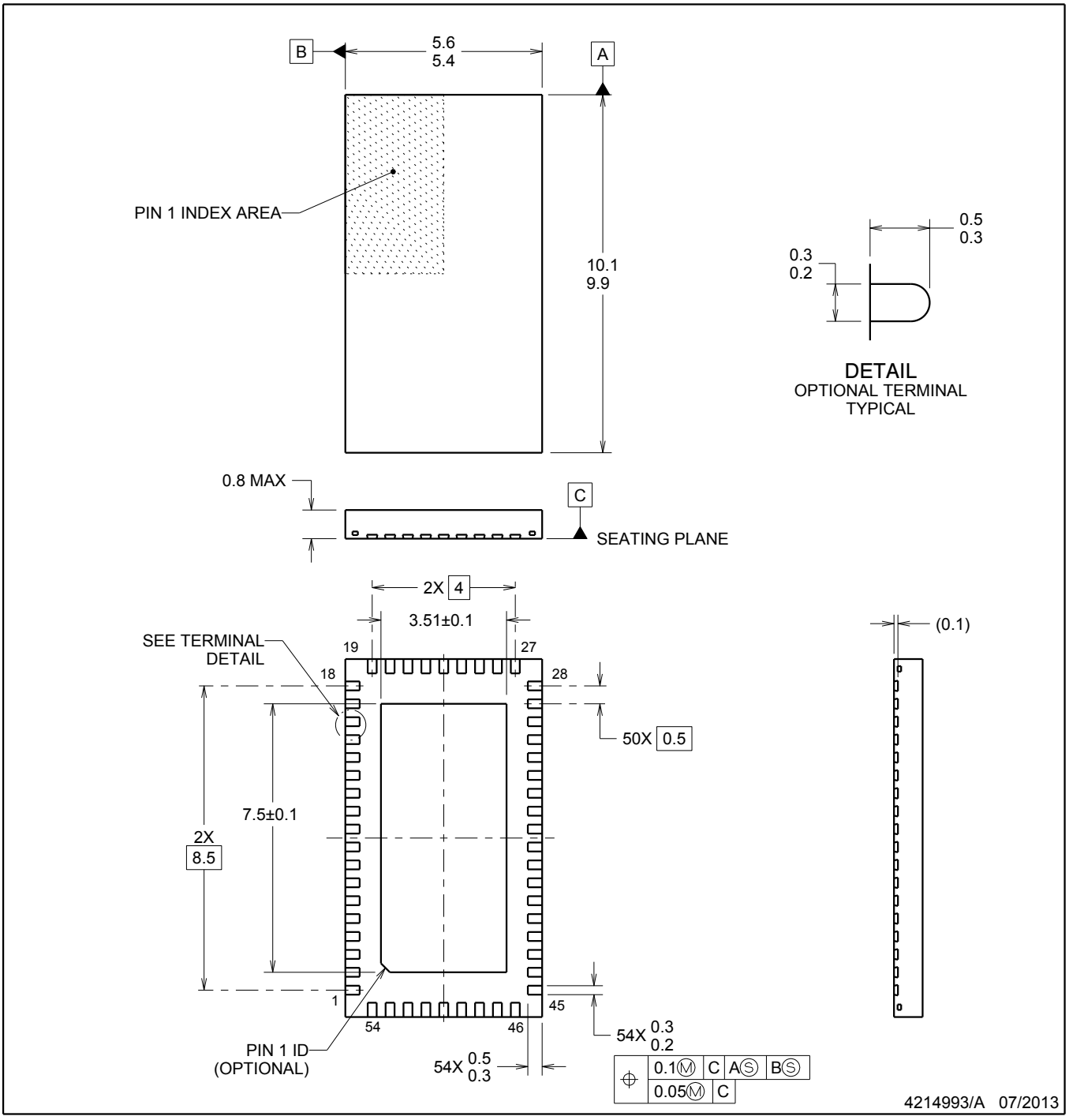
Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
LMP92001SQE/NOPB	WQFN	NJY	54	250	178.0	16.4	5.8	10.3	1.0	12.0	16.0	Q1
LMP92001SQX/NOPB	WQFN	NJY	54	2000	330.0	16.4	5.8	10.3	1.0	12.0	16.0	Q1

TAPE AND REEL BOX DIMENSIONS



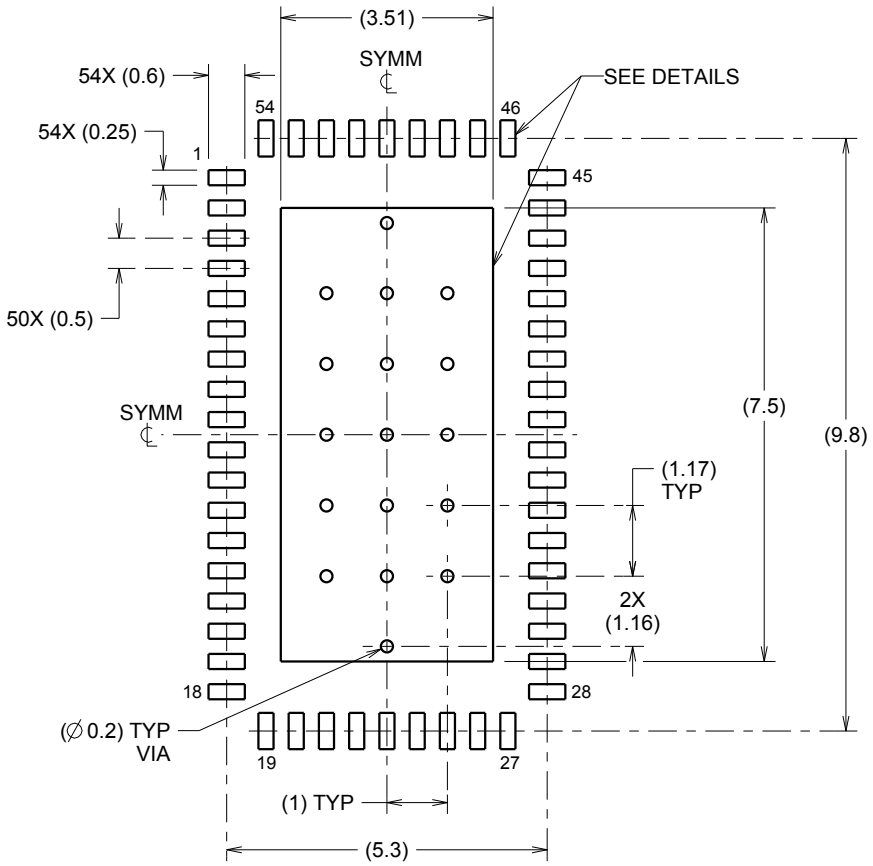
*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
LMP92001SQE/NOPB	WQFN	NJY	54	250	210.0	185.0	35.0
LMP92001SQX/NOPB	WQFN	NJY	54	2000	367.0	367.0	38.0

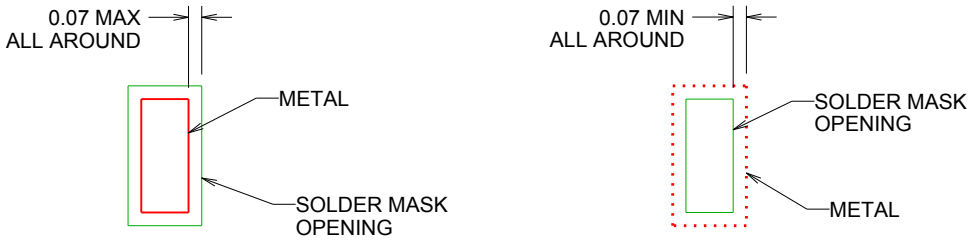


NOTES:

1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.



LAND PATTERN EXAMPLE
SCALE:8X



NON SOLDER MASK
DEFINED
(PREFERRED)

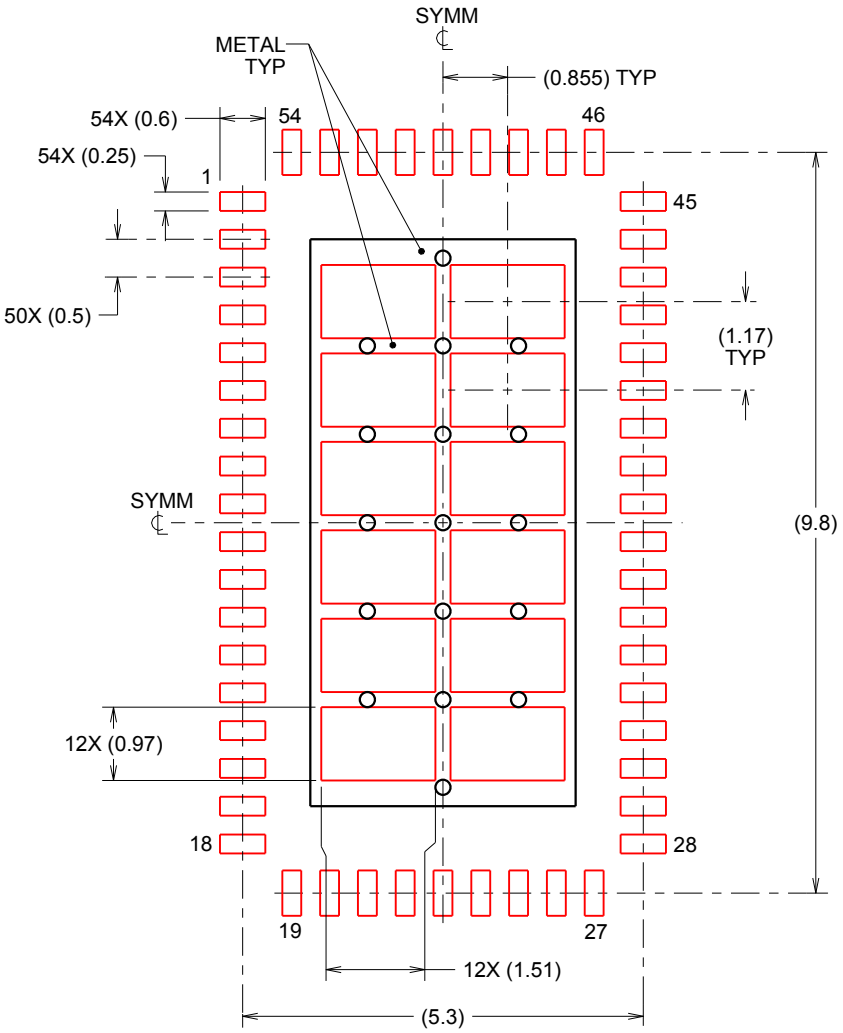
SOLDER MASK
DEFINED

SOLDER MASK DETAILS

4214993/A 07/2013

NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, refer to QFN/SON PCB application note in literature No. SLUA271 (www.ti.com/lit/slua271).



SOLDERPASTE EXAMPLE
BASED ON 0.125mm THICK STENCIL

EXPOSED PAD
67% PRINTED SOLDER COVERAGE BY AREA
SCALE:10X

4214993/A 07/2013

NOTES: (continued)

5. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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