LMP8601, LMP8601-Q1
LMP8602, LMP8602-Q1
LMP8603, LMP8603-Q1

SNOSAR2H – SEPTEMBER 2008 – REVISED APRIL 2016

LMP860x, LMP860x-Q1 60-V, Bidirectional, Low- or High-Side, Voltage-Output, Current-Sensing Amplifiers

1 Features

- Gain = 20x for LMP8601 and LMP8601-Q1
- Gain = 50x for LMP8602 and LMP8602-Q1
- Gain = 100x for LMP8603 and LMP8603-Q1
- TCV_{OS}: 10 µV/°C Maximum
- CMRR: 90-dB Minimum
- Input Offset Voltage: 1-mV Maximum
- CMVR at V_S = 3.3 V: –4 V to 27 V
- CMVR at V_S = 5 V: –22 V to 60 V
- Single-Supply Bidirectional Operation
- All Minimum and Maximum Limits 100% Tested
- Q1 Devices Qualified for Automotive Applications
- Q1 Devices ACE-Q100 Qualified With the Following Results:
  - Device Temperature Grade 1: –40°C to 125°C Ambient Operating Temperature Range
  - Device Temperature Grade 0: –40°C to 150°C (LMP8601EDRQ1 Only)
  - Device HBM ESD Classification Level 2 (3A on inputs)
  - Device CDM ESD Classification Level C6
  - Device MM ESD Classification Level M2

2 Applications

- High-Side and Low-Side Driver Configuration Current Sensing
- Bidirectional Current Measurement
- Current Loop to Voltage Conversion
- Automotive Fuel Injection Control
- Transmission Control
- Power Steering
- Battery Management Systems

3 Description

The LMP8601, LMP8602, LMP8603 (LMP860x) and LMP8601-Q1, LMP8602-Q1, LMP8603-Q1 (LMP860x-Q1) devices are fixed-gain, precision current-sense amplifiers (also referred to as current-shunt monitors). The input common-mode voltage range is –22 V to +60 V when operating from a single 5-V supply, or –4 V to +27 V with a 3.3-V supply. The LMP860x and LMP860x-Q1 are ideal parts for unidirectional and bidirectional current sensing applications.

These devices have a precise gain of 20x (LPM8601, LPM8601-Q1), 50x (LPM8602, LPM8602-Q1), and 100x (LPM8603, LPM8603-Q1), and are adequate in most targeted applications to drive an ADC to full-scale value. The fixed gain is achieved in two separate stages: a preamplifier with a gain of 10x and an output stage buffer amplifier with a gain of 2x (LMP8601, LMP8601-Q1), 5x (LMP8602, LMP8602-Q1), or 10x (LMP8603, LMP8603-Q1). The path between the two stages is brought out on two pins to enable the option of an additional filter network or modifying the gain.

The offset input pin enables these devices for unidirectional or bidirectional single supply voltage current sensing.

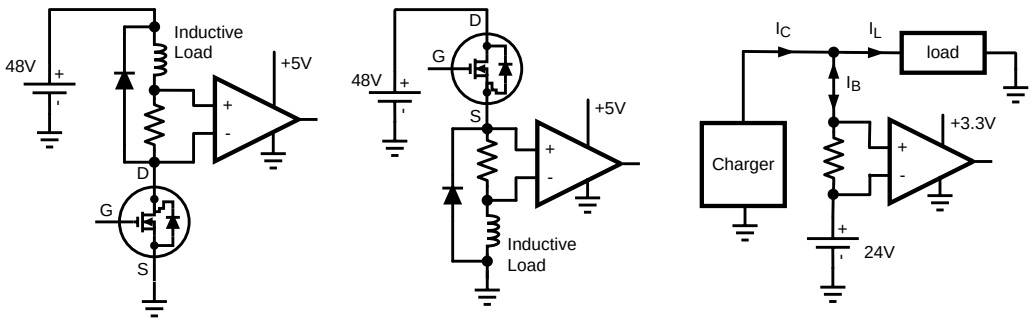
The LMP860x-Q1 devices incorporate enhanced manufacturing and support processes for the automotive market and are compliant with the AEC-Q100 standard.

Device Information(1)

PART NUMBER	PACKAGE	BODY SIZE (NOM)
LMP860x	SOIC (8)	4.90 mm x 3.91 mm
LMP860x-Q1		
LMP8602, LMP8603	VSSOP (8)	3.00 mm × 3.00 mm
LMP8602-Q1, LMP8603-Q1		

(1) For all available packages, see the package option addendum at the end of the data sheet.

Typical Applications



An IMPORTANT NOTICE at the end of this data sheet addresses availability, warranty, changes, use in safety-critical applications, intellectual property matters and other important disclaimers. PRODUCTION DATA.

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4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision G (July 2015) to Revision H — **Page**

- Added new temperature grade 0 version of LMP8601-Q1 ... 1
- Added LMP8602, LMP8602-Q1, LMP8603, and LMP8603-Q1 devices and related information to data sheet ... 1
- Changed *Features* bullets ... 1
- Changed text in *Description* section ... 1
- Added new values to *Thermal Information* table ... 5
- Changed $R_{\theta JA}$ value in *Thermal Information* table ... 5
- Deleted previous Note 1 from *Electrical Characteristics* tables ... 5
- Changed all AV1 to K1 throughout data sheet for consistency ... 6
- Changed all AV2 to K2 throughout data sheet for consistency ... 6
- Deleted previous Note 1 from *Electrical Characteristics* tables ... 7
- Deleted *Related Documentation* section; SNOSB36 data sheet content now combined with this data sheet ... 32

Changes from Revision F (January 2014) to Revision G — **Page**

- Added *ESD Ratings* table, and *Pin Configuration and Functions*, *Feature Description*, *Device Functional Modes*, *Application and Implementation*, *Power Supply Recommendations*, *Layout*, *Device and Documentation Support*, and *Mechanical, Packaging, and Orderable Information* sections. ... 1

Changes from Revision E (March 2013) to Revision F — **Page**

- Added four typical curves ... 17

Changes from Revision D (October 2009) to Revision E — **Page**

- Changed layout of National Data Sheet to TI format ... 30

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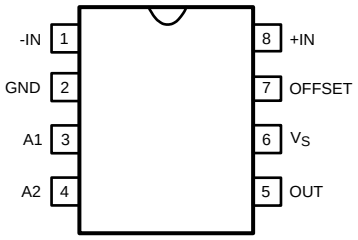
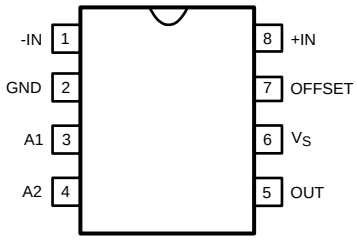
5 Pin Configuration and Functions

D Package
8-Pin SOIC
Top View



DGK Package
8-Pin VSSOP
Top View



Pin Descriptions

PIN		TYPE	DESCRIPTION
NAME	NO.		
A1	3	O	Preamplifier output
A2	4	I	Input from the external filter network and, or A1
GND	2	P	Power ground
+IN	8	I	Positive input
-IN	1	I	Negative input
OFFSET	7	I	DC offset for bidirectional signals
OUT	5	O	Single-ended output
V_S	6	P	Positive supply voltage

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6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

		MIN	MAX	UNIT
Supply voltage (V_S – GND)		–0.3	6	V
Continuous input voltage (–IN and +IN)		–22	60	V
Transient (400 ms)		–25	65	V
Maximum voltage at A1, A2, OFFSET and OUT pins		V_S + 0.3	GND – 0.3	V
Operating temperature, T_A	LMP8601EDRQ1 only	–40	150	°C
	All other devices	–40	125	
Junction temperature(2)		–40	150	°C
Mounting temperature	Infrared or convection (20 sec)		235	°C
	Wave soldering lead (10 sec)		260	
Storage temperature, T_{stg}		–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) The maximum power dissipation must be derated at elevated temperatures and is dictated by $T_{J(MAX)}$, $R_{\theta JA}$, and the ambient temperature, T_A. The maximum allowable power dissipation $P_{DMAX} = (T_{J(MAX)} – T_A) / R_{\theta JA}$ or the number given in *Absolute Maximum Ratings*, whichever is lower.

6.2 ESD Ratings: LMP860x

				VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	All pins except 1 and 8	±2000	V
			Pins 1 and 8	±4000	
		Charged-device model (CDM), per JEDEC specification JESD22-C101(2)		±1000	
		Machine model		±200	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 ESD Ratings: LMP860x-Q1

				VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per AEC Q100-002(1)	All pins except 1 and 8	±2000	V
			Pins 1 and 8	±4000	
		Charged-device model (CDM), per AEC Q100-011		±1000	
		Machine model		±200	

(1) AEC Q100-002 indicates that HBM stressing shall be in accordance with the ANSI/ESDA/JEDEC JS-001 specification.

6.4 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	MAX	UNIT
Supply voltage (V_S – GND)		3	5.5	V
OFFSET voltage (Pin 7)		0	V_S	V
Operating temperature, T_A (1)	LMP8601EDRQ1 only	–40	150	°C
	All other devices	–40	125	

(1) The maximum power dissipation must be derated at elevated temperatures and is dictated by $T_{J(MAX)}$, $R_{\theta JA}$, and the ambient temperature, T_A. The maximum allowable power dissipation $P_{DMAX} = (T_{J(MAX)} – T_A) / R_{\theta JA}$ or the number given in *Absolute Maximum Ratings*, whichever is lower.

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6.5 Thermal Information

THERMAL METRIC[1]		LMP860x, LMP860x-Q1	LMP8602, LMP8602-Q1, LMP8603, LMP8603-Q1	UNIT
		D (SOIC)	DGK (VSSOP)	
		8 PINS	8 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance[2]	113.1	171.1	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	57.3	64.1	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	53.5	91.1	°C/W
ψ_{JT}	Junction-to-top characterization parameter	11.1	9.4	°C/W
ψ_{JB}	Junction-to-board characterization parameter	53.0	89.7	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	N/A	N/A	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report, SPRA953.
(2) The maximum power dissipation must be derated at elevated temperatures and is dictated by $T_{J(MAX)}$, $R_{\theta JA}$, and the ambient temperature, T_A. The maximum allowable power dissipation $P_{DMAX} = (T_{J(MAX)} – T_A) / R_{\theta JA}$ or the number given in *Absolute Maximum Ratings*, whichever is lower.

6.6 Electrical Characteristics: V_S = 3.3 V

at T_A = 25°C, V_S = 3.3 V, GND = 0 V, –4 V ≤ V_{CM} ≤ 27 V, R_L = ∞, OFFSET (pin 7) is grounded, and 10 nF between V_S and GND (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN[1]	TYP[2]	MAX[1]	UNIT
OVERALL PERFORMANCE (FROM -IN (PIN 1) AND +IN (PIN 8) TO OUT (PIN 5) WITH PINS A1 (PIN 3) AND A2 (PIN 4) CONNECTED)							
I_S	Supply current				1		mA
		Over full temperature range		0.6		1.3	
A_V	Total gain	LMP8601, LMP8601-Q1		19.9	20	20.1	V/V
		LMP8602, LMP8602-Q1		49.75	50	50.25	
		LMP8603, LMP8603-Q1		99.5	100	100.5	
	Gain Drift[3]	Over full temperature range			–2.7	±20	ppm/°C
SR	Slew rate[4]	V_{IN} = ±0.165 V		0.4	0.7		V/µs
BW	Bandwidth			50	60		kHz
V_{OS}	Input offset voltage	$V_{CM} = V_S / 2$			0.15	±1	mV
TCV_{OS}	Input offset voltage drift[5]	Over full temperature range			2	±10	µV/°C
e_n	Input-referred voltage noise	0.1 Hz - 10 Hz, 6 sigma			16.4		μV_{P-P}
		Spectral density, 1 kHz			830		$nV/\sqrt{Hz}$
PSRR	Power-supply rejection ratio	3.0 V ≤ V_S ≤ 3.6 V, DC, $V_{CM} = V_S/2$			86		dB
			Over full temperature range	70			
	Midscale offset scaling accuracy	LMP8601, LMP8601-Q1			±0.15%	±0.5%	
			Input referred			±0.413	mV
		LMP8602, LMP8602-Q1			±0.25%	±1%	
			Input referred			±0.33	mV
		LMP8603, LMP8603-Q1			±0.45%	±1.5%	
			Input referred			±0.248	mV

(1) Data sheet min and max limits are specified by test.
(2) Typical values represent the most likely parameter norms at T_A = 25°C, and at the *Recommended Operation Conditions* at the time of product characterization.
(3) Both the gain of preamplifier K1 and the gain of buffer amplifier K2 are measured individually. The overall gain of both amplifiers (A_V) is also measured to assure the gain of all parts is always within the A_V limits.
(4) Slew rate is the average of the rising and falling slew rates.
(5) Offset voltage drift determined by dividing the change in V_{OS} at temperature extremes into the total temperature change.

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Electrical Characteristics: V_S = 3.3 V (continued)

at T_A = 25°C, V_S = 3.3 V, GND = 0 V, –4 V ≤ V_{CM} ≤ 27 V, R_L = ∞, OFFSET (pin 7) is grounded, and 10 nF between V_S and GND (unless otherwise noted)

PARAMETER		TEST CONDITIONS			MIN(1)	TYP(2)	MAX(1)	UNIT
PREAMPLIFIER (FROM INPUT PINS -IN, (PIN 1) AND +IN (PIN 8) TO A1 (PIN 3))								
R_{CM}	Input impedance common mode	–4 V ≤ V_{CM} ≤ 27 V				295		kΩ
			Over full temperature range		250		350	
R_{DM}	Input impedance differential mode	–4 V ≤ V_{CM} ≤ 27 V				590		kΩ
			Over full temperature range		500		700	
V_{OS}	Input offset voltage	V_{CM} = V_S / 2				±0.15	±1	mV
DC CMRR	DC common-mode rejection ratio	–2 V ≤ V_{CM} ≤ 24 V				96		dB
			Over full temperature range		86			
AC CMRR	AC common-mode rejection ratio(6)	f = 1 kHz			80	94		dB
		f = 10 kHz				85		
CMVR	Input common-mode voltage range	for 80-dB CMRR	Over full temperature range		–4		27	V
K1	Preamplifier gain(3)				9.95	10.0	10.05	V/V
R_{F-INT}	Output impedance filter resistor					100		kΩ
		–40°C ≤ T_A ≤ 125°C			99		101	
		–40°C ≤ T_A ≤ 150°C, LMP8601EDRQ1 only			97		103	
TCR_{F-INT}	Output impedance filter resistor drift	Over full temperature range				±5	±50	ppm/°C
A1 V_{OUT}	A1 output voltage swing	V_{OL}, R_L = ∞				2		mV
			Over full temperature range				10	
		V_{OH}, R_L = ∞				3.25		V
			Over full temperature range		3.2			
OUTPUT BUFFER (FROM A2 (PIN 4) TO OUT (PIN 5))								
V_{OS}	Input offset voltage	0V ≤ V_{CM} ≤ V_S			–2	±0.5	2	mV
			Over full temperature range		–2.5		2.5	
K2	Output buffer gain(3)	LMP8601, LMP8601-Q1			1.99	2	2.01	V/V
		LMP8602, LMP8602-Q1			4.975	5	5.025	
		LMP8603, LMP8603-Q1			9.95	10	10.05	
I_B	Input bias current of A2(7),					–40		fA
		Over full temperature range					±20	nA
A2 V_{OUT}	A2 output voltage swing(8) (9)	V_{OL}, R_L = 100 kΩ	LMP8601, LMP8601-Q1,			4		mV
				Over full temperature range			20	
			LMP8602, LMP8602-Q1			10		
				Over full temperature range			40	
			LMP8603, LMP8603-Q1			10		
				Over full temperature range			80	
		V_{OH}, R_L = 100 kΩ				3.29		V
			Over full temperature range		3.28			
I_{SC}	Output short-circuit current(10)	Sourcing, V_{IN} = V_S, V_{OUT} = GND			–25	–38	–60	mA
		Sinking, V_{IN} = GND, V_{OUT} = V_S			30	46	65	

(6) AC common-mode signal is a 5-V_{PP} sine-wave (0 V to 5 V) at the given frequency.
(7) Positive current corresponds to current flowing into the device.
(8) For this test input is driven from A1 stage.
(9) For V_{OL}, R_L is connected to V_S and for V_{OH}, R_L is connected to GND.
(10) Short-Circuit test is a momentary test. Continuous short circuit operation at elevated ambient temperature can result in exceeding the maximum allowed junction temperature of 150°C.

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6.7 Electrical Characteristics: V_S = 5 V

at T_A = 25°C, V_S = 5 V, GND = 0 V, –22 V ≤ V_{CM} ≤ 60 V, R_L = ∞, OFFSET (pin 7) is grounded, and 10 nF between V_S and GND (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN(1)	TYP(2)	MAX(1)	UNIT
OVERALL PERFORMANCE (FROM -IN (PIN 1) AND +IN (PIN 8) TO OUT (PIN 5) WITH PINS A1 (PIN 3) AND A2 (PIN 4) CONNECTED)							
I_S	Supply current				1.1		mA
		Over full temperature range		0.7		1.5	
A_V	Total gain(3)	LMP8601, LMP8601-Q1		19.9	20	20.1	V/V
		LMP8602, LMP8602-Q1		49.75	50	50.25	
		LMP8603, LMP8603-Q1		99.5	100	100.5	
	Gain drift	–40°C ≤ T_A ≤ 125°C			–2.8	±20	ppm/°C
SR	Slew rate(4)	V_{IN} = ±0.25 V		0.6	0.83		V/µs
BW	Bandwidth			50	60		kHz
V_{OS}	Input offset voltage				0.15	±1	mV
TCV_{OS}	Input offset voltage drift(5)	–40°C ≤ T_A ≤ 125°C			2	±10	µV/°C
e_N	Input-referred voltage noise	0.1 Hz - 10 Hz, 6 sigma			17.5		μV_{P-P}
		Spectral density, 1 kHz			890		nV/√Hz
PSRR	Power-supply rejection ratio	4.5 V ≤ V_S ≤ 5.5 V, DC			90		dB
			Over full temperature range	70			
	Midscale offset scaling accuracy	LMP8601, LMP8601-Q1			±0.15%	±0.5%	
			Input-referred			±0.625	mV
		LMP8602, LMP8602-Q1			±0.25%	±1%	
			Input-referred			±0.50	mV
		LMP8603, LMP8603-Q1			±0.45%	±1.5%	
			Input-referred			±0.375	mV

(1) Data sheet min and max limits are specified by test.
(2) Typical values represent the most likely parameter norms at T_A = 25°C, and at the *Recommended Operation Conditions* at the time of product characterization.
(3) Both the gain of preamplifier K1 and the gain of buffer amplifier K2 are measured individually. The overall gain of both amplifiers (A_V) is also measured to assure the gain of all parts is always within the A_V limits.
(4) Slew rate is the average of the rising and falling slew rates.
(5) Offset voltage drift determined by dividing the change in V_{OS} at temperature extremes into the total temperature change.

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Electrical Characteristics: V_S = 5 V (continued)

at T_A = 25°C, V_S = 5 V, GND = 0 V, –22 V ≤ V_{CM} ≤ 60 V, R_L = ∞, OFFSET (pin 7) is grounded, and 10 nF between V_S and GND (unless otherwise noted)

PARAMETER		TEST CONDITIONS			MIN(1)	TYP(2)	MAX(1)	UNIT
PREAMPLIFIER (FROM INPUT PINS -IN (PIN 1) AND +IN (PIN 8) TO A1 (PIN 3))								
R_{CM}	Input impedance, common mode	0 V ≤ V_{CM} ≤ 60 V				295		kΩ
			Over full temperature range		250		350	
		–20 V ≤ V_{CM} ≤ 0 V				193		kΩ
			Over full temperature range		165		250	
R_{DM}	Input impedance, differential mode	0 V ≤ V_{CM} ≤ 60 V				590		kΩ
			Over full temperature range		500		700	
		–20 V ≤ V_{CM} ≤ 0 V				386		kΩ
			Over full temperature range		300		500	
V_{OS}	Input offset voltage	V_{CM} = V_S / 2				±0.15	±1	mV
DC CMRR	DC common-mode rejection ratio	–20 V ≤ V_{CM} ≤ 60 V				105		dB
			Over full temperature range		90			
AC CMRR	AC common-mode rejection ratio(6)	f = 1 kHz			80	96		dB
		f = 10 kHz				83		
CMVR	Input common-mode voltage range	for 80-dB CMRR	Over full temperature range		–22		60	V
K1	Preamplifier gain(3)				9.95	10	10.05	V/V
R_{F-INT}	Output impedance filter resistor					100		kΩ
		–40°C ≤ T_A ≤ 125°C,			99		101	
		–40°C ≤ T_A ≤ 150°C, LMP8601EDRQ1 only			97		103	
TCR_{F-INT}	Output impedance filter resistor drift					±5	±50	ppm/°C
A1 V_{OUT}	A1 output voltage swing	V_{OL}, R_L = ∞				2		mV
			Over full temperature range				10	
		V_{OH}, R_L = ∞				4.985		V
			Over full temperature range		4.95			
OUTPUT BUFFER (FROM A2 (PIN 4) TO OUT (PIN 5))								
V_{OS}	Input offset voltage	0V ≤ V_{CM} ≤ V_S			–2	±0.5	2	mV
			Over full temperature range		–2.5		2.5	
K2	Output buffer gain(3)	LMP8601, LMP8601-Q1			1.99	2	2.01	V/V
		LMP8602, LMP8602-Q1			4.975	5	5.025	
		LMP8603, LMP8603-Q1			9.95	10	10.05	
I_B	Input bias current of A2(7)					–40		fA
		Over full temperature range					±20	nA
A2 V_{OUT}	A2 output voltage swing(8) (9)	V_{OL}, R_L = ∞	LMP8601, LMP8601-Q1,			4		mV
				Over full temperature range			20	
			LMP8602, LMP8602-Q1			10		
				Over full temperature range			40	
			LMP8602, LMP8603-Q1			10		
				Over full temperature range			80	
		V_{OH}, R_L = ∞				4.99		V
			Over full temperature range		4.98			
I_{SC}	Output short-circuit current(10)	Sourcing, V_{IN} = V_S, V_{OUT} = GND			–25	–42	–60	mA
		Sinking, V_{IN} = GND, V_{OUT} = V_S			30	48	65	

(6) AC common-mode signal is a 5-V_{PP} sine-wave (0 V to 5 V) at the given frequency.
(7) Positive current corresponds to current flowing into the device.
(8) For this test input is driven from A1 stage.
(9) For V_{OL}, R_L is connected to V_S and for V_{OH}, R_L is connected to GND.
(10) Short-Circuit test is a momentary test. Continuous short circuit operation at elevated ambient temperature can result in exceeding the maximum allowed junction temperature of 150°C.

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6.8 Typical Characteristics

at T_A = 25°C, V_S = 5 V, GND = 0 V, –22 ≤ V_{CM} ≤ 60 V, R_L = ∞, OFFSET (pin 7) connected to V_S, and 10 nF between V_S and GND (unless otherwise noted)

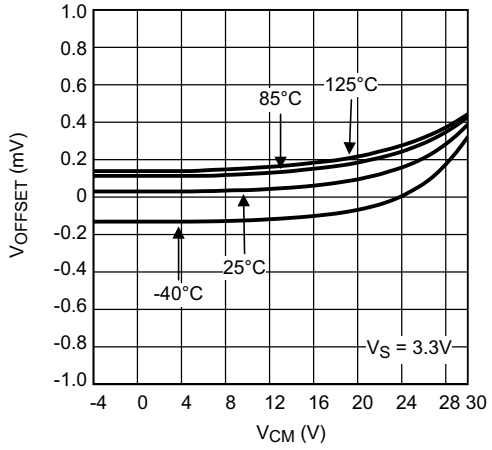

Figure 1. V_{OS} vs V_{CM} at V_S = 3.3 V

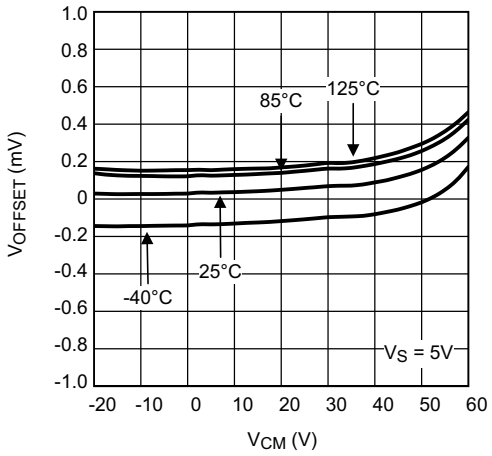

Figure 2. V_{OS} vs V_{CM} at V_S = 5 V

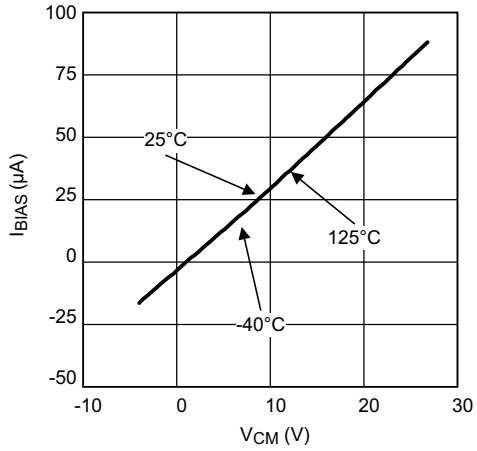

Figure 3. Input Bias Current Over Temperature (+IN and –IN pins) at V_S = 3.3 V

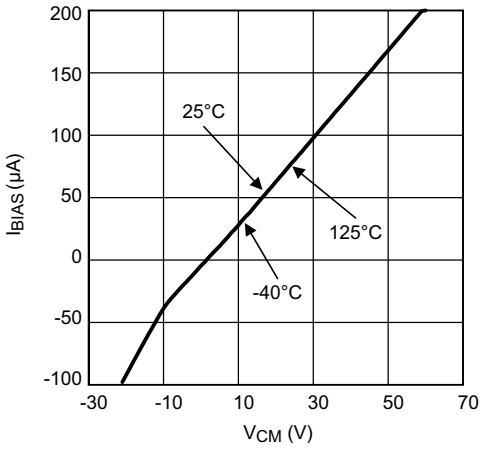

Figure 4. Input Bias Current Over Temperature (+IN and –IN pins) at V_S = 5 V

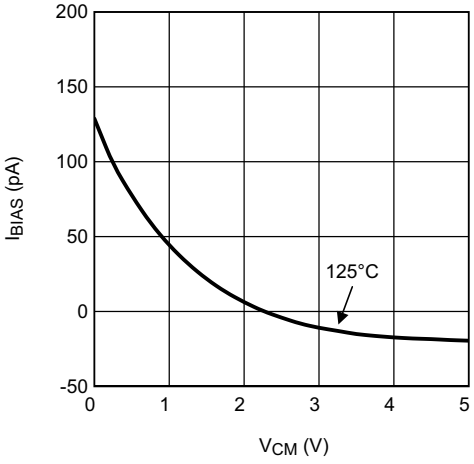

Figure 5. Input Bias Current Over Temperature (A2 pin) at V_S = 5 V

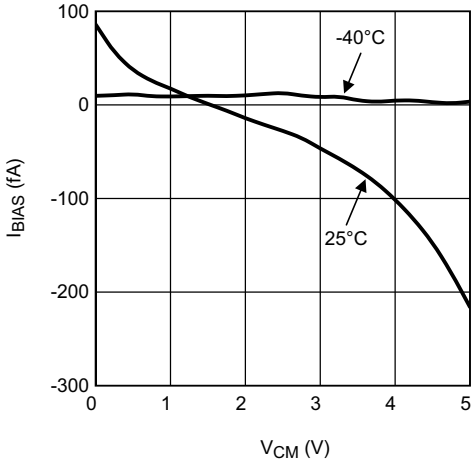

Figure 6. Input Bias Current Over Temperature (A2 pin) at V_S = 5 V

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Typical Characteristics (continued)

at T_A = 25°C, V_S = 5 V, GND = 0 V, –22 ≤ V_{CM} ≤ 60 V, R_L = ∞, OFFSET (pin 7) connected to V_S, and 10 nF between V_S and GND (unless otherwise noted)

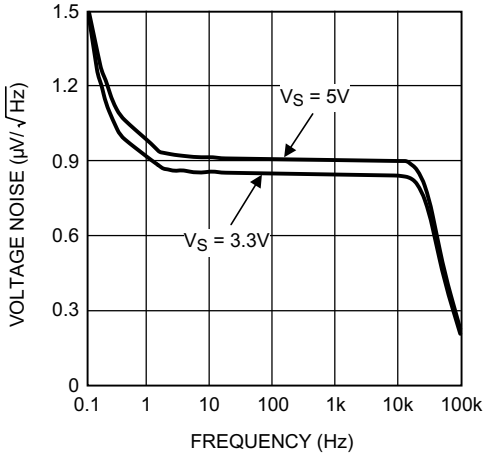

Figure 7. Input-Referred Voltage Noise vs Frequency

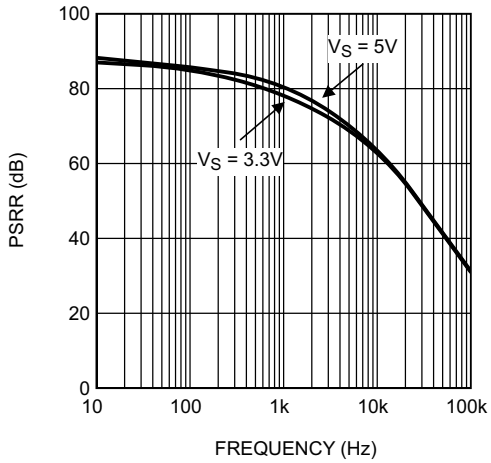

Figure 8. PSRR vs Frequency

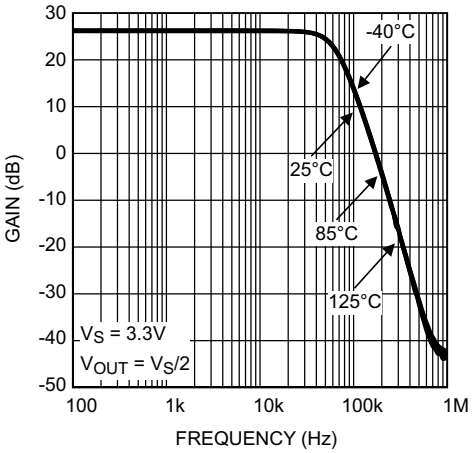

Figure 9. Gain vs Frequency at V_S = 3.3 V

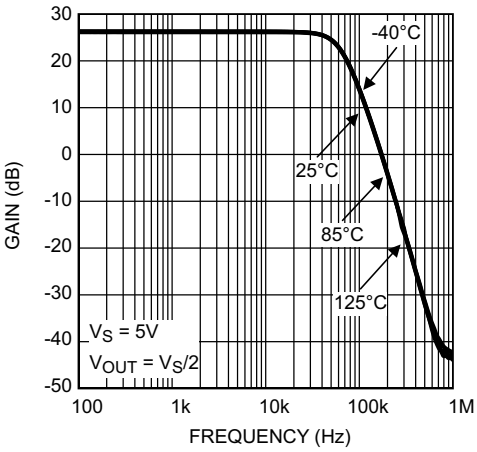

Figure 10. Gain vs Frequency at V_S = 5 V

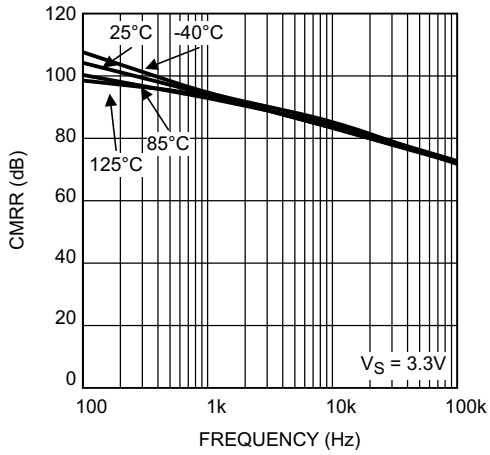

Figure 11. CMRR vs Frequency at V_S = 3.3 V

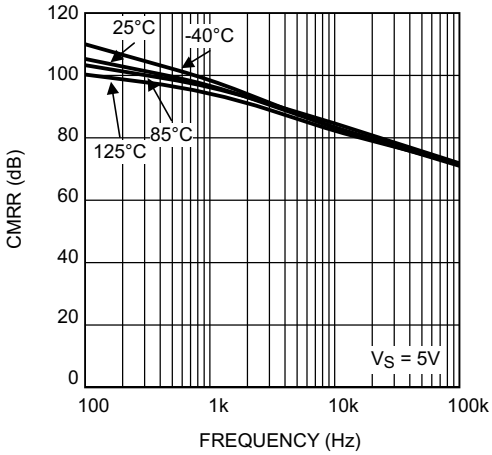

Figure 12. CMRR vs Frequency at V_S = 5 V

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Typical Characteristics (continued)

at T_A = 25°C, V_S = 5 V, GND = 0 V, –22 ≤ V_{CM} ≤ 60 V, R_L = ∞, OFFSET (pin 7) connected to V_S, and 10 nF between V_S and GND (unless otherwise noted)

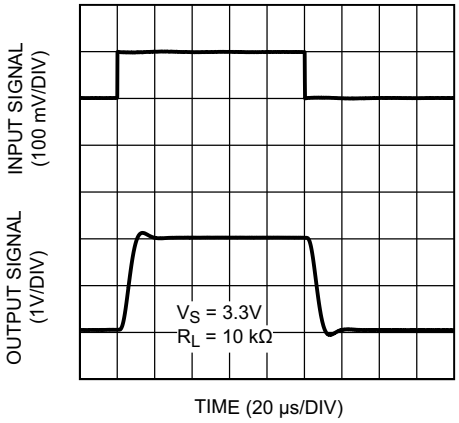

Figure 13. Step Response at V_S = 3.3 V LMP8601 and LMP8601-Q1

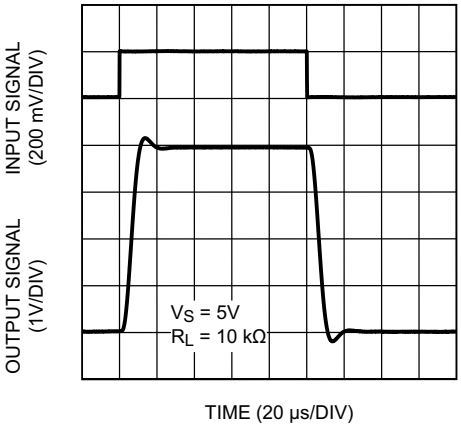

Figure 14. Step Response at V_S = 5 V LMP8601 and LMP8601-Q1

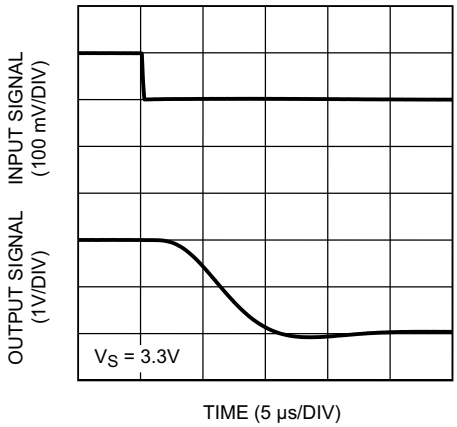

Figure 15. Settling Time (Falling Edge) at V_S = 3.3 V LMP8601 and LMP8601-Q1

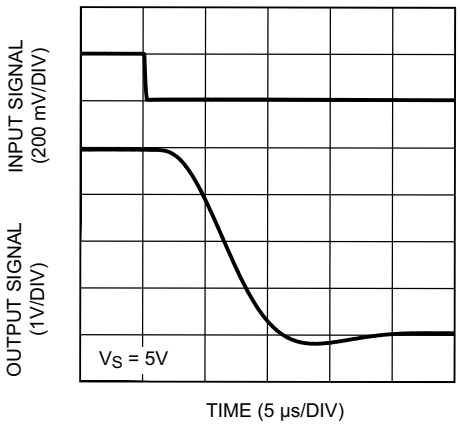

Figure 16. Settling Time (Falling Edge) at V_S = 5 V LMP8601 and LMP8601-Q1

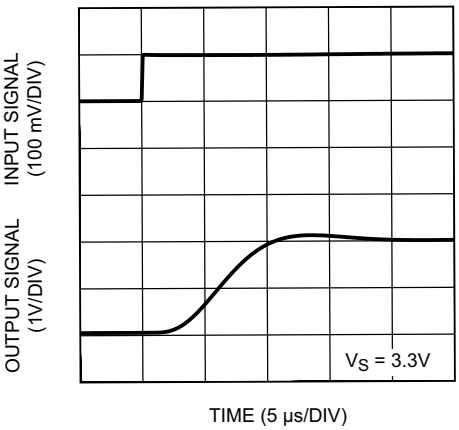

Figure 17. Settling Time (Rising Edge) at V_S = 3.3 V LMP8601 and LMP8601-Q1

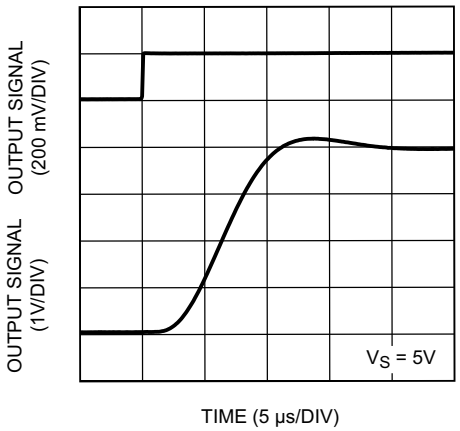

Figure 18. Settling Time (Rising Edge) at V_S = 5 V LMP8601 and LMP8601-Q1

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Typical Characteristics (continued)

at T_A = 25°C, V_S = 5 V, GND = 0 V, –22 ≤ V_{CM} ≤ 60 V, R_L = ∞, OFFSET (pin 7) connected to V_S, and 10 nF between V_S and GND (unless otherwise noted)

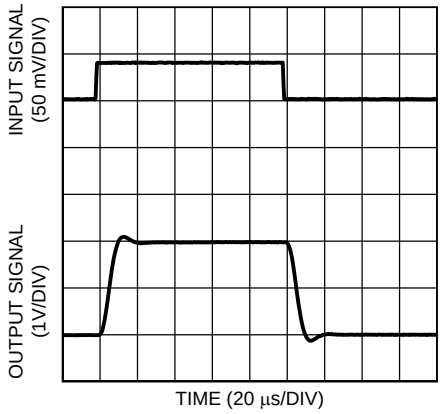

Figure 19. Step Response at V_S = 3.3 V, R_L = 10 kΩ
LMP8602 and LMP8602-Q1

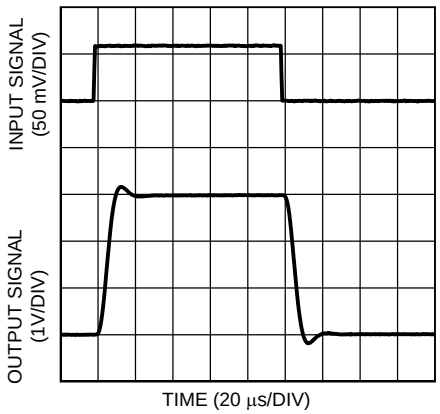

Figure 20. Step Response at V_S = 5 V, R_L = 10 kΩ
LMP8602 and LMP8602-Q1

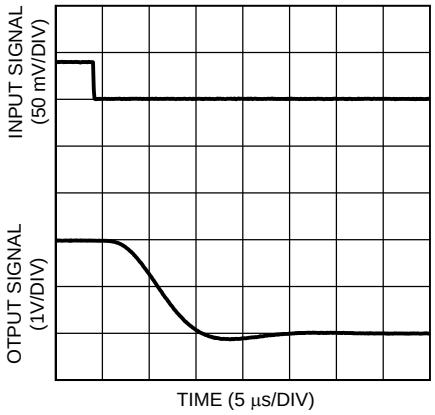

Figure 21. Settling Time (Falling Edge) at V_S = 3.3 V
LMP8602 and LMP8602-Q1

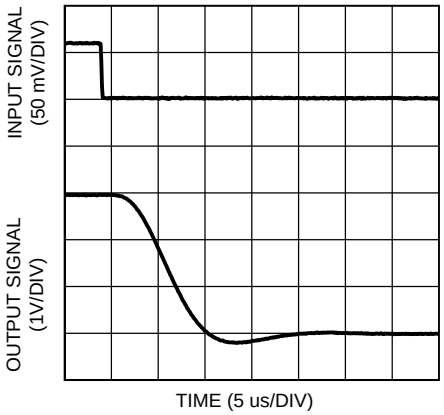

Figure 22. Settling Time (Falling Edge) at V_S = 5 V
LMP8602 and LMP8602-Q1

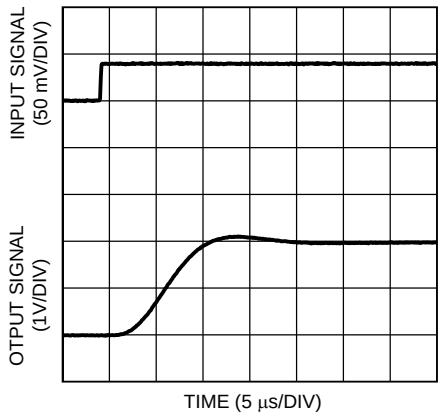

Figure 23. Settling Time (Rising Edge) at V_S = 3.3 V
LMP8602 and LMP8602-Q1

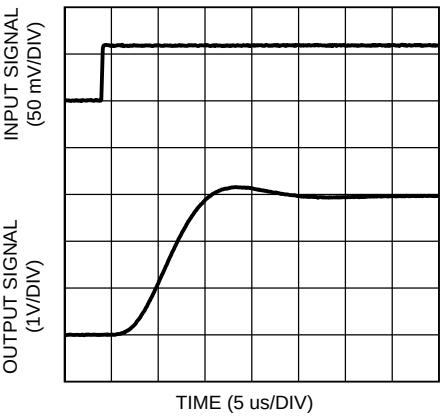

Figure 24. Settling Time (Rising Edge) at V_S = 5 V
LMP8602 and LMP8602-Q1

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Typical Characteristics (continued)

at T_A = 25°C, V_S = 5 V, GND = 0 V, –22 ≤ V_{CM} ≤ 60 V, R_L = ∞, OFFSET (pin 7) connected to V_S, and 10 nF between V_S and GND (unless otherwise noted)

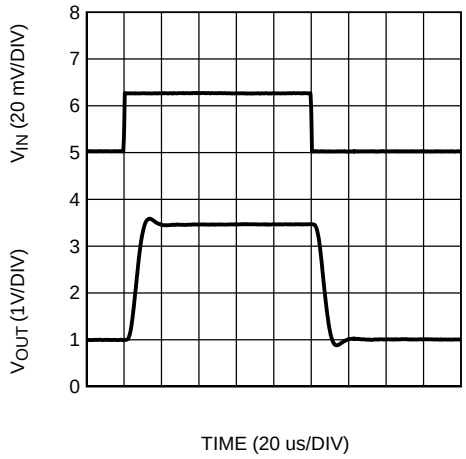

Figure 25. Step Response at V_S = 3.3 V, R_L = 10 kΩ LMP8603 and LMP8603-Q1

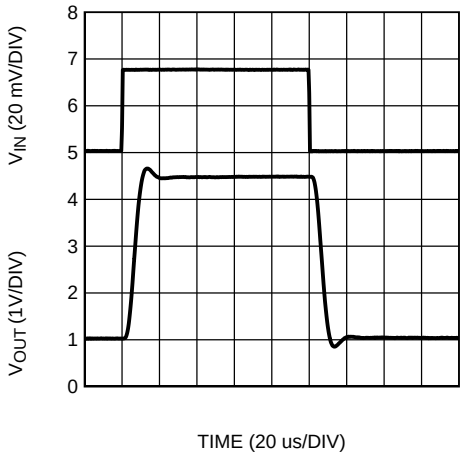

Figure 26. Step Response at V_S = 5 V, R_L = 10 kΩ LMP8603 and LMP8603-Q1

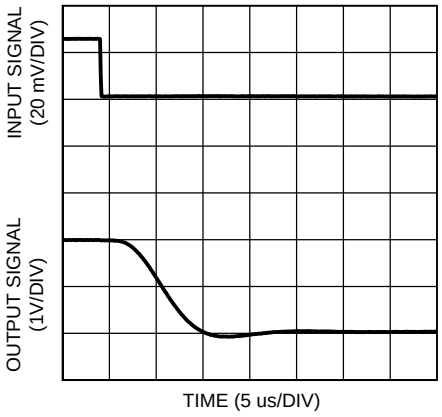

Figure 27. Settling Time (Falling Edge) at V_S = 3.3 V LMP8603 and LMP8603-Q1

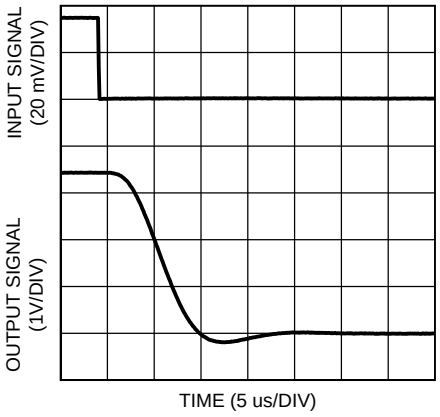

Figure 28. Settling Time (Falling Edge) at V_S = 5 V LMP8603 and LMP8603-Q1

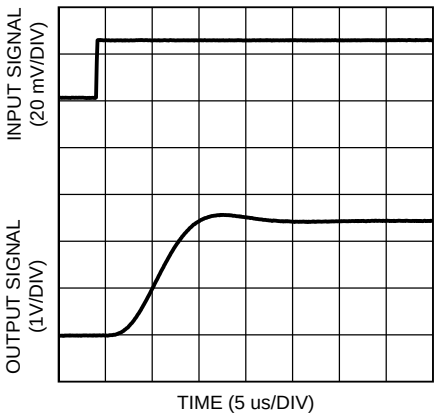

Figure 29. Settling Time (Rising Edge) at V_S = 3.3 V LMP8603 and LMP8603-Q1

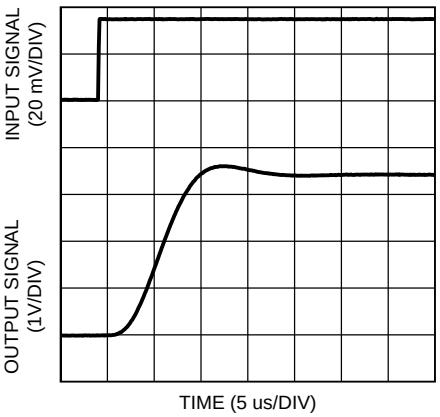

Figure 30. Settling Time (Rising Edge) at V_S = 5 V LMP8603 and LMP8603-Q1

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Typical Characteristics (continued)

at T_A = 25°C, V_S = 5 V, GND = 0 V, –22 ≤ V_{CM} ≤ 60 V, R_L = ∞, OFFSET (pin 7) connected to V_S, and 10 nF between V_S and GND (unless otherwise noted)

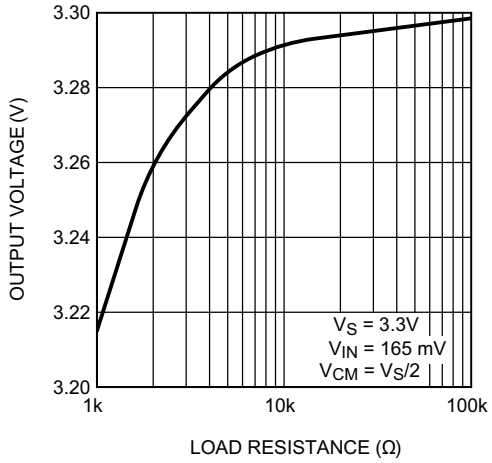

Figure 31. Positive Swing vs R_{LOAD} at V_S = 3.3 V

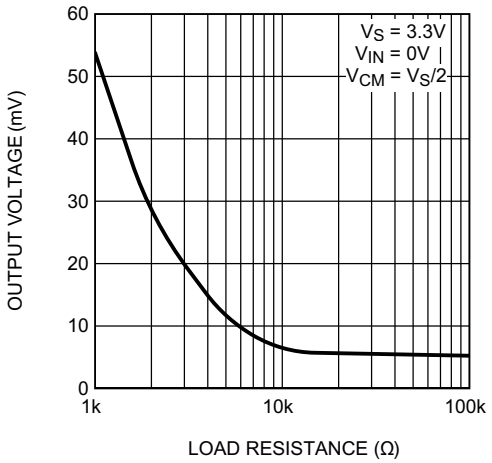

Figure 32. Negative Swing vs R_{LOAD} at V_S = 3.3 V

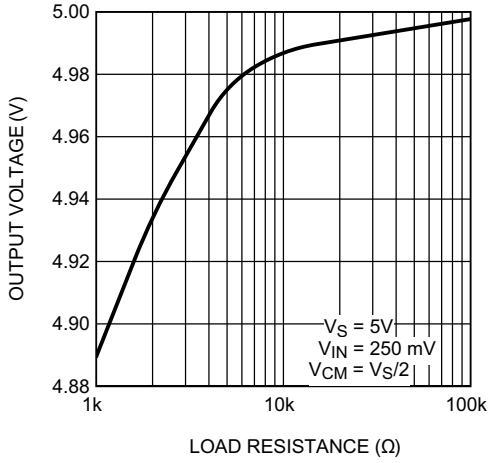

Figure 33. Positive Swing vs R_{LOAD} V_S = 5 V

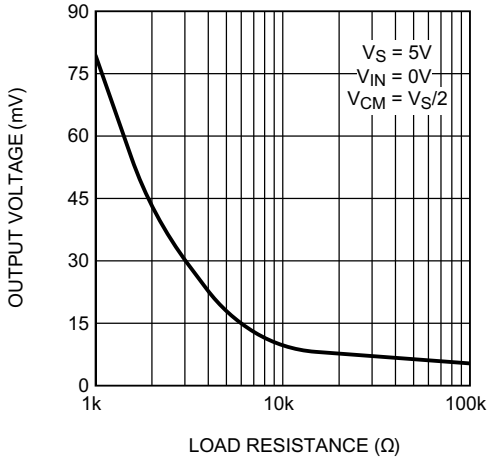

Figure 34. Negative Swing vs R_{LOAD} at V_S = 5 V

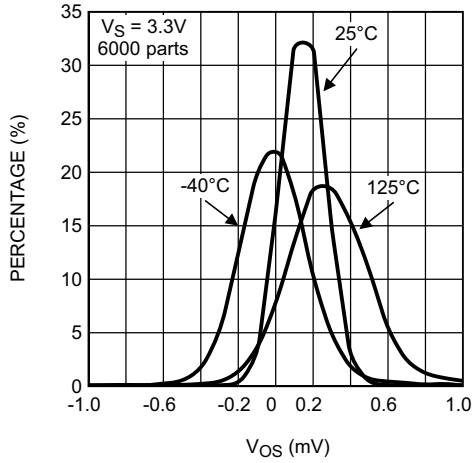

Figure 35. V_{OS} Distribution at V_S = 3.3 V

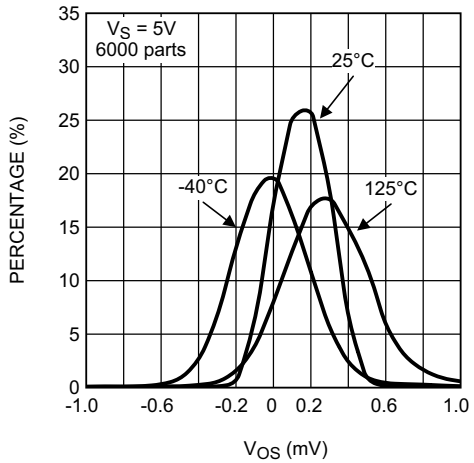

Figure 36. V_{OS} Distribution at V_S = 5 V

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Typical Characteristics (continued)

at T_A = 25°C, V_S = 5 V, GND = 0 V, –22 ≤ V_{CM} ≤ 60 V, R_L = ∞, OFFSET (pin 7) connected to V_S, and 10 nF between V_S and GND (unless otherwise noted)

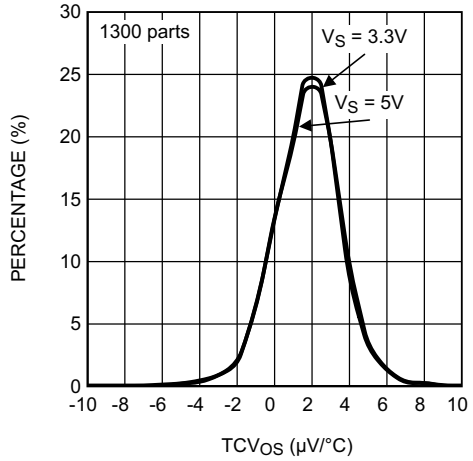

Figure 37. TCV_{OS} Distribution

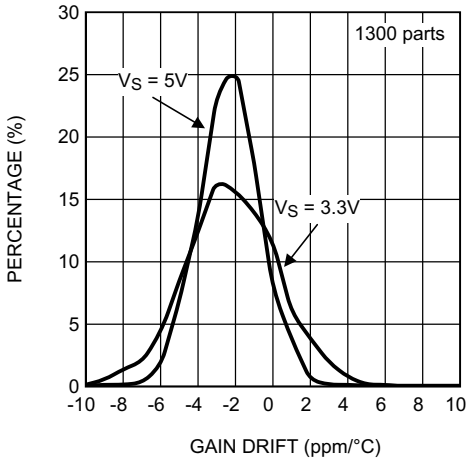

Figure 38. Gain Drift Distribution, 1300 Parts LMP8601 and LMP8601-Q1

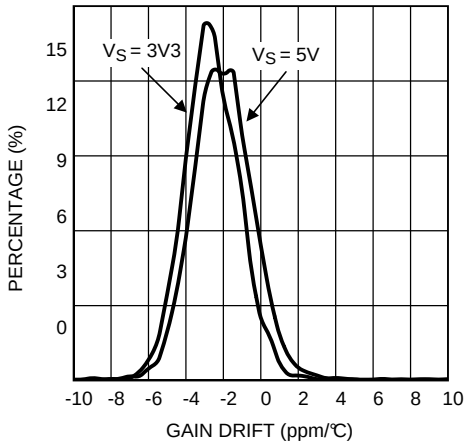

Figure 39. Gain Drift Distribution, 5000 Parts LMP8602 and LMP8602-Q1

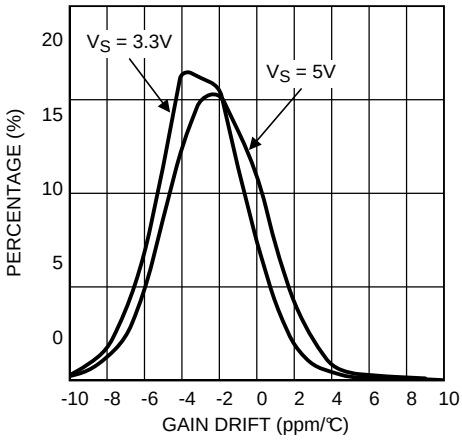

Figure 40. Gain Drift Distribution, 5000 Parts LMP8603 and LMP8603-Q1

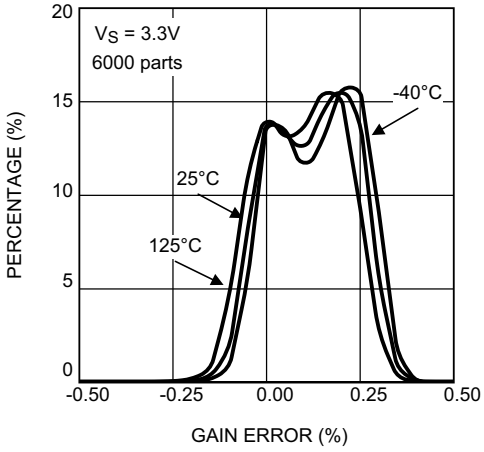

Figure 41. Gain Error Distribution at V_S = 3.3 V LMP8601 and LMP8601-Q1

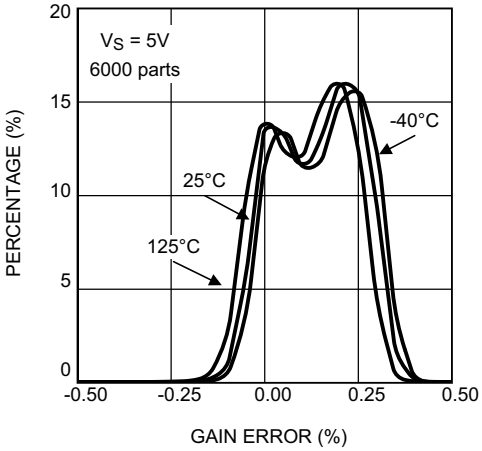

Figure 42. Gain Error Distribution at V_S = 5 V LMP8601 and LMP8601-Q1

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Typical Characteristics (continued)

at T_A = 25°C, V_S = 5 V, GND = 0 V, –22 ≤ V_{CM} ≤ 60 V, R_L = ∞, OFFSET (pin 7) connected to V_S, and 10 nF between V_S and GND (unless otherwise noted)

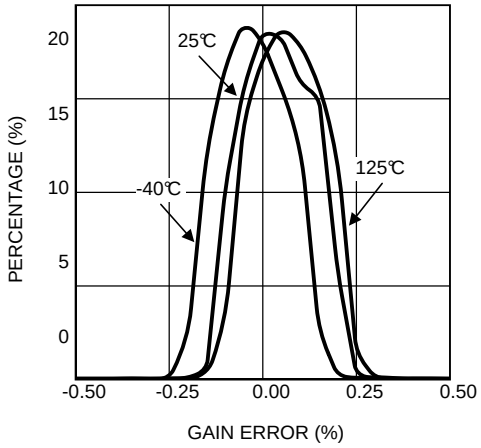

Figure 43. Gain Error Distribution at V_S = 3.3 V, 5000 Parts LMP8602 and LMP8602-Q1

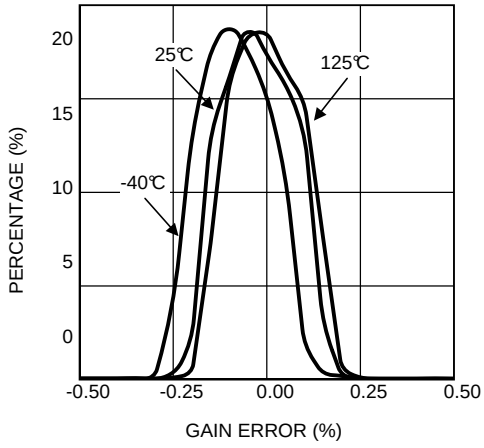

Figure 44. Gain Error Distribution at V_S = 5 V, 5000 Parts LMP8602 and LMP8602-Q1

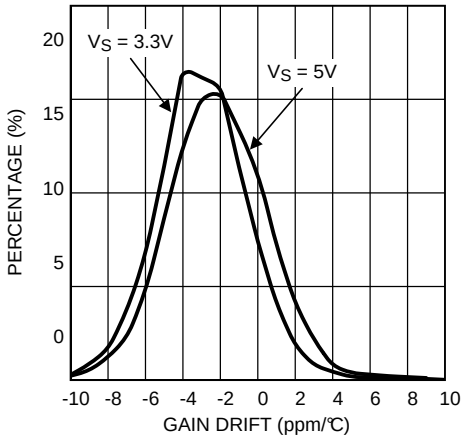

Figure 45. Gain Error Distribution at V_S = 3.3 V, 5000 Parts LMP8603 and LMP8603-Q1

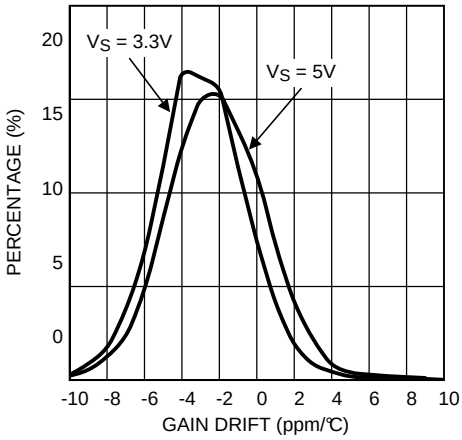

Figure 46. Gain Error Distribution at V_S = 5 V LMP8603 and LMP8603-Q1

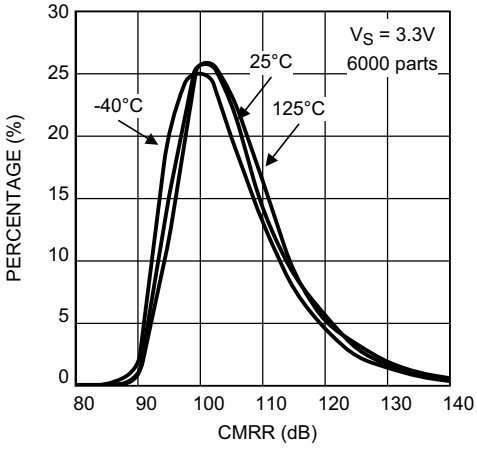

Figure 47. CMRR Distribution at V_S = 3.3 V

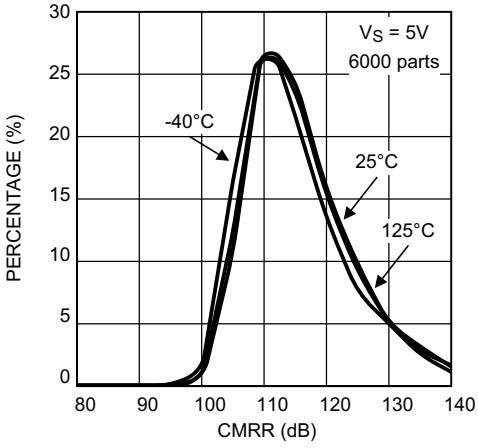

Figure 48. CMRR Distribution at V_S = 5 V

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Typical Characteristics (continued)

at T_A = 25°C, V_S = 5 V, GND = 0 V, –22 ≤ V_{CM} ≤ 60 V, R_L = ∞, OFFSET (pin 7) connected to V_S, and 10 nF between V_S and GND (unless otherwise noted)

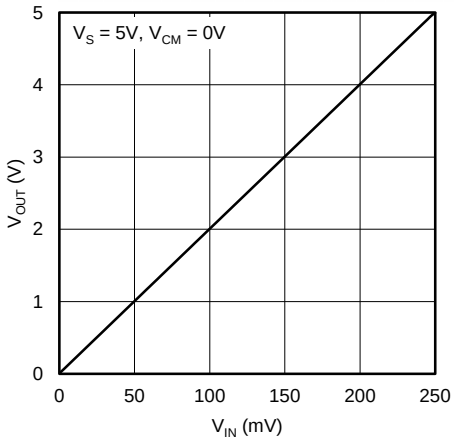

Figure 49. Output Voltage vs VIN

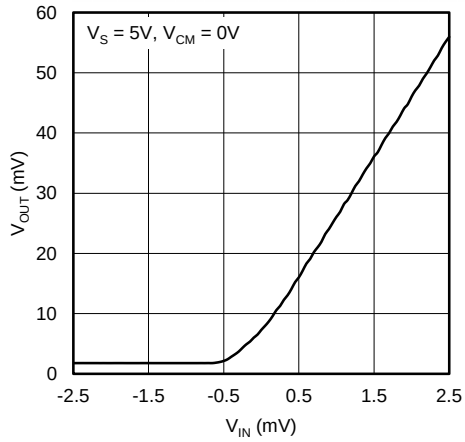

Figure 50. Output Voltage vs VIN (Enlarged Close to 0 V)

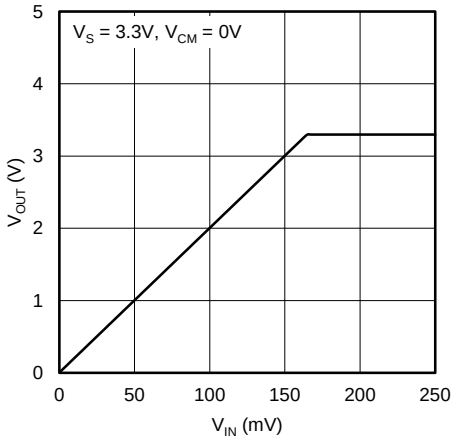

Figure 51. Output Voltage vs VIN

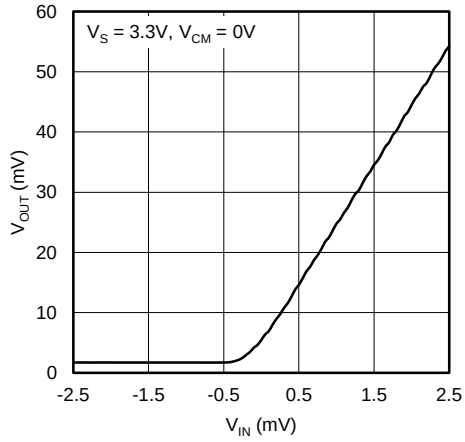

Figure 52. Output Voltage vs VIN (Enlarged Close to 0 V)

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7 Detailed Description

7.1 Overview

The LMP860x and LMP860x-Q1 are fixed gain differential voltage precision amplifiers, with a –22-V to +60-V input common-mode voltage range when operating from a single 5-V supply, or a –4-V to +27-V input common-mode voltage range when operating from a single 3.3-V supply. The LMP8601 and LMP8601-Q1 have a gain of 20x, the LMP8602 and LMP8602-Q1 have a gain of 50x, and the LMP8603 and LMP8603-Q1 have a gain of 100x.

The LMP860x and LMP860x-Q1 are members of the LMP family and are ideal parts for unidirectional and bidirectional current sensing applications. Because of the proprietary chopping level-shift input stage, the LMP860x and LMP860x-Q1 achieve very low offset, very low thermal offset drift, and very high CMRR. The LMP860x and LMP860x-Q1 amplify and filter small differential signals in the presence of high common-mode voltages.

The LMP860x and LMP860x-Q1 use level shift resistors at the inputs. Because of these resistors, the LMP860x and LMP860x-Q1 can easily withstand very large differential input voltages that may exist in fault conditions where some other less protected high-performance current sense amplifiers might sustain permanent damage.

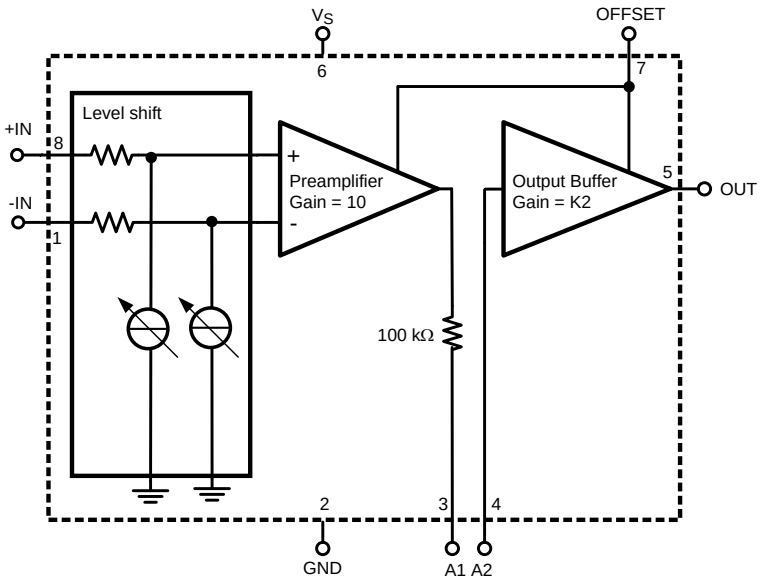
7.1.1 Theory of Operation

The schematic shown in the *Functional Block Diagram* gives a basic representation of the internal operation of the LMP860x and LMP860x-Q1.

The signal on the input pins is typically a small differential voltage developed across a current sensing shunt resistor. The input signal may also appear at a high common-mode voltage. The input signals are accessed through two input resistors that change the voltage into a current. The proprietary chopping level-shift current circuit pulls or pushes current through the input resistors to bring the common-mode voltage behind these resistors within the supply rails.

Subsequently, the signal is gained up by a factor of 10 and brought out on the A1 pin through a trimmed 100-kΩ resistor. In the application, additional gain adjustment or filtering components can be added between the A1 and A2 pins as explained in subsequent sections. The signal on the A2 pin is further amplified by a factor of 2 (LMP8601 and LMP8601-Q1), 5 (LMP8602, LMP8602-Q1), or 10 (LMP8603, LMP8603-Q1), and brought out on the OUT pin.

7.2 Functional Block Diagram



NOTE: K2 = 2 for LMP8601, LMP8601-Q1; 5 for LMP8602, LMP8602-Q1; or 10 for LMP8603, LMP8603-Q1.

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7.3 Feature Description

7.3.1 Offset Input Pin

The OFFSET pin allows the output signal to be level-shifted to enable bidirectional current sensing. The output signal is bidirectional and mid-rail referenced when the offset pin is connected to the positive supply rail. With the offset pin connected to ground, the output signal is unidirectional and ground-referenced.

The signal on the A1 and OUT pins is ground-referenced when the offset pin is connected to ground. This means that the output signal can only represent positive values of the current through the shunt resistor, so only currents flowing in one direction can be measured.

When the offset pin is tied to the positive supply rail, the signal on the A1 and OUT pins is referenced to a mid-rail voltage which allows bidirectional current sensing. The operation of the amplifier will be fully bidirectional and symmetrical around 0 V differential at the input pins. The signal at the output will follow this voltage difference multiplied by the gain and at an offset voltage at the output of half V_S.

When the offset pin is connected to an external voltage source, the output signal will be level shifted to that voltage divided by two. In principle, the output signal can be shifted to any voltage between 0 and V_S / 2 by applying twice that voltage to the OFFSET pin.

NOTE

The OFFSET pin must be driven from a very low-impedance source (< 10 Ω). This low source impedance is required because the OFFSET pin internally connects directly to the resistive feedback networks of the two gain stages. When the OFFSET pin is driven from a relatively large impedance (for example, a resistive divider between the supply rails), accuracy decreases.

Examples:

- **LMP8601, LMP8601-Q1**: A 5-V supply, a gain of 20x, OFFSET pin tied to V_S, and a differential input signal of 10 mV results in 2.7 V at the output pin. Similarly, –10 mV at the input results in 2.3 V at the output pin.
- **LMP8602, LMP8602-Q1**: A 5-V supply, a gain of 50x, and a differential input signal of 10 mV results in 3.0 V at the output pin. Similarly, –10 mV at the input results in 2.0 V at the output pin.
- **LMP8603, LMP8603-Q1**: A 5-V supply, a gain of 100x, and a differential input signal of 10 mV results in 3.5 V at the output pin. Similarly, –10 mV at the input results in 1.5 V at the output pin.(1) (1)

(1) The OFFSET pin must be driven from a very low-impedance source (< 10 Ω) because the OFFSET pin internally connects directly to the resistive feedback networks of the two gain stages. When the OFFSET pin is driven from a relatively large impedance (for example, a resistive divider between the supply rails), accuracy decreases.

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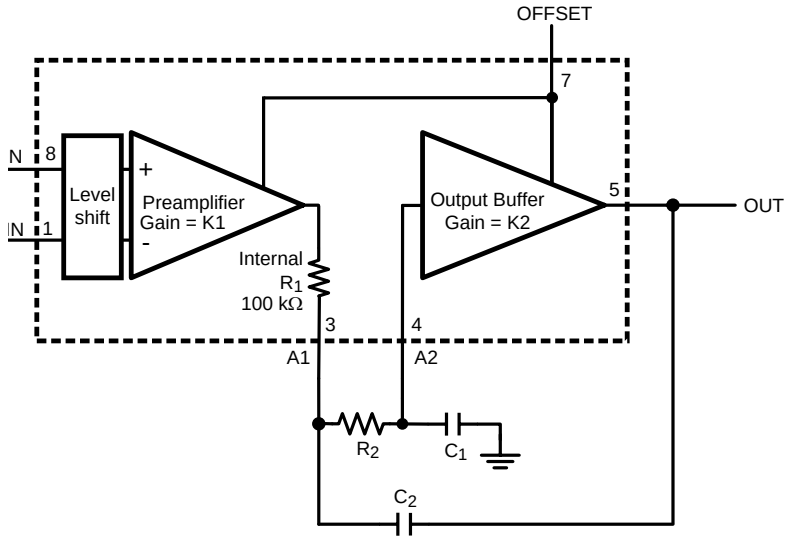
Feature Description (continued)

7.3.2 Additional Second-Order Low-Pass Filter

The LMP86x1 and LMP86x1-Q1 have a third-order Butterworth lowpass characteristic with a typical bandwidth of 60 kHz integrated in the preamplifier stage. The bandwidth of the output buffer can be reduced by adding a capacitor on the A1 pin to create a first-order low-pass filter with a time constant determined by the 100-kΩ internal resistor and the external filter capacitor.

It is also possible to create an additional second-order, Sallen-Key, low-pass filter by adding external components R_2, C_1 and C_2. Together with the internal 100-kΩ resistor R_1 as illustrated in Figure 53, this circuit creates a second-order, low-pass filter characteristic.



NOTE: K1 = 10; K2 = 2 for LMP8601, LMP8601-Q1; 5 for LMP8602, LMP8602-Q1; or 10 for LMP8603, LMP8603-Q1.

Figure 53. Second-Order Low-Pass Filter

When the corner frequency of the additional filter is much lower than 60 kHz, the transfer function of the described amplifier can be written as:

$$H(s) = \frac{K_1 * K_2 \dfrac{1}{R_1R_2C_1C_2}}{s^2 + s * \left[\dfrac{1}{R_1C_2} + \dfrac{1}{R_2C_2} + \dfrac{(1 - K_2)}{R_2C_1}\right] + \dfrac{1}{R_1R_2C_1C_2}}$$

where

- K_1 equals the gain of the preamplifier and K_2 that of the buffer amplifier. (1)

Equation 1 can be written in the normalized frequency response for a second-order lowpass filter:

$$G(j\omega) = K_1 * \frac{K_2}{\dfrac{(j\omega)^2}{\omega_o^2} + \dfrac{j\omega}{Q\omega_o} + 1} \quad (2)$$

The cutoff frequency ω_o in rad/sec (divide by 2π to get the cut-off frequency in Hz) is given by:

$$\omega_o = \frac{1}{\sqrt{R_1R_2C_1C_2}} \quad (3)$$

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Feature Description (continued)

and the quality factor of the filter is given by:

$$Q = \frac{\sqrt{R_1 R_2 C_1 C_2}}{R_1 C_1 + R_2 C_1 + (1 - K_2) * R_1 C_2} \quad (4)$$

With K_2 = 2x, Equation 4 transforms results in:

$$Q = \frac{\sqrt{R_1 R_2 C_1 C_2}}{R_1 C_1 + R_2 C_1 - R_1 C_2} \quad (5)$$

For any filter gain K > 1x, the design procedure can be very simple if the two capacitors are chosen to in a certain ratio.

$$C_2 = \frac{C_1}{K_2 - 1} \quad (6)$$

Inserting this in Equation 4 for Q results in:

$$Q = \frac{\sqrt{R_1 R_2 \frac{C_1^2}{K_2 - 1}}}{R_1 C_1 + R_2 C_1 - \frac{(K_2 - 1) R_1 C_1}{K_2 - 1}} \quad (7)$$

Which results in:

$$Q = \frac{\sqrt{R_1 R_2 \frac{C_1^2}{K_2 - 1}}}{C_1 R_2} = \frac{\sqrt{\frac{R_1 R_2}{K_2 - 1}}}{R_2} \quad (8)$$

In this case, given the predetermined value of R1 = 100 kΩ (the internal resistor), the quality factor is set solely by the value of the resistor R_2.

R_2 can be calculated based on the desired value of Q as the first step of the design procedure with the following equation:

$$R_2 = \frac{R_1}{(K - 1) Q^2} \quad (9)$$

For the gain of 2 for the LMP8601 and LMP8601-Q1, the result is:

$$R_2 = \frac{R_1}{Q^2} \quad (10)$$

For the gain of 5 for the LMP8602 and LMP8602-Q1, the result is:

$$R_2 = \frac{R_1}{4Q^2} \quad (11)$$

For the gain of 10 for the LMP8603 and LMP8603-Q1, the result is:

$$R_2 = \frac{R_1}{9Q^2} \quad (12)$$

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Feature Description (continued)

For instance, the value of Q can be set to 0.5√2 to create a Butterworth response, to 1/√3 to create a Bessel response, or a 0.5 to create a critically damped response. After the value of R_2 has been found, the second and last step of the design procedure is to calculate the required value of C to give the desired low-pass cut-off frequency using:

$$C_1 = \frac{(K_2 - 1)Q}{R_1\omega_0} \tag{13}$$

For the gain = 2, the result is:

$$C = \frac{Q}{R_1\omega_o} \tag{14}$$

The gain = 5 results in:

$$C1 = \frac{4Q}{R_1\omega_0} \tag{15}$$

The gain = 10 gives:

$$C_1 = \frac{9Q}{R_1\omega_0} \tag{16}$$

For C_2 the value is calculated with:

$$C_2 = \frac{C_1}{K_2 - 1} \tag{17}$$

For a gain = 2:

$$C_2 = C_1 \tag{18}$$

Or for a gain = 5:

$$C_2 = \frac{C_1}{4} \tag{19}$$

And for a gain = 10:

$$C_2 = \frac{C_1}{9} \tag{20}$$

Note that the frequency response achieved using this procedure is only accurate if the cut-off frequency of the second-order filter is much smaller than the intrinsic 60-kHz, low-pass filter. In other words, choose the frequency response of the LMP860x or LMP860x-Q1 circuit so that the internal poles do not affect the external second-order filter.

7.4 Device Functional Modes

7.4.1 Gain Adjustment

The gain of the LMP860x and LMP860x-Q1 is fixed; however, the overall gain may be adjusted as the signal path between the two internal amplifiers is available on the A1 and A2 pins.

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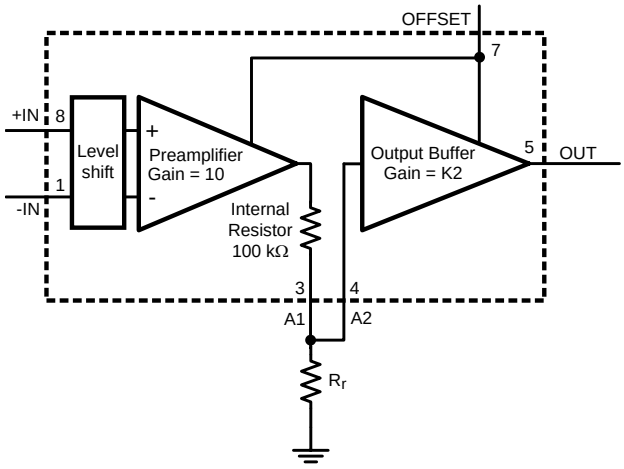
Device Functional Modes (continued)

7.4.1.1 Reducing Gain

Figure 54 shows the configuration that can be used to reduce the gain of the LMP8601 and LMP8601-Q1.



NOTE: K2 = 2 for LMP8601, LMP8601-Q1; 5 for LMP8602, LMP8602-Q1; or 10 for LMP8603, LMP8603-Q1.

Figure 54. Reduce Gain

R_r creates a resistive divider together with the internal 100-kΩ resistor such that the reduced gain G_r becomes:

$$G_r = \frac{20\ R_r}{R_r + 100\ k\Omega} \tag{21}$$

For the LMP8602 and LMP8602-Q1:

$$G_r = \frac{50\ R_r}{R_r + 100\ k\Omega} \tag{22}$$

And for the LMP8603 and LMP8603-Q1:

$$G_r = \frac{100\ R_r}{R_r + 100\ k\Omega} \tag{23}$$

Given a desired value of the reduced gain G_r, using this equation, the LMP8601 and LMP8601-Q1 required value for the R_r is calculated with:

$$R_r = 100\ k\Omega\ X\ \frac{G_r}{20 - G_r} \tag{24}$$

For the LMP8602 and LMP8602-Q1:

$$R_r = 100\ k\Omega\ X\ \frac{G_r}{50 - G_r} \tag{25}$$

And for the LMP8603 and LMP8603-Q1:

$$R_r = 100\ k\Omega\ x\ \frac{G_r}{100 - G_r} \tag{26}$$

7.4.1.2 Increasing Gain

Figure 55 shows the configuration that can be used to increase the gain of the LMP8601 and LMP8601-Q1.

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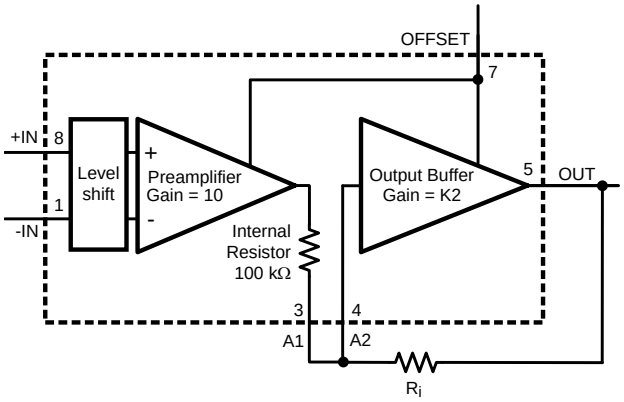
Device Functional Modes (continued)



NOTE: K2 = 2 for LMP8601, LMP8601-Q1; 5 for LMP8602, LMP8602-Q1; or 10 for LMP8603, LMP8603-Q1.

Figure 55. Increase Gain

R_i creates positive feedback from the output pin to the input of the buffer amplifier. The positive feedback increases the gain. The increased gain G_i for the LMP8601 and LMP8601-Q1 becomes:

$$G_i = \frac{20\ R_i}{R_i - 100\ k\Omega} \tag{27}$$

For the LMP8602 and LMP8602-Q1:

$$G_i = \frac{50\ R_i}{R_i - 400\ k\Omega} \tag{28}$$

And for the LMP8603 and LMP8603-Q1:

$$G_i = \frac{100\ R_i}{R_i - 900\ k\Omega} \tag{29}$$

From this equation, for a desired value of the gain, the LMP8601 and LMP8601-Q1 required value of R_i is calculated with:

$$R_i = 100\ k\Omega\ X\ \frac{G_i}{G_i - 20} \tag{30}$$

For the LMP8602 and LMP8602-Q1:

$$R_i = 400\ k\Omega\ X\ \frac{G_i}{G_i - 50} \tag{31}$$

And for the LMP8603 with:

$$R_i = 900\ k\Omega\ x\ \frac{G_i}{G_i - 100} \tag{32}$$

Note that from the equation for the gain G_i, for large gains, R_i approaches 100 kΩ. In this case, the denominator in the equation becomes close to zero. In practice, for large gains, the denominator is determined by tolerances in the value of the external resistor R_i and the internal 100-kΩ resistor. In this case, the gain becomes very inaccurate. If the denominator becomes equal to zero, the system becomes unstable. TI recommends to limit the application of this technique to gain values of 50 or smaller.

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Device Functional Modes (continued)

7.4.2 Driving Switched Capacitive Loads

Some ADCs load their signal source with a sample and hold capacitor. The capacitor may be discharged prior to being connected to the signal source. If the LMP860x and LMP860x-Q1 are driving such ADCs, the sudden current that should be delivered when the sampling occurs may disturb the output signal. This effect was simulated with the circuit shown in Figure 56 where the output is to a capacitor that is driven by a rail-to-rail square wave.

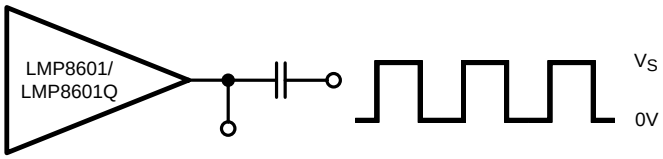

Figure 56. Driving Switched Capacitive Load

This circuit simulates the switched connection of a discharged capacitor to the LMP860x and LMP860x-Q1 output. The resulting V_{OUT} disturbance signals are shown in Figure 57 and Figure 58.

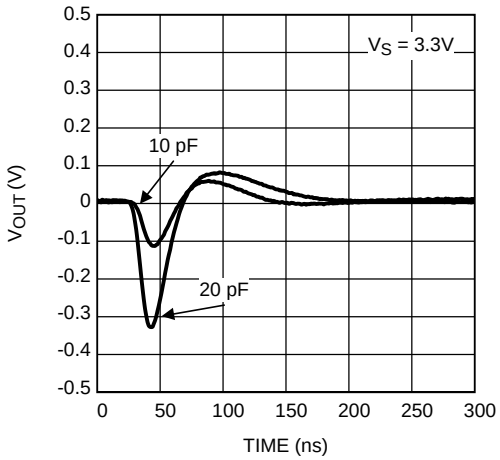

Figure 57. Capacitive Load Response at 3.3 V

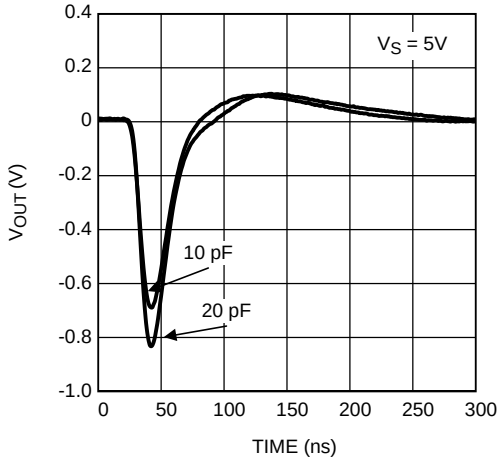

Figure 58. Capacitive Load Response at 5.0 V

These figures can be used to estimate the disturbance that will be caused when driving a switched capacitive load. To minimize the error signal introduced by the sampling that occurs on the ADC input, place an additional RC filter between the LMP860x or LMP860x-Q1 and the ADC, as illustrated in Figure 59.

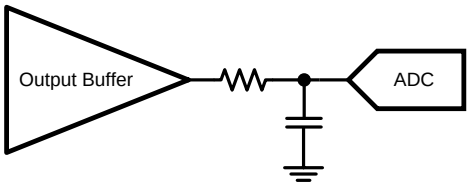

Figure 59. Reduce Error When Driving ADCs

The external capacitor absorbs the charge that flows when the ADC sampling capacitor is connected. The external capacitor should be much larger than the sample-and-hold capacitor at the input of the ADC, and the RC time constant of the external filter should be such that the speed of the system is not affected.

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8 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

8.1 Application Information

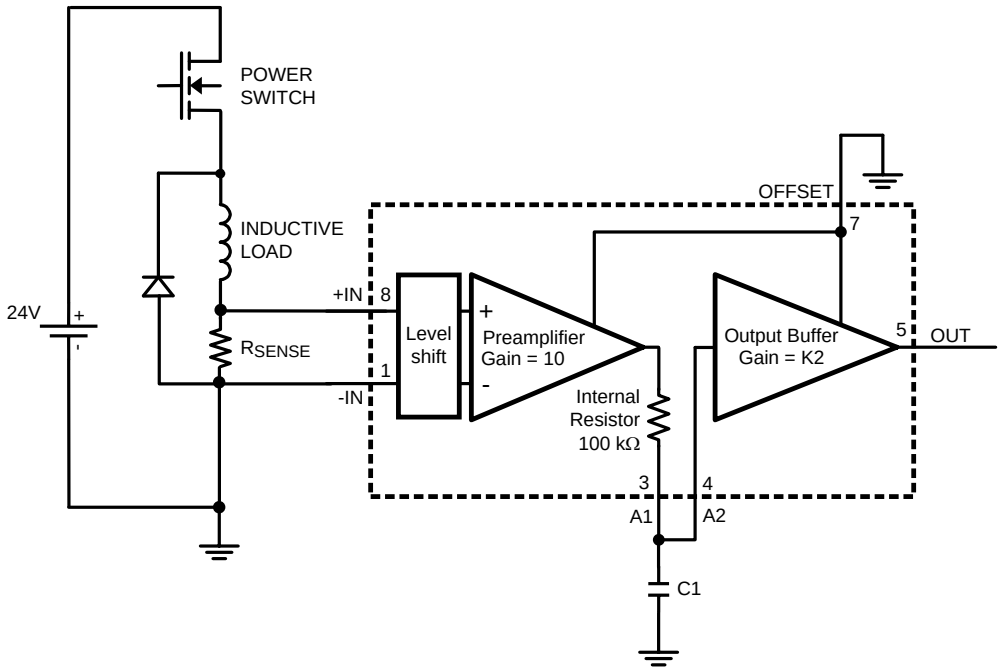
8.1.1 Specifying Performance

To specify the high performance of the LMP860x and LMP860x-Q1, all minimum and maximum values shown in the parameter tables of this data sheet are 100% tested, and all over temperature limits are also 100% tested over temperature.

8.2 Typical Applications

8.2.1 High-Side, Current-Sensing Application

Figure 60 illustrates the application of the LMP860x and LMP860x-Q1 in a high-side sensing application. This application is similar to the low-side sensing discussed below, except in this application the common-mode voltage on the shunt drops below ground when the driver is switched off. Because the common-mode voltage range of the LMP860x and LMP860x-Q1 extends below the negative rail, the LMP860x and LMP860x-Q1 are also very well suited for this application.



NOTE: For this application example, K2 = 2.

Figure 60. High-Side, Current-Sensing Application

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Typical Applications (continued)

8.2.1.1 Design Requirements

Using the circuit in Figure 60, the requirement is to measure coil current up to 10 A and drive the ADC input to a maximum of 3.3 V. The OFFSET pin is grounded, so zero current will result in a zero volt output.

8.2.1.2 Detailed Design Procedure

First, the value of R_{SENSE} must be determined. R_{SENSE} can be found by dividing the maximum desired output swing by the gain to determine the maximum input voltage. In this example, the LMP8601 is used, with a gain of 20 V/V, as shown in Equation 33:

$$V_{INMAX} = \frac{V_{OUTMAX}}{Gain} = \frac{3.3\ V}{20\ V/V} = 165\ mV \quad (33)$$

Knowing 165 mV must be generated, the ideal value of the sense resistor can be determined through simple ohms law:

$$R_{SENSE} = \frac{V_{INMAX}}{I_{LOADMAX}} = \frac{165\ mV}{10A} = 16.5\ m\Omega \quad (34)$$

The ideal sense resistor value is 16.5 mΩ. The closest standard value is 15 mΩ, but this value may cause the output to slightly overrange at 10 V. It is recommended to reduce the expected maximum output by a few percent to allow for overloads and component tolerances. The next most popular values would be 10 mΩ, 15 mΩ, and 20 mΩ. 10 mΩ allows for a maximum output of 2 V at 10 A, but may be too low and not use the full output range. 20 mΩ provides more sensitivity, but limits the maximum current to 8.25 A. 15 mΩ is a good compromise at 11 A maximum, and allows for some component tolerance variation.

If a suitable sense resistor value is not available, it is possible to adjust the gain as detailed in the *Gain Adjustment* section.

The sense resistor does dissipates power, so the maximum wattage rating and appropriate power deratings must be observed. In the example above, the sense resistor dissipates 0.165 V × 10 A = 1.65 W, so a sense resistor of at least twice the maximum expected power should be used (greater than 4 W).

8.2.1.3 Application Curve

Below is the expected output value using a 15-mΩ sense resistor.

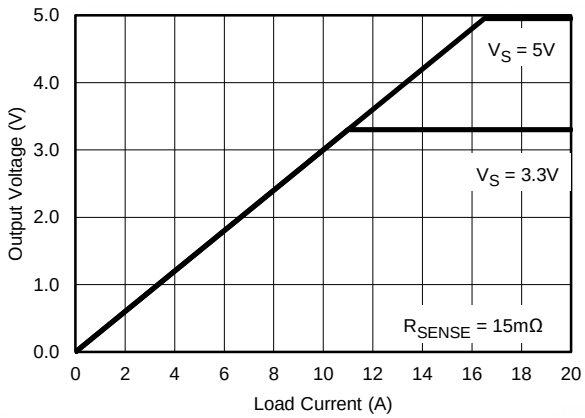
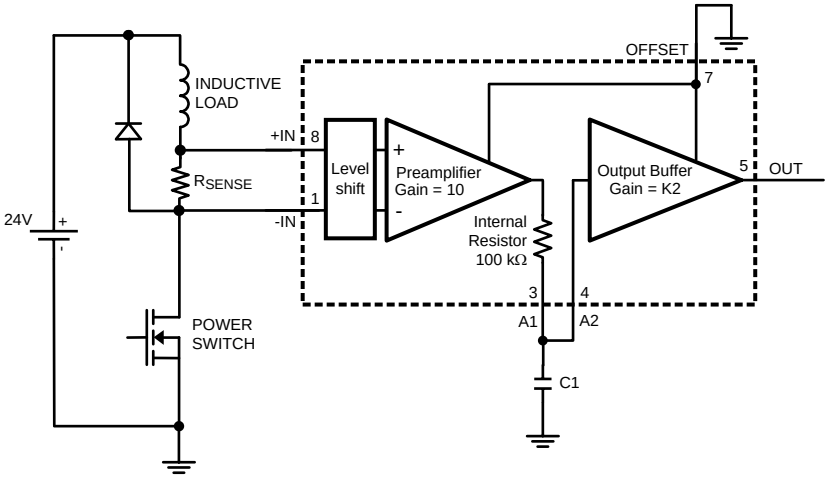


Figure 61. Expected Output Voltage vs Load Current Using 15-mΩ Sense Resistor

Typical Applications (continued)

8.2.2 Low-Side, Current-Sensing Application

Figure 62 illustrates a low-side, current-sensing application with a low-side driver. The power transistor is pulse width modulated to control the average current flowing through the inductive load which is connected to a relatively high battery voltage. The current through the load is measured across a shunt resistor R_{SENSE} in series with the load. When the power transistor is on, current flows from the battery through the inductive load, the shunt resistor and the power transistor to ground. In this case, the common-mode voltage on the shunt is close to ground. When the power transistor is off, current flows through the inductive load, through the shunt resistor and through the freewheeling diode. In this case the common-mode voltage on the shunt is at least one diode voltage drop above the battery voltage. Therefore, in this application the common-mode voltage on the shunt is varying between a large positive voltage and a relatively low voltage. Because the large common-mode voltage range of the LMP860x and LMP860x-Q1 and because of the high ac common-mode rejection ratio, the LMP860x and LMP860x-Q1 are very well suited for this application.



R_{SENSE} = 0.01 Ω, K2 = 2, V_{OUT} = 0.2 V/A

Figure 62. Low-Side Current-Sensing Application

For this application, the following example can be used for the calculation of the sense voltage (V_{SENSE}):

When using a sense resistor, R_{SENSE}, of 0.01 Ω and a current, I_{LOAD}, of 1 A, the sense voltage at the input pins of the LMP860x and LMP860x-Q1 is:

$$V_{SENSE} = R_{SENSE} \times I_{LOAD} = 0.01\ \Omega \times 1\ A = 0.01\ V \quad (35)$$

With the gain of 20 for the LMP8601, the result is an output of 0.2 V. Or in other words, V_{OUT} = 0.2 V/A. The result is the same for the LMP8601-Q1.

For the LMP8602 and LMP8602-Q1 with a gain of 50, the output is 0.5 V/A.

For the LMP8603 and LMP8603-Q1 with a gain of 100, the output is 1 V/A.

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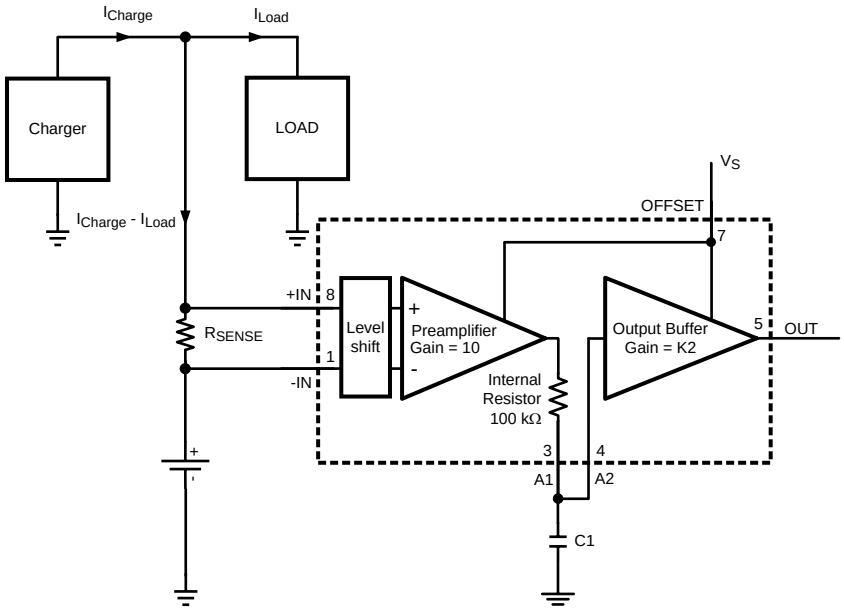
Typical Applications (continued)

8.2.3 Battery Current Monitor Application

This application example shows how the LMP860x and LMP860x-Q1 can be used to monitor the current flowing in and out of a battery pack. The fact that the LMP860x and LMP860x-Q1 can measure small voltages at a high offset voltage outside the parts own supply range makes this part a very good choice for such applications. If the load current of the battery is higher then the charging current, the output voltage of the LMP860x and LMP860x-Q1 will be above the *half offset voltage* for a net current flowing out of the battery. When the charging current is higher then the load current the output will be below this half offset voltage.



NOTE: K2 = 2 for LMP8601, LMP8601-Q1; 5 for LMP8602, LMP8602-Q1; or 10 for LMP8603, LMP8603-Q1.

Figure 63. Battery Current Monitor Application

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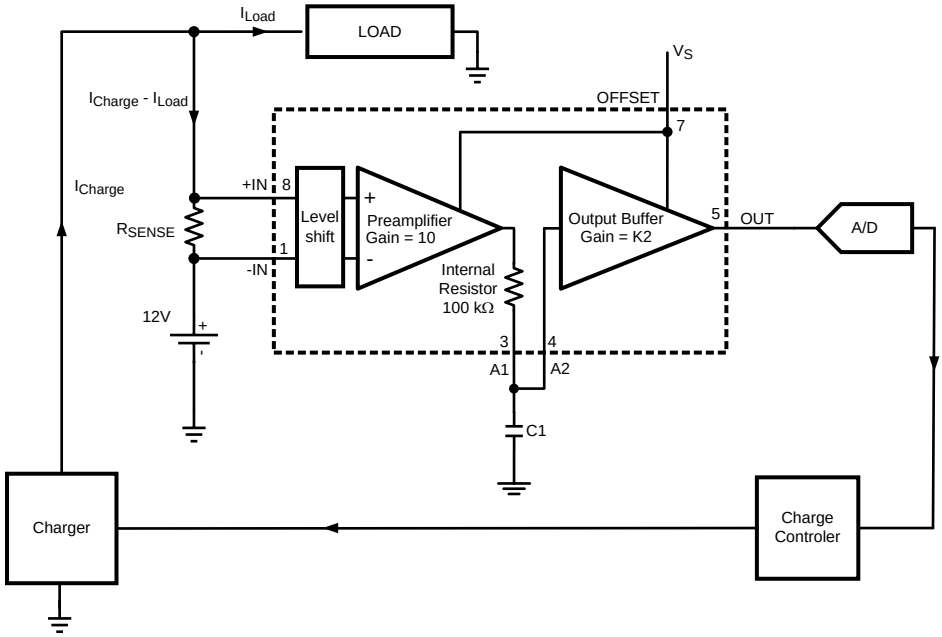
Typical Applications (continued)

8.2.4 Advanced Battery Charger Application

Figure 63 can be used to realize an advanced battery charger that has the capability to monitor the exact net current that flows in and out the battery as show in Figure 64. The output signal of the LMP860x and LMP860x-Q1 is digitized with the ADC and used as an input for the charge controller. The Charge controller can be used to regulate the charger circuit to deliver exactly the current that is required by the load, avoiding overcharging a fully loaded battery.

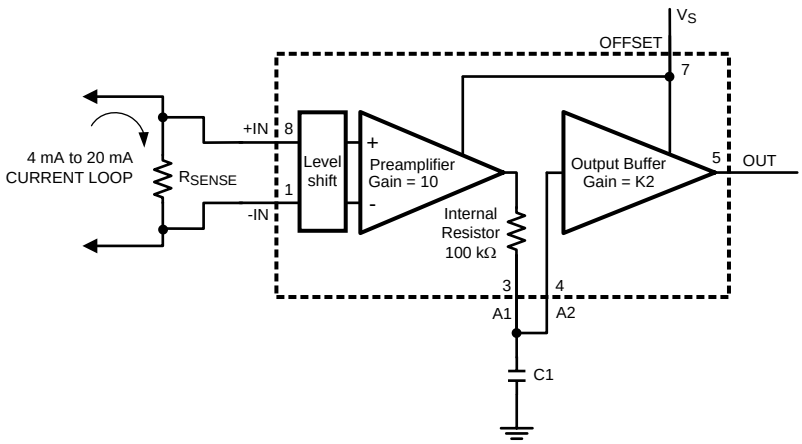


NOTE: K2 = 2 for LMP8601, LMP8601-Q1; 5 for LMP8602, LMP8602-Q1; or 10 for LMP8603, LMP8603-Q1.

Figure 64. Advanced Battery Charger Application

8.2.5 Current Loop Receiver Application

Many industrial applications use 4-mA to 20-mA transmitters to send an analog value of a sensor to a central control room. The LMP860x and LMP860x-Q1 can be used as a current loop receiver as shown in Figure 65.



NOTE: K2 = 2 for LMP8601, LMP8601-Q1; 5 for LMP8602, LMP8602-Q1; or 10 for LMP8603, LMP8603-Q1.

Figure 65. Current-Loop Receiver Application

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9 Power Supply Recommendations

In order to decouple the LMP860x and LMP860x-Q1 from AC noise on the power supply, place a 0.1-µF bypass capacitor between the V_S and GND pins. Place this capacitor as close as possible to the supply pins. In some cases, an additional 10-µF bypass capacitor may further reduce the supply noise.

10 Layout

10.1 Layout Guidelines

The traces leading to and from the sense resistor can be significant error sources. With small value sense resistors (< 100 mΩ), any trace resistance shared with the load current can cause significant errors.

The amplifier inputs should be directly connected to the sense resistor pads using Kelvin or 4-wire connection techniques. The traces should be one continuous piece of copper from the sense resistor pad to the amplifier input pin pad, and ideally on the same copper layer with minimal vias or connectors. This can be important around the sense resistor if it is generating any significant heat gradients.

To minimize noise pickup and thermal errors, the input traces should be treated as a differential signal pair and routed tightly together with a direct path to the input pins. The input traces should be run away from noise sources, such as digital lines, switching supplies or motor drive lines. Remember that these traces can contain high voltage, and should have the appropriate trace routing clearances.

Since the sense traces only carry the amplifier bias current, the connecting input traces can be thinner, signal level traces. Excessive Resistance in the trace should also be avoided.

The paths of the traces should be identical, including connectors and vias, so that any errors will be equal and cancel.

The sense resistor will heat up as the load increases. As the resistor heats up, the resistance generally goes up, which will cause a change in the readings. The sense resistor should have as much heatsinking as possible to remove this heat through the use of heatsinks or large copper areas coupled to the resistor pads. A reading drifting over time after turnon can usually be traced back to sense resistor heating.

10.2 Layout Example

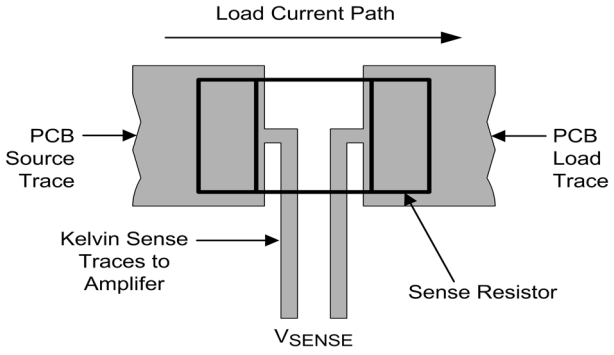

Figure 66. Kelvin or 4–wire Connection to the Sense Resistor

11 Device and Documentation Support

11.1 Device Support

11.1.1 Development Support

LMP8601 TINA SPICE Model, SNOM084

TINA-TI SPICE-Based Analog Simulation Program, http://www.ti.com/tool/tina-ti

11.2 Related Links

Table 1 lists quick access links. Categories include technical documents, support and community resources, tools and software, and quick access to sample or buy.

Table 1. Related Links

PARTS	PRODUCT FOLDER	SAMPLE & BUY	TECHNICAL DOCUMENTS	TOOLS & SOFTWARE	SUPPORT & COMMUNITY
LMP8601	Click here	Click here	Click here	Click here	Click here
LMP8601-Q1	Click here	Click here	Click here	Click here	Click here
LMP8602	Click here	Click here	Click here	Click here	Click here
LMP8602-Q1	Click here	Click here	Click here	Click here	Click here
LMP8603	Click here	Click here	Click here	Click here	Click here
LMP8603-Q1	Click here	Click here	Click here	Click here	Click here

11.3 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

TI E2E™ Online Community ***TI's Engineer-to-Engineer (E2E) Community.*** Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support ***TI's Design Support*** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

11.4 Trademarks

E2E is a trademark of Texas Instruments.
All other trademarks are the property of their respective owners.

11.5 Electrostatic Discharge Caution

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

11.6 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

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PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
LMP8601EDRQ1	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	SN	Level-1-260C-UNLIM	-40 to 150	LMP86 01EDQ1	Samples
LMP8601MA/NOPB	ACTIVE	SOIC	D	8	95	Green (RoHS & no Sb/Br)	SN	Level-1-260C-UNLIM	-40 to 125	LMP86 01MA	Samples
LMP8601MAX/NOPB	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	SN	Level-1-260C-UNLIM	-40 to 125	LMP86 01MA	Samples
LMP8601QMA/NOPB	ACTIVE	SOIC	D	8	95	Green (RoHS & no Sb/Br)	SN	Level-1-260C-UNLIM	-40 to 125	LMP86 01QMA	Samples
LMP8601QMAX/NOPB	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	SN	Level-1-260C-UNLIM	-40 to 125	LMP86 01QMA	Samples
LMP8602MA/NOPB	ACTIVE	SOIC	D	8	95	Green (RoHS & no Sb/Br)	SN	Level-1-260C-UNLIM	-40 to 125	LMP86 02MA	Samples
LMP8602MAX/NOPB	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	SN	Level-1-260C-UNLIM	-40 to 125	LMP86 02MA	Samples
LMP8602MM/NOPB	ACTIVE	VSSOP	DGK	8	1000	Green (RoHS & no Sb/Br)	SN	Level-1-260C-UNLIM	-40 to 125	AN3A	Samples
LMP8602MME/NOPB	ACTIVE	VSSOP	DGK	8	250	Green (RoHS & no Sb/Br)	SN	Level-1-260C-UNLIM	-40 to 125	AN3A	Samples
LMP8602MMX/NOPB	ACTIVE	VSSOP	DGK	8	3500	Green (RoHS & no Sb/Br)	SN	Level-1-260C-UNLIM	-40 to 125	AN3A	Samples
LMP8602QMA/NOPB	ACTIVE	SOIC	D	8	95	Green (RoHS & no Sb/Br)	SN	Level-1-260C-UNLIM	-40 to 125	LMP86 02QMA	Samples
LMP8602QMAX/NOPB	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	SN	Level-1-260C-UNLIM	-40 to 125	LMP86 02QMA	Samples
LMP8602QMM/NOPB	ACTIVE	VSSOP	DGK	8	1000	Green (RoHS & no Sb/Br)	SN	Level-1-260C-UNLIM	-40 to 125	AF7A	Samples
LMP8602QMME/NOPB	ACTIVE	VSSOP	DGK	8	250	Green (RoHS & no Sb/Br)	SN	Level-1-260C-UNLIM	-40 to 125	AF7A	Samples
LMP8602QMMX/NOPB	ACTIVE	VSSOP	DGK	8	3500	Green (RoHS & no Sb/Br)	SN	Level-1-260C-UNLIM	-40 to 125	AF7A	Samples
LMP8603MA/NOPB	ACTIVE	SOIC	D	8	95	Green (RoHS & no Sb/Br)	SN	Level-1-260C-UNLIM	-40 to 125	LMP86 03MA	Samples
LMP8603MAX/NOPB	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	SN	Level-1-260C-UNLIM	-40 to 125	LMP86 03MA	Samples

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
LMP8603MM/NOPB	ACTIVE	VSSOP	DGK	8	1000	Green (RoHS & no Sb/Br)	SN	Level-1-260C-UNLIM	-40 to 125	AP3A	Samples
LMP8603MME/NOPB	ACTIVE	VSSOP	DGK	8	250	Green (RoHS & no Sb/Br)	SN	Level-1-260C-UNLIM	-40 to 125	AP3A	Samples
LMP8603MMX/NOPB	ACTIVE	VSSOP	DGK	8	3500	Green (RoHS & no Sb/Br)	SN	Level-1-260C-UNLIM	-40 to 125	AP3A	Samples
LMP8603QMA/NOPB	ACTIVE	SOIC	D	8	95	Green (RoHS & no Sb/Br)	SN	Level-1-260C-UNLIM	-40 to 125	LMP86 03QMA	Samples
LMP8603QMAX/NOPB	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	SN	Level-1-260C-UNLIM	-40 to 125	LMP86 03QMA	Samples
LMP8603QMM/NOPB	ACTIVE	VSSOP	DGK	8	1000	Green (RoHS & no Sb/Br)	SN	Level-1-260C-UNLIM	-40 to 125	AH7A	Samples
LMP8603QMME/NOPB	ACTIVE	VSSOP	DGK	8	250	Green (RoHS & no Sb/Br)	SN	Level-1-260C-UNLIM	-40 to 125	AH7A	Samples
LMP8603QMMX/NOPB	ACTIVE	VSSOP	DGK	8	3500	Green (RoHS & no Sb/Br)	SN	Level-1-260C-UNLIM	-40 to 125	AH7A	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

OTHER QUALIFIED VERSIONS OF LMP8601, LMP8601-Q1, LMP8602, LMP8602-Q1, LMP8603, LMP8603-Q1 :

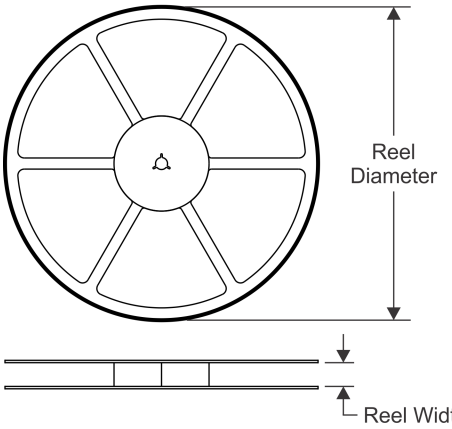
- Catalog: LMP8601, LMP8602, LMP8603
- Automotive: LMP8601-Q1, LMP8602-Q1, LMP8603-Q1

NOTE: Qualified Version Definitions:

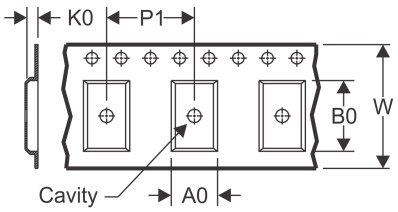
- Catalog - TI's standard catalog product
- Automotive - Q100 devices qualified for high-reliability automotive applications targeting zero defects

TAPE AND REEL INFORMATION

REEL DIMENSIONS

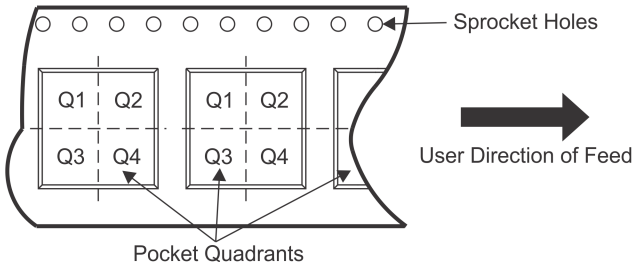


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE

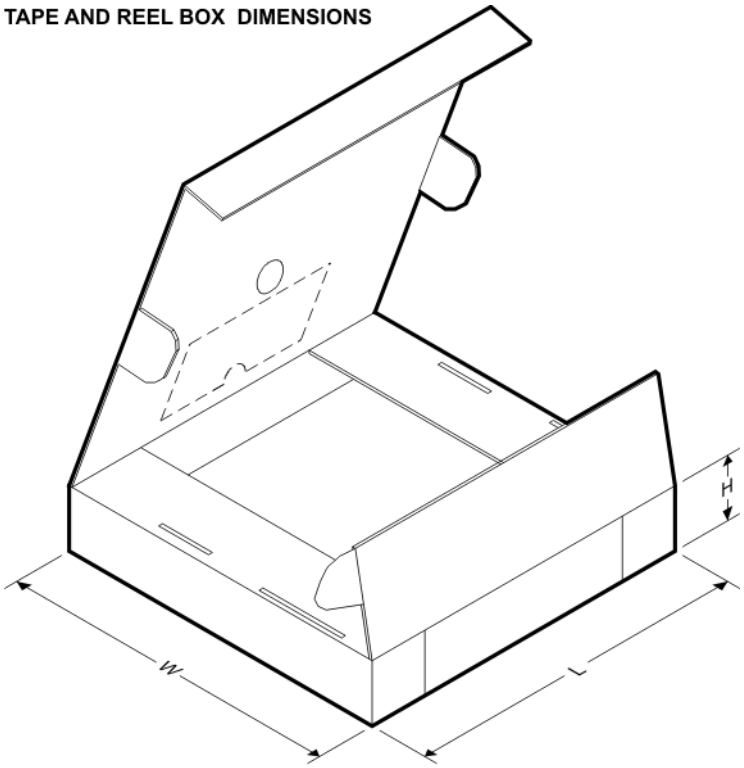


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
LMP8601EDRQ1	SOIC	D	8	2500	330.0	12.4	6.5	5.4	2.0	8.0	12.0	Q1
LMP8601MAX/NOPB	SOIC	D	8	2500	330.0	12.4	6.5	5.4	2.0	8.0	12.0	Q1
LMP8601QMAX/NOPB	SOIC	D	8	2500	330.0	12.4	6.5	5.4	2.0	8.0	12.0	Q1
LMP8602MAX/NOPB	SOIC	D	8	2500	330.0	12.4	6.5	5.4	2.0	8.0	12.0	Q1
LMP8602MM/NOPB	VSSOP	DGK	8	1000	178.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
LMP8602MME/NOPB	VSSOP	DGK	8	250	178.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
LMP8602MMX/NOPB	VSSOP	DGK	8	3500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
LMP8602QMAX/NOPB	SOIC	D	8	2500	330.0	12.4	6.5	5.4	2.0	8.0	12.0	Q1
LMP8602QMM/NOPB	VSSOP	DGK	8	1000	178.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
LMP8602QMME/NOPB	VSSOP	DGK	8	250	178.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
LMP8602QMMX/NOPB	VSSOP	DGK	8	3500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
LMP8603MAX/NOPB	SOIC	D	8	2500	330.0	12.4	6.5	5.4	2.0	8.0	12.0	Q1
LMP8603MM/NOPB	VSSOP	DGK	8	1000	178.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
LMP8603MME/NOPB	VSSOP	DGK	8	250	178.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
LMP8603MMX/NOPB	VSSOP	DGK	8	3500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
LMP8603QMAX/NOPB	SOIC	D	8	2500	330.0	12.4	6.5	5.4	2.0	8.0	12.0	Q1
LMP8603QMM/NOPB	VSSOP	DGK	8	1000	178.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
LMP8603QMME/NOPB	VSSOP	DGK	8	250	178.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
LMP8603QMMX/NOPB	VSSOP	DGK	8	3500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1

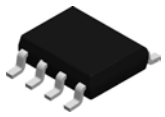
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
LMP8601EDRQ1	SOIC	D	8	2500	367.0	367.0	35.0
LMP8601MAX/NOPB	SOIC	D	8	2500	367.0	367.0	35.0
LMP8601QMAX/NOPB	SOIC	D	8	2500	367.0	367.0	35.0
LMP8602MAX/NOPB	SOIC	D	8	2500	367.0	367.0	35.0
LMP8602MM/NOPB	VSSOP	DGK	8	1000	210.0	185.0	35.0
LMP8602MME/NOPB	VSSOP	DGK	8	250	210.0	185.0	35.0
LMP8602MMX/NOPB	VSSOP	DGK	8	3500	367.0	367.0	35.0
LMP8602QMAX/NOPB	SOIC	D	8	2500	367.0	367.0	35.0
LMP8602QMM/NOPB	VSSOP	DGK	8	1000	210.0	185.0	35.0
LMP8602QMME/NOPB	VSSOP	DGK	8	250	210.0	185.0	35.0
LMP8602QMMX/NOPB	VSSOP	DGK	8	3500	367.0	367.0	35.0
LMP8603MAX/NOPB	SOIC	D	8	2500	367.0	367.0	35.0
LMP8603MM/NOPB	VSSOP	DGK	8	1000	210.0	185.0	35.0
LMP8603MME/NOPB	VSSOP	DGK	8	250	210.0	185.0	35.0
LMP8603MMX/NOPB	VSSOP	DGK	8	3500	367.0	367.0	35.0
LMP8603QMAX/NOPB	SOIC	D	8	2500	367.0	367.0	35.0

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
LMP8603QMM/NOPB	VSSOP	DGK	8	1000	210.0	185.0	35.0
LMP8603QMME/NOPB	VSSOP	DGK	8	250	210.0	185.0	35.0
LMP8603QMMX/NOPB	VSSOP	DGK	8	3500	367.0	367.0	35.0

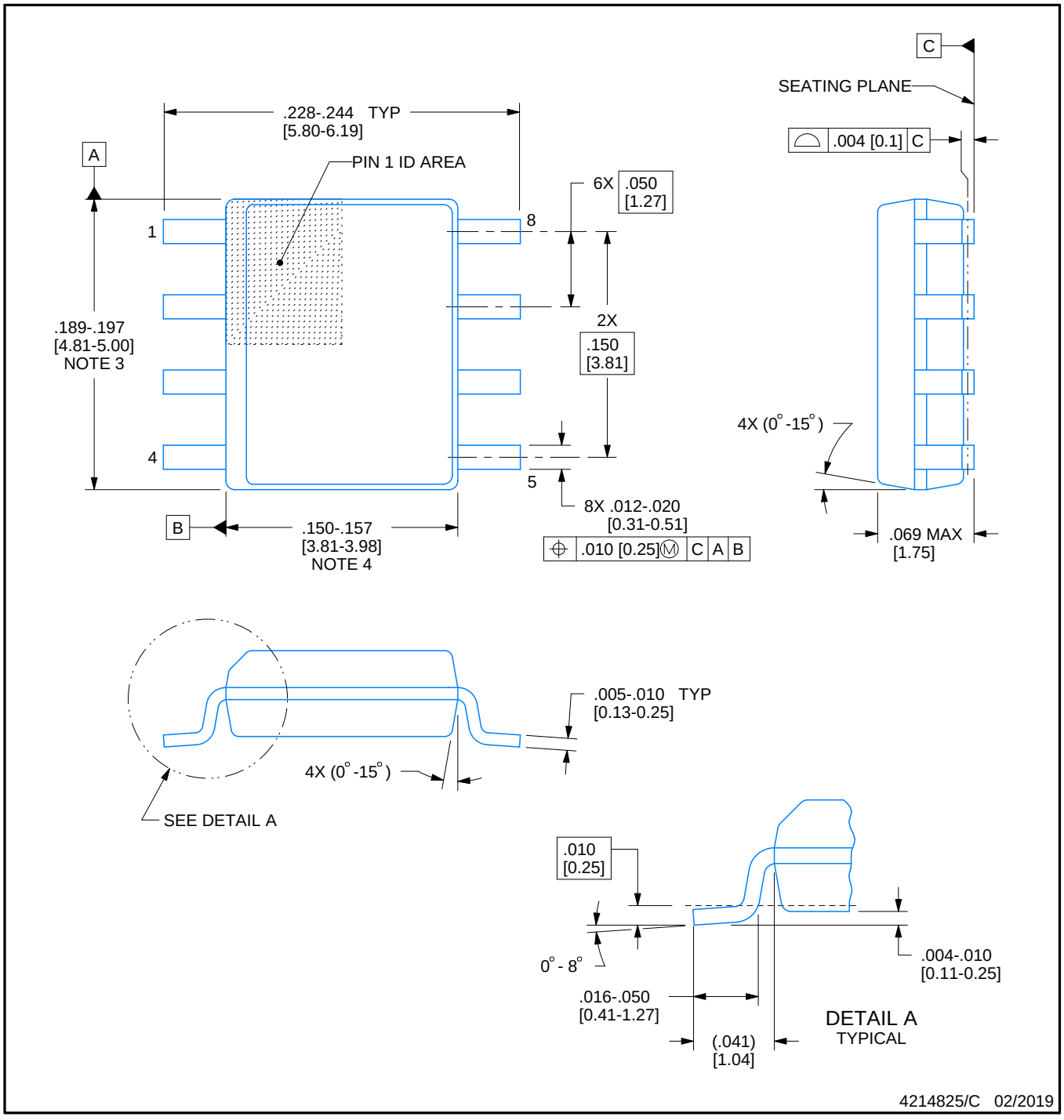


PACKAGE OUTLINE

D0008A

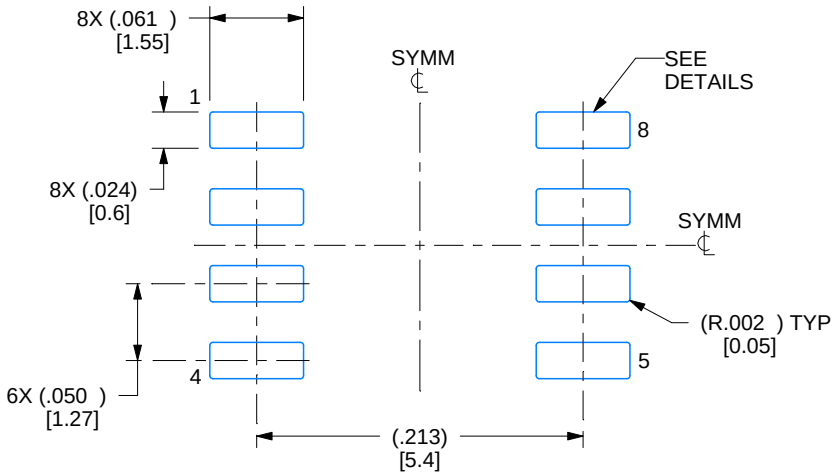
SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT

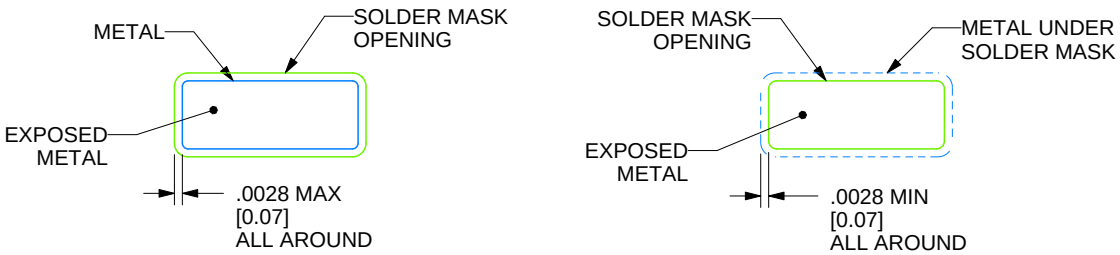


NOTES:

1. Linear dimensions are in inches [millimeters]. Dimensions in parenthesis are for reference only. Controlling dimensions are in inches. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 [0.15] per side.
4. This dimension does not include interlead flash.
5. Reference JEDEC registration MS-012, variation AA.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:8X



SOLDER MASK DETAILS

4214825/C 02/2019

NOTES: (continued)

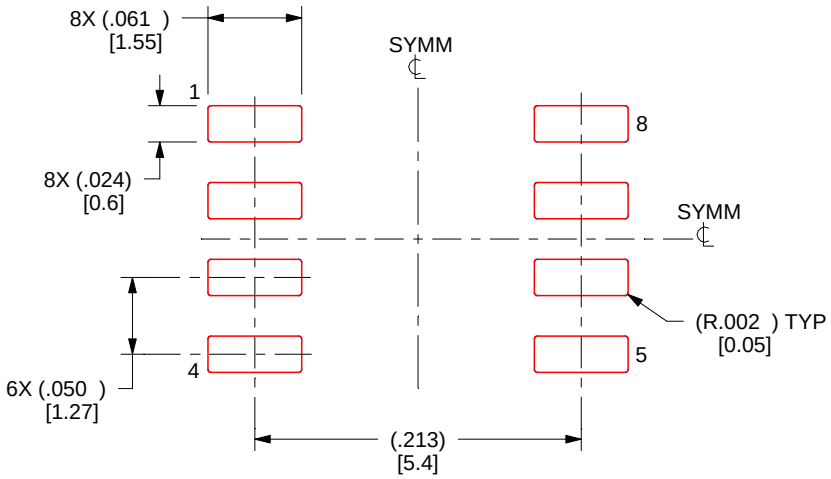
6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

D0008A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



SOLDER PASTE EXAMPLE
BASED ON .005 INCH [0.125 MM] THICK STENCIL
SCALE:8X

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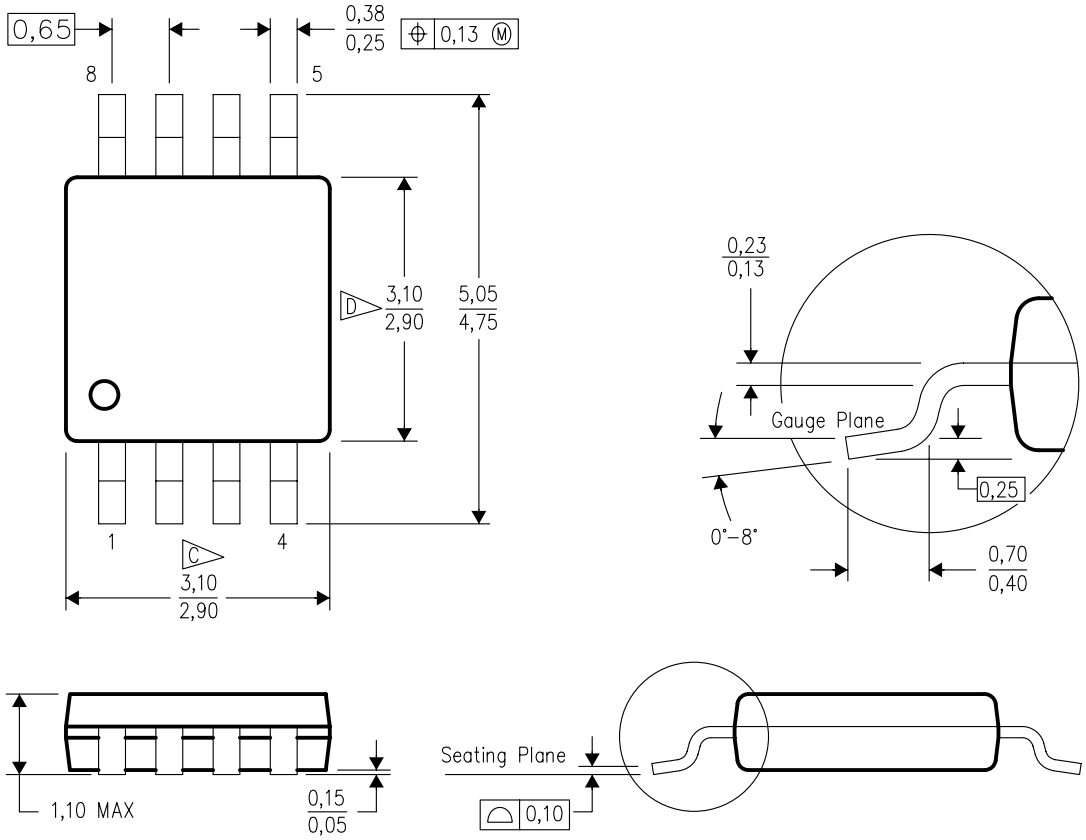
NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

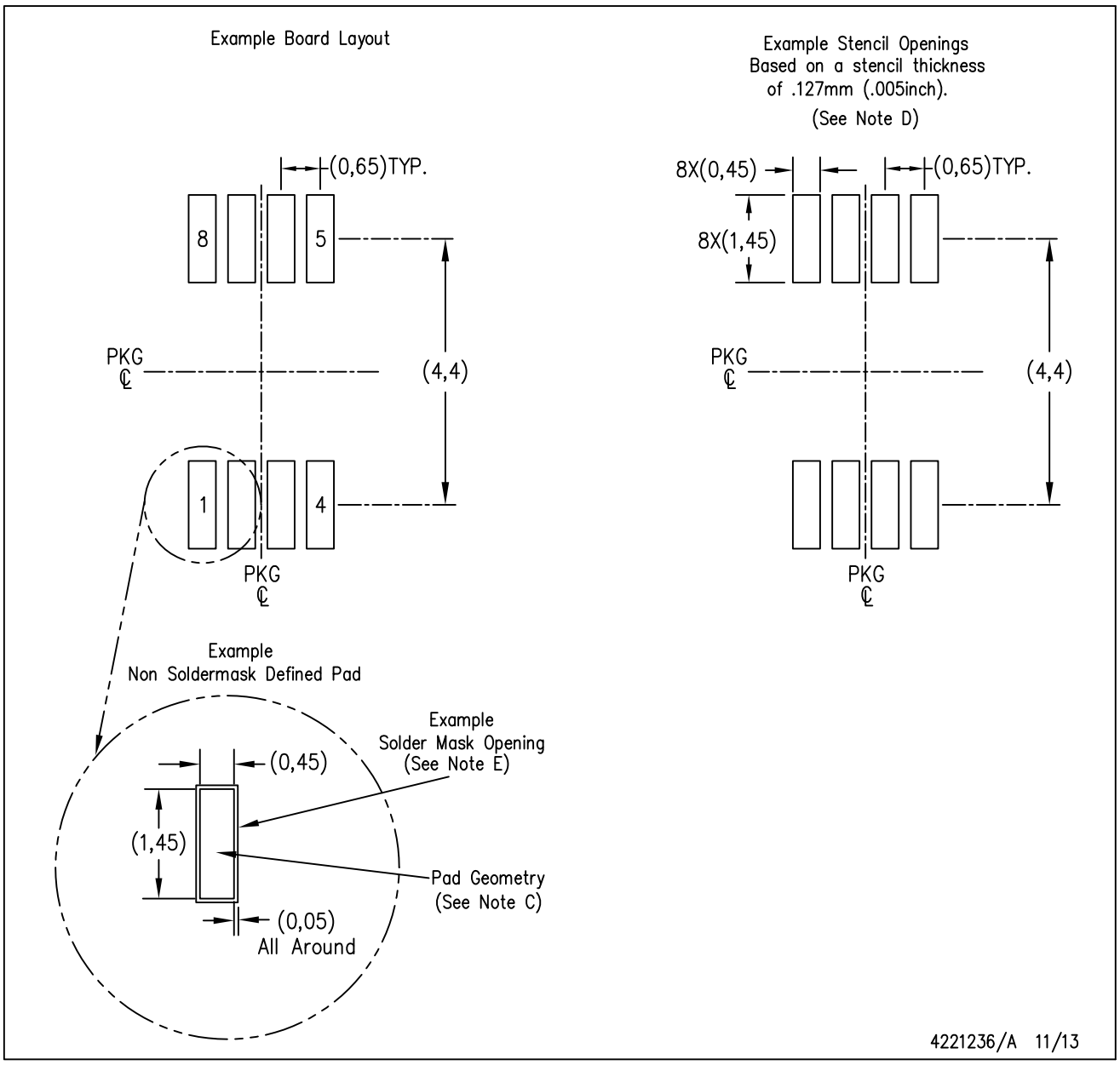
DGK (S–PDSO–G8) PLASTIC SMALL–OUTLINE PACKAGE



4073329/E 05/06

NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 per end.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0.50 per side.
E. Falls within JEDEC MO–187 variation AA, except interlead flash.

DGK (S–PDSO–G8) PLASTIC SMALL OUTLINE PACKAGE



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC–7525 for other stencil recommendations.
E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

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