LMK030xxC Evaluation Board

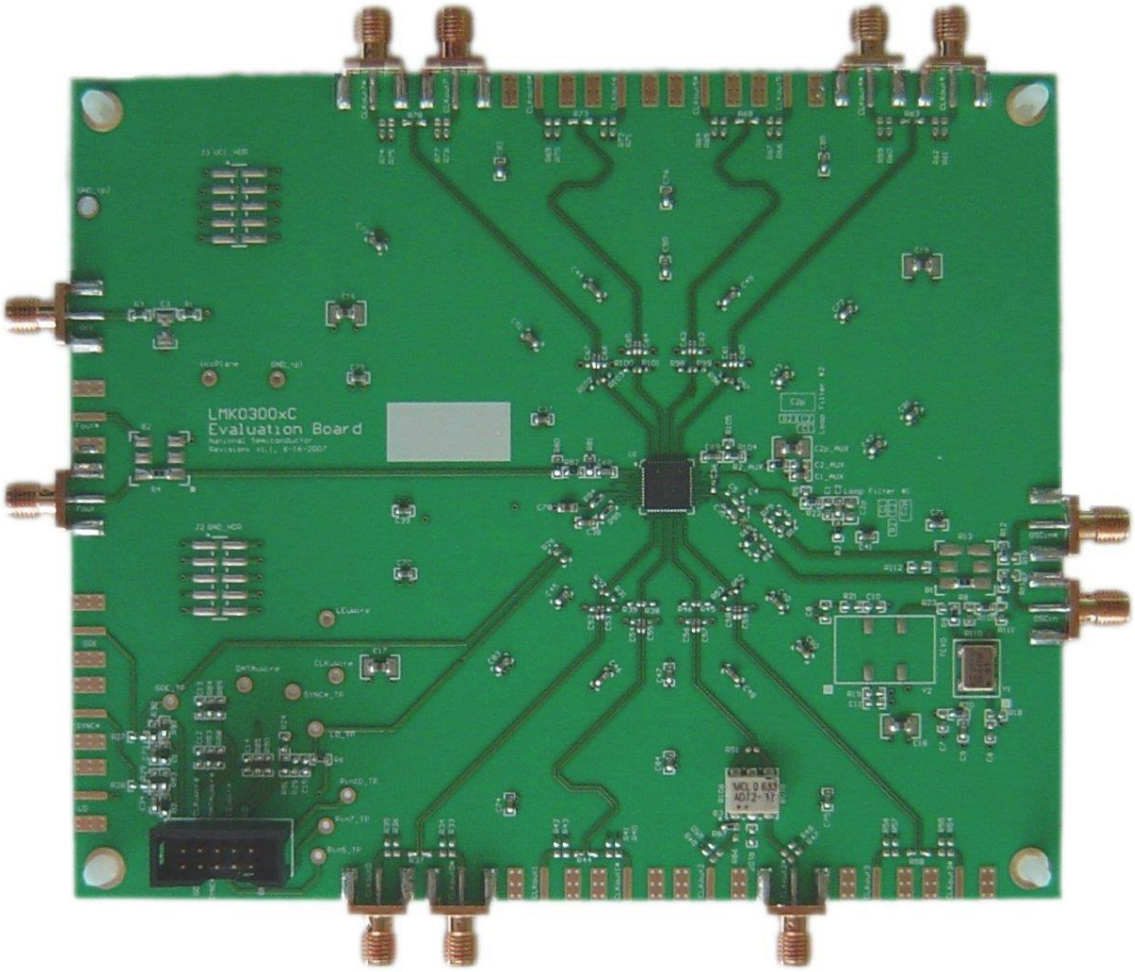
User's Guide

November 2013
SNAU040A

LMK03000C/01C/02C/33C

Precision Clock Conditioner with Integrated VCO
Evaluation Board Operating Instructions

April 2009



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Equipment

Power Supply

The Power Supply should be a low noise power supply. An Agilent 6623A Triple power supply with LC filters on the output to reduce noise was used in creating these evaluation board instructions.

Phase Noise / Spectrum Analyzer

For measuring phase noise an Agilent E5052A is recommended. An Agilent E4445A PSA Spectrum Analyzer with the Phase Noise option is also usable although the architecture of the E5052A is superior for phase noise measurements. At frequencies less than 100 MHz the local oscillator noise of the PSA is too high and measurements will be of the local oscillator, not the device under test.

Oscilloscope

The oscilloscope and probes should be capable of measuring the output frequencies of interest when evaluating this board. The Agilent Infiniium DSO81204A was used in creating these evaluation board instructions.

Reference Oscillator

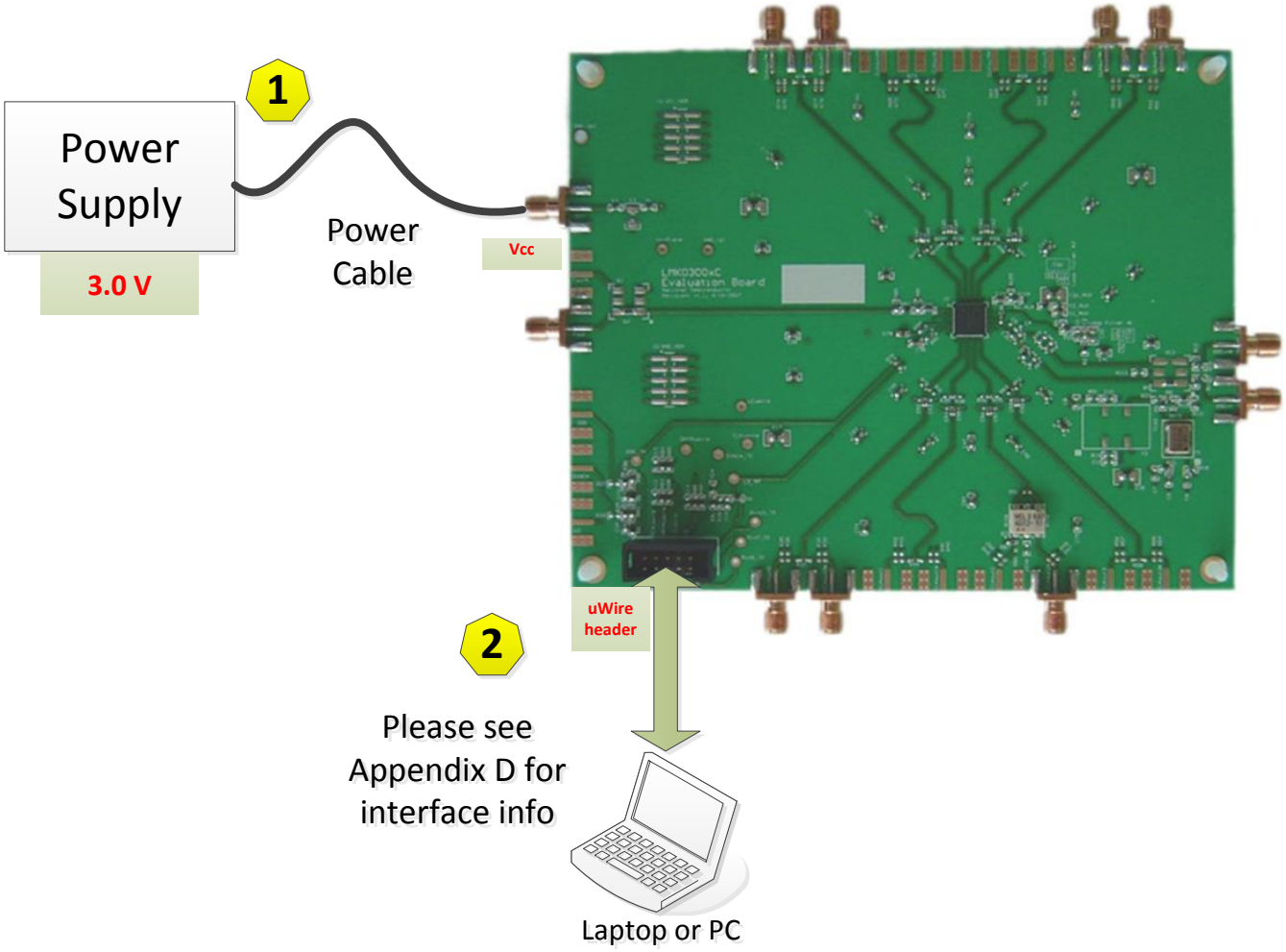
The on board crystal oscillator will provide a low noise reference signal to the device at offsets greater than 1 kHz.

Note: The default loop filter has a loop bandwidth of ~60 kHz. Inside the loop bandwidth of a PLL the noise is greatly affected by any noise on the reference oscillator (OSCin). Therefore any noise on the oscillator less than 60 kHz will be passed through and seen on the outputs. For this reason the main output of a Signal Generator is not recommended for driving OSCin in this setup.

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Basic Operation

1. Connect a low noise **3.3 V** power supply to the **Vcc** connector located at the top left of the board.
2. Please see **Appendix D** for quick start on interfacing the board. Connect PC to the **uWire** header.

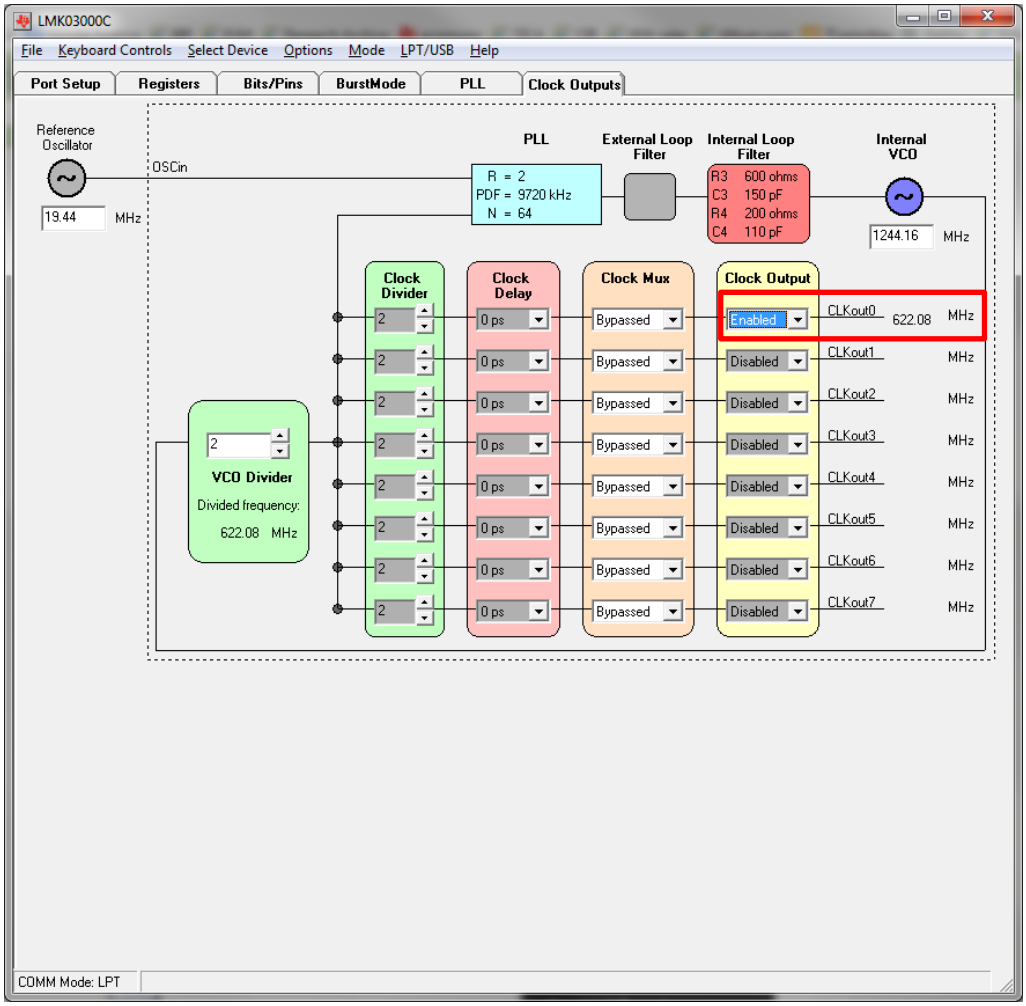


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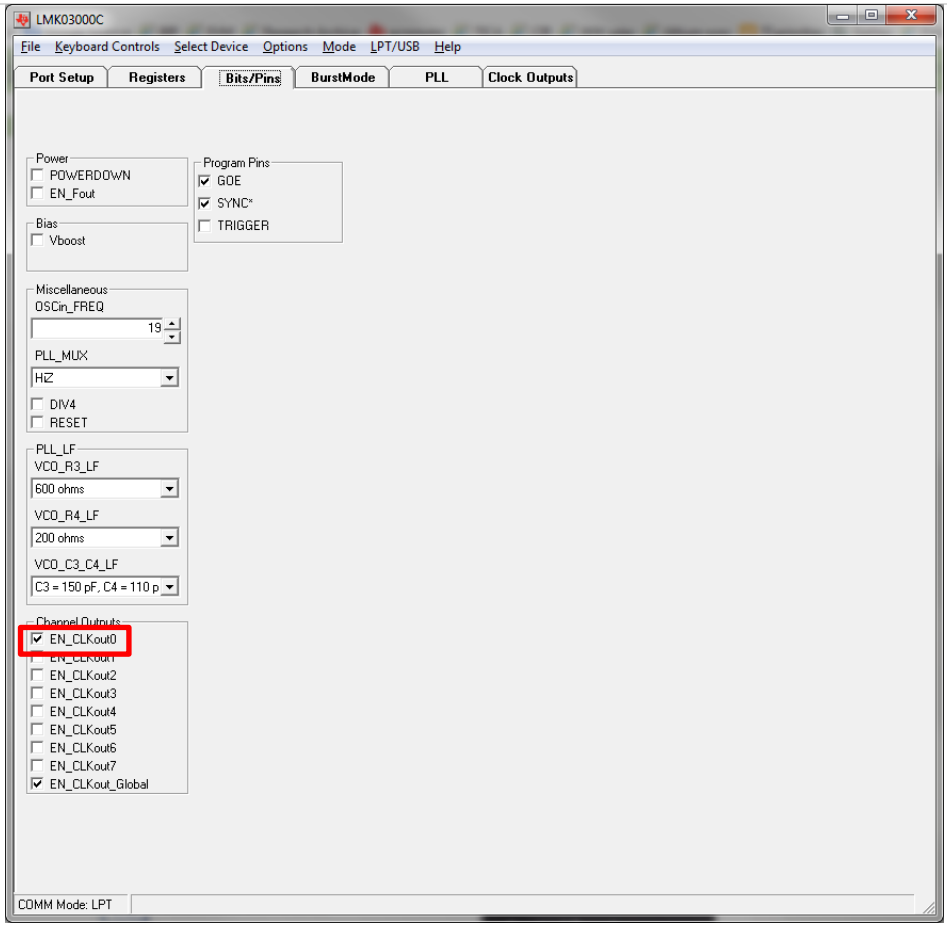
3. Start CodeLoader4.exe.

4. Select the USB or LPT Communication Mode on the Port Setup tab as appropriate.

5. Enable output to be measured, any of CLKout(0-7) or EN_Fout from either Clock Outputs or Bits/Pins tab. In example below, CLKout0 is enabled.



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Program Bits	
POWERDOWN	Powers the part down.
EN_Fout	Turns on the Fout pin for measuring the internal VCO.
OSCin_FREQ	Must be set to the OSCin frequency in MHz.
PLL_MUX	Programmable to many different values to support Lock Detect or aid troubleshooting.
DIV4	Shall be checked for OSCin frequencies greater than 20 MHz.
RESET	The registers can be defaulted by checking and unchecking RESET. Software bits will not reflect this.
VCO_R3_LF VCO_R4_LF VCO_C3_C4_LF	Internal loop filter values, also accessible from Clock Outputs tab.
EN_CLKout0..7	Enable CLKout bits from CLKout0 to CLKout7. Also accessible from Clock Outputs tab.
EN_CLKout_Global	Enable all clock outs. If unselected then the EN_CLKouts are overridden and the outputs are all disabled.

Program Pins	
GOE	Set Global Output Enable to high or low logic level.
SYNC*	Set SYNC* pin to high or low logic level.
TRIGGER	Set auxiliary trigger pin to high or low logic level.

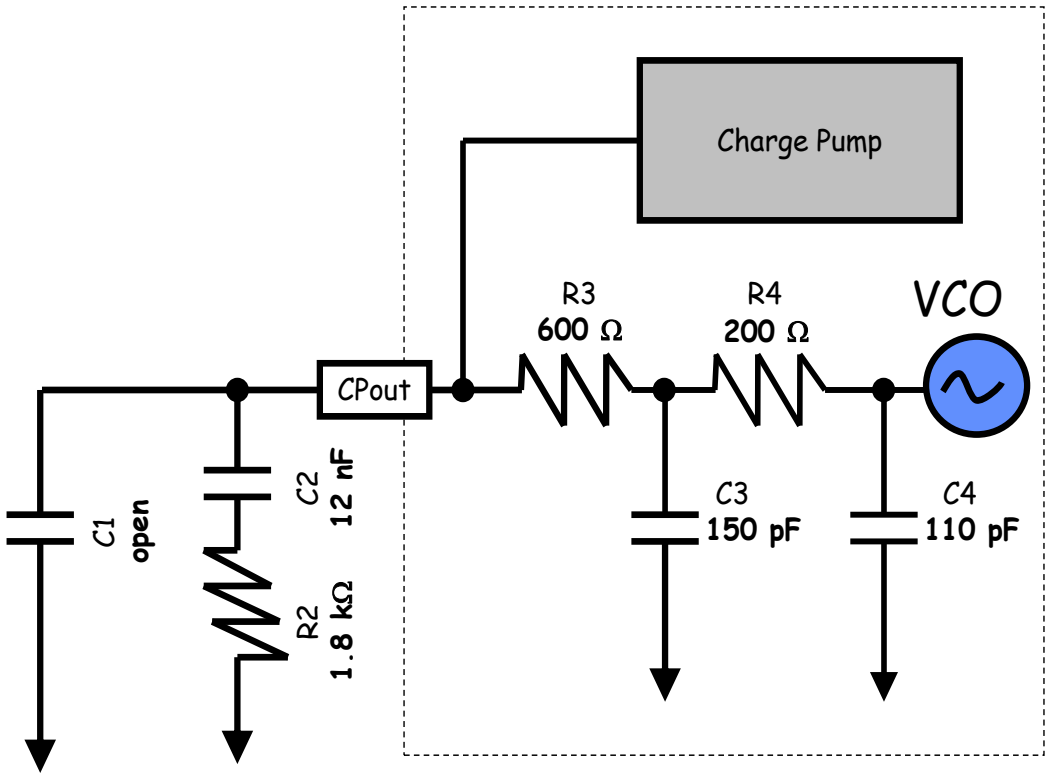
6. Program the part by clicking "Keyboard Controls" → "Load Device" OR by shortcut "**Ctrl+L**".

7. Make measurements… After programming, the uWire cabling can be unplugged from the evaluation board to minimize noise and EMI.

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LMK03000C Board information

Loop Filter #1			
Phase Margin	70.0º	**K**	3200 uA
Loop Bandwidth	55.3 kHz	**f_{PD}**	9.72 MHz
Crystal Frequency	19.44 MHz	**Output Frequency**	1185 to 1296 MHz
Supply Voltage	3.3 Volts	**VCO Gain**	8 MHz/Volt



Loop filter #1 is selected by placing a 0 ohm resistor on pad R22.

This loop filter has been designed for optimal RMS jitter using a low noise reference.

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OSCin

By default the board is configured to use the on-board crystal oscillator. It is also possible to use the board with a single ended or differential reference source at the OSCin port. Below are several possible configurations for driving OSCin.

OSCin using on board crystal oscillator [default]	
0 ohm	R8, R11, R20 [power to crystal oscillator], R109
39 ohm	R9 [can also be 0 ohm – depends on oscillator output power, 39 ohms to be a voltage divider]
51 ohm	R15
0.1 uF	C35, C36 (C5 is a 0.1 uF 0402 cap which may be moved to C36)
Open	C4, C5 R7, R10, R12, R13, R14, R16, R17, R79, R112

Differential OSCin setup	
0 ohm	R7, R8, R10, R13
100 ohm	R44
0.1 uF	C5, C35 (C36 is a 0.1 uF 0402 cap which may be moved to C5)
Open	C4, C36 R11, R12, R14, R15, R16, R79 R20 [remove power from crystal oscillator for noise reasons]

Single ended OSCin setup	
0 ohm	R7, R8
51 ohm	R15
0.1 uF	C35, C36 (C5 is a 0.1 uF 0402 cap which may be moved to C36)
Open	C4, C5 R10, R11, R12, R13, R14, R16, R17, R79 R20 [remove power from crystal oscillator for noise reasons]

Fout

Fout allows direct access to the internal VCO before the clock distribution section. The EN_Fout bit must be selected to enable Fout. A 3 dB pad is placed on R80, R81, and R82.

Loop Filter

R22 and R5 form a “resistor switch” which allows either one of two different loop filters to be selected.

Loop Filter	**Resistor Switch**	**Loop Filter Components**	**Default Loop Bandwidth**
Loop Filter #1 [default]	R22 Shorted	C1, C2, C2p, R2	59.1 kHz
Loop Filter #2	R5 Shorted	C1_AUX, C2_AUX, C2p_AUX, R2_AUX	77 Hz

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Features of the board

- Either one of two loop filters can be selected by shorting either R22 or R5. More info about each loop filter can be found in the General Description and Appendix A.
- Test points for each of the uWire lines are scattered in the lower left corner of the board and include: GOE_TP, DATAuWire, CLKuWire, LEuWire, SYNC_TP, and LD_TP.

- **Ground** is located on the unstuffed 10 pin header on the left side of the board.
- **Ground** is located on the GND_tp2 in the upper left corner of the board and GND_tp1 located to the right of the Vcc SMA connector.
- **Ground** is located on the bottom side of the board on each pad of the unstuffed 10 pin header GND_J2.

- **Vcc** is located on the unstuffed 10 pin header on the upper left side of the board.
- **Vcc** is located on VccPlane test point located to the right of the Vcc SMA.
- **Vcc** is located on the bottom side of the board on each pad of the unstuffed 10 pin header VCC_J2

Other Important Notes

- When changing the OSCin frequency, the OSCin frequency register needs to be changed to match.
- Toggle the SYNC* pin to synchronize the clock outputs when in divided mode.
- For both loop filters, a helper silkscreen is offset from the loop filters to help identify the components according to Texas Instruments Incorporated's traditional reference designators associated with loop filters.

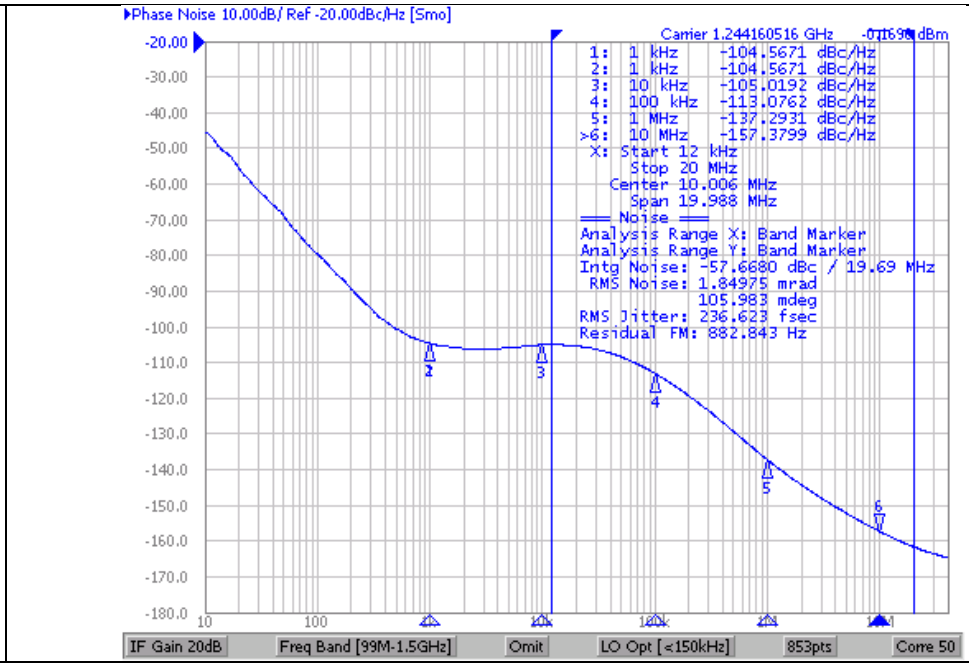
Evaluation Board Revision v1.0 Errata

- SYNC* is labeled on the PCB as SYNC, however the logic of SYNC* is still active low!

Results

Phase Noise

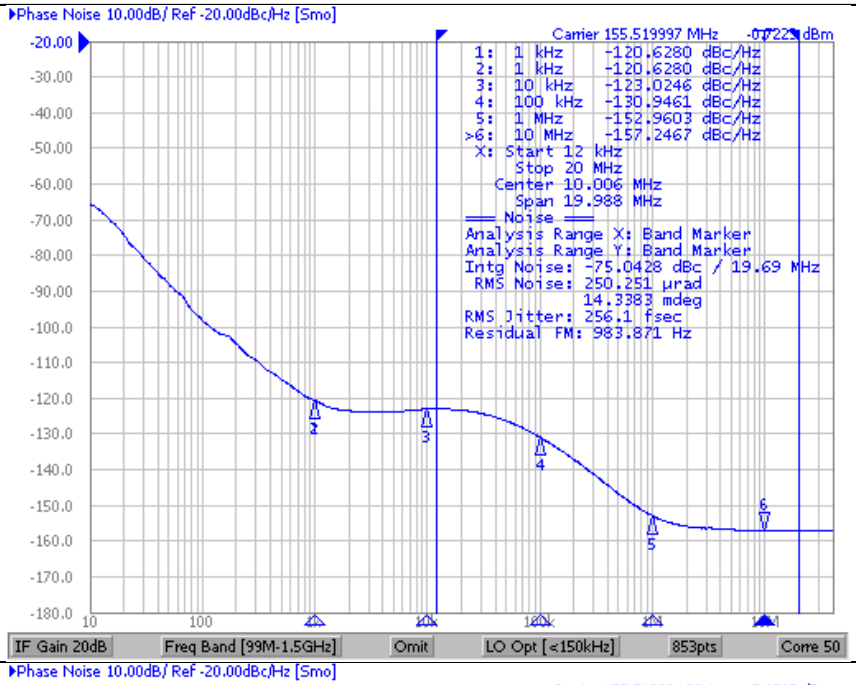
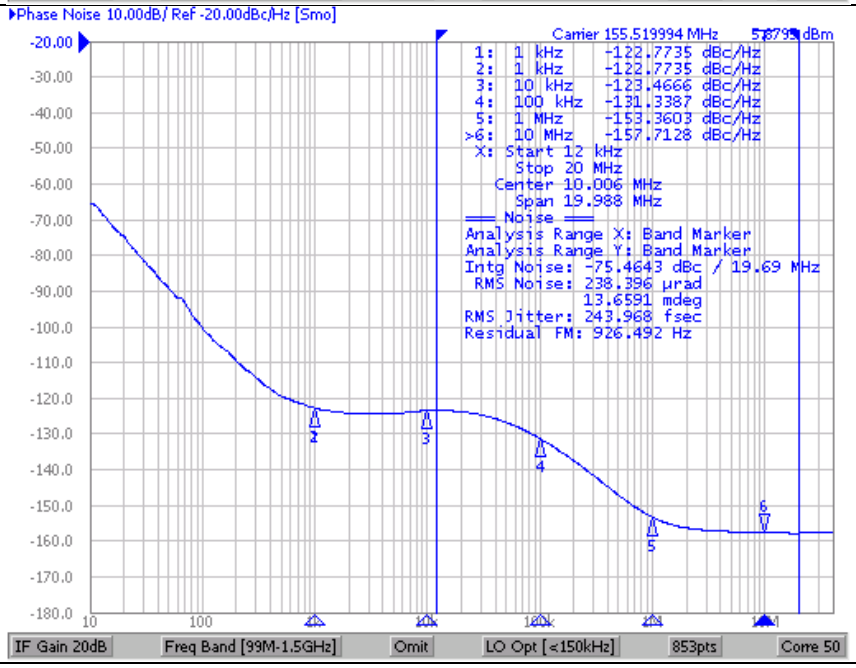
Output Frequency = 1244.16 MHz
Internal VCO, Fout output



Reference source is on board 19.44 MHz crystal

Below ~1 kHz phase noise is dominated by the crystal
10 Hz – 20 MHz integrated RMS jitter = 2.1 ps
100 Hz – 20 MHz integrated RMS jitter = 287 fs
12 kHz – 20 MHz integrated RMS jitter = 236 fs

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LVDS output CLKout0 VCO Frequency = 1244.16 MHz, VCO_DIV=2, CLKout0_div=4 LVDS output (155.52 MHz)		Output is measured with a Minicircuits ADT2-1T balun. Reference source is on board 19.44 MHz crystal Below ~1 kHz phase noise is dominated by the crystal 10 Hz – 20 MHz integrated RMS jitter = 1.8 ps 100 Hz – 20 MHz integrated RMS jitter = 315 fs 12 kHz – 20 MHz integrated RMS jitter = 256 fs (shown)
LVPECL output CLKout4 VCO Frequency = 1244.16 MHz, VCO_DIV=2, CLKout4_div=4 LVPECL output (155.52 MHz)		Output is measured with a Minicircuits ADT2-1T balun. Reference source is on board 19.44 MHz crystal Below ~1 kHz phase noise is dominated by the crystal 10 Hz – 20 MHz integrated RMS jitter = 1.7 ps 100 Hz – 20 MHz integrated RMS jitter = 281 fs 12 kHz – 20 MHz integrated RMS jitter = 244 fs (shown)

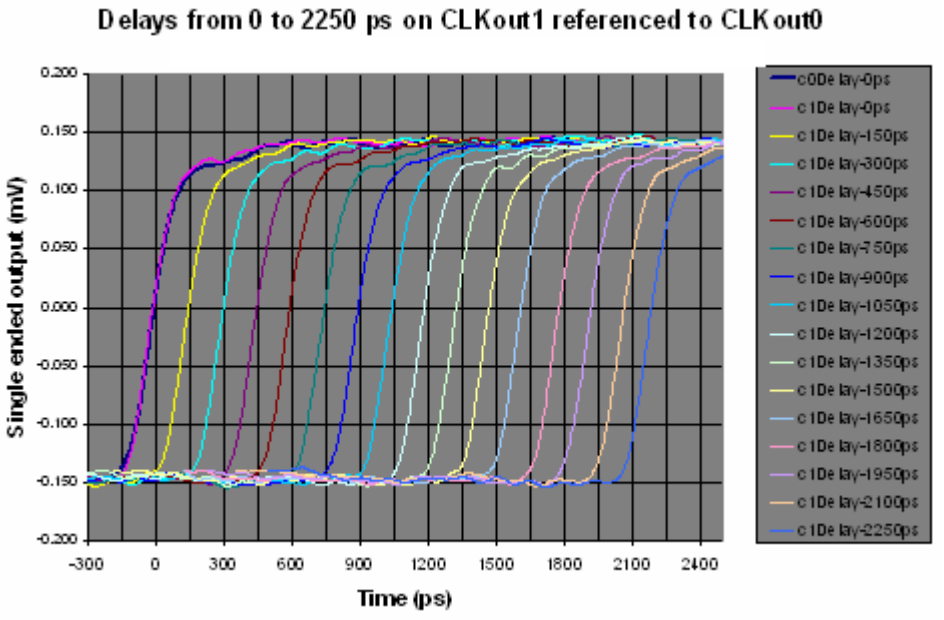
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Delays

These delay measurements illustrate how skew errors due to different length traces may be tuned out.
The delay may be adjusted in steps of 150 ps.



Delays 150, 300, 450, 600, 750



CLKout0_DLY = 0 ps

CLKout1_DLY = all delays programmed: 0, 150, 300, 450, 600, 750, 900, 1050, 1200, 1350, 1500, 1650, 1800, 1950, 2100, and 2250 ps

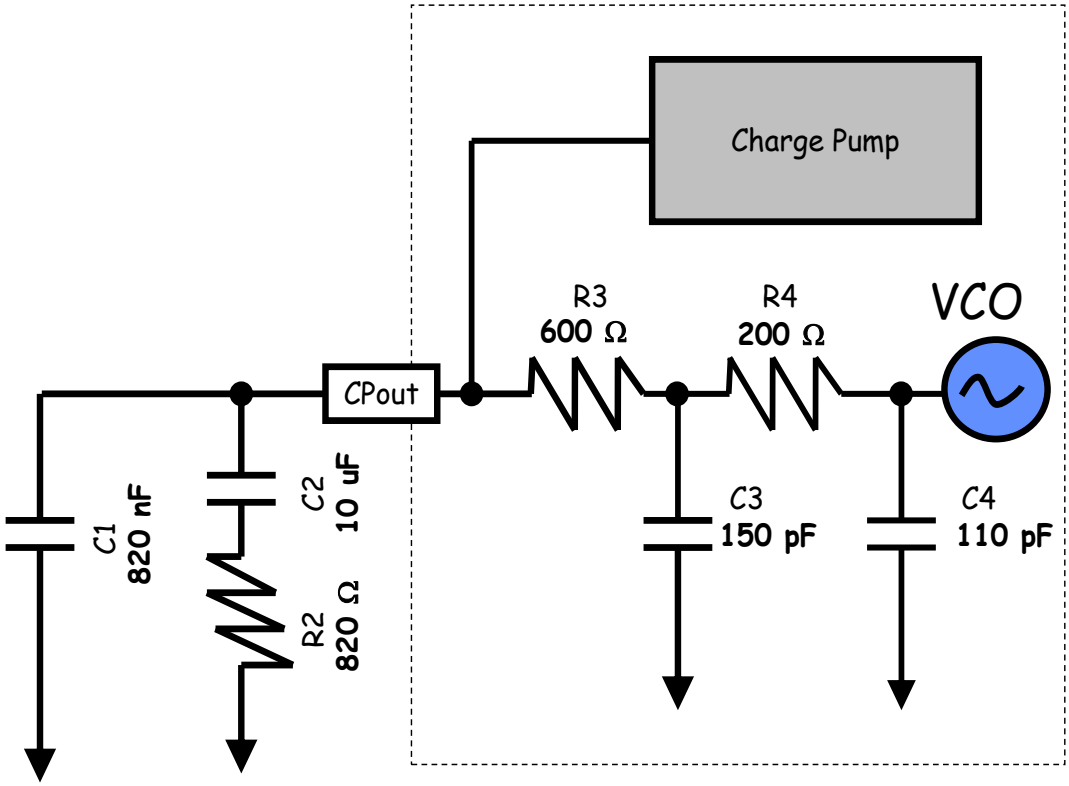
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VCO Performance

The internal VCO performance is measured by using a narrow bandwidth loop filter. By default the narrow loop bandwidth filter is stuffed as Loop Filter #2 in positions C1_AUX, C2_AUX, C2p_AUX, and R2_AUX and has a loop bandwidth of 77 Hz.

See the Loop Filter section in Board Options for more detail about switching between the two different loop filters.

Loop Filter			
Phase Margin	58.7º	**K**	100 uA
Loop Bandwidth	77 Hz	**f_{PD}**	1.023 MHz
Crystal Frequency	19.44 MHz	**Output Frequency**	1185 to 1296 MHz
Supply Voltage	3.3 Volts	**VCO Gain**	10 MHz/Volt

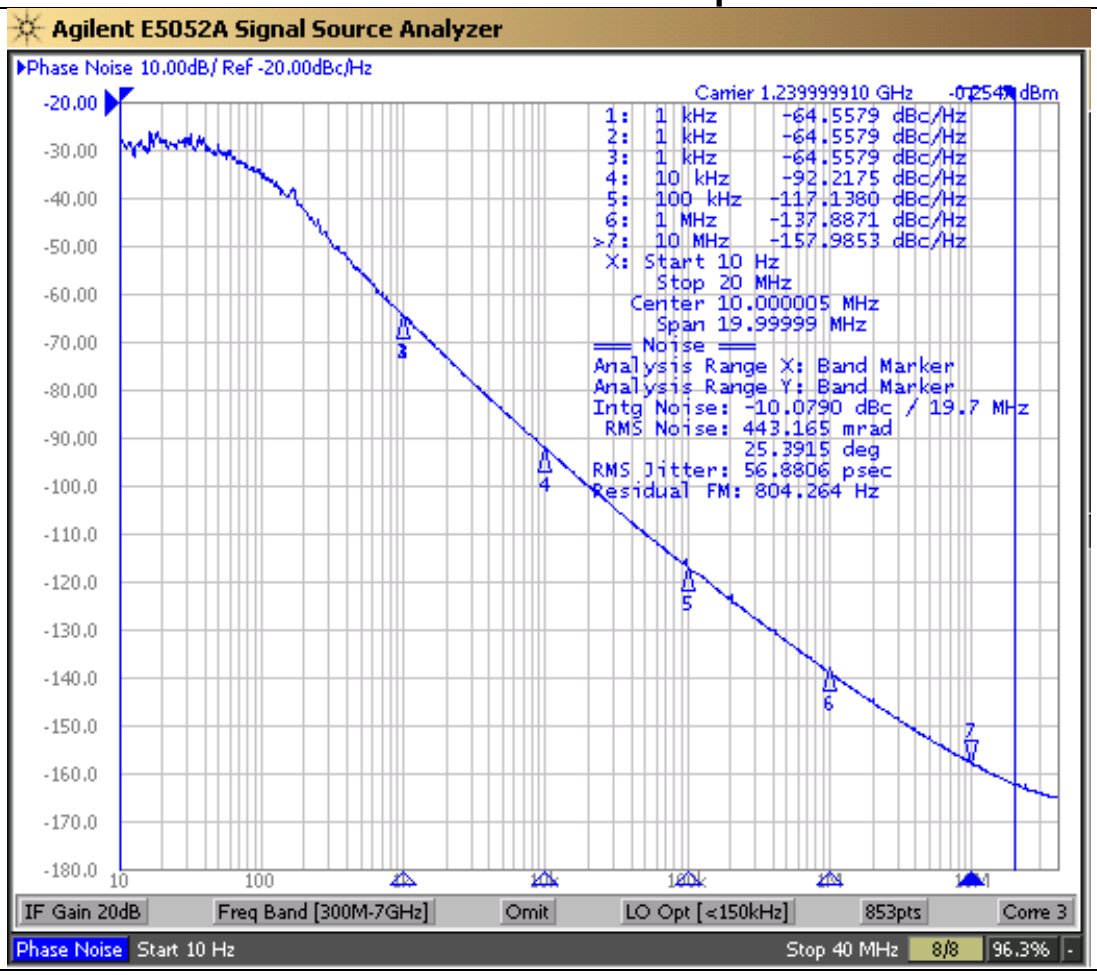


This loop filter is located on the top side of the PCB and is selected by placing a 0 ohm resistor on pad R5.

This loop filter has been designed with a very small loop bandwidth to minimize the PLL from interacting with the noise of the VCO to permit a VCO phase noise measurement.

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VCO Phase Noise - Narrow Loop Bandwidth



This plot shows the noise of the VCO at 1240 MHz using a 1 MHz Phase Detector Frequency. An external oscillator was used for this plot, since the VCO noise dominates, reference oscillator noise is not critical.

The loop bandwidth has been minimized so that the VCO is the dominant noise contributor.

10 Hz – 20 MHz integrated RMS jitter = 56.9 ps (shown)
100 Hz – 20 MHz integrated RMS jitter = 25.0 ps
12 kHz – 20 MHz integrated RMS jitter = 0.304 ps (datasheet)

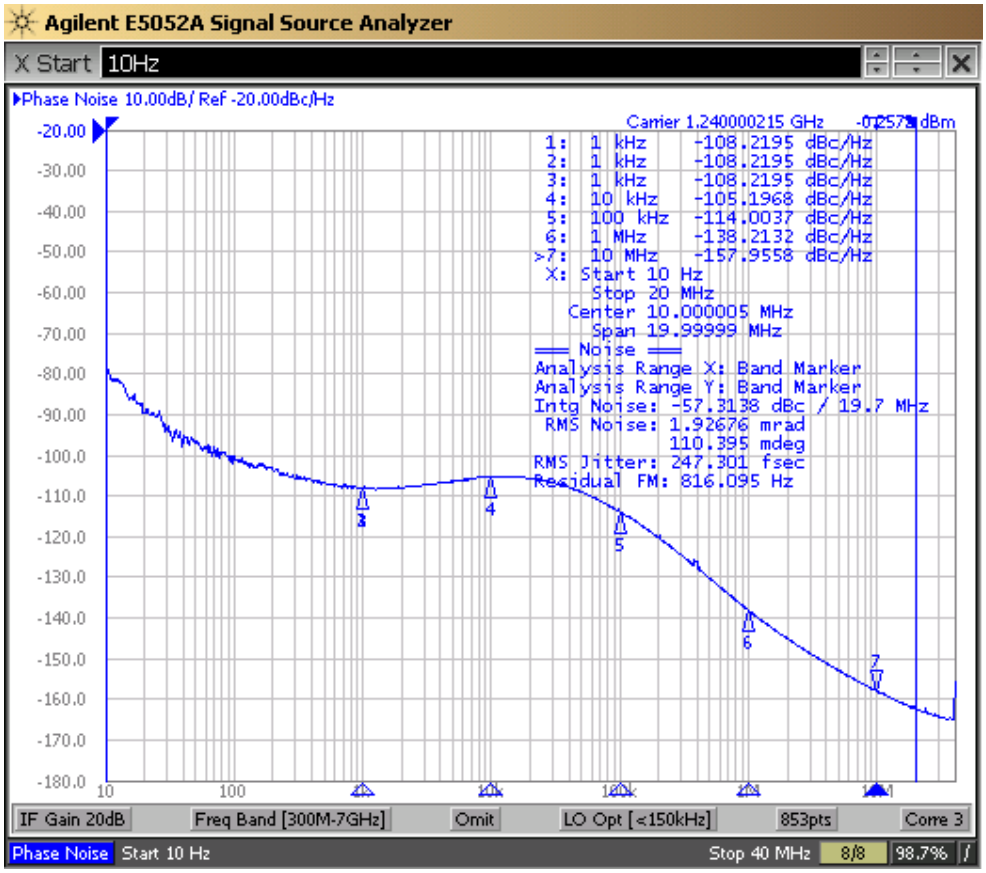
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Impact of Reference on Phase Noise

Inside the loop bandwidth of a PLL the phase noise is set by the quality of the reference oscillator used. For this reason it is important to select a reference oscillator suitable for the application.

Test Setup

Using the same loop filter as described in the General Description and by driving the OSCin frequency with an ultra low jitter 100 MHz Wetzel Crystal (501-04517D) and setting R = 10 to achieve a phase detector frequency of 10 MHz. A very low integrated RMS jitter of 247 fs is measured vs. the 2.1 ps measured in the Phase Noise section with 19.44 MHz crystal in the bandwidth of 10 Hz to 20 MHz.



10 Hz – 20 MHz integrated RMS jitter = 247 fs (shown)
100 Hz – 20 MHz integrated RMS jitter = 243 fs
12 kHz – 20 MHz integrated RMS jitter = 222 fs

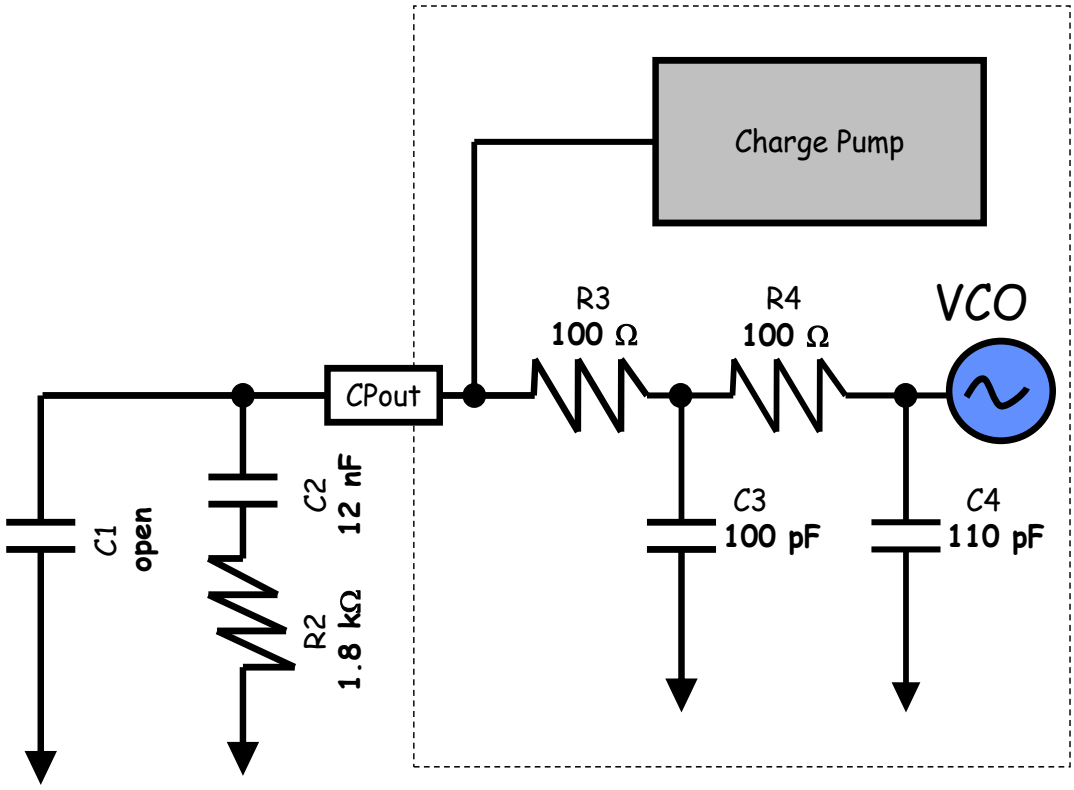
Conclusion

This diagram illustrates how the phase noise inside the loop bandwidth is set by the quality of the reference oscillator used. Phase noise outside the loop bandwidth is set by the VCO noise level.

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LMK03001C Board information

Loop Filter #1			
Phase Margin	74.4º	**K□**	3200 uA
Loop Bandwidth	59.1 kHz	**Fcomp**	12.288 MHz
Crystal Frequency	12.288 MHz	**Output Frequency**	1470 to 1570 MHz
Supply Voltage	3.3 Volts	**VCO Gain**	10 MHz/Volt



Loop filter #1 is selected by placing a 0 ohm resistor on pad R22.

This loop filter has been designed for optimal RMS jitter using a low noise reference.

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OSCin

By default the board is configured to use the on-board crystal oscillator. It is also possible to use the board with a single ended or differential reference source at the OSCin port. Below are several possible configurations for driving OSCin.

OSCin using on board crystal oscillator [default]	
0 ohm	R8, R11, R20 [power to crystal oscillator], R109
39 ohm	R9 [can also be 0 ohm – depends on oscillator output power, 39 ohms to be a voltage divider]
51 ohm	R15
0.1 uF	C35, C36 (C5 is a 0.1 uF 0402 cap which may be moved to C36)
Open	C4, C5 R7, R10, R12, R13, R14, R16, R17, R79, R112

Differential OSCin setup	
0 ohm	R7, R8, R10, R13
100 ohm	R44
0.1 uF	C5, C35 (C36 is a 0.1 uF 0402 cap which may be moved to C5)
Open	C4, C36 R11, R12, R14, R15, R16, R79 R20 [remove power from crystal oscillator for noise reasons]

Single ended OSCin setup	
0 ohm	R7, R8
51 ohm	R15
0.1 uF	C35, C36 (C5 is a 0.1 uF 0402 cap which may be moved to C36)
Open	C4, C5 R10, R11, R12, R13, R14, R16, R17, R79 R20 [remove power from crystal oscillator for noise reasons]

Fout

Fout allows direct access to the internal VCO before the clock distribution section. The EN_Fout bit must be selected to enable Fout. A 3 dB pad is placed on R80, R81, and R82.

Loop Filter

R22 and R5 form a “resistor switch” which allows either one of two different loop filters to be selected.

Loop Filter	**Resistor Switch**	**Loop Filter Components**	**Default Loop Bandwidth**
Loop Filter #1 [default]	R22 Shorted	C1, C2, C2p, R2	59.1 kHz
Loop Filter #2	R5 Shorted	C1_AUX, C2_AUX, C2p_AUX, R2_AUX	77 Hz

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Features of the board

- Either one of two loop filters can be selected by shorting either R22 or R5. More info about each loop filter can be found in the General Description and Appendix A.
- Test points for each of the uWire lines are scattered in the lower left corner of the board and include: GOE_TP, DATAuWire, CLKuWire, LEuWire, SYNC_TP, and LD_TP.

- **Ground** is located on the unstuffed 10 pin header on the left side of the board.
- **Ground** is located on the GND_tp2 in the upper left corner of the board and GND_tp1 located to the right of the Vcc SMA connector.
- **Ground** is located on the bottom side of the board on each pad of the unstuffed 10 pin header GND_J2.

- **Vcc** is located on the unstuffed 10 pin header on the upper left side of the board.
- **Vcc** is located on VccPlane test point located to the right of the Vcc SMA.
- **Vcc** is located on the bottom side of the board on each pad of the unstuffed 10 pin header VCC_J2

Other Important Notes

- When changing the OSCin frequency, the OSCin frequency register needs to be changed to match.
- Toggle the SYNC* pin to synchronize the clock outputs when in divided mode.
- For both loop filters, a helper silkscreen is offset from the loop filters to help identify the components according to Texas Instruments Incorporated's traditional reference designators associated with loop filters.

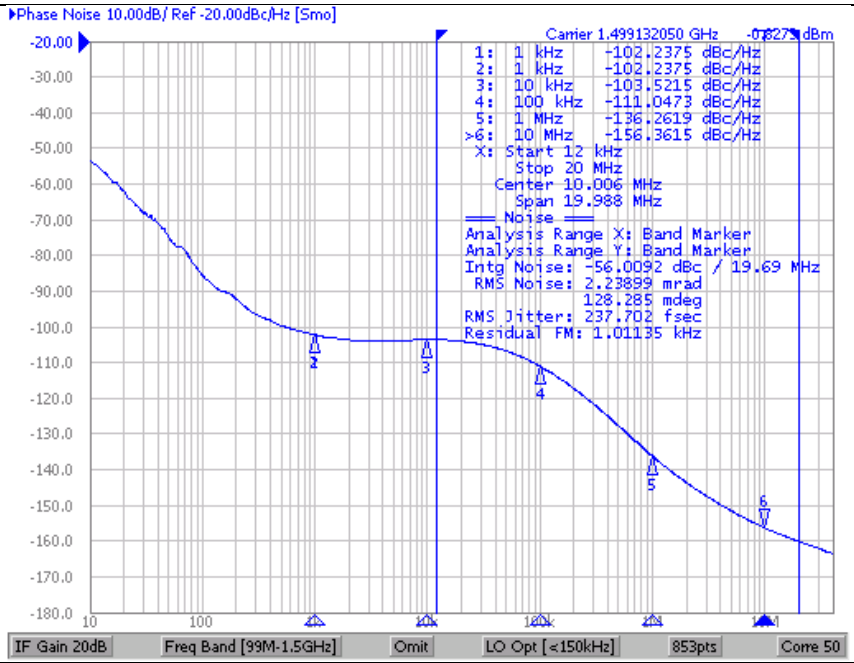
Evaluation Board Revision v1.0 Errata

- SYNC* is labeled on the PCB as SYNC, however the logic of SYNC* is still active low!

Results

Phase Noise

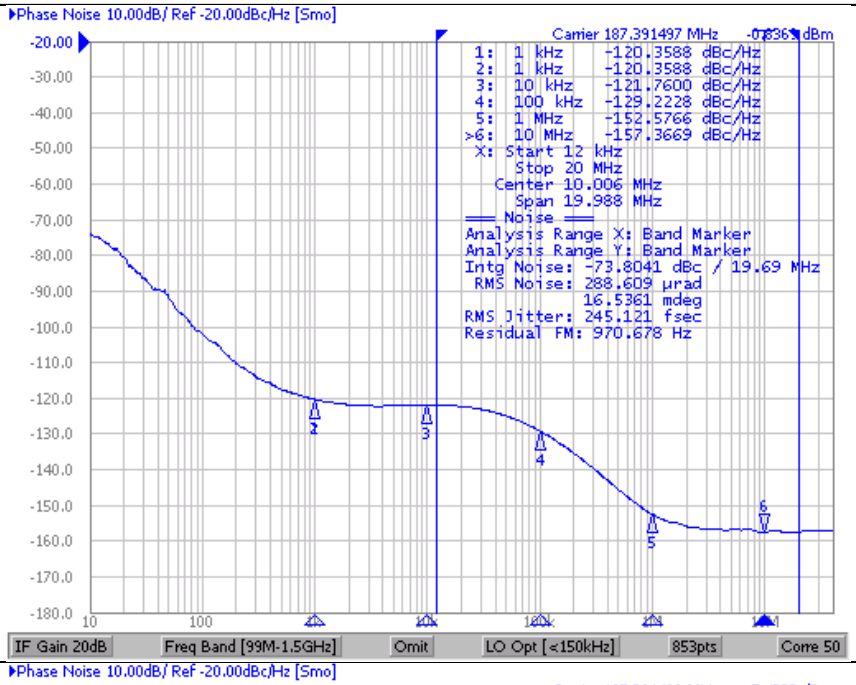
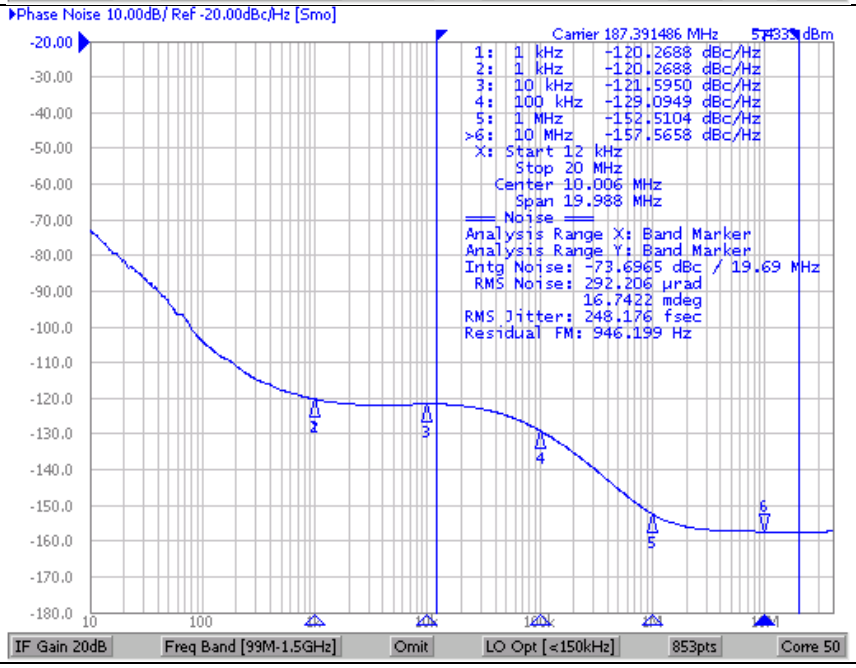
Output Frequency = 1499.136 MHz
Internal VCO, Fout output



Reference source is on board 12.288 MHz crystal

Below ~1 kHz phase noise is dominated by the crystal
10 Hz – 20 MHz integrated RMS jitter = 782 fs
100 Hz – 20 MHz integrated RMS jitter = 269 fs
12 kHz – 20 MHz integrated RMS jitter = 238 fs

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LVDS output CLKout0 VCO Frequency = 1499.136 MHz, INPUT_DIV=2, CLKout0_div=4 LVDS output (187.392 MHz)		Output is measured with a Minicircuits ADT2-1T balun. Reference source is on board 12.288 MHz crystal Below ~1 kHz phase noise is dominated by the crystal 10 Hz – 20 MHz integrated RMS jitter = 702 fs 100 Hz – 20 MHz integrated RMS jitter = 277 fs 12 kHz – 20 MHz integrated RMS jitter = 245 fs (shown)
LVPECL output CLKout4 VCO Frequency = 1499.136 MHz, INPUT_DIV=2, CLKout4_div=4 LVPECL output (187.392 MHz)		Output is measured with a Minicircuits ADT2-1T balun. Reference source is on board 12.288 MHz crystal Below ~1 kHz phase noise is dominated by the crystal 10 Hz – 20 MHz integrated RMS jitter = 679 fs 100 Hz – 20 MHz integrated RMS jitter = 278 fs 12 kHz – 20 MHz integrated RMS jitter = 248 fs (shown)

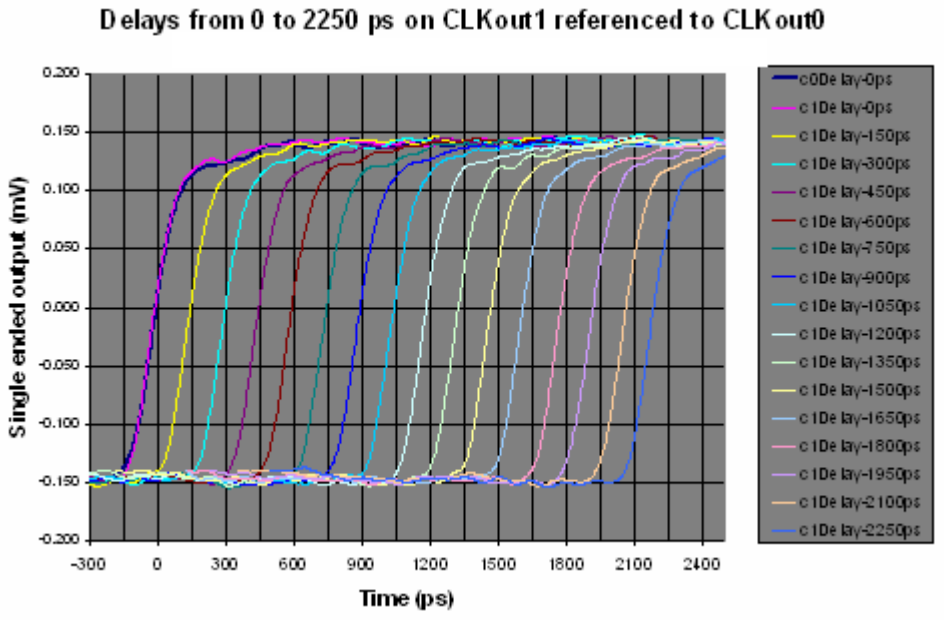
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Delays

These delay measurements illustrate how skew errors due to different length traces may be tuned out.
The delay may be adjusted in steps of 150 ps.



Delays 150, 300, 450, 600, 750



CLKout0_DLY = 0 ps

CLKout1_DLY = all delays programmed: 0, 150, 300, 450, 600, 750, 900, 1050, 1200, 1350, 1500, 1650, 1800, 1950, 2100, and 2250 ps

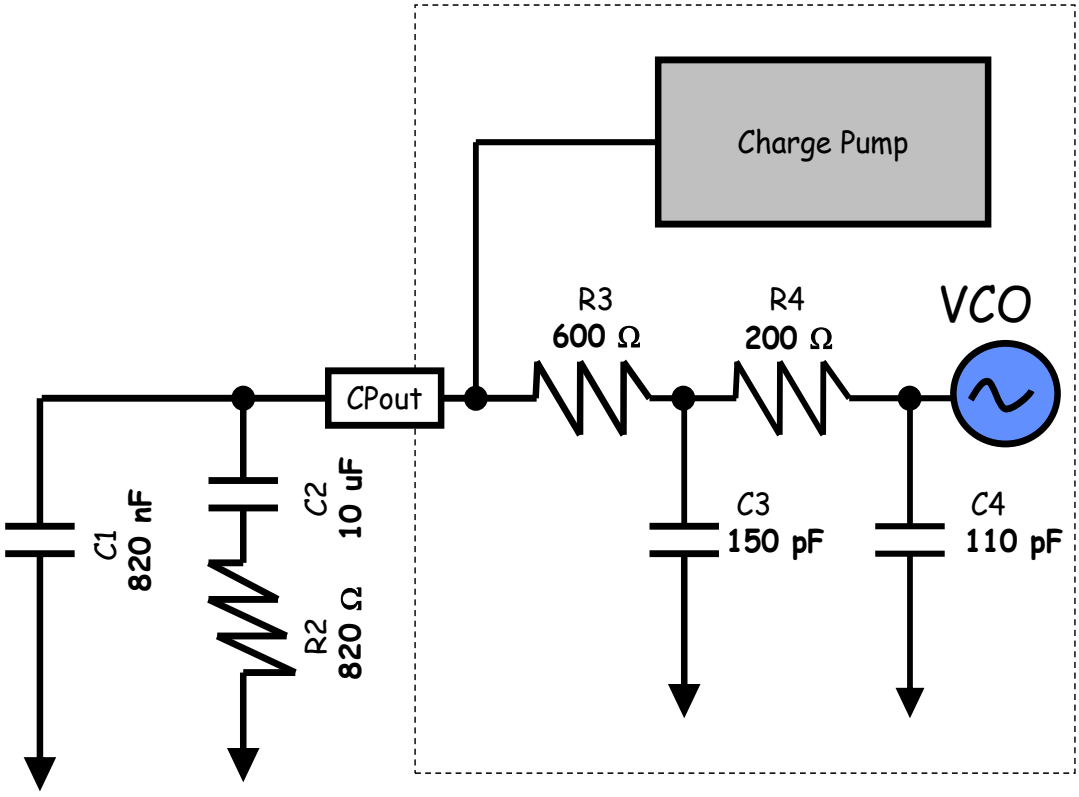
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VCO Performance

The internal VCO performance is measured by using a narrow bandwidth loop filter. By default the narrow loop bandwidth filter is stuffed as Loop Filter #2 in positions C1_AUX, C2_AUX, C2p_AUX, and R2_AUX and has a loop bandwidth of 77 Hz.

See the Loop Filter section in Board Options for more detail about switching between the two different loop filters.

Loop Filter			
Phase Margin	58.7º	**K**	100 uA
Loop Bandwidth	77 Hz	**Fcomp**	1.024 MHz
Crystal Frequency	12.288 MHz	**Output Frequency**	1470 to 1570 MHz
Supply Voltage	3.3 Volts	**VCO Gain**	10 MHz/Volt

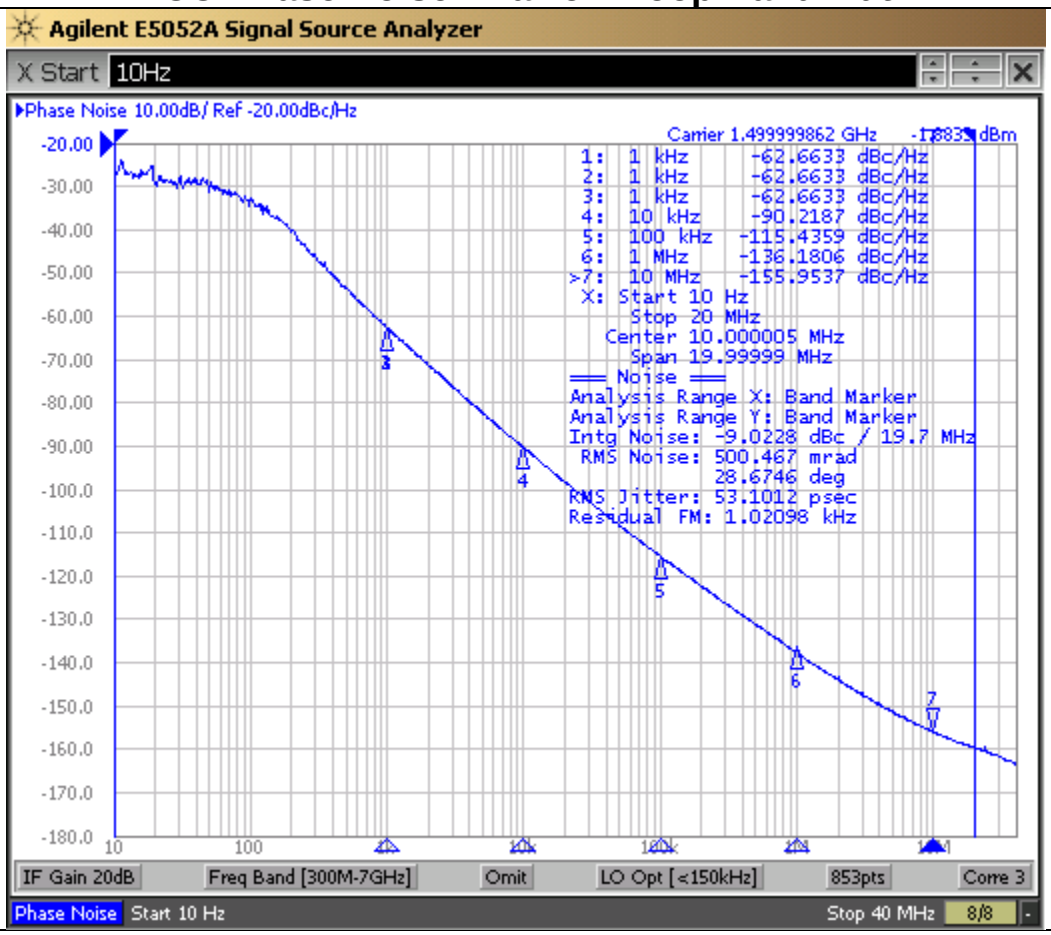


This loop filter is located on the top side of the PCB and is selected by placing a 0 ohm resistor on pad R5.

This loop filter has been designed with a very small loop bandwidth to minimize the PLL from interacting with the noise of the VCO to permit a VCO phase noise measurement.

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VCO Phase Noise - Narrow Loop Bandwidth



This plot shows the noise of the VCO at 1500 MHz using a 1 MHz Phase Detector Frequency. An external oscillator was used for this plot, since the VCO noise dominates, reference oscillator noise is not critical.

The loop bandwidth has been minimized so that the VCO is the dominant noise contributor.

10 Hz – 20 MHz integrated RMS jitter = 53.1 ps (shown)
100 Hz – 20 MHz integrated RMS jitter = 26.3 ps
12 kHz – 20 MHz integrated RMS jitter = 0.310 ps

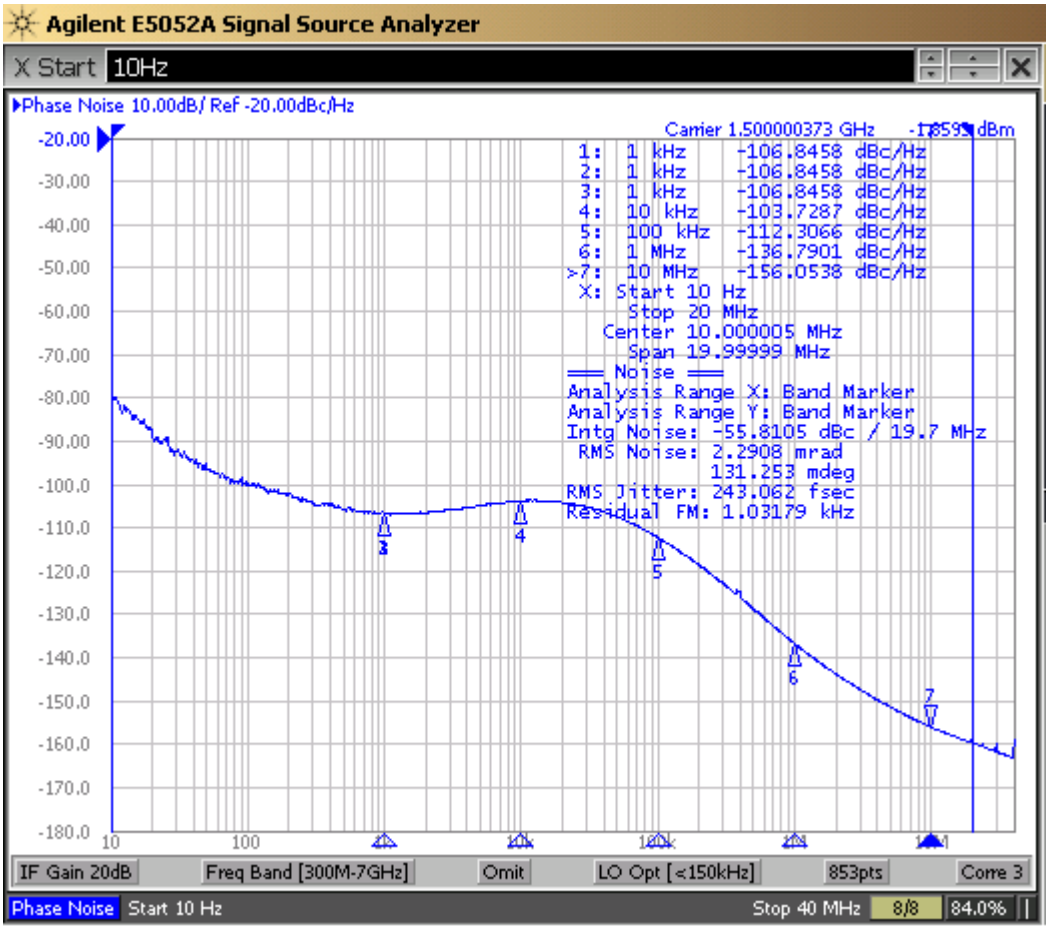
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Impact of Reference on Phase Noise

Inside the loop bandwidth of a PLL the phase noise is set by the quality of the reference oscillator used. For this reason it is important to select a reference oscillator suitable for the application.

Test Setup

Using the same loop filter as described in the General Description and by driving the OSCin frequency with an ultra low jitter 100 MHz Wetzel Crystal (501-04517D) and setting R = 10 to achieve a phase detector frequency of 10 MHz. A very low integrated RMS jitter of 243 fs is measured vs. the 782 fs measured in the Phase Noise section with 12.288 MHz crystal in the bandwidth of 10 Hz to 20 MHz.



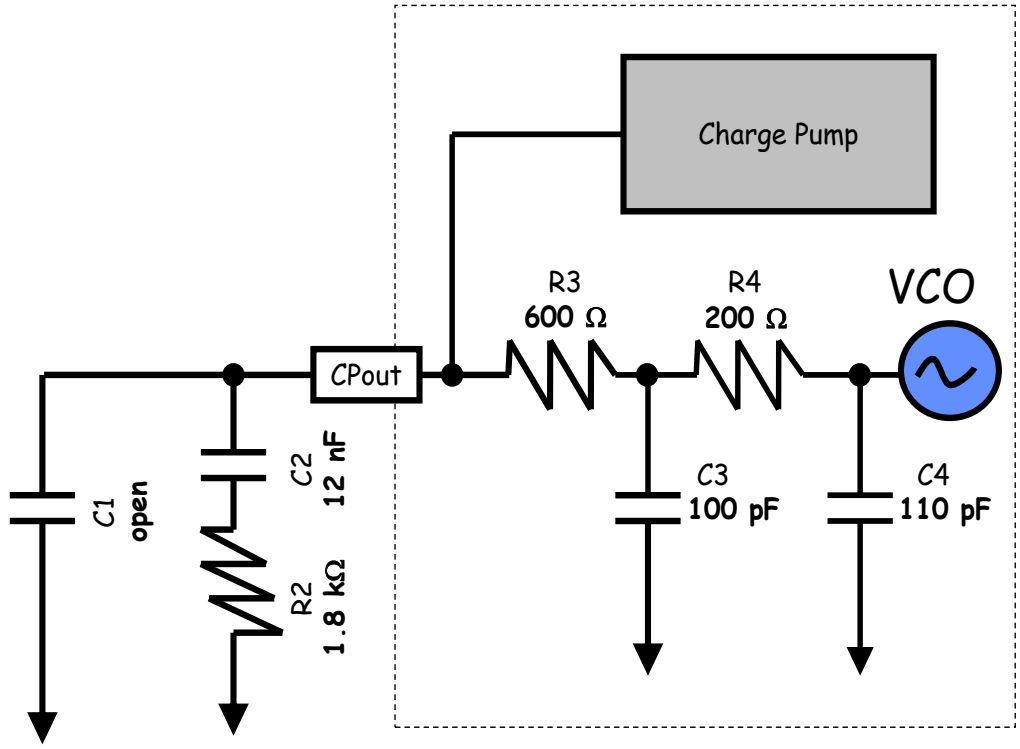
10 Hz – 20 MHz integrated RMS jitter = 243 fs (shown)
100 Hz – 20 MHz integrated RMS jitter = 240 fs
12 kHz – 20 MHz integrated RMS jitter = 220 fs

Conclusion

This diagram illustrates how the phase noise inside the loop bandwidth is set by the quality of the reference oscillator used. Phase noise outside the loop bandwidth is set by the VCO noise level.

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Loop Filter #1			
Phase Margin	63º	**K**	3200 uA
Loop Bandwidth	105 kHz	**Fcomp**	16 MHz
Crystal Frequency	16 MHz	**Output Frequency**	1566 to 1724 MHz
Supply Voltage	3.3 Volts	**VCO Gain**	13 MHz/Volt



(Loop filter #1 is selected by placing a 0 ohm resistor on pad R22)

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OSCin

By default the board is configured to use the on-board crystal oscillator. It is also possible to use the board with a single ended or differential reference source at the OSCin port. Below are several possible configurations for driving OSCin.

OSCin using on board crystal oscillator [default]	
0 ohm	R8, R11, R20 [power to crystal oscillator], R109
39 ohm	R9 [can also be 0 ohm – depends on oscillator output power, 39 ohms to be a voltage divider]
51 ohm	R15
0.1 uF	C35, C36 (C5 is a 0.1 uF 0402 cap which may be moved to C36)
Open	C4, C5 R7, R10, R12, R13, R14, R16, R17, R79, R112

Differential OSCin setup	
0 ohm	R7, R8, R10, R13
100 ohm	R17
0.1 uF	C5, C35 (C36 is a 0.1 uF 0402 cap which may be moved to C5)
Open	C4, C36 R11, R12, R14, R15, R16, R79 R20 [remove power from crystal oscillator for noise reasons]

Single ended OSCin setup	
0 ohm	R7, R8
51 ohm	R15
0.1 uF	C35, C36 (C5 is a 0.1 uF 0402 cap which may be moved to C36)
Open	C4, C5 R10, R11, R12, R13, R14, R16, R17, R79 R20 [remove power from crystal oscillator for noise reasons]

Fout

Fout allows direct access to the internal VCO before the clock distribution section. The EN_Fout bit must be selected to enable Fout. A 3 dB pad is placed on R80, R81, and R82.

Loop Filter

R22 and R5 form a “resistor switch” which allows either one of two different loop filters to be selected.

Loop Filter	**Resistor Switch**	**Loop Filter Components**	**Default Loop Bandwidth**
Loop Filter #1 [default]	R22 Shorted	C1, C2, C2p, R2	105 kHz
Loop Filter #2	R5 Shorted	C1_AUX, C2_AUX, C2p_AUX, R2_AUX	55 Hz

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Features of the board

- Either one of two loop filters can be selected by shorting either R22 or R5. More info about each loop filter can be found in the General Description and Appendix A.
- Test points for each of the uWire lines are scattered in the lower left corner of the board and include: GOE_TP, DATAuWire, CLKuWire, LEuWire, SYNC_TP, and LD_TP.

- **Ground** is located on the unstuffed 10 pin header on the left side of the board.
- **Ground** is located on the GND_tp2 in the upper left corner of the board and GND_tp1 located to the right of the Vcc SMA connector.
- **Ground** is located on the bottom side of the board on each pad of the unstuffed 10 pin header GND_J2.

- **Vcc** is located on the unstuffed 10 pin header on the upper left side of the board.
- **Vcc** is located on VccPlane test point located to the right of the Vcc SMA.
- **Vcc** is located on the bottom side of the board on each pad of the unstuffed 10 pin header VCC_J2

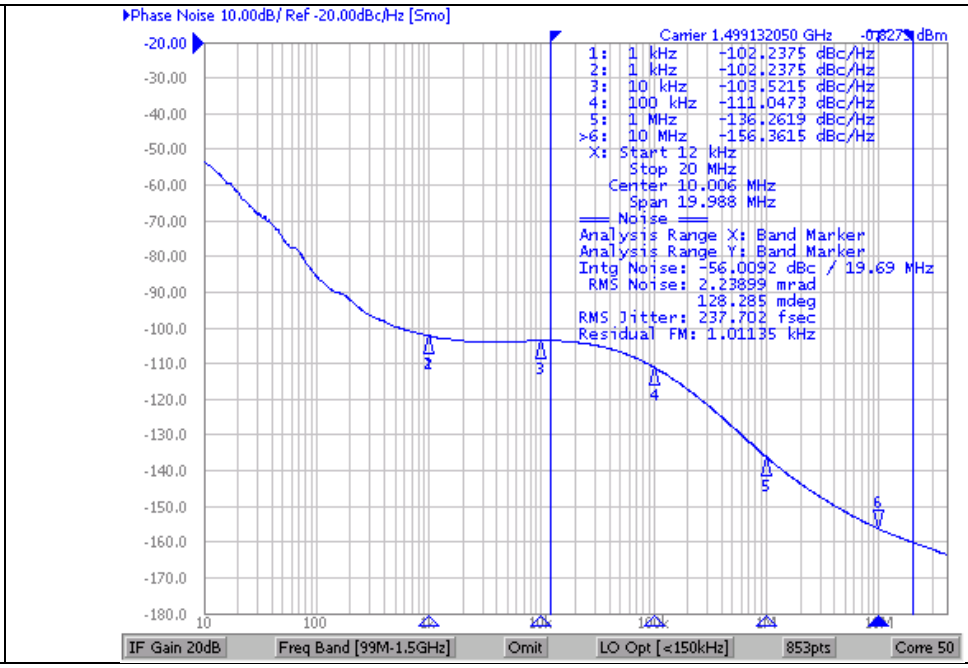
Other Important Notes

- When changing the OSCin frequency, the OSCin frequency register needs to be changed to match.
- Toggle the SYNC* pin to synchronize the clock outputs when in divided mode.
- For both loop filters, a helper silkscreen is offset from the loop filters to help identify the components according to Texas Instruments Incorporated's traditional reference designators associated with loop filters.

Results

Phase Noise

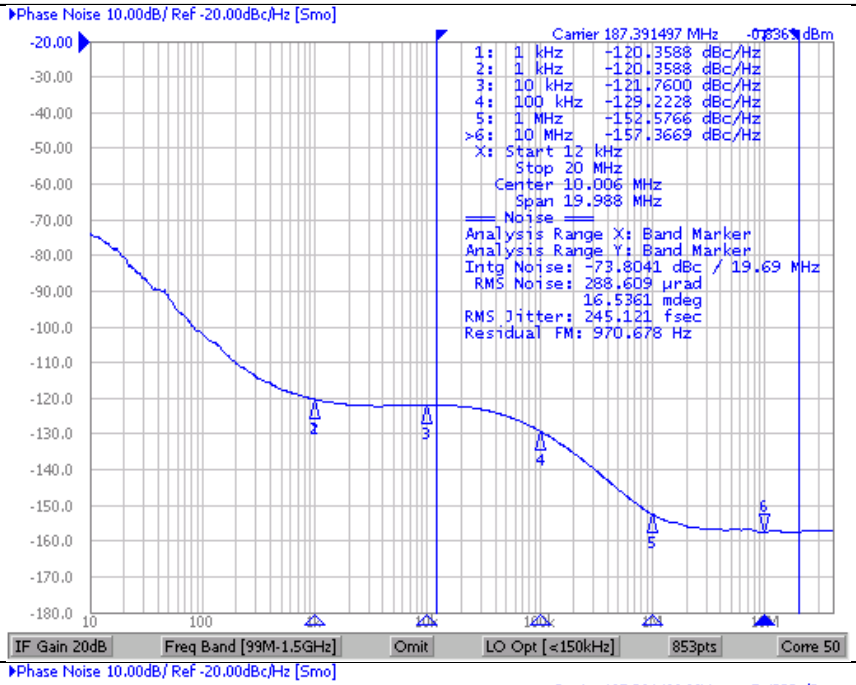
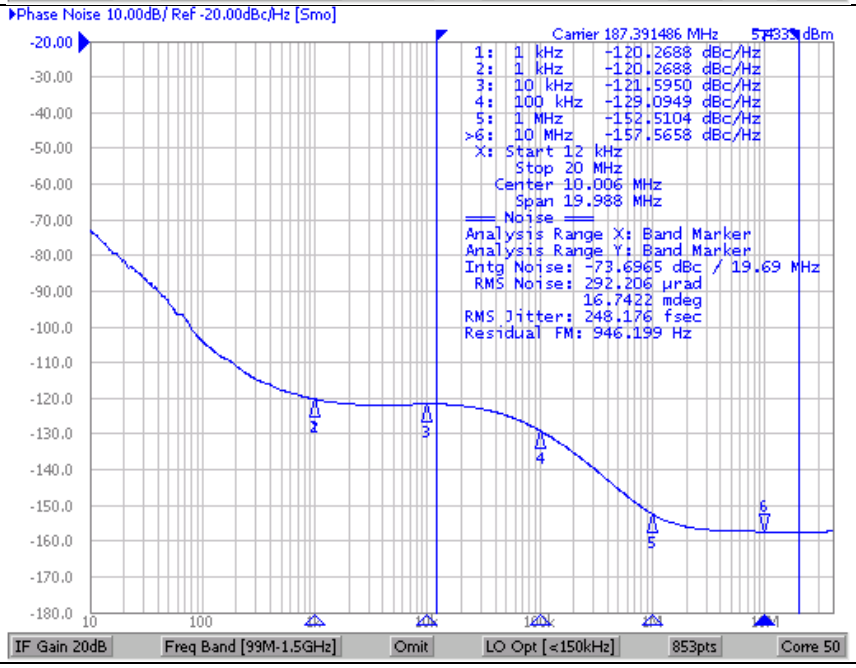
Output Frequency = 1499.136 MHz
Internal VCO, Fout output



Reference source is on board 12.288 MHz crystal

Below ~1 kHz phase noise is dominated by the crystal
10 Hz – 20 MHz integrated RMS jitter = 782 fs
100 Hz – 20 MHz integrated RMS jitter = 269 fs
12 kHz – 20 MHz integrated RMS jitter = 238 fs

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LVDS output CLKout0 VCO Frequency = 1499.136 MHz, INPUT_DIV=2, CLKout0_div=4 LVDS output (187.392 MHz)		Output is measured with a Minicircuits ADT2-1T balun. Reference source is on board 12.288 MHz crystal Below ~1 kHz phase noise is dominated by the crystal 10 Hz – 20 MHz integrated RMS jitter = 702 fs 100 Hz – 20 MHz integrated RMS jitter = 277 fs 12 kHz – 20 MHz integrated RMS jitter = 245 fs (shown)
LVPECL output CLKout4 VCO Frequency = 1499.136 MHz, INPUT_DIV=2, CLKout4_div=4 LVPECL output (187.392 MHz)		Output is measured with a Minicircuits ADT2-1T balun. Reference source is on board 12.288 MHz crystal Below ~1 kHz phase noise is dominated by the crystal 10 Hz – 20 MHz integrated RMS jitter = 679 fs 100 Hz – 20 MHz integrated RMS jitter = 278 fs 12 kHz – 20 MHz integrated RMS jitter = 248 fs (shown)

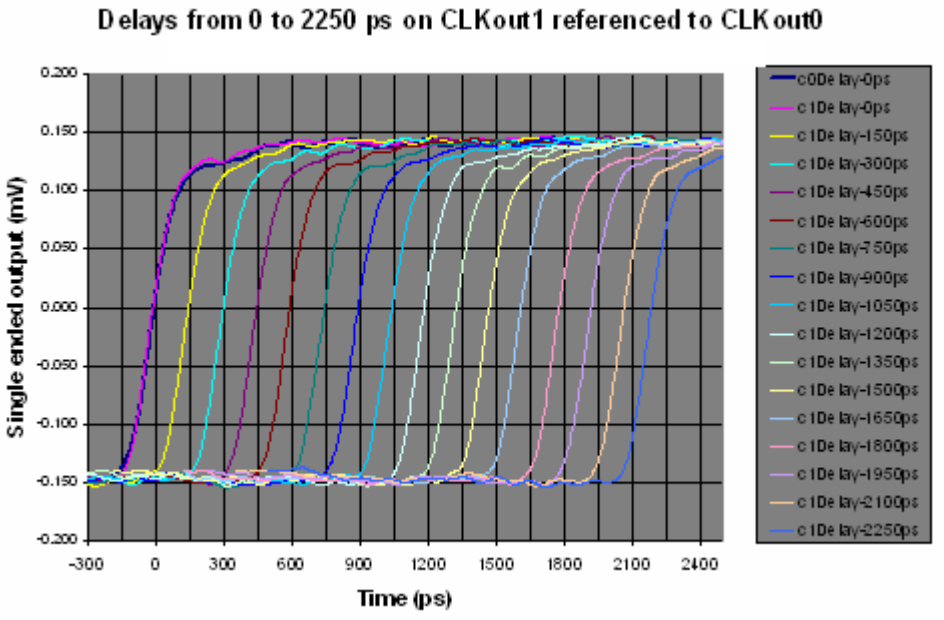
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Delays

These delay measurements illustrate how skew errors due to different length traces may be tuned out.
The delay may be adjusted in steps of 150 ps.



Delays 150, 300, 450, 600, 750



CLKout0_DLY = 0 ps

CLKout1_DLY = all delays programmed: 0, 150, 300, 450, 600, 750, 900, 1050, 1200, 1350, 1500, 1650, 1800, 1950, 2100, and 2250 ps

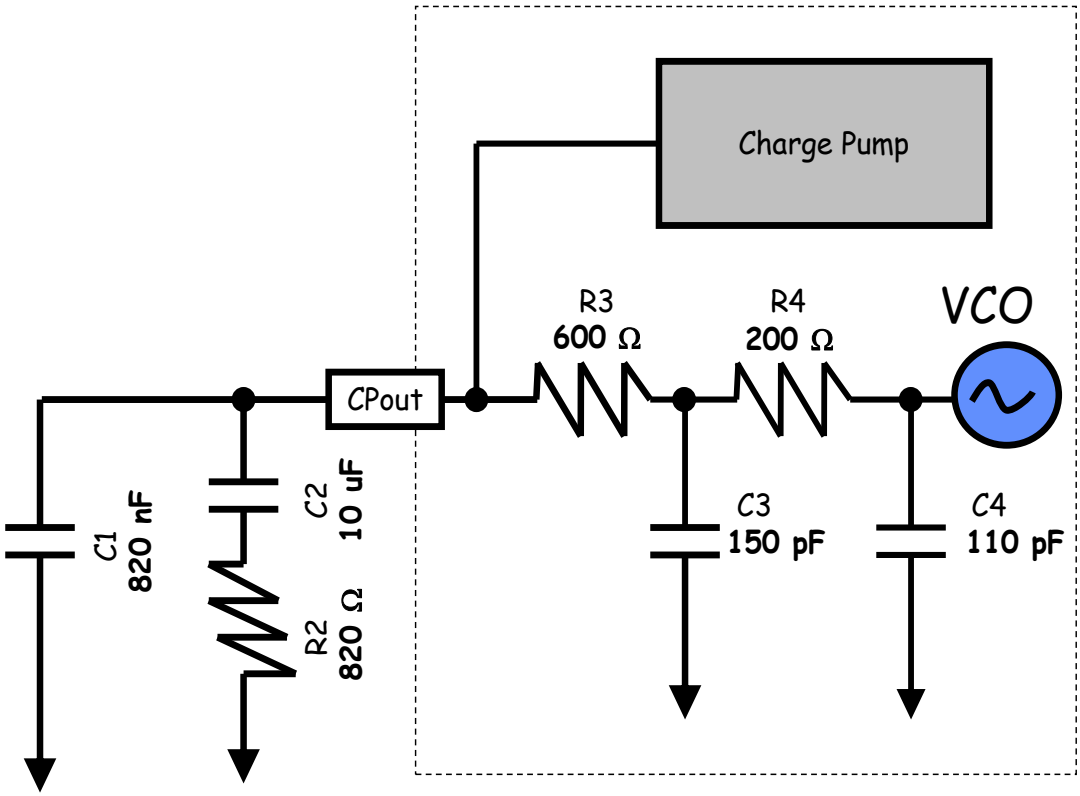
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VCO Performance

The internal VCO performance is measured by using a narrow bandwidth loop filter. By default the narrow loop bandwidth filter is stuffed as Loop Filter #2 in positions C1_AUX, C2_AUX, C2p_AUX, and R2_AUX and has a loop bandwidth of 55 Hz.

See the Loop Filter section in Board Options for more detail about switching between the two different loop filters.

Loop Filter #2			
Phase Margin	58º	**K**	100 uA
Loop Bandwidth	55 Hz	**Fcomp**	500 kHz
Crystal Frequency	16 MHz	**Output Frequency**	1566 to 1724 MHz
Supply Voltage	3.3 Volts	**VCO Gain**	13 MHz/Volt

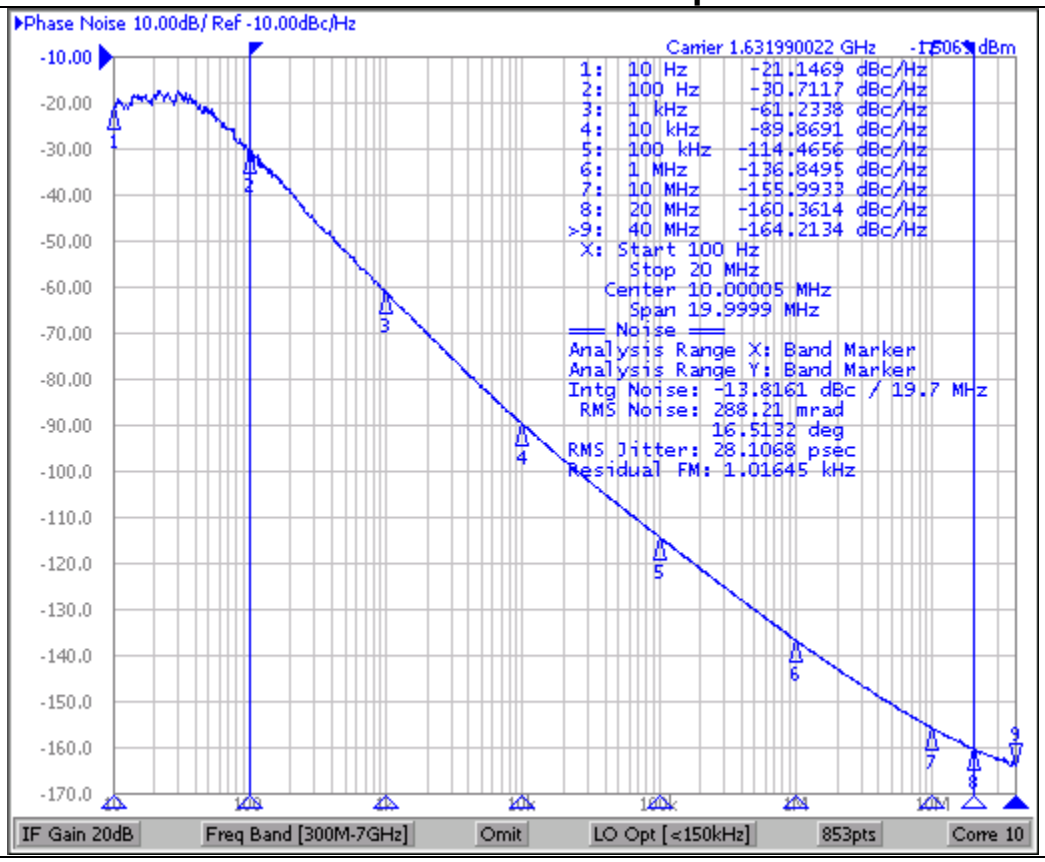


This loop filter is located on the top side of the PCB and is selected by placing a 0 ohm resistor on pad R5.

This loop filter has been designed with a very small loop bandwidth to minimize the PLL from interacting with the noise of the VCO to permit a VCO phase noise measurement.

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VCO Phase Noise – Narrow Loop Bandwidth



This plot shows the noise of the VCO at 1632 MHz using a 500 kHz Phase Detector Frequency. An external oscillator was used for this plot, since the VCO noise dominates, reference oscillator noise is not critical.

The loop bandwidth has been minimized so that the VCO is the dominant noise contributor.

10 Hz – 20 MHz integrated RMS jitter = 107.6 ps
100 Hz – 20 MHz integrated RMS jitter = 28.1 ps (shown)
1 kHz – 20 MHz integrated RMS jitter = 2.7 ps
12 kHz – 20 MHz integrated RMS jitter = 0.303 ps

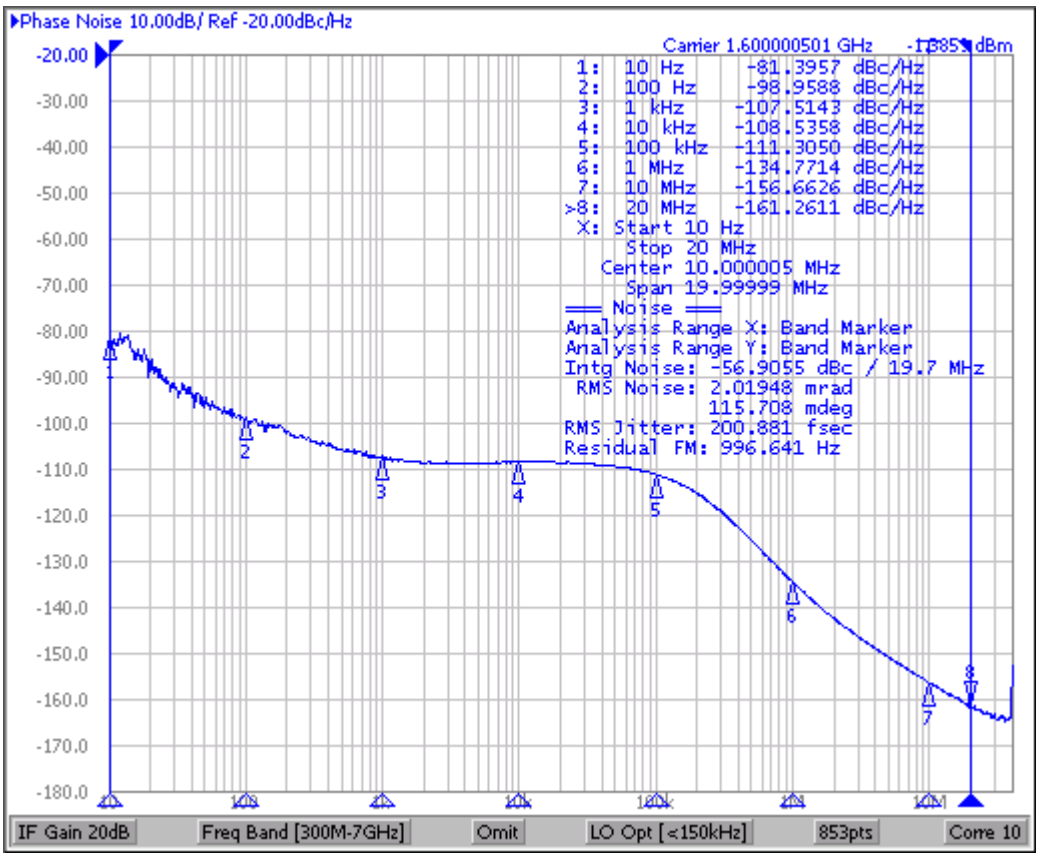
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Impact of Reference on Phase Noise

Inside the loop bandwidth of a PLL the phase noise is set by the quality of the reference oscillator used. For this reason it is important to select a reference oscillator suitable for the application.

Test Setup

Using the same loop filter as described in the General Description and by driving the OSCin frequency with an ultra low jitter 100 MHz Wetzel Crystal (501-04517D) and setting R = 5 to achieve a phase detector frequency of 20 MHz. A very low integrated RMS jitter of 201 fs is measured vs. the 474 fs measured in the Phase Noise section with 16 MHz crystal in the bandwidth of 10 Hz to 20 MHz.



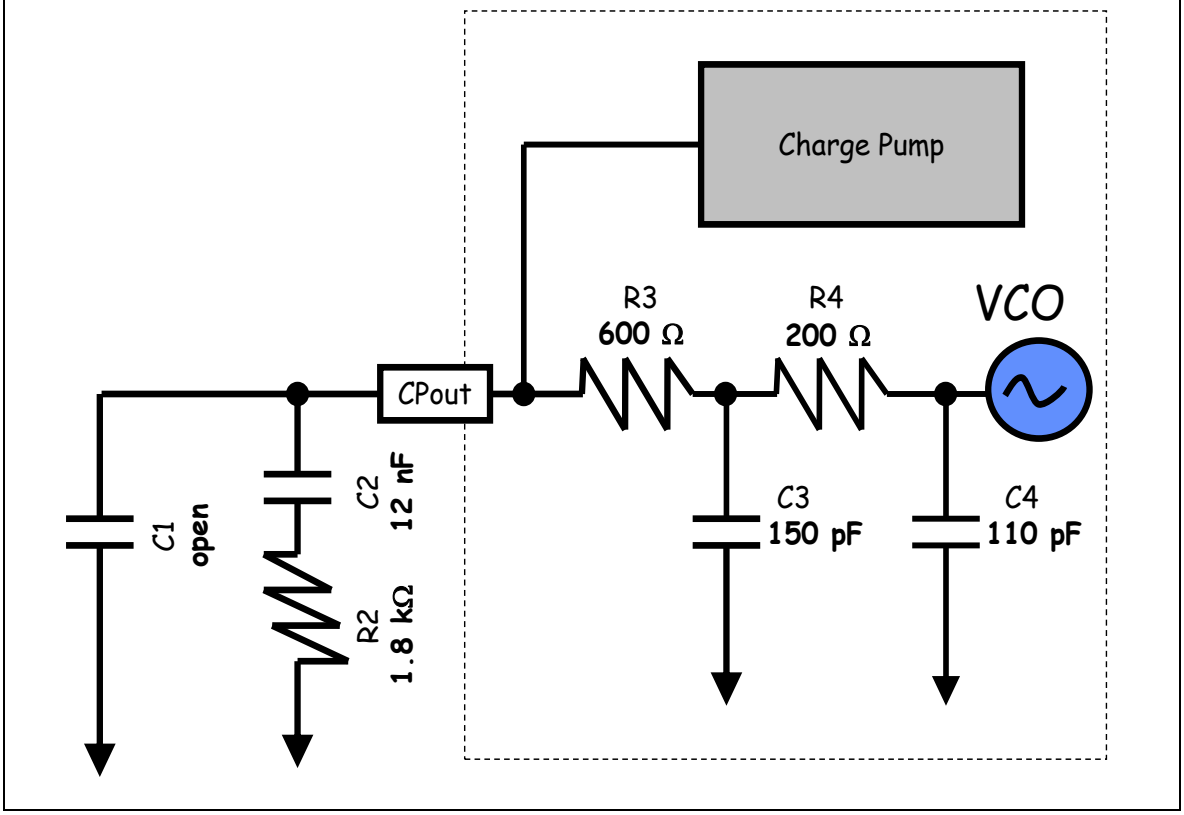
10 Hz – 20 MHz integrated RMS jitter = 201 fs (shown)
100 Hz – 20 MHz integrated RMS jitter = 197 fs
1 kHz – 20 MHz integrated RMS jitter = 196 fs
12 kHz – 20 MHz integrated RMS jitter = 188 fs

Conclusion

This diagram illustrates how the phase noise inside the loop bandwidth is set by the quality of the reference oscillator used. Phase noise outside the loop bandwidth is set by the VCO noise level.

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Loop Filter #1			
Phase Margin	63.5 deg	**K**	3200 uA
Loop Bandwidth	104 kHz	**Fcomp**	12.288 MHz
Crystal Frequency	12.288 MHz	**Output Frequency**	1843 to 2160 MHz
Supply Voltage	3.3 Volts	**VCO Gain**	20 MHz/Volt



OSCin

By default the board is configured to use the on-board crystal oscillator. It is also possible to use the board with a single ended or differential reference source at the OSCin port. Below are several possible configurations for driving OSCin.

OSCin using on board crystal oscillator [default]	
0 ohm	R8, R11, R20 [power to crystal oscillator], R109
39 ohm	R9 [can also be 0 ohm – depends on oscillator output power, 39 ohms to be a voltage divider]
51 ohm	R15
0.1 uF	C35, C36 (C5 is a 0.1 uF 0402 cap which may be moved to C36)
Open	C4, C5 R7, R10, R12, R13, R14, R16, R17, R79, R112

Differential OSCin setup	
0 ohm	R7, R8, R10, R13

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100 ohm	R44
0.1 uF	C5, C35 (C36 is a 0.1 uF 0402 cap which may be moved to C5)
Open	C4, C36 R11, R12, R14, R15, R16, R79 R20 [remove power from crystal oscillator for noise reasons]

Single ended OSCin setup	
0 ohm	R7, R8
51 ohm	R15
0.1 uF	C35, C36 (C5 is a 0.1 uF 0402 cap which may be moved to C36)
Open	C4, C5 R10, R11, R12, R13, R14, R16, R17, R79 R20 [remove power from crystal oscillator for noise reasons]

Fout

Fout allows direct access to the internal VCO before the clock distribution section. The EN_Fout bit must be selected to enable Fout. A 3 dB pad is placed on R80, R81, and R82.

Loop Filter

R22 and R5 form a “resistor switch” which allows either one of two different loop filters to be selected.

Loop Filter	**Resistor Switch**	**Loop Filter Components**	**Default Loop Bandwidth**
Loop Filter #1 [default]	R22 Shorted	C1, C2, C2p, R2	
Loop Filter #2	R5 Shorted	C1_AUX, C2_AUX, C2p_AUX, R2_AUX	

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Features of the board

- Either one of two loop filters can be selected by shorting either R22 or R5. More info about each loop filter can be found in the General Description and Appendix A.
- Test points for each of the uWire lines are scattered in the lower left corner of the board and include: GOE_TP, DATAuWire, CLKuWire, LEuWire, SYNC_TP, and LD_TP.

- **Ground** is located on the unstuffed 10 pin header on the left side of the board.
- **Ground** is located on the GND_tp2 in the upper left corner of the board and GND_tp1 located to the right of the V_{CC} SMA connector.
- **Ground** is located on the bottom side of the board on each pad of the unstuffed 10 pin header GND_J2.

- **V_{CC}** is located on the unstuffed 10 pin header on the upper left side of the board.
- **V_{CC}** is located on V_{CC}Plane test point located to the right of the V_{CC} SMA.
- **V_{CC}** is located on the bottom side of the board on each pad of the unstuffed 10 pin header VCC_J2

Other Important Notes

- When changing the OSCin frequency, the OSCin frequency register needs to be changed to match.
- Toggle the SYNC* pin to synchronize the clock outputs when in divided mode.
- For both loop filters, a helper silkscreen is offset from the loop filters to help identify the components according to Texas Instruments Incorporated's traditional reference designators associated with loop filters.

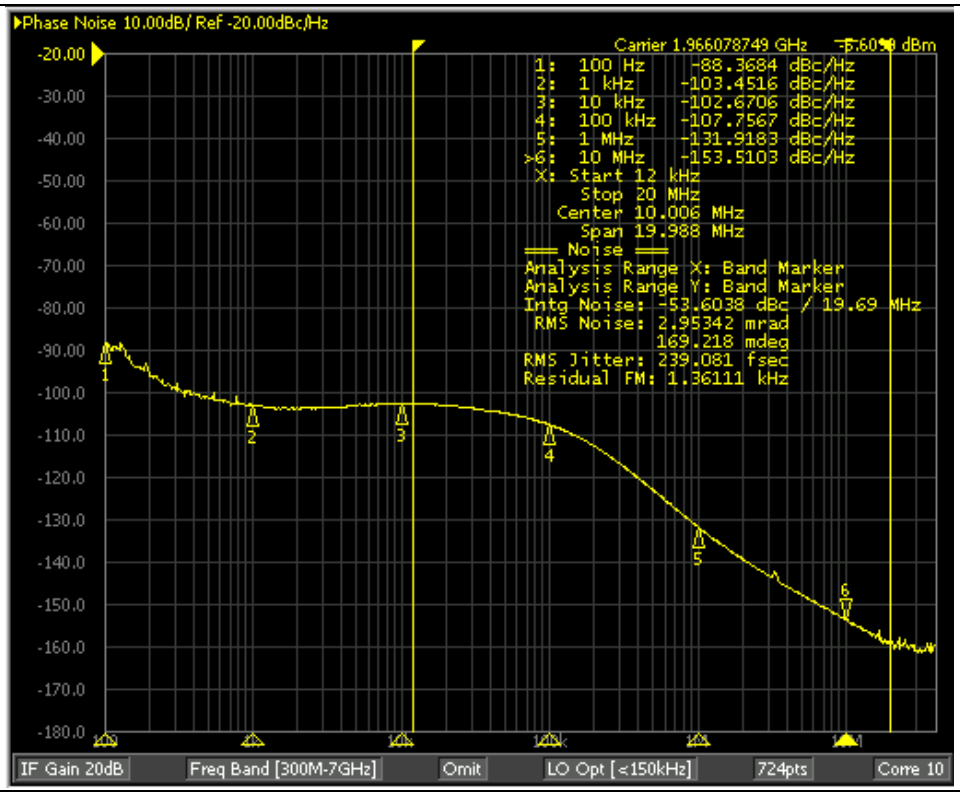
Evaluation Board Revision v1.0 Errata

- SYNC* is labeled on the PCB as SYNC, however the logic of SYNC* is still active low!

Results

Phase Noise

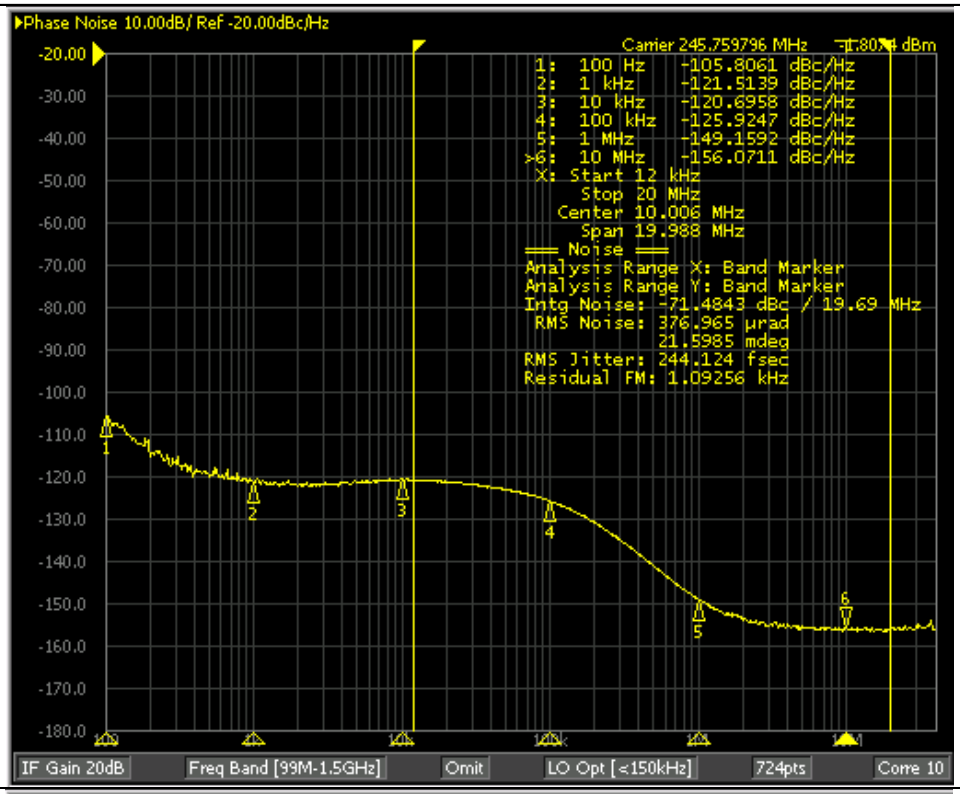
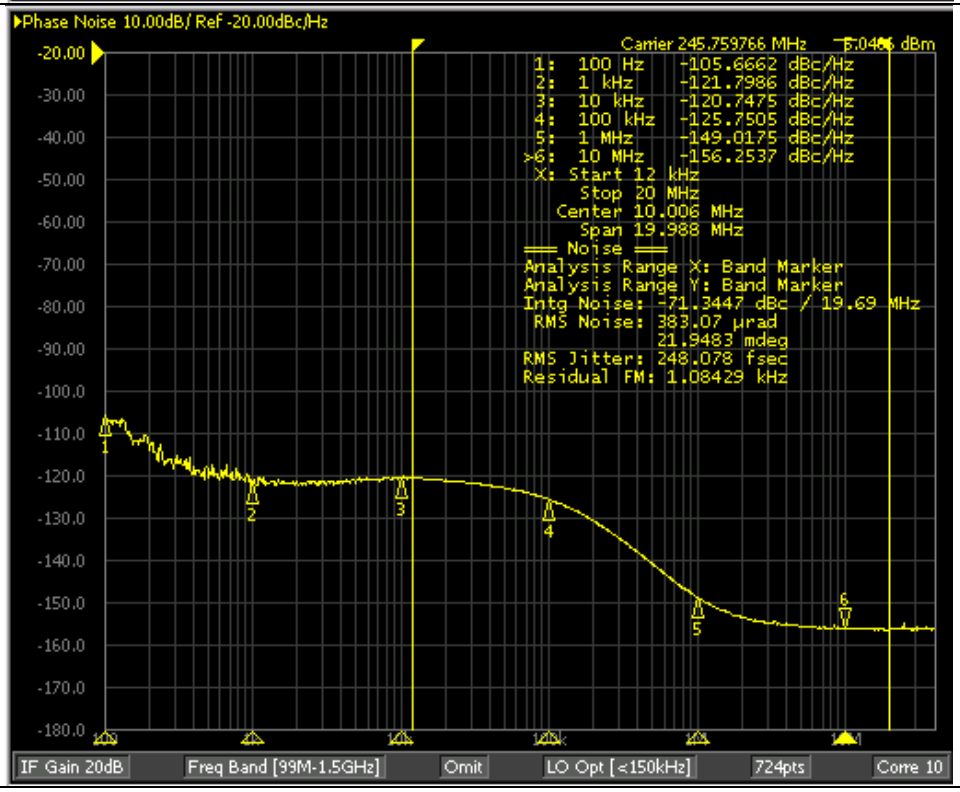
Output Frequency = 1966.08 MHz
Internal VCO, Fout output



Reference source is on board 12.288 MHz crystal

Below ~100 Hz phase noise is dominated by the crystal
100 Hz – 20 MHz integrated RMS jitter = 256 fs
12 kHz – 20 MHz integrated RMS jitter = 239 fs (shown)

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LVDS output CLKout0 VCO Frequency = 1966.08 MHz, VCO_DIV=2, CLKout0_div=4 LVDS output (245.76 MHz)		Output is measured with a Minicircuits ADT2-1T balun. Reference source is on board 12.288 MHz crystal Below –100 Hz phase noise is dominated by the crystal 100 Hz – 20 MHz integrated RMS jitter = 261 fs 12 kHz – 20 MHz integrated RMS jitter = 244 fs (shown)
LVPECL output CLKout4 VCO Frequency = 1966.08 MHz, VCO_DIV=2, CLKout4_div=4 LVPECL output (245.76 MHz)		Output is measured with a Minicircuits ADT2-1T balun. Reference source is on board 12.288 MHz crystal Below –100 Hz phase noise is dominated by the crystal 100 Hz – 20 MHz integrated RMS jitter = 265 fs 12 kHz – 20 MHz integrated RMS jitter = 248 fs (shown)

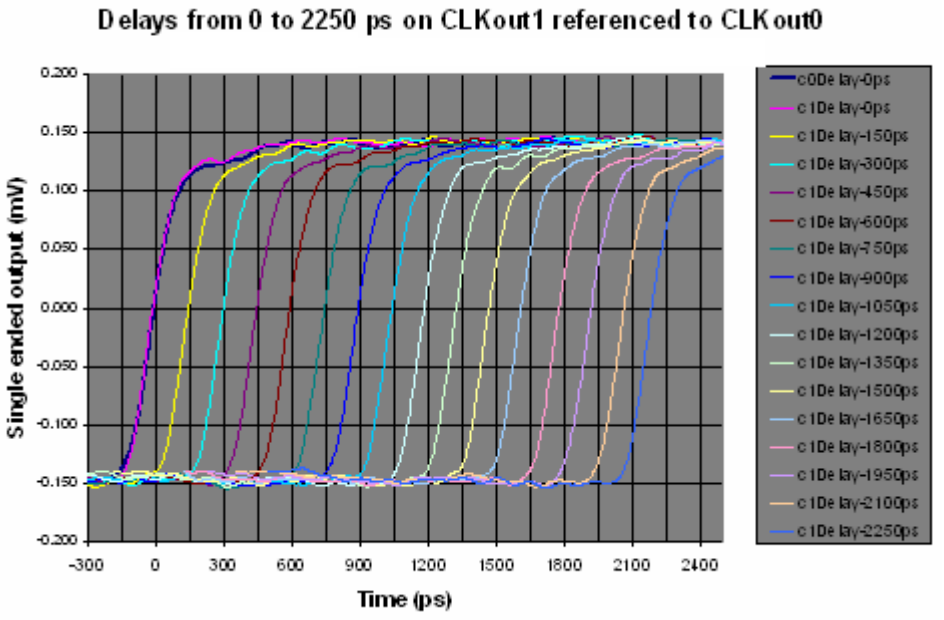
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Delays

These delay measurements illustrate how skew errors due to different length traces may be tuned out.
The delay may be adjusted in steps of 150 ps.



Delays 150, 300, 450, 600, 750



CLKout0_DLY = 0 ps

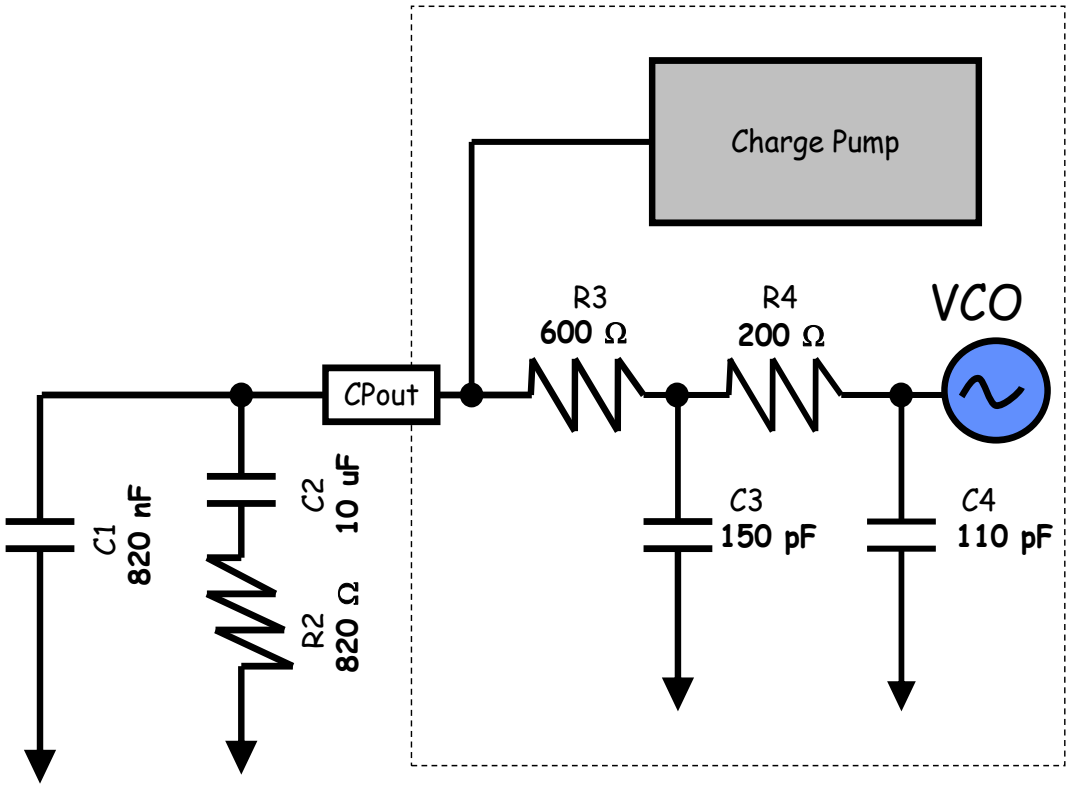
CLKout1_DLY = all delays programmed: 0, 150, 300, 450, 600, 750, 900, 1050, 1200, 1350, 1500, 1650, 1800, 1950, 2100, and 2250 ps

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VCO Performance

The internal VCO performance is measured by using a narrow bandwidth loop filter. By default the narrow loop bandwidth filter is stuffed as Loop Filter #2 in positions C1_AUX, C2_AUX, C2p_AUX, and R2_AUX and has a narrow loop bandwidth.
See the Loop Filter section in Board Options for more detail about switching between the two different loop filters.

Loop Filter			
Phase Margin		**K**	100 uA
Loop Bandwidth	<100 Hz	**Fcomp**	1.2288 MHz
Crystal Frequency	12.288 MHz	**Output Frequency**	1843 to 2160 MHz
Supply Voltage	3.3 Volts	**VCO Gain**	20 MHz/Volt

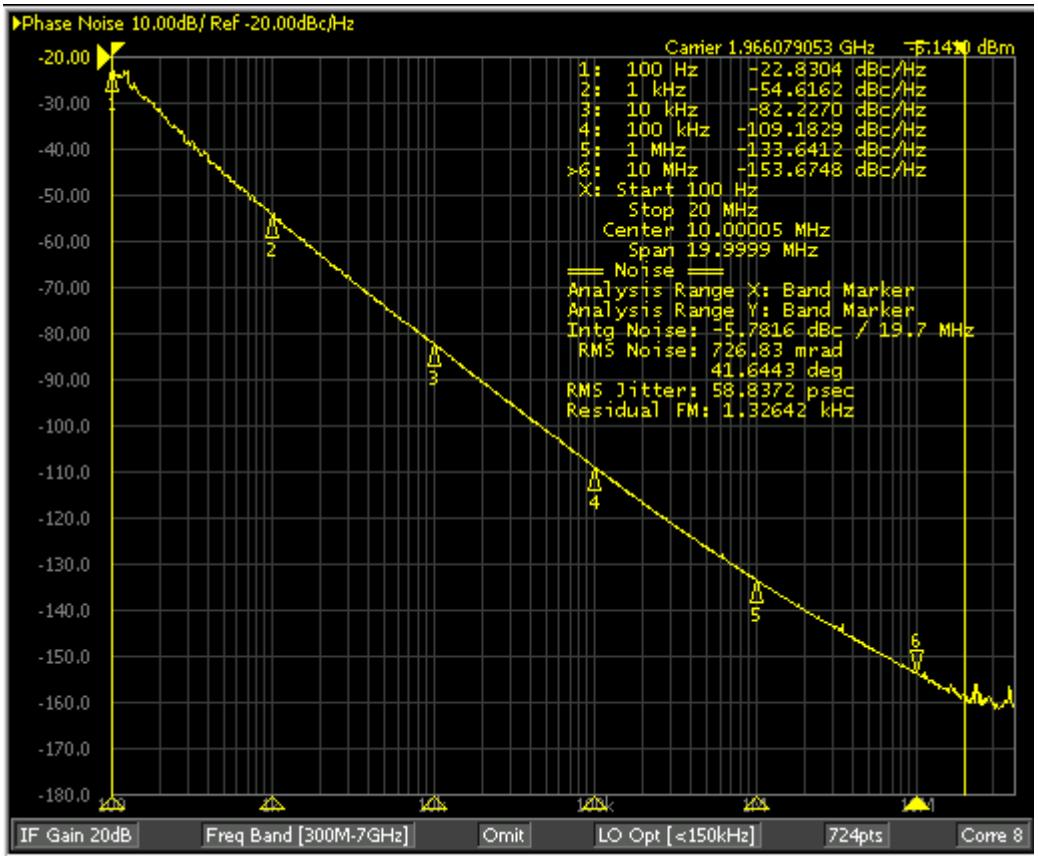


This loop filter is located on the top side of the PCB and is selected by placing a 0 ohm resistor on pad R5.

This loop filter has been designed with a very small loop bandwidth to minimize the PLL from interacting with the noise of the VCO to permit a VCO phase noise measurement.

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VCO Phase Noise - Narrow Loop Bandwidth



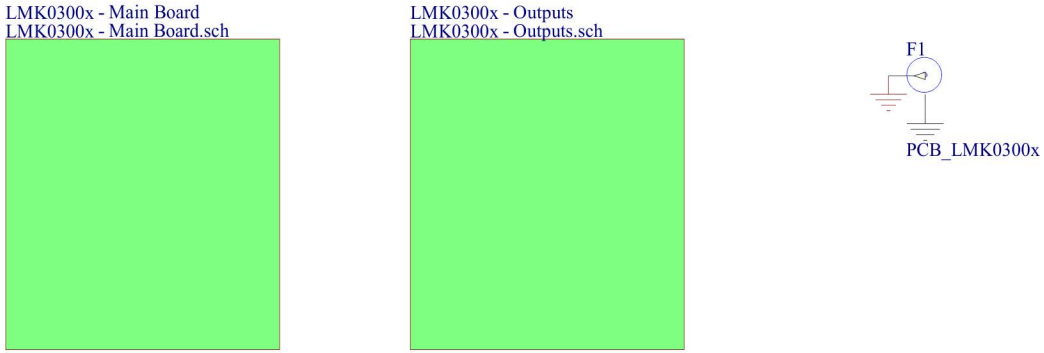
This plot shows the noise of the VCO at 1966.08 MHz using a 614.4 MHz Phase Detector Frequency. An external oscillator was used for this plot, since the VCO noise dominates, reference oscillator noise is not critical.

The loop bandwidth has been minimized so that the VCO is the dominant noise contributor.

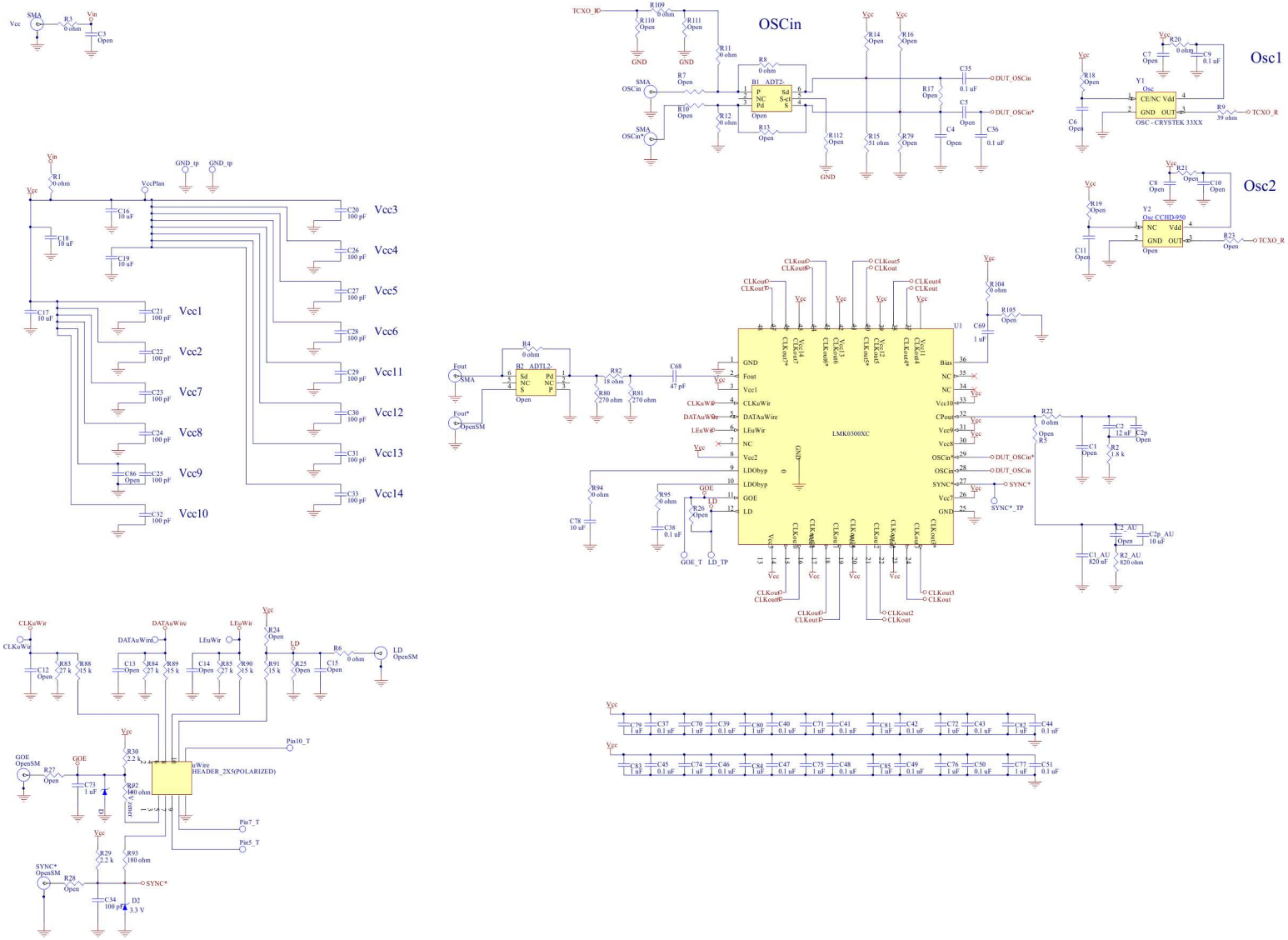
100 Hz – 20 MHz integrated RMS jitter = 58.8 ps (shown)

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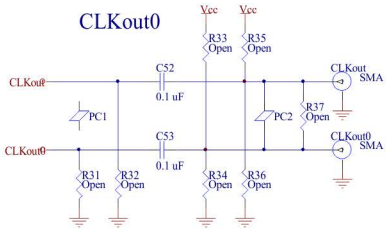
Appendix A: Schematics

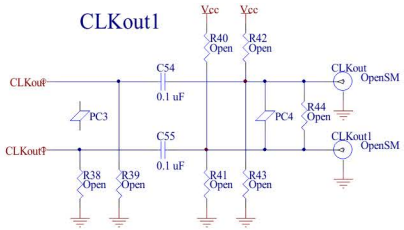


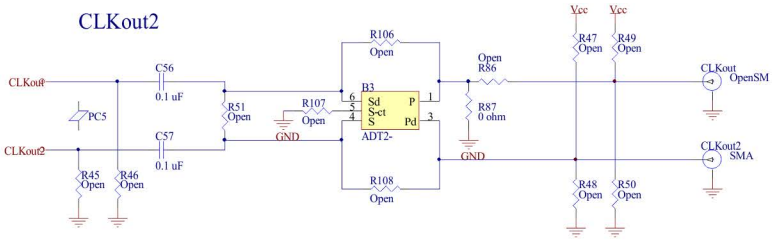
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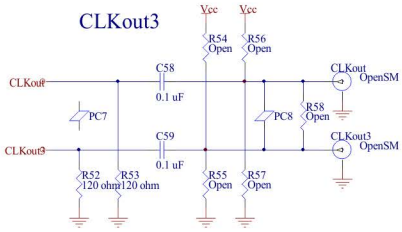


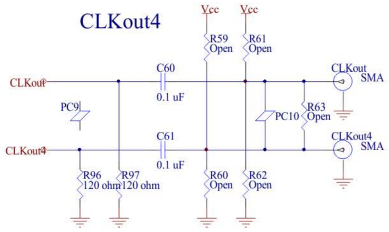
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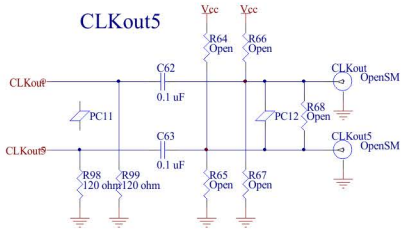


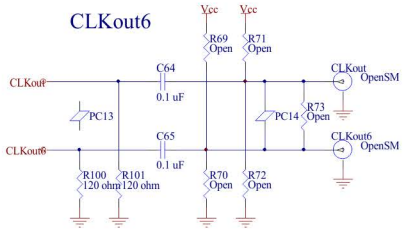


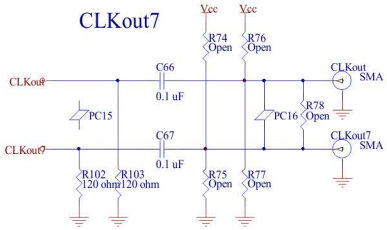












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Appendix B: Bill of Materials

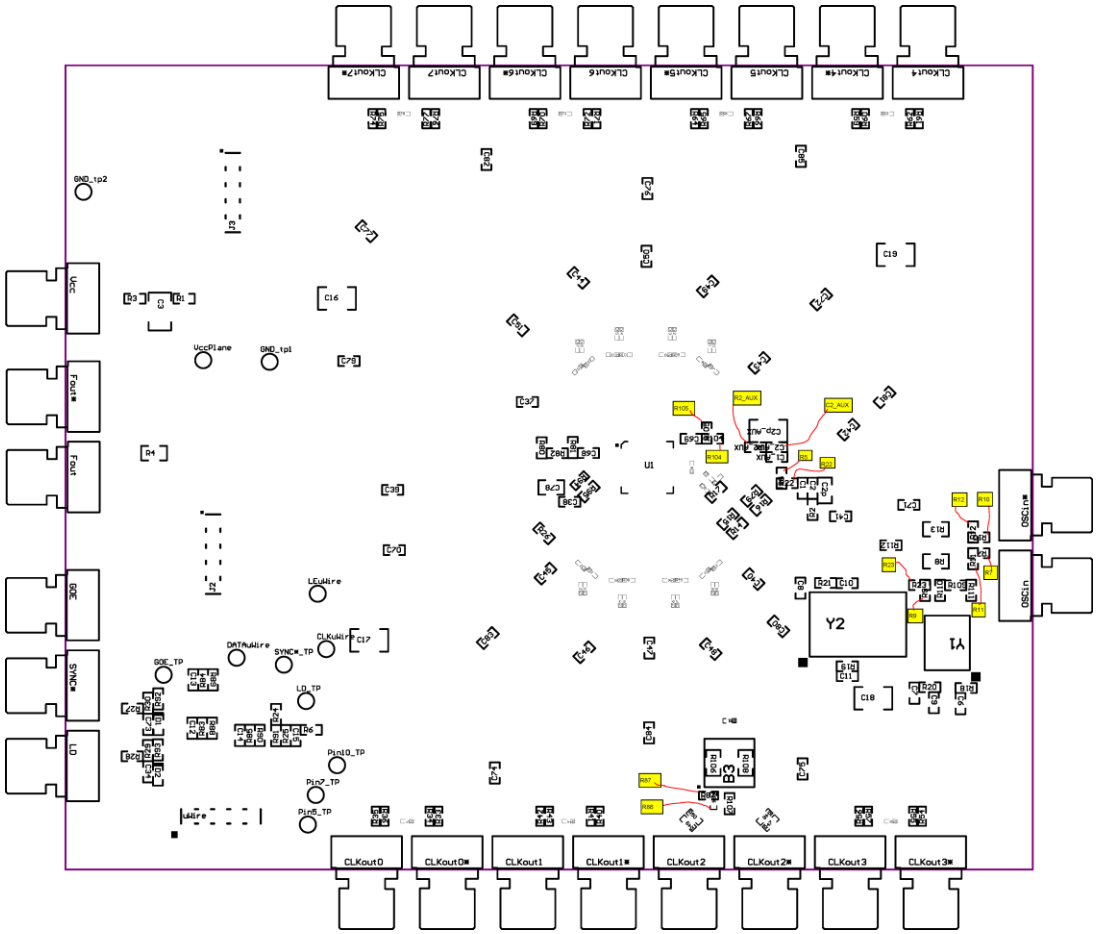
Part	Manufacturer	Part Number	Qnt	Identifier
Capacitors				
47 pF	Kemet	C0603C470J5GAC	1	C68
100 pF	Kemet	C0402C101J5GAC	14	C20, C21, C22, C23, C24, C25, C26, C27, C28, C29, C30, C31, C32, C33
100 pF	Kemet	C0603C101J5GAC	1	C34
12 nF	Kemet	C0603C123K1RACTU	1	C2
0.1 uF	Kemet	C0603C104J3RAC	16	C9, C37, C38, C39, C40, C41, C42, C43, C44, C45, C46, C47, C48, C49, C50, C51
0.1 uF	Kemet	C0402C104J4RAC	18	C35, C36, C52, C53, C54, C55, C56, C57, C58, C59, C60, C61, C62, C63, C64, C65, C66, C67
820 nF	Kemet	C0603C824K8PAC	1	C1_AUX
1 uF	Kemet	C0603C105K8VAC	16	C69, C70, C71, C72, C73, C74, C75, C76, C77, C79, C80, C81, C82, C83, C84, C85
10 uF	Kemet	C0805C106K9PAC	5	C2p_AUX, C16, C17, C18, C19
10 uF	Kemet	C0805C106K9PAC	1	C78
Resistors				
0 ohm	Vishay	CRCW0603000ZRT1	10	R1, R3, R6, R11, R12, R20, R22, R95, R104, R109
0 ohm	Yageo	RC0805JR-070RL	2	R4, R8
0 ohm	Vishay	CRCW0603000ZRT1	2	R87, R94
18 ohm	Vishay	CRCW0603180JRT1	1	R82
39 ohm	Vishay	CRCW0603390JRT1	1	R9
51 ohm	Vishay/Dale	CRCW060351R0JNEA	1	R15
120 ohm	Vishay	CRCW0402120RJNED	10	R52, R53, R96, R97, R98, R99, R100, R101, R102, R103
180 ohm	Vishay	CRCW0603181JRT1	2	R92, R93
270 ohm	Vishay	CRCW0603271JRT1	2	R80, R81
820 ohm	Vishay	CRCW0603821JRT1	1	R2_AUX
1.8 k	Vishay/Dale	CRCW06031K80JNEA	1	R2
2.2 k	Vishay/Dale	CRCW06032K20JNEA	2	R29, R30
15 k	Vishay	CRCW0603153JRT1	4	R88, R89, R90, R91
27 k	Vishay	CRCW0603273JRT1	3	R83, R84, R85

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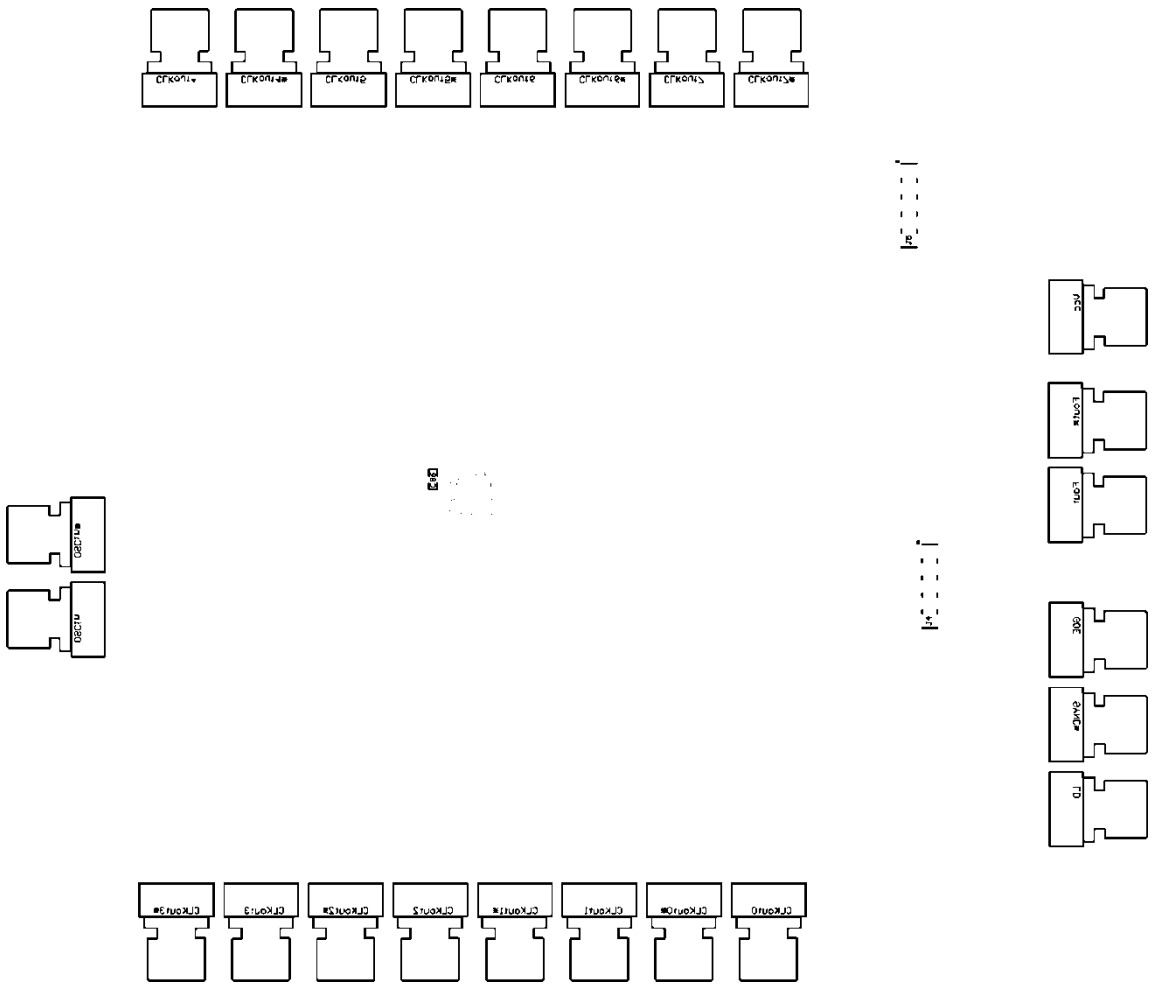
Other				
LMK030xxC	Texas Instruments	LMK03000C/LMK03001C / LMK03002C/LMK03033C	1	U1
OSC - CRYSTEK 33xx	Crystek	C3391-19.440	1	Y1
ADT2-1T	Minicircuits	ADT2-1T	1	B3
SMA	Johnson Components	142-0701-851	11	CLKout0, CLKout0*, CLKout2*, CLKout4, CLKout4*, CLKout7, CLKout7*, Fout, OSCin, OSCin*, Vcc
3.3 V zener	Comchip	CZRU52C3V3	2	D1, D2
PCB_LMK0300x	Printed Circuits Corp	PCB_LMK0300x rev 1.1, 6-16-2007	1	F1
HEADER_2X5(POLARIZED)	FCI Electronics	52601-S10-8	1	uWire
SPCS-8	SPC Technology	SPCS-8	4	Standoffs in the four corners (insert from bottom)
Open				
Open	-	Open	2	B1, B2
Open	-	603	32	C1, C2_AUX, C6, C7, C8, C10, C11, C12, C13, C14, C15, R5, R7, R10, R14, R16, R17, R18, R19, R21, R23, R24, R25, R26, R27, R28, R79, R105, R107, R110, R111, R112
Open	-	805	1	C2p
Open	-	Open	1	C3
Open	-	402	16	C4, C5, R31, R32, R37, R38, R39, R44, R45, R46, R51, R58, R63, R68, R73, R78
Open	-	603	34	C86, R33, R34, R35, R36, R40, R41, R42, R43, R47, R48, R49, R50, R54, R55, R56, R57, R59, R60, R61, R62, R64, R65, R66, R67, R69, R70, R71, R72, R74, R75, R76, R77, R86
OpenSMA	-	Open	13	CLKout1, CLKout1*, CLKout2, CLKout3, CLKout3*, CLKout5, CLKout5*, CLKout6, CLKout6*, Fout*, GOE, LD, SYNC*
Open	-	HEADER_2X5	2	J2, J4
Open	-	HEADER_2X5	2	J3, J5
Open	-	805	3	R13, R106, R108
Open	-	Open	1	Y2

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Appendix C: Build Diagram



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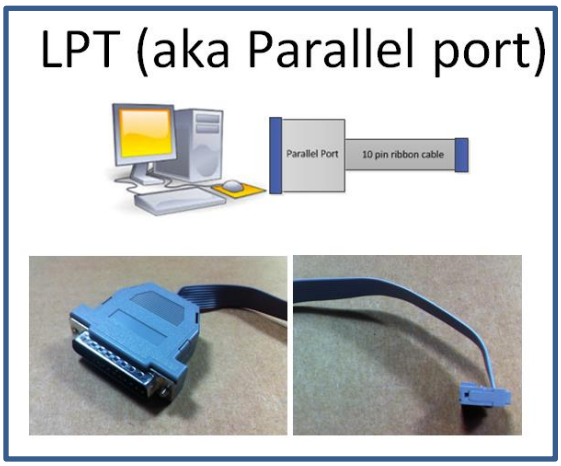


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Appendix D: Quick Start on EVM Communication

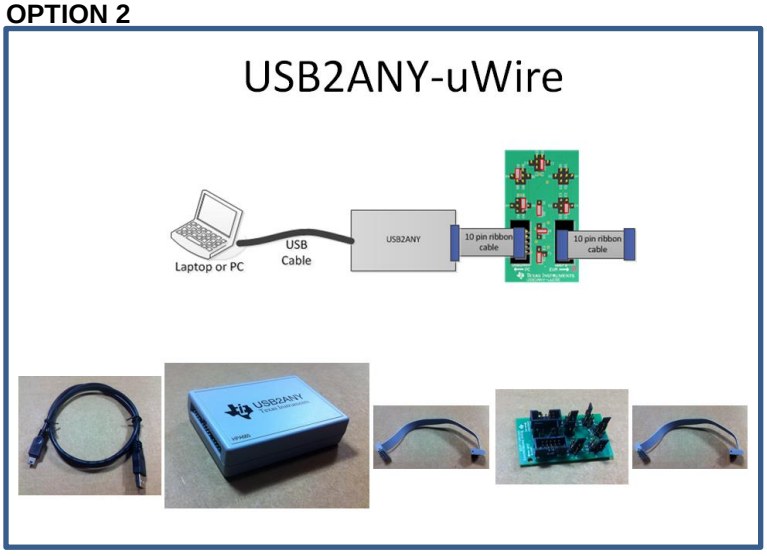
Codeloader is the software used to communicate with the EVM (Please download the latest version from TI.com - http://www.ti.com/tool/codeloader). This EVM can be controlled through the uWire interface on board. There are two options in communicating with the uWire interface from the computer.

OPTION 1



Open Codeloader.exe → Click “Select Device” → Click “Port Setup” tab → Click “LPT” (in Communication Mode)

OPTION 2



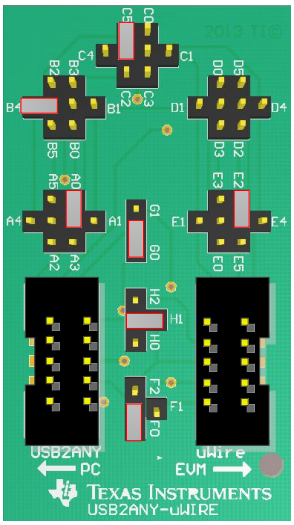
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The Adapter Board

This table describes the pins configuration on the adapter board for each EVM board (See examples below table)

EVM	Jumper Bank								Code Loader Configuration
	A	B	C	D	E	F	G	H	
LMX2581	A4	B1	C2		E5	F1	G1	H1	BUFEN (pin 1), Trigger (pin 7)
LMX2541	A4		C3		E4	F1	G1	H1	CE (pin 1), Trigger (pin 10)
LMK0400x	A0		C3		E5	F1	G1	H1	GOE (pin 7)
LMK01000	A0		C1		E5	F1	G1	H1	GOE (pin 7)
LMK030xx	A0		C1		E5	F1	G1	H1	SYNC (pin 7)
LMK02000	A0		C1		E5	F1	G1	H1	SYNC (pin 7)
LMK0480x	A0	B2	C3		E5	F0	G0	H1	Status_CLKin1 (pin 3)
LMK04816/4906	A0	B2	C3		E5	F0	G0	H1	Status_CLKin1 (pin 3)
LMK01801	A0	B4	C5		E2	F0	G0	H1	Test (pin 3), SYNC0 (pin 10)
LMK0482x (prelease)	A0	B5	C3	D2	E4	F0	G0	H1	CLKin1_SEL (pin 6), Reset (pin 10)
LMX2531	A0				E5	F2	G1	H2	Trigger (pin 1)
LMX2485/7	A0		C1		E5	F2	G1	H0	ENOSC (pin 7), CE (pin 10)
LMK03200	A0				E5	F0	G0	H1	SYNC (pin 7)
LMK03806	A0		C1		E5	F0	G0	H1	
LMK04100	A0		C1		E5	F1	G1	H1	

Example adapter configuration (LMK01801)



Open Codeloader.exe → Click “Select Device” → Click “Port Setup” Tab → Click “USB” (in Communication Mode)

**Remember to also make modifications in “Pin Configuration” Section according to Table above.*

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