LMH6715 Dual Wideband Video Op Amp

Check for Samples: LMH6715

FEATURES

- **T_A = 25°C, R_L = 100Ω, Typical Values Unless Specified.**
- **Very Low Diff. Gain, Phase: 0.02%, 0.02°**
- **Wide Bandwidth: 480MHz (A_V = +1V/V); 400MHz (A_V = +2V/V)**
- **0.1dB Gain Flatness to 100MHz**
- **Low Power: 5.8mA/Channel**
- **−70dB Channel-to-Channel Crosstalk (10MHz)**
- **Fast Slew Rate: 1300V/µs**
- **Unity Gain Stable**
- **Improved Replacement for CLC412**

APPLICATIONS

- **HDTV, NTSC & PAL Video Systems**
- **Video Switching and Distribution**
- **IQ Amplifiers**
- **Wideband Active Filters**
- **Cable Drivers**
- **DC Coupled Single-to-Differential Conversions**

DESCRIPTION

The LMH6715 combines TI's VIP10 high speed complementary bipolar process with TI's current feedback topology to produce a very high speed dual op amp. The LMH6715 provides 400MHz small signal bandwidth at a gain of +2V/V and 1300V/µs slew rate while consuming only 5.8mA per amplifier from ±5V supplies.

The LMH6715 offers exceptional video performance with its 0.02% and 0.02° differential gain and phase errors for NTSC and PAL video signals while driving up to four back terminated 75Ω loads. The LMH6715 also offers a flat gain response of 0.1dB to 100MHz and very low channel-to-channel crosstalk of −70dB at 10MHz. Additionally, each amplifier can deliver 70mA of output current. This level of performance makes the LMH6715 an ideal dual op amp for high density, broadcast quality video systems.

The LMH6715's two very well matched amplifiers support a number of applications such as differential line drivers and receivers. In addition, the LMH6715 is well suited for Sallen Key active filters in applications such as anti-aliasing filters for high speed A/D converters. Its small 8-pin SOIC package, low power requirement, low noise and distortion allow the LMH6715 to serve portable RF applications such as IQ channels.

Differential Gain & Phase with Multiple Video Loads

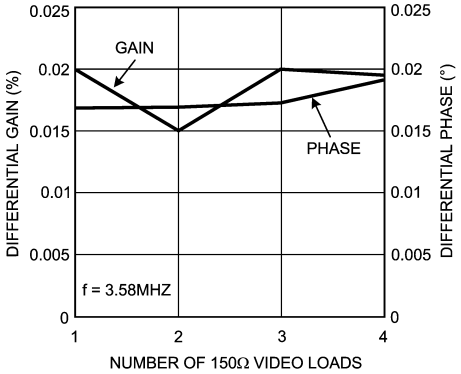


Figure 1.

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Frequency Response vs. V_{OUT}

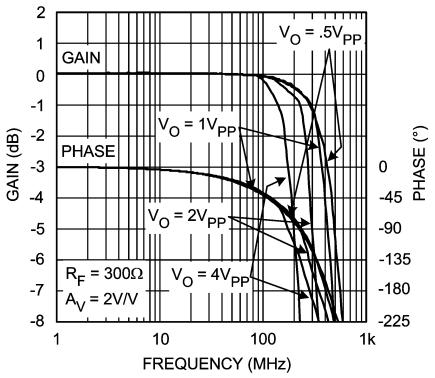


Figure 2.

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

Absolute Maximum Ratings(1)(2)

ESD Tolerance(3)	Human Body Model	2000V
	Machine Model	150V
V_{CC}		±6.75V
I_{OUT}		See(4)
Common-Mode Input Voltage		±V_{CC}
Differential Input Voltage		2.2V
Maximum Junction Temperature		+150°C
Storage Temperature Range		−65°C to +150°C
Lead Temperature (Soldering 10 sec)		+300°C

(1) Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Operating Ratings indicate conditions for which the device is intended to be functional, but specific performance is not ensured. For ensured specifications, see the Electrical Characteristics tables.
(2) If Military/Aerospace specified devices are required, please contact the Texas Instruments Sales Office/ Distributors for availability and specifications.
(3) Human body model, 1.5kΩ in series with 100pF. Machine model, 0Ω In series with 200pF.
(4) The maximum output current (I_{OUT}) is determined by device power dissipation limitations. See the POWER DISSIPATION section for more details.

Operating Ratings

Thermal Resistance		
Package	(θ_{JC})	(θ_{JA})
SOIC	65°C/W	145°C/W
Operating Temperature Range		−40°C to +85°C
Nominal Operating Voltage		±5V to ±6V

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Electrical Characteristics(1)

A_V = +2, R_F = 500Ω, V_{CC} = ±5 V, R_L = 100Ω; unless otherwise specified. **Boldface** limits apply at the temperature extremes.

Symbol	Parameter	Conditions	Min	Typ	Max	Units
Frequency Domain Response						
SSBW	-3dB Bandwidth	V_{OUT} < 0.5V_{PP}, R_F = 300Ω	280	400		MHz
LSBW	-3dB Bandwidth	V_{OUT} < 4.0V_{PP}, R_F = 300Ω		170		MHz
	Gain Flatness	V_{OUT} < 0.5V_{PP}				
GFP	Peaking	DC to 100MHz, R_F = 300Ω		0.1		dB
GFR	Rolloff	DC to 100MHz, R_F = 300Ω		0.1		dB
LPD	Linear Phase Deviation	DC to 100MHz, R_F = 300Ω		0.25		deg
DG	Differential Gain	R_L = 150Ω, 4.43MHz		0.02		%
DP	Differential Phase	R_L = 150Ω, 4.43MHz		0.02		deg
Time Domain Response						
Tr	Rise and Fall Time	0.5V Step		1.4		ns
		4V Step		3		ns
Ts	Settling Time to 0.05%	2V Step		12		ns
OS	Overshoot	0.5V Step		1		%
SR	Slew Rate	2V Step		1300		V/µs
Distortion And Noise Response						
HD2	2nd Harmonic Distortion	2V_{PP}, 20MHz		−60		dBc
HD3	3rd Harmonic Distortion	2V_{PP}, 20MHz		−75		dBc
	Equivalent Input Noise					
V_N	Non-Inverting Voltage	>1MHz		3.4		nV/√Hz
I_N	Inverting Current	>1MHz		10.0		pA/√Hz
I_{NN}	Non-Inverting Current	>1MHz		1.4		pA/√Hz
SNF	Noise Floor	>1MHz		−153		dB_{1Hz}
XTLKA	Crosstalk	Input Referred 10MHz		−70		dB
Static, DC Performance						
V_{IO}	Input Offset Voltage			±2	±6 **±8**	mV
DV_{IO}	Average Drift			±30		µV/°C
I_{BN}	Input Bias Current	Non-Inverting		±5	±12 **±20**	µA
DI_{BN}	Average Drift			±30		nA/°C
I_{BI}	Input Bias Current	Inverting		±6	±21 **±35**	µA
DI_{BI}	Average Drift			±20		nA/°C
PSRR	Power Supply Rejection Ratio	DC	46 **44**	60		dB
CMRR	Common Mode Rejection Ratio	DC	50 **47**	56		dB
I_{CC}	Supply Current per Amplifier	R_L = ∞	4.7 **4.1**	5.8	7.6 **8.1**	mA
Miscellaneous Performance						
R_{IN}	Input Resistance	Non-Inverting		1000		kΩ
C_{IN}	Input Capacitance	Non-Inverting		1.0		pF
R_{OUT}	Output Resistance	Closed Loop		.06		Ω

(1) Electrical Table values apply only for factory testing conditions at the temperature indicated. Factory testing conditions result in very limited self-heating of the device such that $T_J = T_A$. No specification of parametric performance is indicated in the electrical tables under conditions of internal self heating where $T_J > T_A$. See Application Section for information on temperature de-rating of this device." Min/Max ratings are based on product characterization and simulation. Individual parameters are tested as noted.

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Electrical Characteristics[1] (continued)

A_V = +2, R_F = 500Ω, V_{CC} = ±5 V, R_L = 100Ω; unless otherwise specified. **Boldface** limits apply at the temperature extremes.

Symbol	Parameter	Conditions	Min	Typ	Max	Units
V_O	Output Voltage Range	R_L = ∞		±4.0		V
V_{OL}		R_L = 100Ω	±3.5 **±3.4**	±3.9		V
CMIR	Input Voltage Range	Common Mode		±2.2		V
I_O	Output Current			70		mA

Connection Diagram

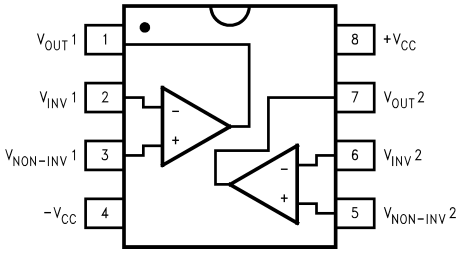


Figure 3. 8-Pin SOIC, Top View

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Typical Performance Characteristics

(T_A = 25°C, V_{CC} = ±5V, A_V = ±2V/V, R_F = 500Ω, R_L = 100Ω, unless otherwise specified).

Non-Inverting Freq·uency Response

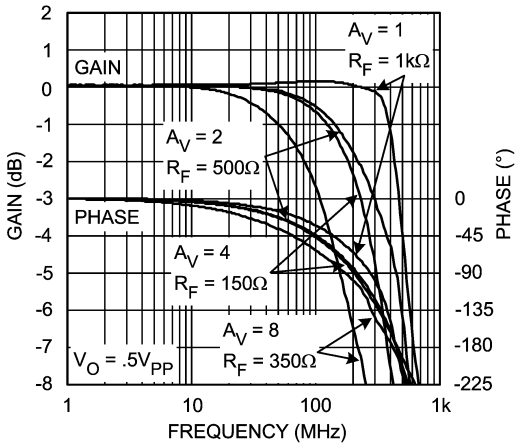


Figure 4.

Inverting Frequency Response

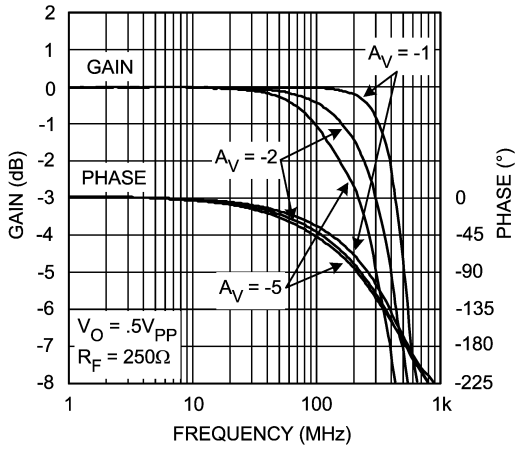


Figure 5.

Non-Inverting Frequency Response vs. V_{OUT}

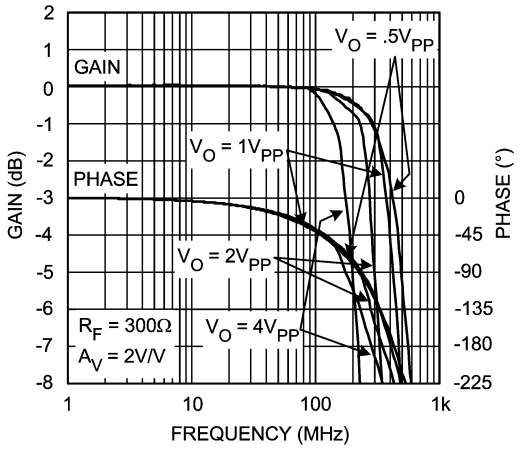


Figure 6.

Small Signal Channel Matching

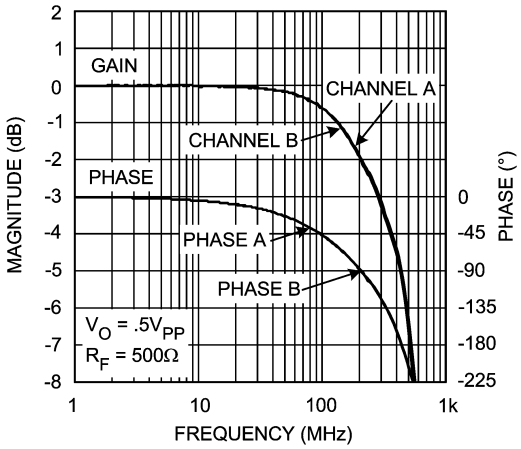


Figure 7.

Frequency Response vs. Load Resistance

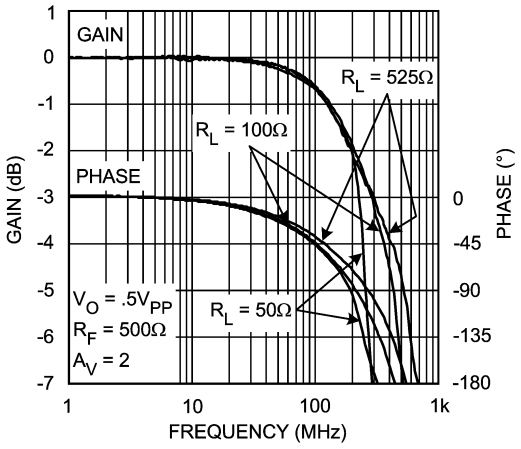


Figure 8.

Non-Inverting Frequency Response vs. R_F

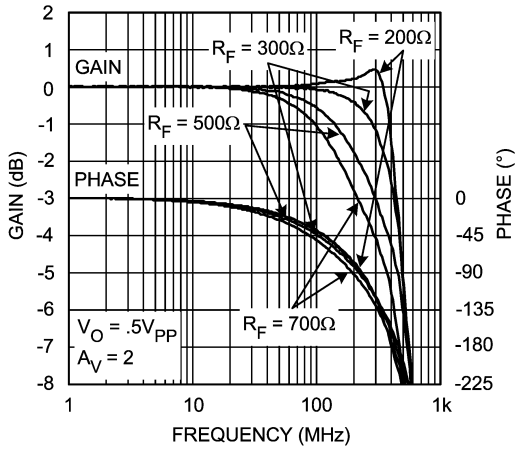


Figure 9.

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Typical Performance Characteristics (continued)

(T_A = 25°C, V_{CC} = ±5V, A_V = ±2V/V, R_F = 500Ω, R_L = 100Ω, unless otherwise specified).

Small Signal Pulse Response

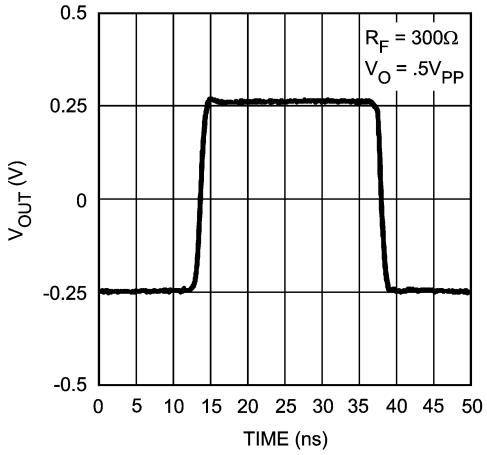


Figure 10.

Large Signal Pulse Response

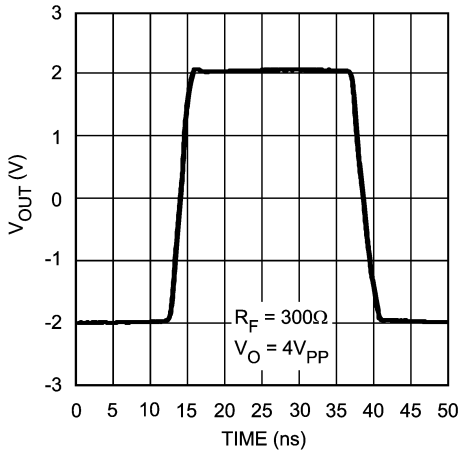


Figure 11.

Input-Referred Crosstalk

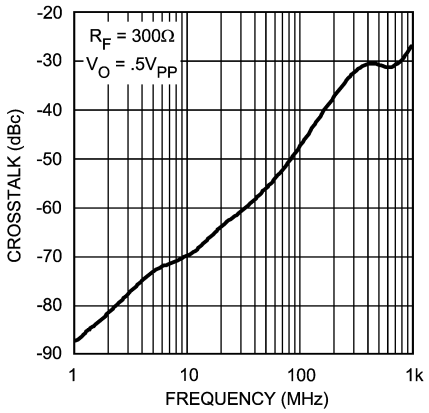


Figure 12.

Settling Time vs. Accuracy

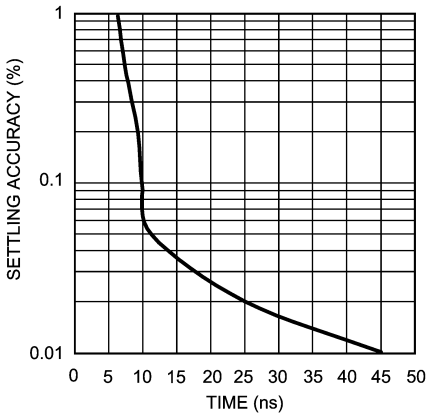


Figure 13.

−3dB Bandwidth vs. V_{OUT}

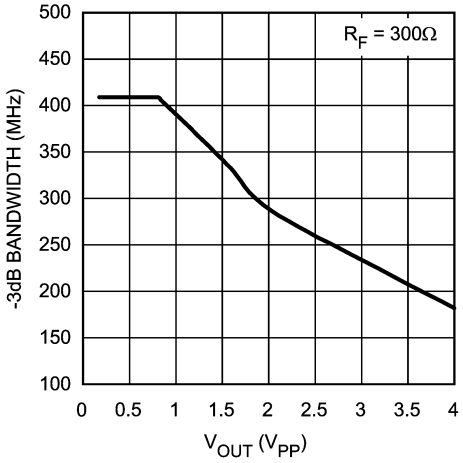


Figure 14.

DC Errors vs. Temperature

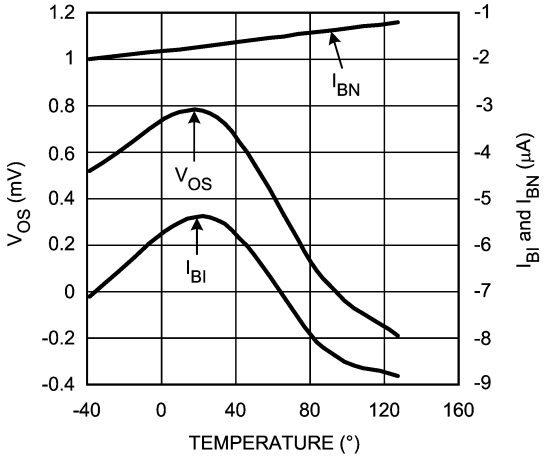


Figure 15.

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Typical Performance Characteristics (continued)

(T_A = 25°C, V_{CC} = ±5V, A_V = ±2V/V, R_F = 500Ω, R_L = 100Ω, unless otherwise specified).

Open Loop Transimpedance, Z(s)

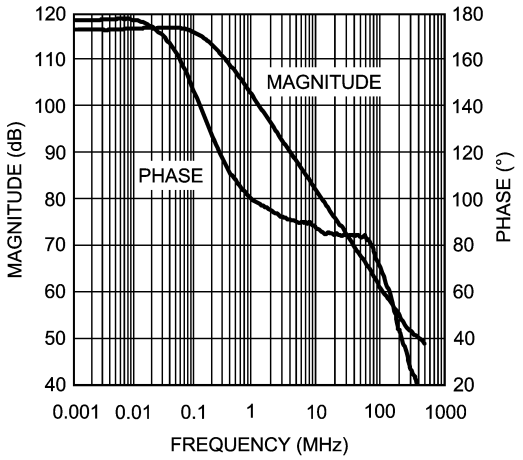


Figure 16.

Equivalent Input Noise vs. Frequency

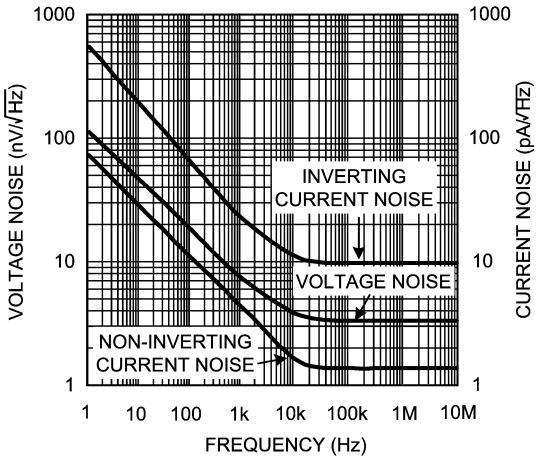


Figure 17.

Differential Gain & Phase vs. Load

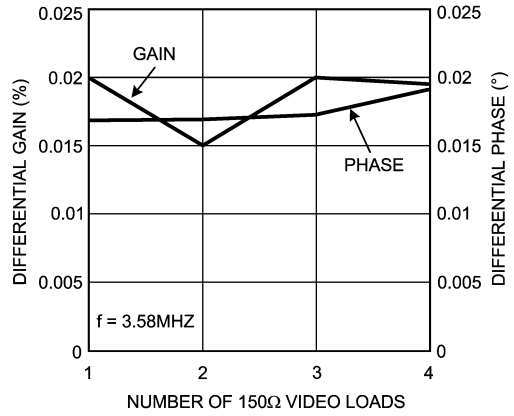


Figure 18.

Differential Gain vs. Frequency

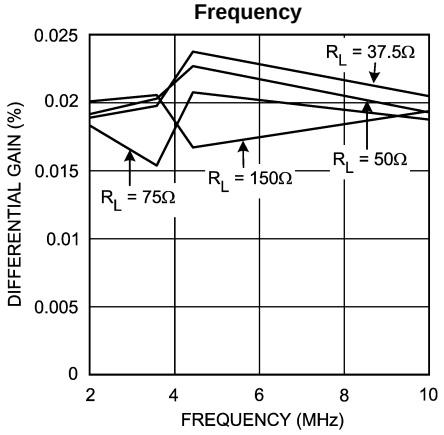


Figure 19.

Differential Phase vs. Frequency

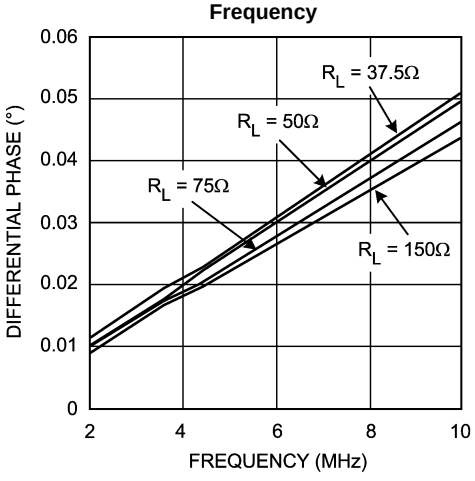


Figure 20.

Gain Flatness & Linear Phase Deviation

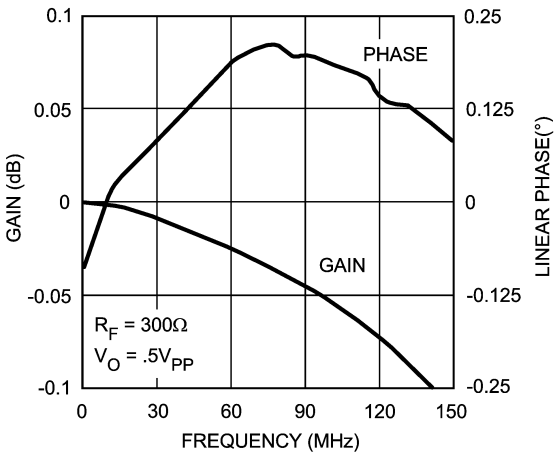


Figure 21.

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Typical Performance Characteristics (continued)

(T_A = 25°C, V_{CC} = ±5V, A_V = ±2V/V, R_F = 500Ω, R_L = 100Ω, unless otherwise specified).

2nd Harmonic Distortion vs. Output Voltage

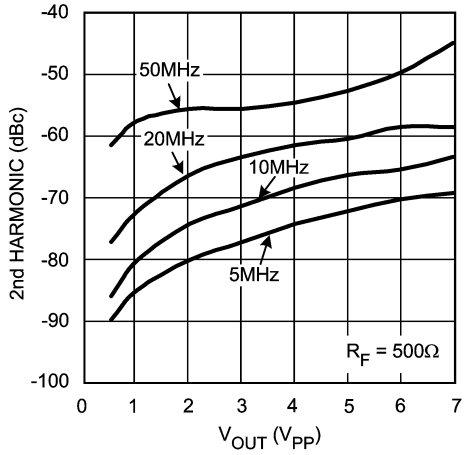


Figure 22.

3rd Harmonic Distortion vs. Output Voltage

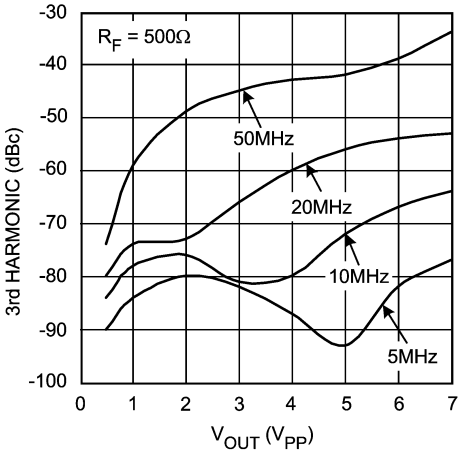


Figure 23.

Closed Loop Output Resistance

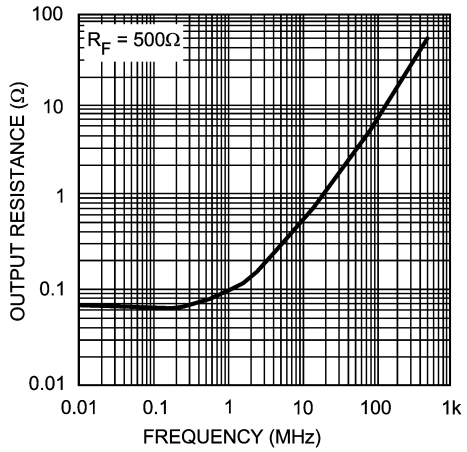


Figure 24.

PSRR & CMRR

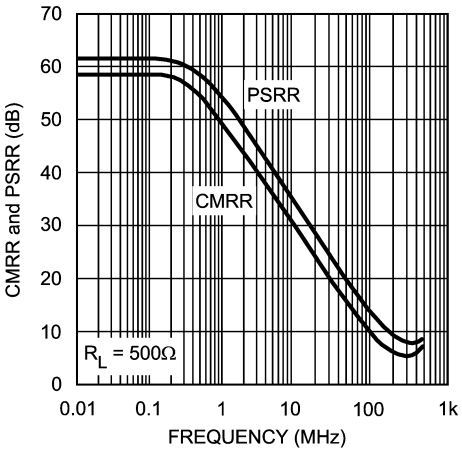


Figure 25.

Suggested R_S vs. C_L

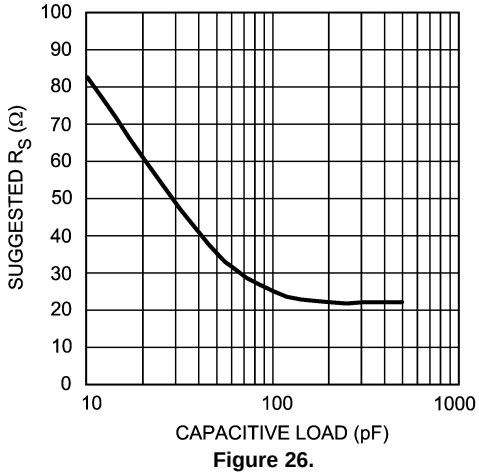


Figure 26.

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APPLICATION SECTION

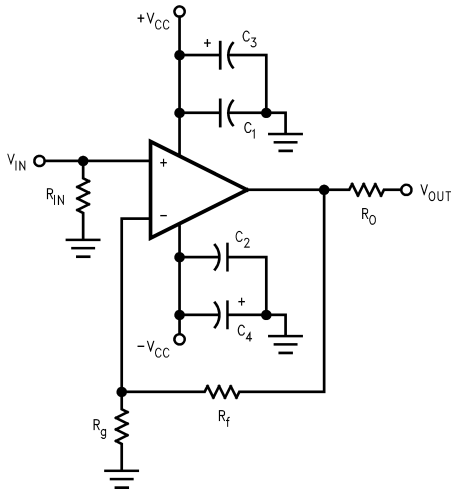


Figure 27. Non-Inverting Configuration with Power Supply Bypassing

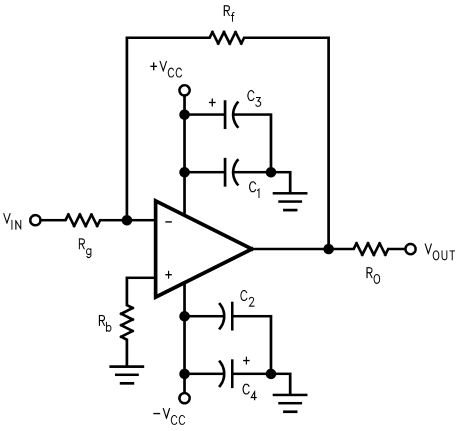


Figure 28. Inverting Configuration with Power Supply Bypassing

Application Introduction

Offered in an 8-pin package for reduced space and cost, the wideband LMH6715 dual current-feedback op amp provides closely matched DC and AC electrical performance characteristics making the part an ideal choice for wideband signal processing. Applications such as broadcast quality video systems, IQ amplifiers, filter blocks, high speed peak detectors, integrators and transimedance amplifiers will all find superior performance in the LMH6715 dual op amp.

FEEDBACK RESISTOR SELECTION

One of the key benefits of a current feedback operational amplifier is the ability to maintain optimum frequency response independent of gain by using appropriate values for the feedback resistor (R_F). The Electrical Characteristics and Typical Performance plots specify an R_F of 500Ω, a gain of +2V/V and ±5V power supplies (unless otherwise specified). Generally, lowering R_F from it's recommended value will peak the frequency response and extend the bandwidth while increasing the value of R_F will cause the frequency response to roll off faster. Reducing the value of R_F too far below it's recommended value will cause overshoot, ringing and, eventually, oscillation.

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Frequency Response vs. R_F

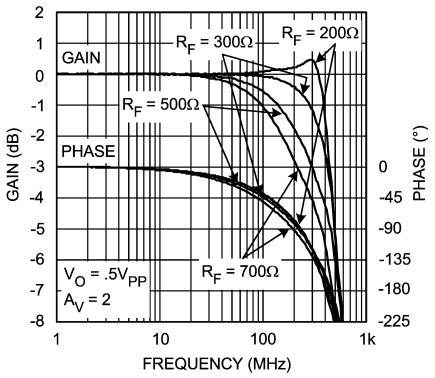


Figure 29.

Figure 29 shows the LMH6715's frequency response as R_F is varied (R_L = 100Ω, A_V = +2). This plot shows that an R_F of 200Ω results in peaking and marginal stability. An R_F of 300Ω gives near maximal bandwidth and gain flatness with good stability, but with very light loads (R_L > 300Ω) the device may show some peaking. An R_F of 500Ω gives excellent stability with good bandwidth and is the recommended value for most applications. Since all applications are slightly different it is worth some experimentation to find the optimal R_F for a given circuit. For more information see Application Note OA-13 (Literature Number SNOA366) which describes the relationship between R_F and closed-loop frequency response for current feedback operational amplifiers.

When configuring the LMH6715 for gains other than +2V/V, it is usually necessary to adjust the value of the feedback resistor. The two plots labeled shown in Figure 30 and Figure 31 provide recommended feedback resistor values for a number of gain selections.

R_F vs. Non-Inverting Gain

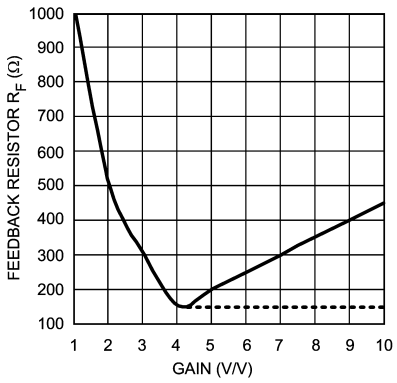


Figure 30.

Both plots show the value of R_F approaching a minimum value (dashed line) at high gains. Reducing the feedback resistor below this value will result in instability and possibly oscillation. The recommended value of R_F is depicted by the solid line, which begins to increase at higher gains. The reason that a higher R_F is required at higher gains is the need to keep R_G from decreasing too far below the output impedance of the input buffer. For the LMH6715 the output resistance of the input buffer is approximately 160Ω and 50Ω is a practical lower limit for R_G. Due to the limitations on R_G the LMH6715 begins to operate in a gain bandwidth limited fashion for gains of ±5V/V or greater.

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R_F vs. Inverting Gain

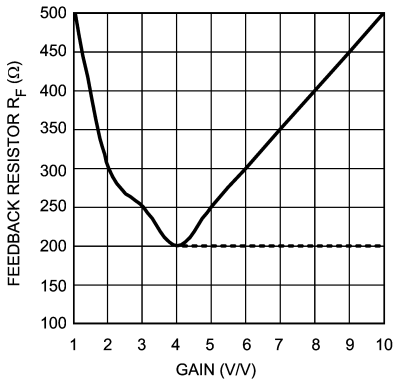


Figure 31.

When using the LMH6715 as a replacement for the CLC412, identical bandwidth can be obtained by using an appropriate value of R_F . The chart "Frequency Response vs. R_F" (see Figure 29) shows that an R_F of approximately 700Ω will provide bandwidth very close to that of the CLC412. At other gains a similar increase in R_F can be used to match the new and old parts.

CIRCUIT LAYOUT

With all high frequency devices, board layouts with stray capacitances have a strong influence over AC performance. The LMH6715 is no exception and its input and output pins are particularly sensitive to the coupling of parasitic capacitances (to AC ground) arising from traces or pads placed too closely (<0.1") to power or ground planes. In some cases, due to the frequency response peaking caused by these parasitics, a small adjustment of the feedback resistor value will serve to compensate the frequency response. Also, it is very important to keep the parasitic capacitance across the feedback resistor to an absolute minimum.

The performance plots in the data sheet can be reproduced using the evaluation boards available from Texas Instruments. The LMH730036 board uses all SMT parts for the evaluation of the LMH6715. The board can serve as an example layout for the final production printed circuit board.

Care must also be taken with the LMH6715's layout in order to achieve the best circuit performance, particularly channel-to-channel isolation. The decoupling capacitors (both tantalum and ceramic) must be chosen with good high frequency characteristics to decouple the power supplies and the physical placement of the LMH6715's external components is critical. Grouping each amplifier's external components with their own ground connection and separating them from the external components of the opposing channel with the maximum possible distance is recommended. The input (R_{IN}) and gain setting resistors (R_F) are the most critical. It is also recommended that the ceramic decoupling capacitor (0.1µF chip or radial-leaded with low ESR) should be placed as closely to the power pins as possible.

POWER DISSIPATION

Follow these steps to determine the Maximum power dissipation for the LMH6715:

1. Calculate the quiescent (no-load) power: $P_{AMP} = I_{CC} (V_{CC} - V_{EE})$

2. Calculate the RMS power at the output stage: $P_O = (V_{CC} - V_{LOAD})(I_{LOAD})$, where V_{LOAD} and I_{LOAD} are the voltage and current across the external load.

3. Calculate the total RMS power: $Pt = P_{AMP} + P_O$

The maximum power that the LMH6715, package can dissipate at a given temperature can be derived with the following equation:

$$Pmax = (150^{o} - Tamb)/ \theta_{JA}$$ (1)

where Tamb = Ambient temperature (°C) and θ_{JA} = Thermal resistance, from junction to ambient, for a given package (°C/W). For the SOIC package θ_{JA} is 145°C/W.

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MATCHING PERFORMANCE

With proper board layout, the AC performance match between the two LMH6715's amplifiers can be tightly controlled as shown in Typical Performance plot labeled “Small-Signal Channel Matching”.

The measurements were performed with SMT components using a feedback resistor of 300Ω at a gain of +2V/V.

The LMH6715's amplifiers, built on the same die, provide the advantage of having tightly matched DC characteristics.

SLEW RATE AND SETTLING TIME

One of the advantages of current-feedback topology is an inherently high slew rate which produces a wider full power bandwidth. The LMH6715 has a typical slew rate of 1300V/µs. The required slew rate for a design can be calculated by the following equation: $SR = 2\pi f V_{pk}$.

Careful attention to parasitic capacitances is critical to achieving the best settling time performance. The LMH6715 has a typical short term settling time to 0.05% of 12ns for a 2V step. Also, the amplifier is virtually free of any long term thermal tail effects at low gains.

When measuring settling time, a solid ground plane should be used in order to reduce ground inductance which can cause common-ground-impedance coupling. Power supply and ground trace parasitic capacitances and the load capacitance will also affect settling time.

Placing a series resistor (R_S) at the output pin is recommended for optimal settling time performance when driving a capacitive load. The Typical Performance plot labeled “R_S and Settling Time vs. Capacitive Load” provides a means for selecting a value of R_S for a given capacitive load.

DC & NOISE PERFORMANCE

A current-feedback amplifier's input stage does not have equal nor correlated bias currents, therefore they cannot be canceled and each contributes to the total DC offset voltage at the output by the following equation:

$$V_{OFFSET} = \pm \left[I_{BN} \times R_S \left[1 + \frac{R_f}{R_g} \right] + V_{IO} \left[1 + \frac{R_f}{R_g} \right] + I_{BI} \times R_f \right] \quad (2)$$

The input resistance is the resistance looking from the non-inverting input back toward the source. For inverting DC-offset calculations, the source resistance seen by the input resistor R_g must be included in the output offset calculation as a part of the non-inverting gain equation. Application note OA-07 (Literature Number SNOA365) gives several circuits for DC offset correction. The noise currents for the inverting and non-inverting inputs are graphed in the Typical Performance plot labeled “Equivalent Input Noise”. A more complete discussion of amplifier input-referred noise and external resistor noise contribution can be found in OA-12 (Literature Number SNOA375).

DIFFERENTIAL GAIN & PHASE

The LMH6715 can drive multiple video loads with very low differential gain and phase errors. Figure 19 and Figure 20 show performance for loads from 1 to 4. The Electrical Characteristics table also specifies performance for one 150Ω load at 4.43MHz. For NTSC video, the performance specifications also apply. Application note OA-24 (Literature Number SNOA370) “Measuring and Improving Differential Gain & Differential Phase for Video”, describes in detail the techniques used to measure differential gain and phase.

I/O VOLTAGE & OUTPUT CURRENT

The usable common-mode input voltage range (CMIR) of the LMH6715 specified in the Electrical Characteristics table of the data sheet shows a range of ±2.2 volts. Exceeding this range will cause the input stage to saturate and clip the output signal.

The output voltage range is determined by the load resistor and the choice of power supplies. With ±5 volts the class A/B output driver will typically drive ±3.9V into a load resistance of 100Ω. Increasing the supply voltages will change the common-mode input and output voltage swings while at the same time increase the internal junction temperature.

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Applications Circuits

SINGLE-TO-DIFFERENTIAL LINE DRIVER

The LMH6715's well matched AC channel-response allows a single-ended input to be transformed to highly matched push-pull driver. From a 1V single-ended input the circuit of Figure 32 produces 1V differential signal between the two outputs. For larger signals the input voltage divider ($R_1 = 2R_2$) is necessary to limit the input voltage on channel 2.

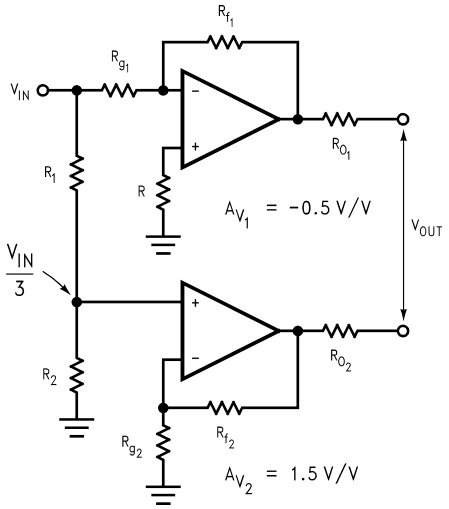


Figure 32. Single-to-Differential Line Driver

DIFFERENTIAL LINE RECEIVER

Figure 33 and Figure 34 show two different implementations of an instrumentation amplifier which convert differential signals to single-ended. Figure 34 allows CMRR adjustment through R_2.

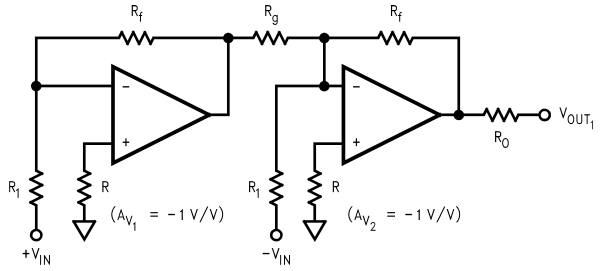


Figure 33. Differential Line Receiver

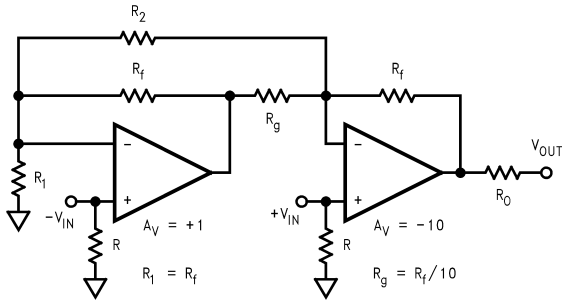


Figure 34. Differential Line Receiver with CMRR Adjustment

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NON-INVERTING CURRENT-FEEDBACK INTEGRATOR

The circuit of Figure 35 achieves its high speed integration by placing one of the LMH6715's amplifiers in the feedback loop of the second amplifier configured as shown.

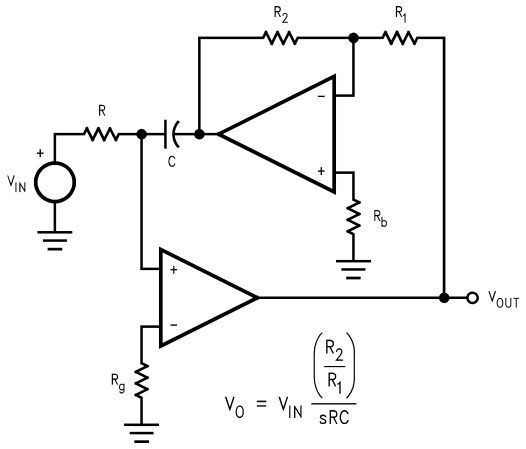


Figure 35. Current Feedback Integrator

LOW NOISE WIDE-BANDWIDTH TRANSIMPEDANCE AMPLIFIER

Figure 36 implements a low noise transimpedance amplifier using both channels of the LMH6715. This circuit takes advantage of the lower input bias current noise of the non-inverting input and achieves negative feedback through the second LMH6715 channel. The output voltage is set by the value of R_F while frequency compensation is achieved through the adjustment of R_T.

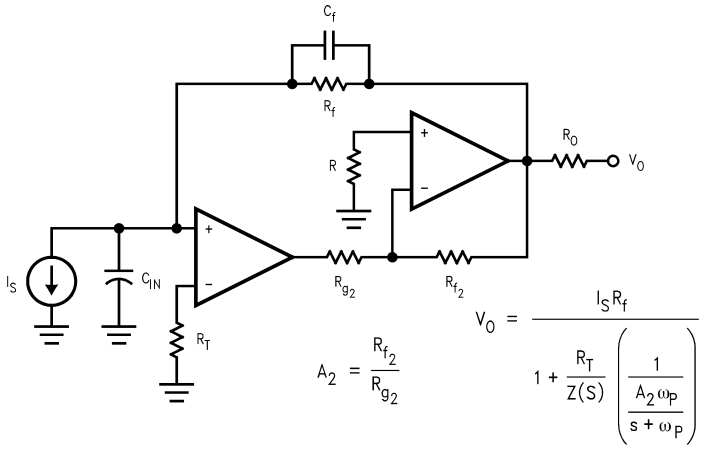


Figure 36. Low-Noise, Wide Bandwidth, Transimpedance Amp.

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REVISION HISTORY

Changes from Revision B (April 2013) to Revision C **Page**

- Changed layout of National Data Sheet to TI format 14

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PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
LMH6715 MDC	ACTIVE	DIESALE	Y	0	400	Green (RoHS & no Sb/Br)	Call TI	Level-1-NA-UNLIM	-40 to 85		Samples
LMH6715MA	NRND	SOIC	D	8	95	TBD	Call TI	Call TI	-40 to 85		
LMH6715MA/NOPB	ACTIVE	SOIC	D	8	95	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 85	LMH67 15MA	Samples
LMH6715MAX/NOPB	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 85	LMH67 15MA	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

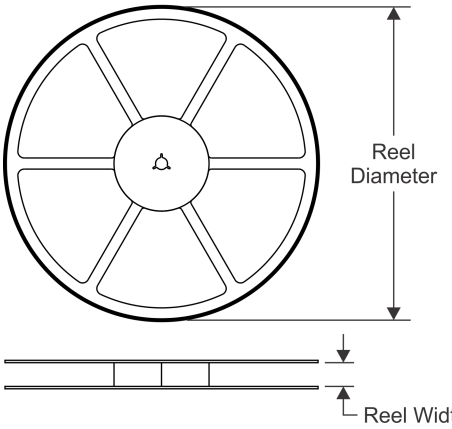
(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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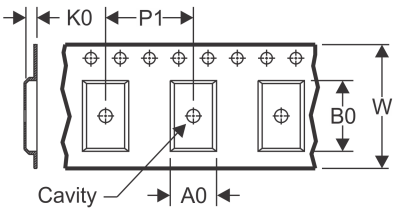
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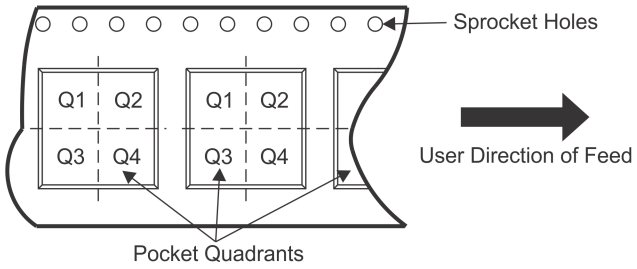


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

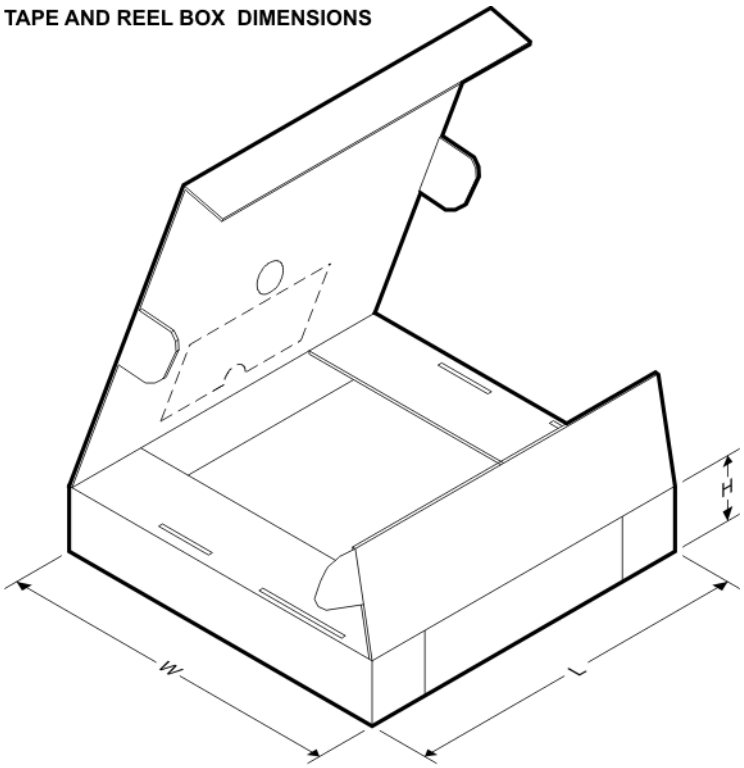
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
LMH6715MAX/NOPB	SOIC	D	8	2500	330.0	12.4	6.5	5.4	2.0	8.0	12.0	Q1

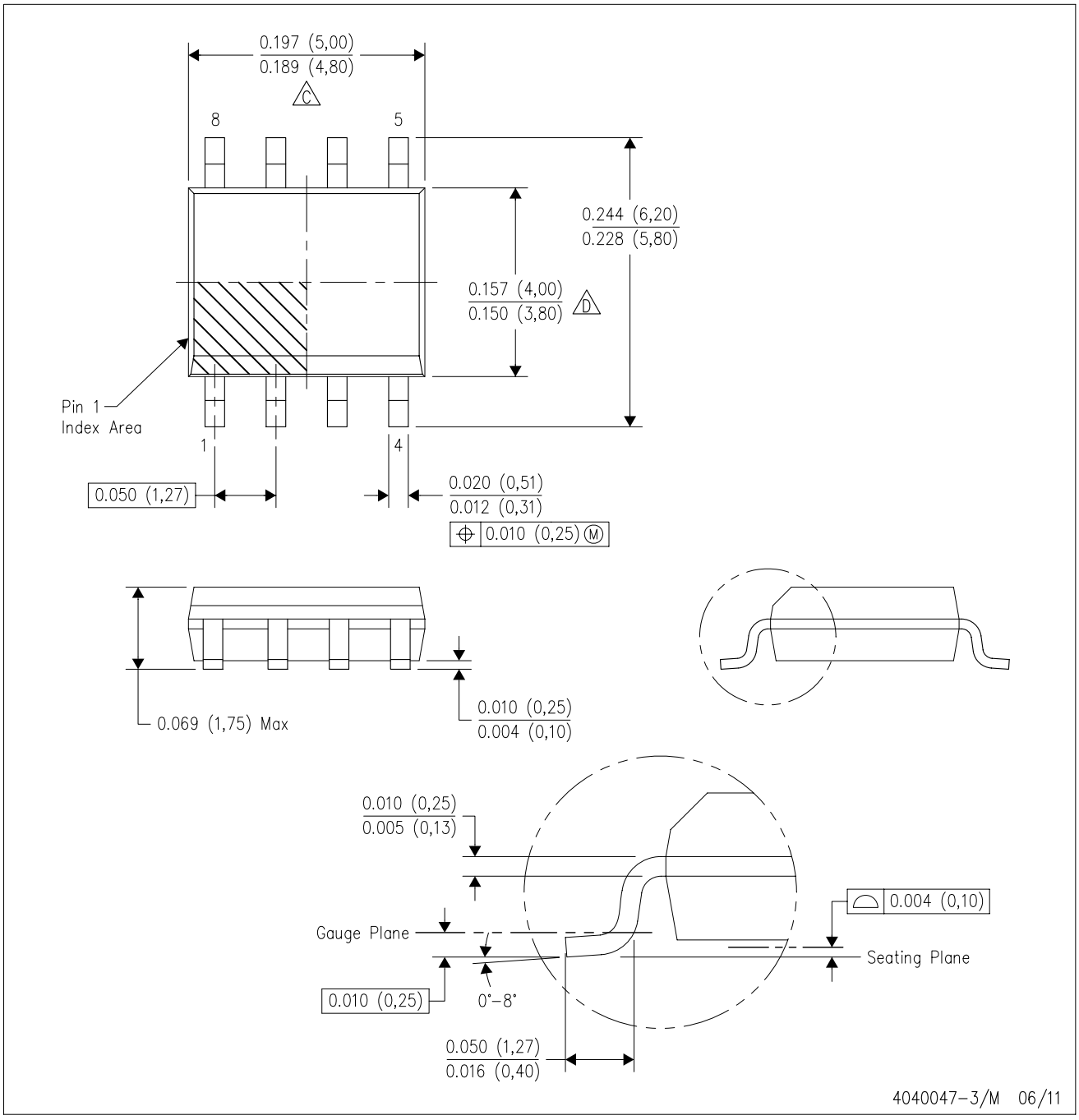
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
LMH6715MAX/NOPB	SOIC	D	8	2500	367.0	367.0	35.0

D (R–PDSO–G8) PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
E. Reference JEDEC MS–012 variation AA.

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