National Semiconductor

June 2003

LMH6702
Ultra Low Distortion, Wideband Op Amp

General Description

The LMH6702 is a very wideband, DC coupled monolithic operational amplifier designed specifically for wide dynamic range systems requiring exceptional signal fidelity. Benefiting from National's current feedback architecture, the LMH6702 offers unity gain stability at exceptional speed without need for external compensation.

With its 720MHz bandwidth (A_V = 2V/V, V_O = $2V_{PP}$), 10-bit distortion levels through 60MHz (R_L = 100Ω), 1.83nV/$\sqrt{Hz}$ input referred noise and 12.5mA supply current, the LMH6702 is the ideal driver or buffer for high-speed flash A/D and D/A converters.

Wide dynamic range systems such as radar and communication receivers, requiring a wideband amplifier offering exceptional signal purity, will find the LMH6702's low input referred noise and low harmonic and intermodulation distortion make it an attractive high speed solution.

The LMH6702 is constructed using National's VIP10™ complimentary bipolar process and National's proven current feedback architecture. The LMH6702 is available in SOIC and SOT23-5 packages.

Features

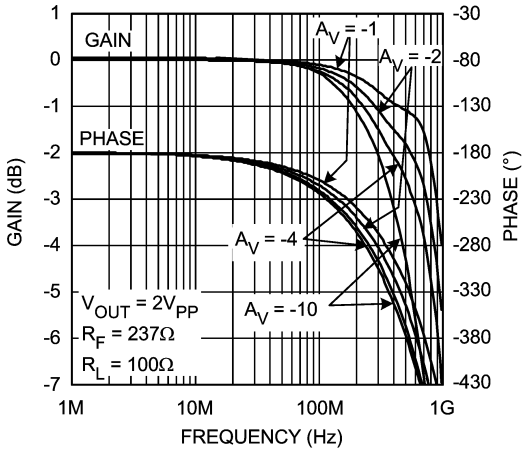
V_S = ±5V, T_A = 25˚C, A_V = +2V/V, R_L = 100Ω, V_{OUT} = $2V_{PP}$, Typical unless Noted:

- $2^{nd}/3^{rd}$ Harmonics (5MHz, SOT23-5) –100/–96dBc
- –3dB Bandwidth (V_{OUT} = $2V_{PP}$) 720MHz
- Low noise 1.83nV/$\sqrt{Hz}$
- Fast settling to 0.1% 13.4ns
- Fast slew rate 3100V/µs
- Supply current 12.5mA
- Output current 80mA
- Low Intermodulation Distortion (75MHz) –67dBc
- Improved Replacement for CLC409 and CLC449

Applications

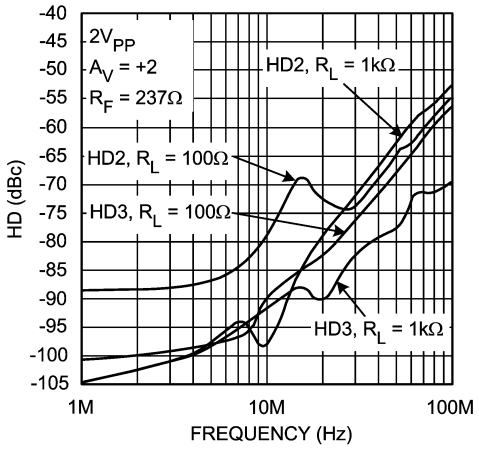
- Flash A/D driver
- D/A transimpedance buffer
- Wide dynamic range IF amp
- Radar/communication receivers
- Line driver
- High resolution video

Inverting Frequency Response



20039002

Harmonic Distortion vs. Load and Frequency



20039007

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Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

V_S	±6.75V
I_{OUT}	(Note 3)
Common Mode Input Voltage	V^- to V^+
Maximum Junction Temperature	+150˚C
Storage Temperature Range	−65˚C to +150˚C
Soldering Information	
Infrared or Convection (20 sec.)	235˚C
Wave Soldering (10 sec.)	260˚C
ESD Tolerance (Note 4)	
Human Body Model	2000V
Machine Model	200V
Storage Temperature Range	−65˚C to +150˚C

Operating Ratings (Note 1)

Thermal Resistance		
Package	**(θ_{JC})**	**(θ_{JA})**
8-Pin SOIC	75˚C/W	160˚C/W
5-Pin SOT23	120˚C/W	187˚C/W
Operating Temperature		−40˚C to +85˚C
Nominal Supply Voltage		±5V to ±6V

Electrical Characteristics (Note 2)

A_V = +2, V_S = ±5V, R_L = 100Ω, R_F = 237Ω; unless specified

Symbol	Parameter	Conditions	Min (Note 6)	Typ (Note 6)	Max (Note 6)	Units
Frequency Domain Performance						
$SSBW_{LG}$	-3dB Bandwidth	V_{OUT} = $2V_{PP}$		720		MHz
$LSBW_{LG}$		V_{OUT} = $4V_{PP}$		480		
$SSBW_{HG}$		V_{OUT} = $2V_{PP}$, A_V = +10		140		
$GF_{0.1dB}$	0.1dB Gain Flatness	V_{OUT} = $2V_{PP}$		120		MHz
LPD	Linear Phase Deviation	DC to 100MHz		0.09		deg
DG	Differential Gain	R_L =150Ω, 3.58MHz/4.43MHz		0.024/0.021		%
DP	Differential Phase	R_L = 150Ω, 3.58MHz/4.43MHz		0.004/0.007		deg
Time Domain Response						
TRS/TRL	Rise and Fall Time	2V Step		0.87/0.77		ns
		6V Step		1.70/1.70		ns
OS	Overshoot	2V Step		0		%
SR	Slew Rate	$6V_{PP}$, 40% to 60% (Note 5)		3100		V/µs
T_s	Settling Time to 0.1%	2V Step		13.4		ns
Distortion And Noise Response						
HD2L	2^{nd} Harmonic Distortion	$2V_{PP}$, 5MHz (Note 9) (SOT23-5/SOIC)		−100/ −87		dBc
HD2		$2V_{PP}$, 20MHz (Note 9) (SOT23-5/SOIC)		−79/ −72		dBc
HD2H		$2V_{PP}$, 60MHz (Note 9) (SOT23-5/SOIC)		−63/ −64		dBc
HD3L	3^{rd} Harmonic Distortion	$2V_{PP}$, 5MHz (Note 9) (SOT23-5/SOIC)		−96/ −98		dBc
HD3		$2V_{PP}$, 20MHz (Note 9) (SOT23-5/SOIC)		−88/ −82		dBc
HD3H		$2V_{PP}$, 60MHz (Note 9) (SOT23-5/SOIC)		−70/ −65		dBc
OIM3	IMD	75MHz, P_O = 10dBm/ tone		−67		dBc
V_N	Input Referred Voltage Noise	>1MHz		1.83		nV/ $\sqrt{Hz}$
I_N	Input Referred Inverting Noise Current	>1MHz		18.5		pA/ $\sqrt{Hz}$
I_{NN}	Input Referred Non-Inverting Noise Current	>1MHz		3.0		pA/ $\sqrt{Hz}$
SNF	Total Input Noise Floor	>1MHz		−158		dBm_{1Hz}
INV	Total Integrated Input Noise	1MHz to 150MHz		35		µV

Electrical Characteristics (Note 2) (Continued)

A_V = +2, V_S = ±5V, R_L = 100Ω, R_F = 237Ω; unless specified

Symbol	Parameter	Conditions	Min (Note 6)	Typ (Note 6)	Max (Note 6)	Units
Static, DC Performance						
V_{IO}	Input Offset Voltage			±1.0	±4.5 **±6.0**	mV
DV_{IO}	Input Offset Voltage Average Drift	(Note 8)		−13		µV/˚C
I_{BN}	Input Bias Current	Non-Inverting (Note 7)		−6	±15 **±21**	µA
DI_{BN}	Input Bias Current Average Drift	Non-Inverting (Note 8)		+40		nA/˚C
I_{BI}	Input Bias Current	Inverting (Note 7)		−8	±30 **±34**	µA
DI_{BI}	Input Bias Current Average Drift	Inverting (Note 8)		−10		nA/˚C
PSRR	Power Supply Rejection Ratio	DC	47 **45**	52		dB
CMRR	Common Mode Rejection Ration	DC	45 **44**	48		dB
I_{CC}	Supply Current	R_L = ∞	11.0 **10.0**	12.5	16.1 **17.5**	mA
Miscellaneous Performance						
R_{IN}	Input Resistance	Non-Inverting		1.4		MΩ
C_{IN}	Input Capacitance	Non-Inverting		1.6		pF
R_{OUT}	Output Resistance	Closed Loop		30		mΩ
V_{OL}	Output Voltage Range	R_L = 100Ω	±3.3 **±3.2**	±3.5		V
CMIR	Input Voltage Range	Common Mode	±1.9	±2.2		V
I_O	Output Current		50	80		mA

Note 1: Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Operating Ratings indicate conditions for which the device is intended to be functional, but specific performance is not guaranteed. For guaranteed specifications, see the Electrical Characteristics tables.

Note 2: Electrical Table values apply only for factory testing conditions at the temperature indicated. Factory testing conditions result in very limited self-heating of the device such that $T_J = T_A$. No guarantee of parametric performance is indicated in the electrical tables under conditions of internal self-heating where $T_J > T_A$. Min/Max ratings are based on production testing unless otherwise specified.

Note 3: The maximum output current (I_{OUT}) is determined by device power dissipation limitations.

Note 4: Human body model: 1.5kΩ in series with 100pF. Machine model: 0Ω in series with 200pF.

Note 5: Slew Rate is the average of the rising and falling edges.

Note 6: Typical numbers are the most likely parametric norm. Bold numbers refer to over temperature limits.

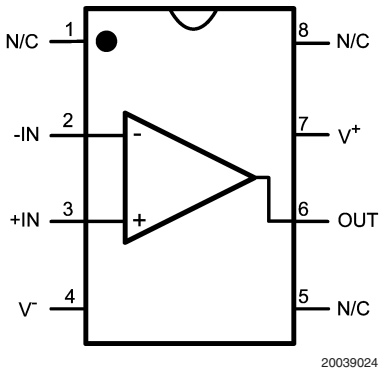
Note 7: Negative input current implies current flowing out of the device.

Note 8: Drift determined by dividing the change in parameter at temperature extremes by the total temperature change.

Note 9: Harmonic distortion is strongly influenced by package type (SOT23-5 or SOIC). See Application Note section under "Harmonic Distortion" for more information.

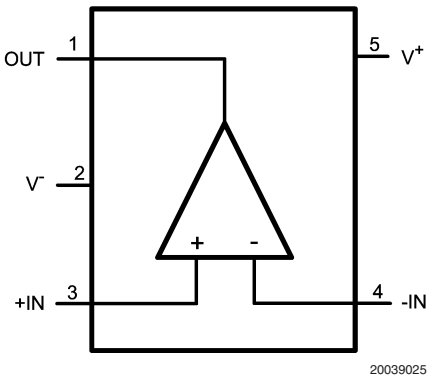
Connection Diagrams

8-Pin SOIC



Top View

5-Pin SOT23



Top View

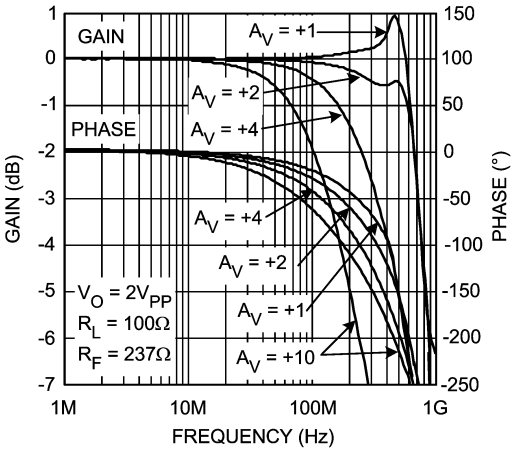
Ordering Information

Package	Part Number	Package Marking	Transport Media	NSC Drawing
8-pin SOIC	LMH6702MA	LMH6702MA	95 Units/Rail	M08A
	LMH6702MAX		2.5k Units Tape and Reel	
5-Pin SOT23	LMH6702MF	A83A	1k Units Tape and Reel	MF05A
	LMH6702MFX		3k Units Tape and Reel	

Typical Performance Characteristics

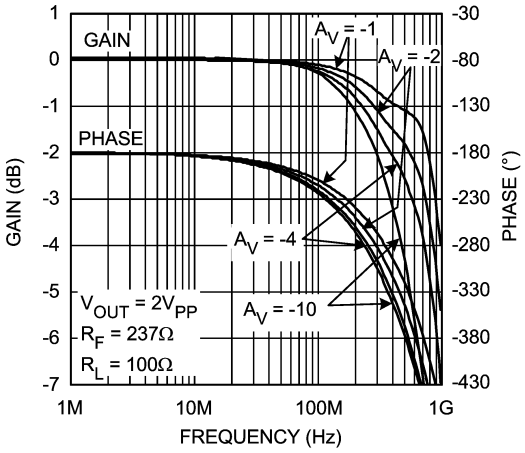
(T_A = 25˚C, V_S = ±5V, R_L = 100Ω, R_f = 237Ω; Unless Specified).

Non-Inverting Frequency Response



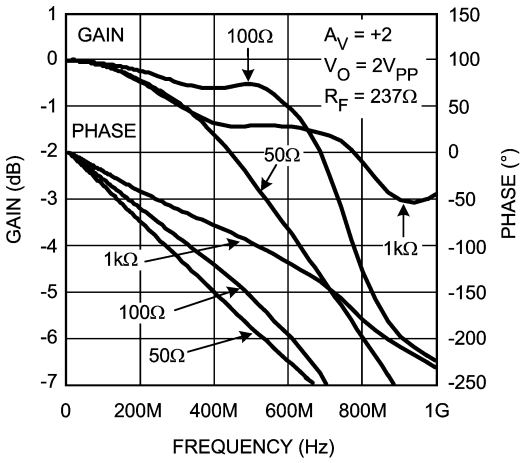
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Inverting Frequency Response



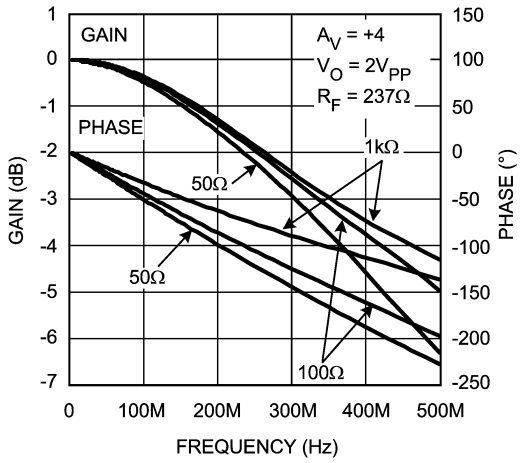
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Frequency Response for Various R_L's, A_V = +2



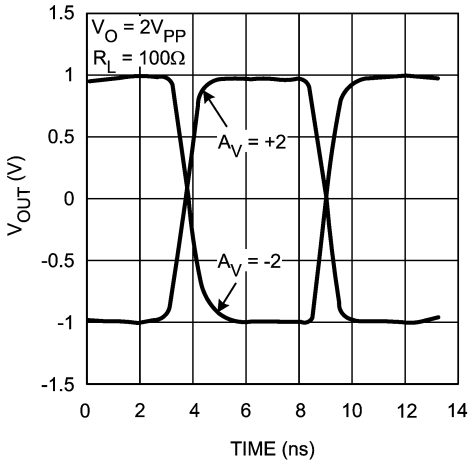
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Frequency Response for Various R_L's, A_V = +4



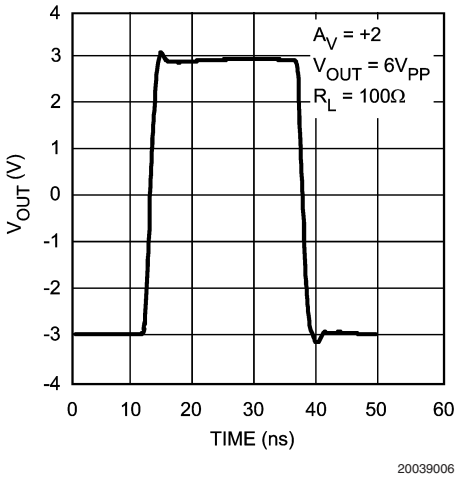
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Step Response, $2V_{PP}$



20039005

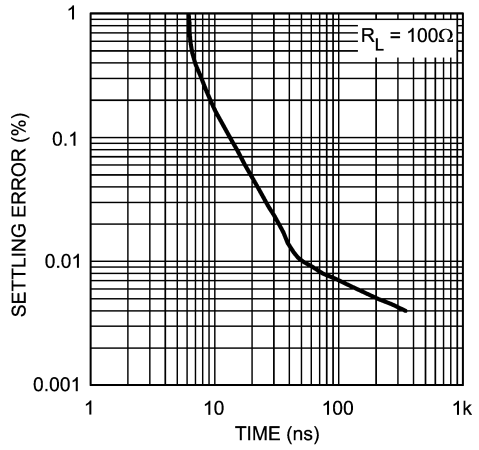
Step Response, $6V_{PP}$



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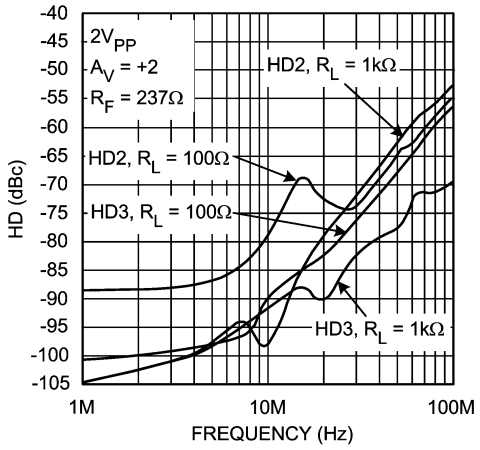
Typical Performance Characteristics (T_A = 25˚C, V_S = ±5V, R_L = 100Ω, R_f = 237Ω; Unless Specified). (Continued)

Percent Settling vs. Time



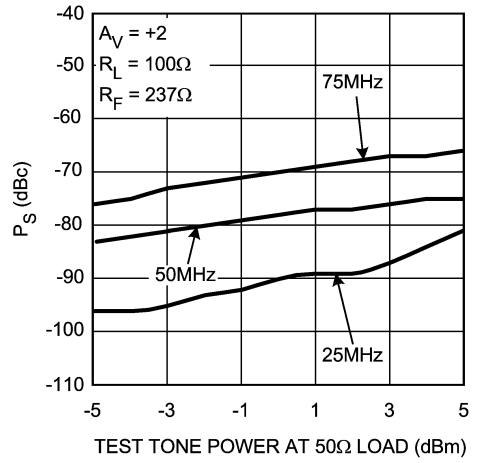
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Harmonic Distortion vs. Load and Frequency (SOIC package)



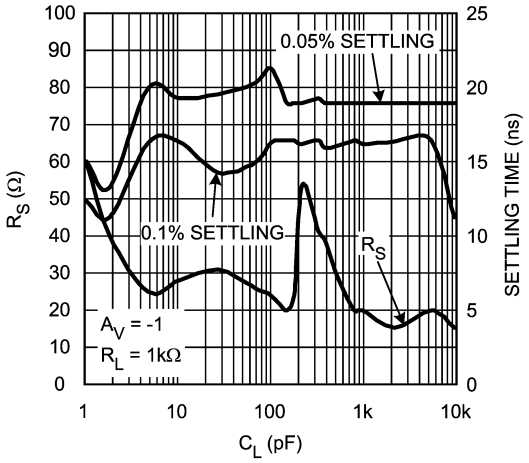
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2 Tone 3rd Order Spurious Level (SOIC package)



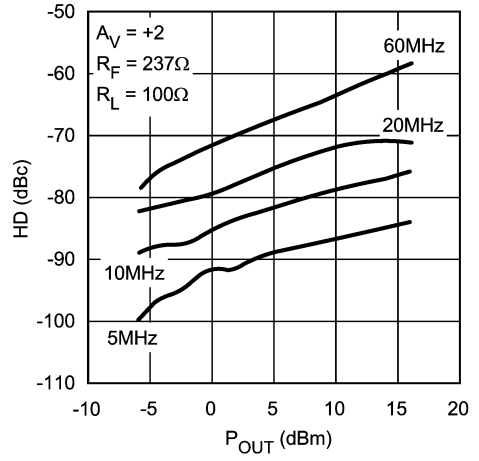
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R_S and Settling Time vs. C_L



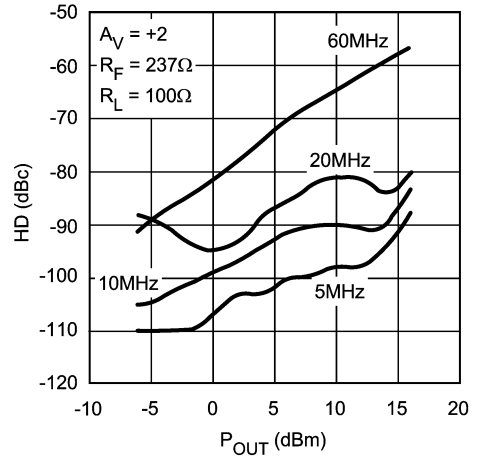
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HD2 vs. Output Power (across 100Ω) (SOIC package)



20039008

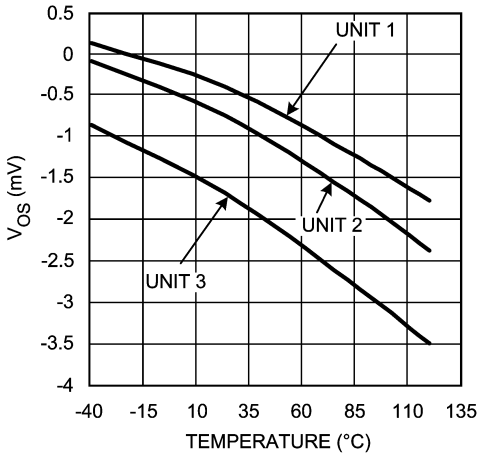
HD3 vs. Output Power (across 100Ω) (SOIC package)



20039009

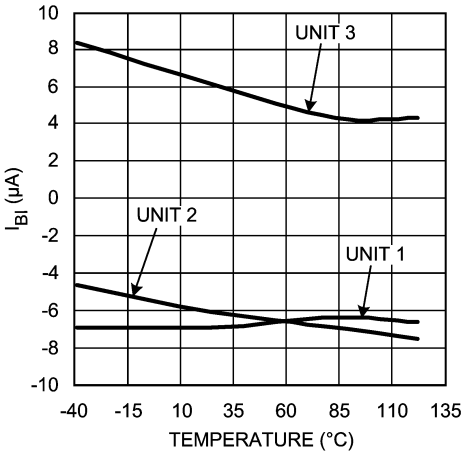
Typical Performance Characteristics (T_A = 25˚C, V_S = ±5V, R_L = 100Ω, R_f = 237Ω; Unless Specified). (Continued)

Input Offset for 3 Representative Units



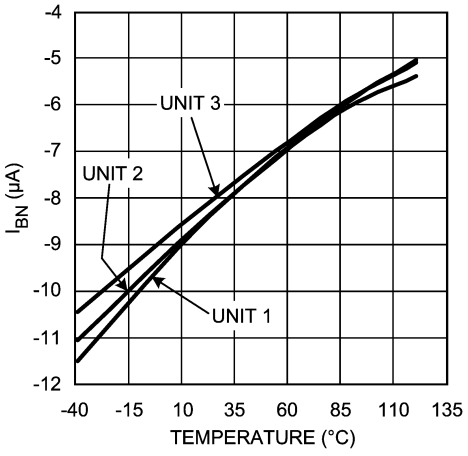
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Inverting Input Bias for 3 Representative Units



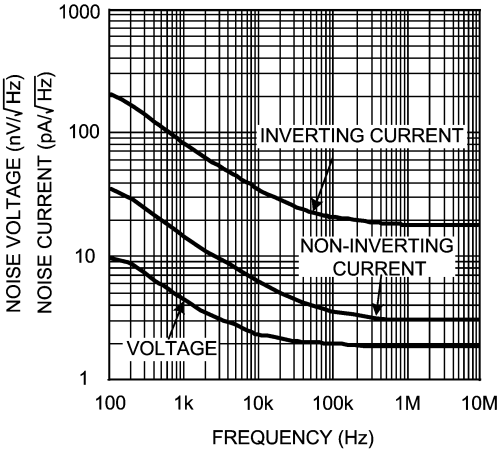
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Non-Inverting Input Bias for 3 Representative Units



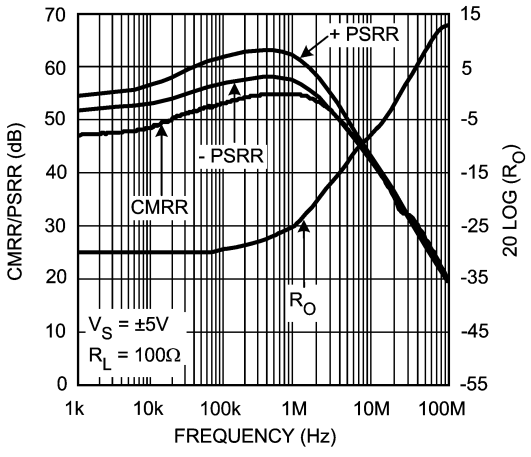
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Noise



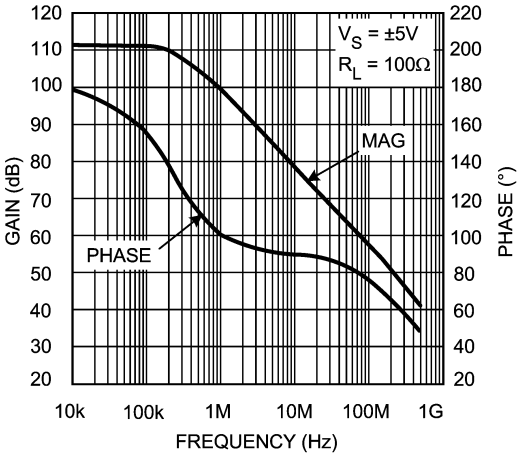
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CMRR, PSRR, R_{OUT}



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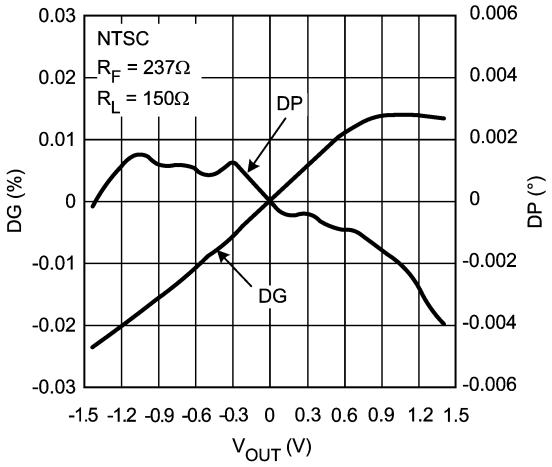
Transimpedance



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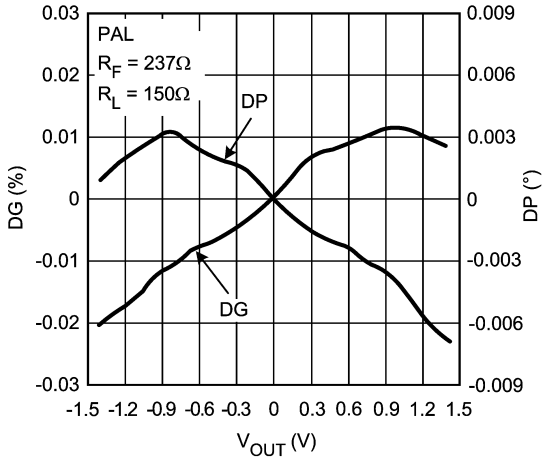
Typical Performance Characteristics (T_A = 25˚C, V_S = ±5V, R_L = 100Ω, R_f = 237Ω; Unless Specified). (Continued)

DG/DP (NTSC)



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DG/DP (PAL)



20039003

Application Section

FEEDBACK RESISTOR

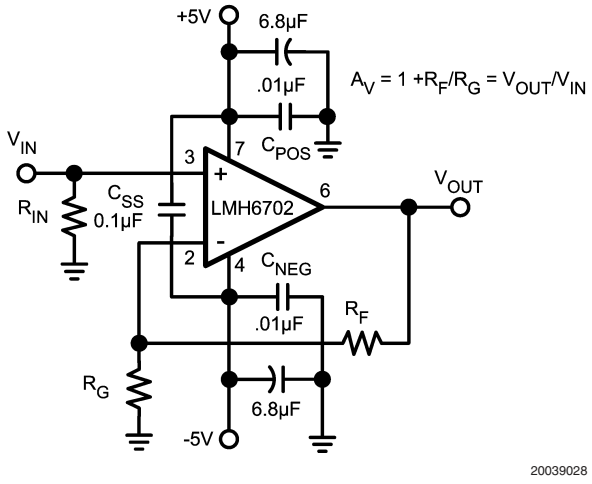


FIGURE 1. Recommended Non-Inverting Gain Circuit

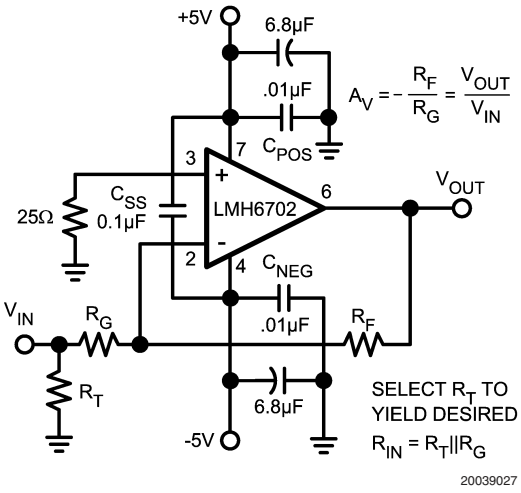


FIGURE 2. Recommended Inverting Gain Circuit

The LMH6702 achieves its excellent pulse and distortion performance by using the current feedback topology. The loop gain for a current feedback op amp, and hence the frequency response, is predominantly set by the feedback resistor value. The LMH6702 is optimized for use with a 237Ω feedback resistor. Using lower values can lead to excessive ringing in the pulse response while a higher value will limit the bandwidth. Application Note OA-13 discusses this in detail along with the occasions where a different R_F might be advantageous.

HARMONIC DISTORTION

The LMH6702 has been optimized for exceptionally low harmonic distortion while driving very demanding resistive or capacitive loads. Generally, when used as the input amplifier to very high speed flash ADCs, the distortions introduced by the converter will dominate over the low LMH6702 distortions shown in the Typical Performance Characteristics section. The capacitor C_{SS}, shown across the supplies in *Figure 1* and *Figure 2*, is critical to achieving the lowest 2nd harmonic distortion. For absolute minimum distortion levels, it is also advisable to keep the supply decoupling currents (ground connections to C_{POS}, and C_{NEG} in *Figure 1* and *Figure 2*) separate from the ground connections to sensitive input circuitry (such as R_G, R_T, and R_{IN} ground connections). Splitting the ground plane in this fashion and separately routing the high frequency current spikes on the decoupling caps back to the power supply (similar to "Star Connection" layout technique) ensures minimum coupling back to the input circuitry and results in best harmonic distortion response (especially 2nd order distortion).

If this lay out technique has not been observed on a particular application board, designer may actually find that supply decoupling caps could adversely affect HD2 performance by increasing the coupling phenomenon already mentioned. *Figure 3* below shows actual HD2 data on a board where the ground plane is "shared" between the supply decoupling capacitors and the rest of the circuit. Once these capacitors are removed, the HD2 distortion levels reduce significantly, especially between 10MHz-20MHz, as shown in *Figure 3* below:

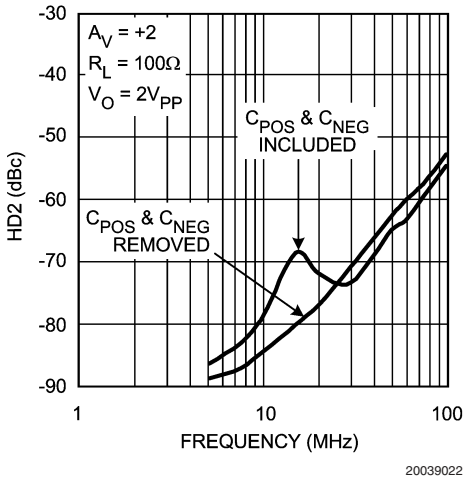


FIGURE 3. Decoupling Current Adverse Effect on a Board with Shared Ground Plane

At these extremely low distortion levels, the high frequency behavior of decoupling capacitors themselves could be significant. In general, lower value decoupling caps tend to have higher resonance frequencies making them more effective for higher frequency regions. A particular application board which has been laid out correctly with ground returns "split" to minimize coupling, would benefit the most by having low value and higher value capacitors paralleled to take advantage of the effective bandwidth of each and extend low distortion frequency range.

Another important variable in getting the highest fidelity signal from the LMH6702 is the package itself. As already noted, coupling between high frequency current transients on supply lines and the device input can lead to excess harmonic distortion. An important source of this coupling is in fact through the device bonding wires. A smaller package, in general, will have shorter bonding wires and therefore lower coupling. This is true in the case of the SOT23-5 compared to the SOIC package where a marked improvement in HD can be measured in the SOT23-5 package. *Figure 4* below shows the HD comparing SOT23-5 to SOIC package:

Application Section (Continued)

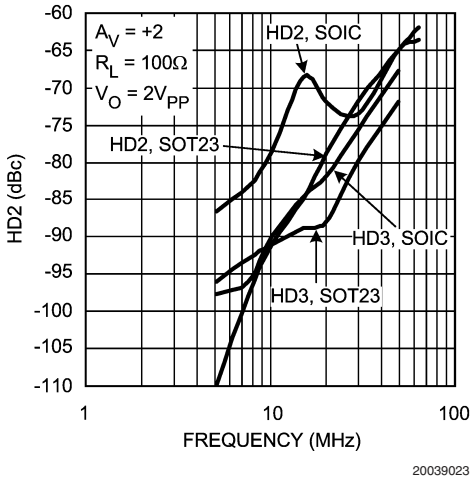


FIGURE 4. SOIC and SOT23-5 Packages Distortion Terms Compared

The LMH6702 data sheet shows both SOT23 and SOIC data in the Electrical Characteristic section to aid in selecting the right package. The Typical Performance Characteristics section shows SOIC package plots only.

2-TONE 3rd ORDER INTERMODULATION

The 2-tone, 3rd order spurious plot shows a relatively constant difference between the test power level and the spurious level with the difference depending on frequency. The LMH6702 does not show an intercept type performance, (where the relative spurious levels change at a 2X rate vs. the test tone powers), due to an internal full power bandwidth enhancement circuit that boosts the performance as the output swing increases while dissipating negligible quiescent power under low output power conditions. This feature enhances the distortion performance and full power bandwidth to match that of much higher quiescent supply current parts.

CAPACITIVE LOAD DRIVE

Figure 5 shows a typical application using the LMH6702 to drive an ADC.

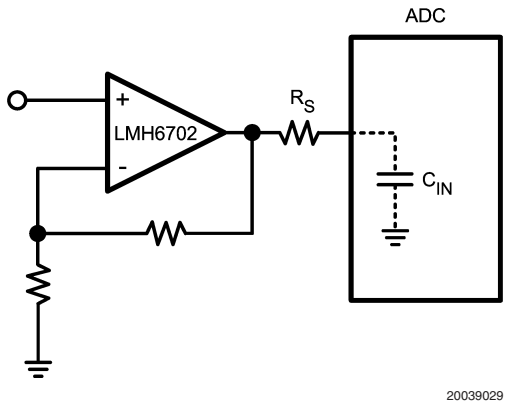


FIGURE 5. Input Amplifier to ADC

The series resistor, R_S, between the amplifier output and the ADC input is critical to achieving best system performance. This load capacitance, if applied directly to the output pin, can quickly lead to unacceptable levels of ringing in the pulse response. The plot of "R_S and Settling Time vs. C_L" in the Typical Performance Characteristics section is an excellent starting point for selecting R_S. The value derived in that plot minimizes the step settling time into a fixed discrete capacitive load with the output driving a very light resistive load (1kΩ). Sensitivity to capacitive loading is greatly reduced once the output is loaded more heavily. Therefore, for cases where the output is heavily loaded, R_S value may be reduced. The exact value may best be determined experimentally for these cases.

In applications where the LMH6702 is replacing the CLC409, care must be taken when the device is lightly loaded and some capacitance is present at the output. Due to the much higher frequency response of the LMH6702 compared to the CLC409, there could be increased susceptibility to low value output capacitance (parasitic or inherent to the board layout or otherwise being part of the output load). As already mentioned, this susceptibility is most noticeable when the LMH6702's resistive load is light. Parasitic capacitance can be minimized by careful lay out. Addition of an output snubber R-C network will also help by increasing the high frequency resistive loading.

Referring back to *Figure 5*, it must be noted that several additional constraints should be considered in driving the capacitive input of an ADC. There is an option to increase R_S, band-limiting at the ADC input for either noise or Nyquist band-limiting purposes. Increasing R_S too much, however, can induce an unacceptably large input glitch due to switching transients coupling through from the "convert" signal. Also, C_{IN} is oftentimes a voltage dependent capacitance. This input impedance non-linearity will induce distortion terms that will increase as R_S is increased. Only slight adjustments up or down from the recommended R_S value should therefore be attempted in optimizing system performance.

Application Section (Continued)

DC ACCURACY AND NOISE

Example below shows the output offset computation equation for the non-inverting configuration using the typical bias current and offset specifications for A_V = + 2:

Output Offset : $V_O = (\pm I_{BN} \cdot R_{IN} \pm V_{IO}) (1 + R_F/R_G) \pm I_{BI} \cdot R_F$

Where R_{IN} is the equivalent input impedance on the non-inverting input.

Example computation for A_V = +2, R_F = 237Ω, R_{IN} = 25Ω:

$V_O = (\pm 6\mu A \cdot 25\Omega \pm 1mV) (1 + 237/237) \pm 8\mu A \cdot 237 = \pm 4.20mV$

A good design, however, should include a worst case calculation using Min/Max numbers in the data sheet tables, in order to ensure "worst case" operation.

Further improvement in the output offset voltage and drift is possible using the composite amplifiers described in Application Note OA-7. The two input bias currents are physically unrelated in both magnitude and polarity for the current feedback topology. It is not possible, therefore, to cancel their effects by matching the source impedance for the two inputs (as is commonly done for matched input bias current devices).

The total output noise is computed in a similar fashion to the output offset voltage. Using the input noise voltage and the two input noise currents, the output noise is developed through the same gain equations for each term but combined as the square root of the sum of squared contributing elements. See Application Note OA-12 for a full discussion of noise calculations for current feedback amplifiers.

PRINTED CIRCUIT LAYOUT

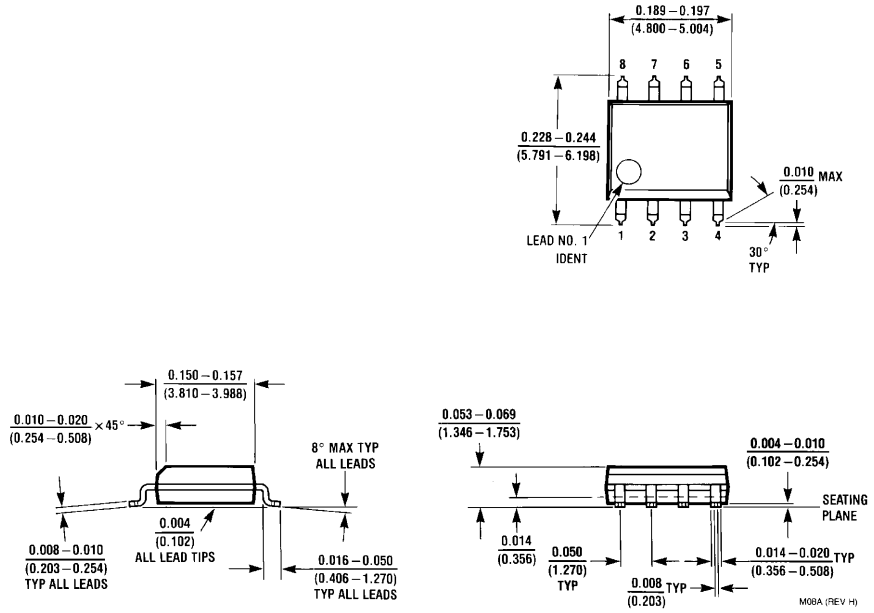
Generally, a good high frequency layout will keep power supply and ground traces away from the inverting input and output pins. Parasitic capacitances on these nodes to ground will cause frequency response peaking and possible circuit oscillations (see Application Note OA-15 for more information). National Semiconductor suggests the following evaluation boards as a guide for high frequency layout and as an aid in device testing and characterization:

Device	Package	Evaluation Board Part Number
LMH6702MF	SOT23-5	CLC730216
LMH6702MA	SOIC	CLC730227

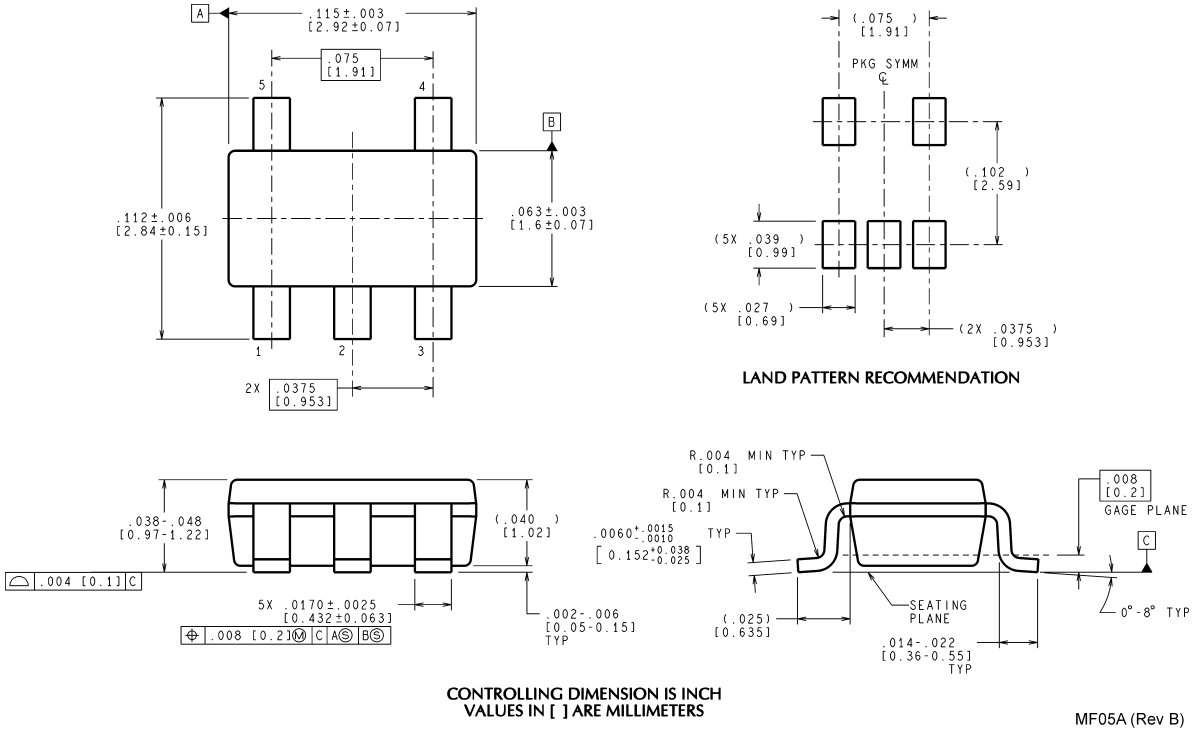
These free evaluation boards are shipped when a device sample request is placed with National Semiconductor.

Physical Dimensions inches (millimeters)

unless otherwise noted



8-Pin SOIC
NS Package Number M08A



5-Pin SOT23
NS Package Number MA05A

Notes

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