National Semiconductor

December 2004

LMH6550
Differential, High Speed Op Amp

General Description

The LMH™6550 is a high performance voltage feedback differential amplifier. The LMH6550 has the high speed and low distortion necessary for driving high performance ADCs as well as the current handling capability to drive signals over balanced transmission lines like CAT 5 data cables. The LMH6550 can handle a wide range of video and data formats.

With external gain set resistors, the LMH6550 can be used at any desired gain. Gain flexibility coupled with high speed makes the LMH6550 suitable for use as an IF amplifier in high performance communications equipment.

The LMH6550 is available in the space saving SOIC package.

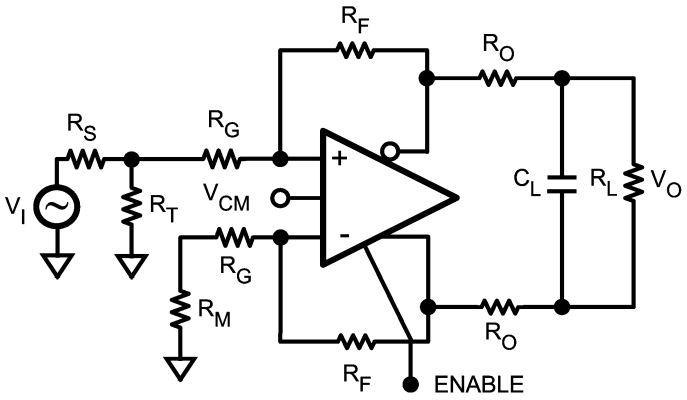
Features

- 400 MHz –3 dB bandwidth (V_{OUT} = 0.5 V_{PP})
- 90 MHz 0.1 dB bandwidth
- 3000 V/µs slew Rate
- 8 ns settling time to 0.1%
- –92/–103 dB HD2/HD3 @ 5 MHz
- 10 ns shutdown/enable

Applications

- Differential AD driver
- Video over twisted pair
- Differential line driver
- Single end to differential converter
- High speed differential signaling
- IF/RF amplifier
- SAW filter buffer/driver

Typical Application



$$\text{SET } R_M = R_T || R_S$$

$$\text{SET } R_T = \frac{1}{\left(\frac{1}{R_S} - \frac{1}{R_{IN}}\right)} \qquad R_{IN} = \frac{R_G}{1 - \left(\frac{R_F}{2^* (R_F + R_G)}\right)}$$

20130110

Single Ended Input Differential Output.

Gain = A_V=0.5 * R_F/R_G

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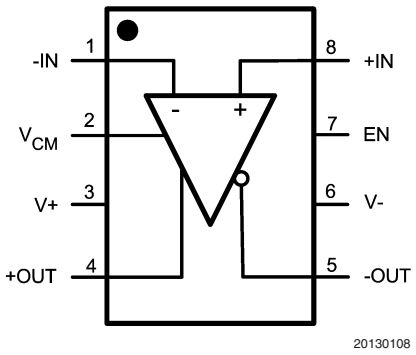
Connection Diagram

8-Pin SOIC



Top View

Ordering Information

Package	Part Number	Package Marking	Transport Media	NSC Drawing
8-Pin SOIC	LMH6550MA	LMH6550MA	95/Rails	M08A
	LMH6550MAX		2.5k Units Tape and Reel	

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

ESD Tolerance (Note 5)	
Human Body Model	2000V
Machine Model	200V
Supply Voltage	13.2V
Common Mode Input Voltage	±Vs
Maximum Input Current (pins 1, 2, 7, 8)	30mA
Maximum Output Current (pins 4, 5)	(Note 3)
Soldering Information	
Infrared or Convection (20 sec)	235˚C
Wave Soldering (10 sec)	260˚C

Operating Ratings (Note 1)

Operating Temperature Range	−40˚C to +85˚C
Storage Temperature Range	−65˚C to +150˚C
Total Supply Voltage	4.5V to 12V
Package Thermal Resistance (θ_{JA}) (Note 4)	
8-Pin SOIC	150˚C/W

±5V Electrical Characteristics (Note 2)

Single ended in differential out, T_A= 25˚C, A_V= +1, V_S = ±5V, V_{CM} = 0V, R_F = R_G = 365Ω, R_L = 500Ω;; Unless specified **Boldface** limits apply at the temperature extremes.

Symbol	Parameter	Conditions	Min (Note 8)	Typ (Note 7)	Max (Note 8)	Units
AC Performance (Differential)						
SSBW	Small Signal −3 dB Bandwidth	V_{OUT} = 0.5 V_{PP}		400		MHz
LSBW	Large Signal −3 dB Bandwidth	V_{OUT} = 2 V_{PP}		380		MHz
	Large Signal −3 dB Bandwidth	V_{OUT} = 4 V_{PP}		320		MHz
	0.1 dB Bandwidth	V_{OUT} = 0.5 V_{PP}		90		MHz
	Slew Rate	4V Step(Note 6)	2000	3000		V/µs
	Rise/Fall Time	2V Step		1		ns
	Settling Time	2V Step, 0.1%		8		ns
V_{CM} Pin AC Performance (Common Mode Feedback Amplifier)						
	Common Mode Small Signal Bandwidth	V_{CM}bypass capacitor removed		210		MHz
	Slew Rate	V_{CM}bypass capacitor removed		200		V/µs
Distortion and Noise Response						
HD2	2nd Harmonic Distortion	V_O = 2 V_{PP}, f = 5 MHz, R_L=800Ω		−92		dBc
HD2		V_O = 2 V_{PP}, f = 20 MHz, R_L=800Ω		−78		dBc
HD2		V_O = 2 V_{PP}, f = 70 MHz, R_L=800Ω		−59		dBc
HD3	3rd Harmonic Distortion	V_O = 2 V_{PP}, f = 5 MHz, R_L=800Ω		−103		dBc
HD3		V_O = 2 V_{PP}, f = 20 MHz, R_L=800Ω		−88		dBc
HD3		V_O = 2 V_{PP}, f = 70 MHz, R_L=800Ω		−50		dBc
e_n	Input Referred Voltage Noise	Freq ≥ 1 MHz		6.0		nV/$\sqrt{Hz}$
i_n	Input Referred Noise Current	Freq ≥ 1 MHz		1.5		pA/$\sqrt{Hz}$
Input Characteristics (Differential)						
V_{OSD}	Input Offset Voltage	Differential Mode, V_{ID} = 0, V_{CM} = 0		1	±4 **±6**	mV
	Input Offset Voltage Average Temperature Drift	(Note 10)		1.6		µV/˚C
I_{BI}	Input Bias Current	(Note 9)	0	-8	−16	µA
	Input Bias Current Average Temperature Drift	(Note 10)		9.6		nA/˚C
	Input Bias Difference	Difference in Bias currents between the two inputs		0.3		µA
CMRR	Common Mode Rejection Ratio	DC, V_{CM} = 0V, V_{ID} = 0V	72	82		dBc
R_{IN}	Input Resistance	Differential		5		MΩ
C_{IN}	Input Capacitance	Differential		1		pF

±5V Electrical Characteristics (Note 2) (Continued)

Single ended in differential out, T_A= 25˚C, A_V= +1, V_S = ±5V, V_{CM} = 0V, R_F = R_G = 365Ω, R_L = 500Ω;; Unless specified **Boldface** limits apply at the temperature extremes.

Symbol	Parameter	Conditions	Min (Note 8)	Typ (Note 7)	Max (Note 8)	Units
CMVR	Input Common Mode Voltage Range	CMRR > 53dB	+3.1 –4.6	+3.2 –4.7		V
V_{CM}Pin Input Characteristics (Common Mode Feedback Amplifier)						
V_{OSC}	Input Offset Voltage	Common Mode, V_{ID} = 0		1	±5 **±8**	mV
	Input Offset Voltage Average Temperature Drift	(Note 10)		25		µV/˚C
	Input Bias Current	(Note 9)		–2		µA
	V_{CM} CMRR	V_{ID} = 0V, 1V step on V_{CM} pin, measure V_{OD}	70	75		dB
	Input Resistance			25		kΩ
	Common Mode Gain	▲$V_{O,CM}$/▲V_{CM}	0.995	0.997	1.005	V/V
Output Performance						
	Output Voltage Swing	Single Ended, Peak to Peak,	±7.38 **±7.18**	±7.8		V
	Output Common Mode Voltage Range	V_{ID} = 0 V,	±3.69	±3.8		V
I_{OUT}	Linear Output Current	V_{OUT} = 0V	±63	±75		mA
I_{SC}	Short Circuit Current	Output Shorted to Ground V_{IN} = 3V Single Ended(Note 3)I		±200		mA
	Output Balance Error	ΔV_{OUT}Common Mode /ΔV_{OUT}DIfferential , V_{OUT} = 1Vpp Differential, f = 10 MHz		–68		dB
Miscellaneous Performance						
	Enable/Disable Time			10		ns
A_{VOL}	Open Loop Gain	Differential		70		dB
PSRR	Power Supply Rejection Ratio	DC, ΔV_S = ±1V	74	90		dB
	Supply Current	R_L = ∞	18	20	24 **27**	mA
	Disabled Supply Current			1	1.2	mA

5V Electrical Characteristics (Note 2)

Single ended in differential out, T_A= 25˚C, A_V= +1, V_S = 5V, V_{CM} = 2.5V, R_F = R_G = 365Ω, R_L = 500Ω; ; Unless specified**Boldface** limits apply at the temperature extremes.

Symbol	Parameter	Conditions	Min (Note 8)	Typ (Note 7)	Max (Note 8)	Units
SSBW	Small Signal –3 dB Bandwidth	R_L = 500Ω, V_{OUT} = 0.5 V_{PP}		350		MHz
LSBW	Large Signal –3 dB Bandwidth	R_L = 500Ω, V_{OUT} = 2 V_{PP}		330		MHz
	0.1 dB Bandwidth			60		MHz
	Slew Rate	2V Step(Note 6)		1500		V/µs
	Rise/Fall Time, 10% to 90%	1V Step		1		ns
	Settling Time	1V Step, 0.05%		12		ns
V_{CM} Pin AC Performance (Common Mode Feedback Amplifier)						
	Common Mode Small Signal Bandwidth			185		MHz
	Slew Rate			180		V/µs
Distortion and Noise Response						
HD2	2nd Harmonic Distortion	V_O = 2 V_{PP}, f = 5 MHz, R_L=800Ω		–89		dBc

5V Electrical Characteristics (Note 2) (Continued)

Single ended in differential out, T_A= 25˚C, A_V= +1, V_S = 5V, V_{CM} = 2.5V, R_F = R_G = 365Ω, R_L = 500Ω; ; Unless specified**Boldface** limits apply at the temperature extremes.

Symbol	Parameter	Conditions	Min (Note 8)	Typ (Note 7)	Max (Note 8)	Units
HD2		V_O = 2 V_{PP}, f = 20 MHz, R_L=800Ω		–88		dBc
HD3	3rd Harmonic Distortion	V_O = 2 V_{PP}, f = 5 MHz, R_L=800Ω		–85		dBc
HD3		V_O = 2 V_{PP}, f = 20 MHz, R_L=800Ω		–70		dBc
e_n	Input Referred Noise Voltage	Freq ≥ 1 MHz		6.0		nV/ $\sqrt{Hz}$
i_n	Input Referred Noise Current	Freq ≥ 1 MHz		1.5		pA/ $\sqrt{Hz}$
Input Characteristics (Differential)						
V_{OSD}	Input Offset Voltage	Differential Mode, V_{ID} = 0, V_{CM} = 0		1	±4 **±6**	mV
	Input Offset Voltage Average Temperature Drift	(Note 10)		1.6		µV/˚C
I_{BIAS}	Input Bias Current	(Note 9)	0	–8	–16	µA
	Input Bias Current Average Temperature Drift	(Note 10)		9.5		nA/˚C
	Input Bias Current Difference	Difference in Bias currents between the two inputs		0.3		µA
CMRR	Common-Mode Rejection Ratio	DC, V_{ID} = 0V	70	80		dBc
	Input Resistance	Differential		5		MΩ
	Input Capacitance	Differential		1		pF
V_{ICM}	Input Common Mode Range	CMRR > 53 dB	+3.1 +0.4	+3.2 +0.3		
V_{CM}Pin Input Characteristics (Common Mode Feedback Amplifier)						
	Input Offset Voltage	Common Mode, V_{ID} = 0		1	±5 **±8**	mV
	Input Offset Voltage Average Temperature Drift			18.6		µV/˚C
	Input Bias Current			3		µA
	V_{CM} CMRR	V_{ID} = 0, 1V step on V_{CM} pin, measure V_{OD}	70	75		dB
	Input Resistance	V_{CM} pin to ground		25		kΩ
	Common Mode Gain	▲$V_{O,CM}$/▲V_{CM}		0.991		V/V
Output Performance						
V_{OUT}	Output Voltage Swing	Single Ended, Peak to Peak, V_S= ±2.5V, V_{CM}= 0V	±2.4	±2.8		V
I_{OUT}	Linear Output Current	V_{OUT} = 0V Differential	±54	±70		mA
I_{SC}	Output Short Circuit Current	Output Shorted to Ground V_{IN} = 3V Single Ended(Note 3)		250		mA
CMVR	Common Mode Voltage Range	V_{ID} = 0, V_{CM}pin = 1.2V and 3.8V	3.72 1.23	3.8 1.2		V
	Output Balance Error	ΔV_{OUT}Common Mode /ΔV_{OUT}DIfferential , V_{OUT} = 1Vpp Differential, f = 10 MHz		–65		dB
Miscellaneous Performance						
	Enable/Disable Time			10		ns
	Open Loop Gain	DC, Differential		70		dB
PSRR	Power Supply Rejection Ratio	DC, ΔV_S = ±0.5V	72	77		dB
I_S	Supply Current	R_L = ∞	16.5	19	23.5 **26.5**	mA
I_{SD}	Disabled Supply Current			1	1.2	mA

5V Electrical Characteristics (Note 2) (Continued)

Note 1: Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Operating Ratings indicate conditions for which the device is intended to be functional, but specific performance is not guaranteed. For guaranteed specifications, see the Electrical Characteristics tables.

Note 2: Electrical Table values apply only for factory testing conditions at the temperature indicated. Factory testing conditions result in very limited self-heating of the device such that $T_J = T_A$. No guarantee of parametric performance is indicated in the electrical tables under conditions of internal self-heating where $T_J > T_A$.

Note 3: The maximum output current (I_{OUT}) is determined by device power dissipation limitations.

Note 4: The maximum power dissipation is a function of $T_{J(MAX)}$, θ_{JA} and T_A. The maximum allowable power dissipation at any ambient temperature is $P_D = (T_{J(MAX)} - T_A)/\theta_{JA}$. All numbers apply for package soldered directly into a 2 layer PC board with zero air flow.

Note 5: Human body model: 1.5 kΩ in series with 100 pF. Machine model: 0Ω in series with 200pF.

Note 6: Slew Rate is the average of the rising and falling edges.

Note 7: Typical numbers are the most likely parametric norm.

Note 8: Limits are 100% production tested at 25˚C. Limits over the operating temperature range are guaranteed through correlation using Statistical Quality Control (SQC) methods.

Note 9: Negative input current implies current flowing out of the device.

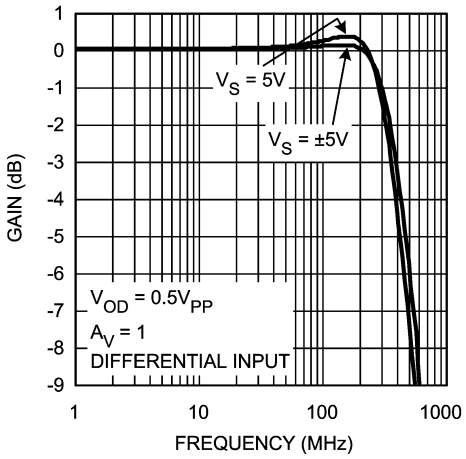
Note 10: Drift determined by dividing the change in parameter at temperature extremes by the total temperature change.

Note 11: Parameter is guaranteed by design.

Typical Performance Characteristics

(T_A = 25˚C, V_S = ±5V, R_L = 500Ω, R_F = 365Ω, A_V=+1; Unless Specified).

Frequency Response vs. Supply Voltage



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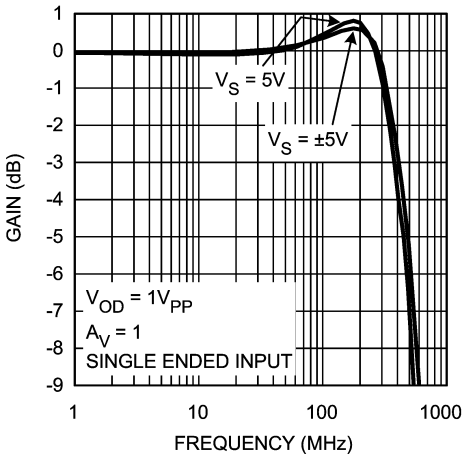
Frequency Response



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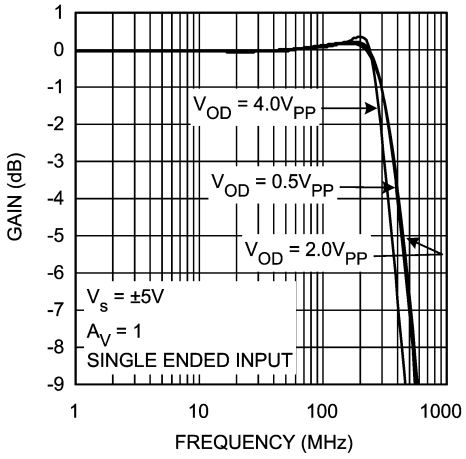
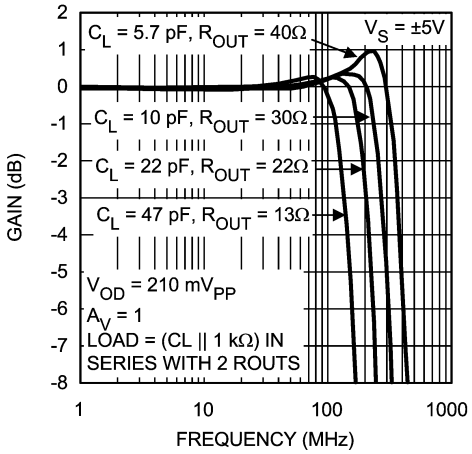
Frequency Response vs. V_{OUT}



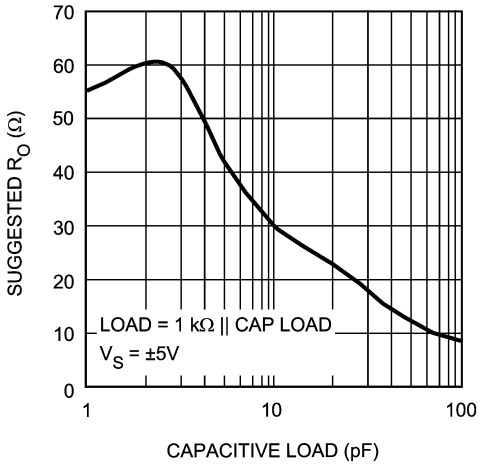
20130116

Frequency Response vs. Capacitive Load



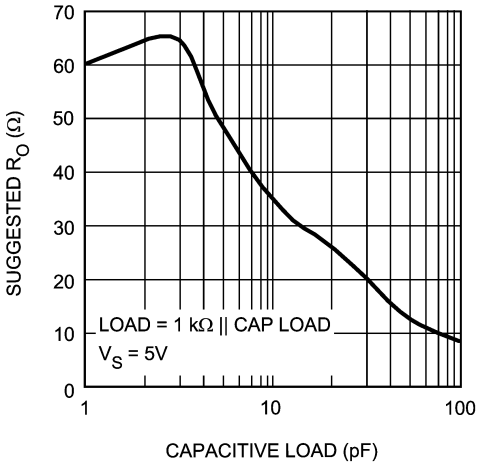
20130121

Suggested R_{OUT} vs. Cap Load



20130122

Suggested R_{OUT} vs. Cap Load



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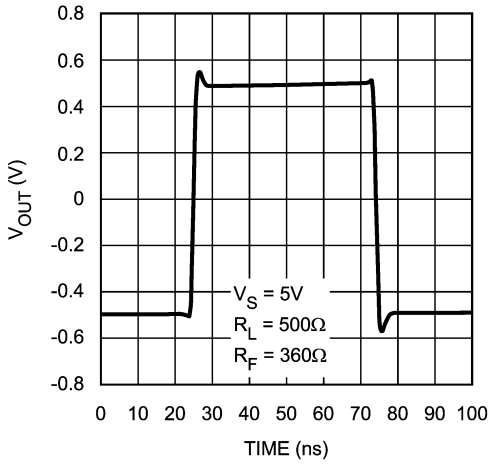
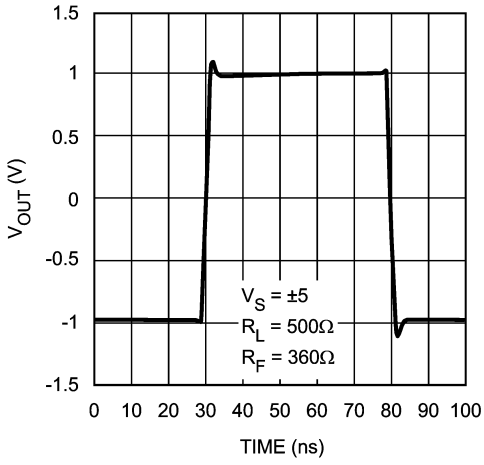
Typical Performance Characteristics (T_A = 25˚C, V_S = ±5V, R_L = 500Ω, R_F = 365Ω, A_V=+1; Unless Specified). (Continued)

1 V_{PP} Pulse Response Single Ended Input



20130126

2 V_{PP} Pulse Response Single Ended Input



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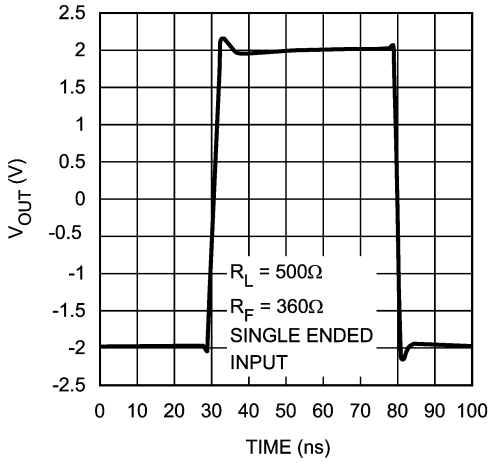
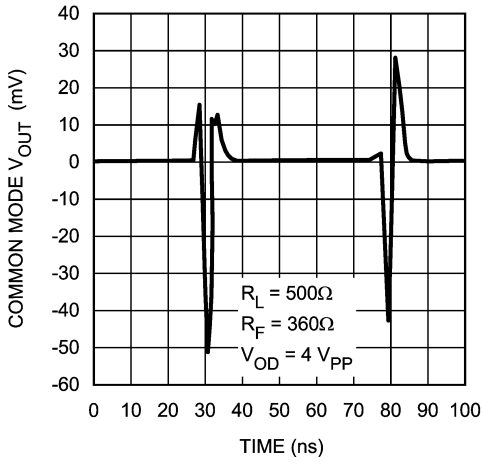
Large Signal Pulse Response



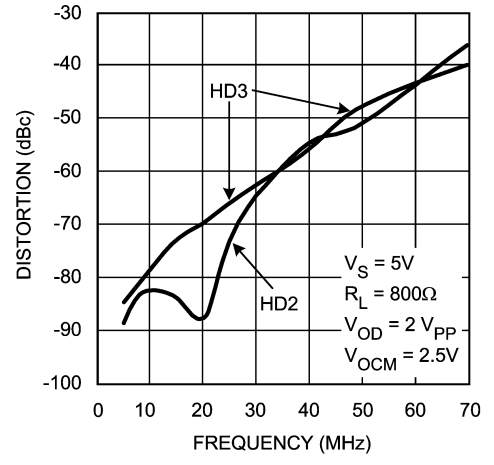
20130125

Output Common Mode Pulse Response



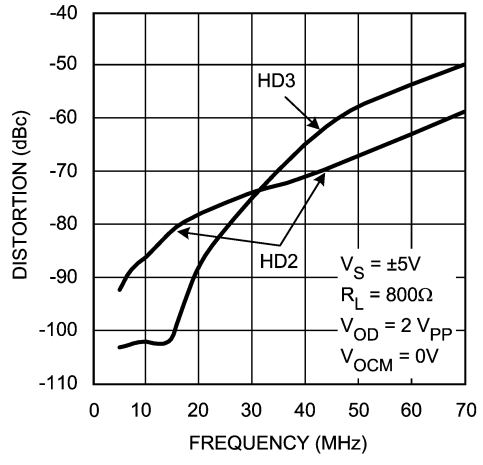
20130124

Distortion vs. Frequency Single Ended Input



20130128

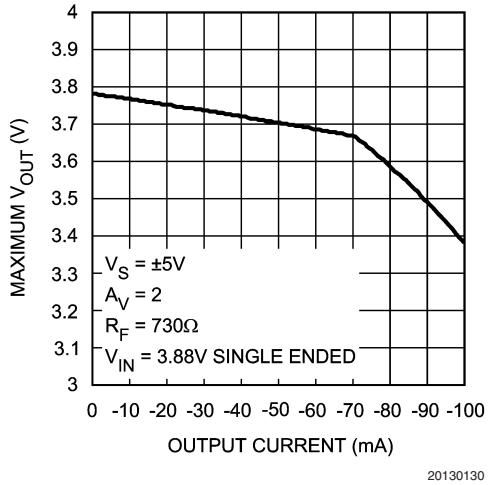
Distortion vs. Frequency Single Ended Input



20130129

Typical Performance Characteristics (T_A = 25˚C, V_S = ±5V, R_L = 500Ω, R_F = 365Ω, A_V=+1; Unless Specified). (Continued)

Maximum V_{OUT} vs. I_{OUT}



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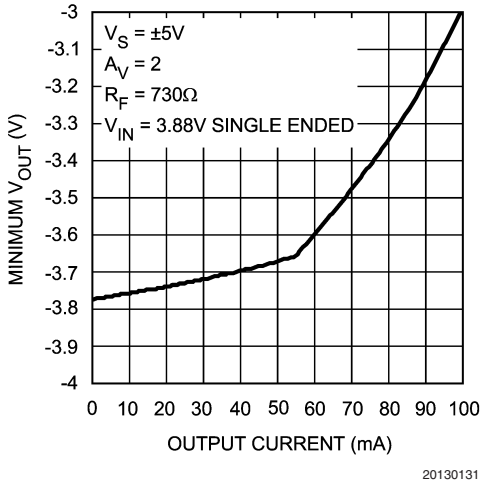
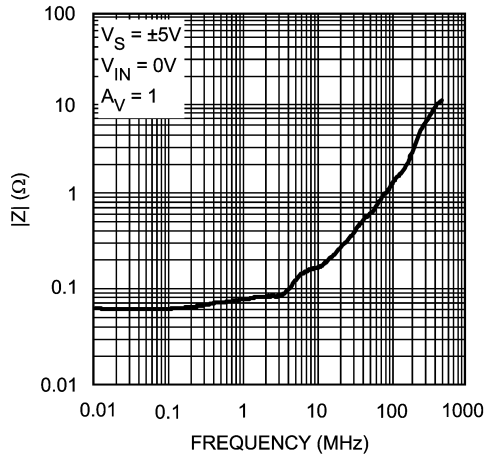
Minimum V_{OUT} vs. I_{OUT}



20130131

Closed Loop Output Impedance



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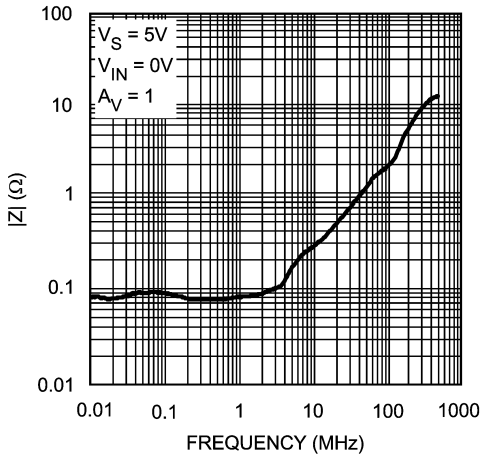
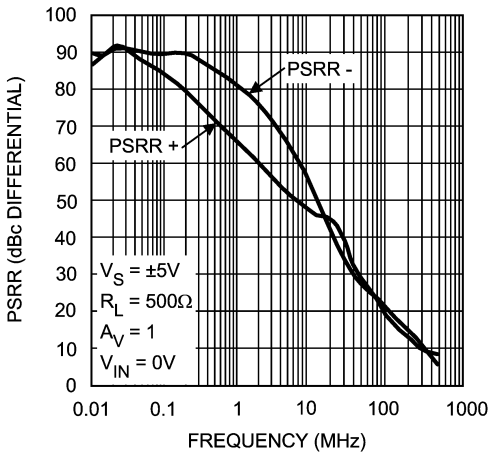
Closed Loop Output Impedance



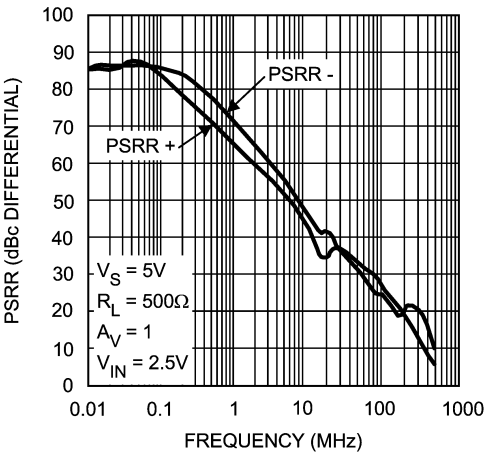
20130118

PSRR



20130119

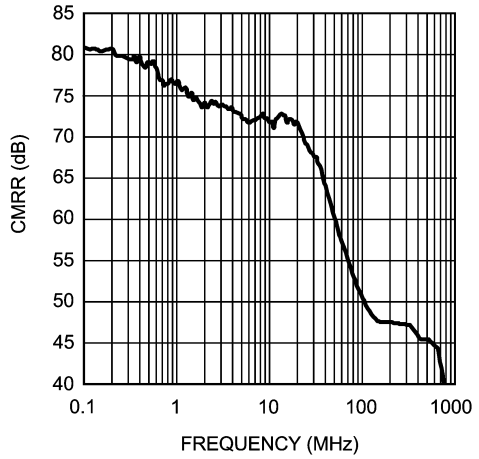
PSRR



20130120

Typical Performance Characteristics (T_A = 25˚C, V_S = ±5V, R_L = 500Ω, R_F = 365Ω, A_V=+1; Unless Specified). (Continued)

CMRR



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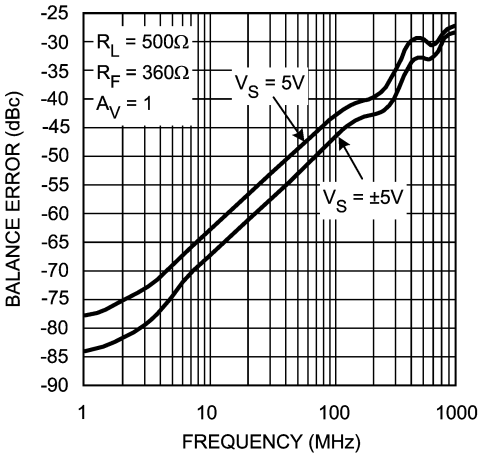
Balance Error



20130113

Application Section

The LMH6550 is a fully differential amplifier designed to provide low distortion amplification to wide bandwidth differential signals. The LMH6550, though fully integrated for ultimate balance and distortion performance, functionally provides three channels. Two of these channels are the V^+ and V^- signal path channels, which function similarly to inverting mode operational amplifiers and are the primary signal paths. The third channel is the common mode feedback circuit. This is the circuit that sets the output common mode as well as driving the V^+ and V^- outputs to be equal magnitude and opposite phase, even when only one of the two input channels is driven. The common mode feedback circuit allows single ended to differential operation.

The LMH6550 is a voltage feedback amplifier with gain set by external resistors. Output common mode voltage is set by the V_{CM} pin. This pin should be driven by a low impedance reference and should be bypassed to ground with a 0.1 µF ceramic capacitor. Any signal coupling into the V_{CM} will be passed along to the output and will reduce the dynamic range of the amplifier.

The LMH6550 is equipped with a ENABLE pin to reduce power consumption when not in use. The ENABLE pin floats to logic high. If this pin is not used it can be left floating. The amplifier output stage goes into a high impedance state when the amplifier is disabled. The feedback and gain set resistors will then set the impedance of the circuit. For this reason input to output isolation will be poor in the disabled state.

FULLY DIFFERENTIAL OPERATION

The LMH6550 will perform best when used with split supplies and in a fully differential configuration. See *Figure 1* and *Figure 3* for recommend circuits.

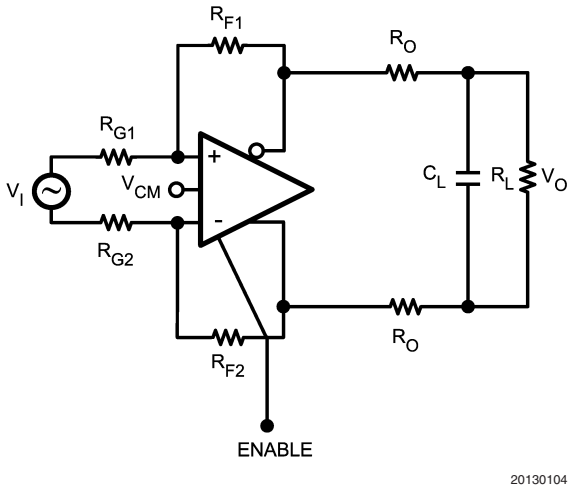


FIGURE 1. Typical Application

The circuit shown in *Figure 1* is a typical fully differential application as might be used to drive an ADC. In this circuit closed loop gain, $(A_V) = V_{OUT}/ V_{IN} = R_F/R_G$. For all the applications in this data sheet $V_{IN}$is presumed to be the voltage presented to the circuit by the signal source. For differential signals this will be the difference of the signals on each input (which will be double the magnitude of each individual signal), while in single ended inputs it will just be the driven input signal.

The resistors R_O help keep the amplifier stable when presented with a load C_L as is typical in an analog to digital converter (ADC). When fed with a differential signal, the LMH6550 provides excellent distortion, balance and common mode rejection provided the resistors R_F, R_G and R_O are well matched and strict symmetry is observed in board layout. With a DC CMRR of over 80dB, the DC and low frequency CMRR of most circuits will be dominated by the external resistors and board trace resistance. At higher frequencies board layout symmetry becomes a factor as well. Precision resistors of at least 0.1% accuracy are recommended and careful board layout will also be required.

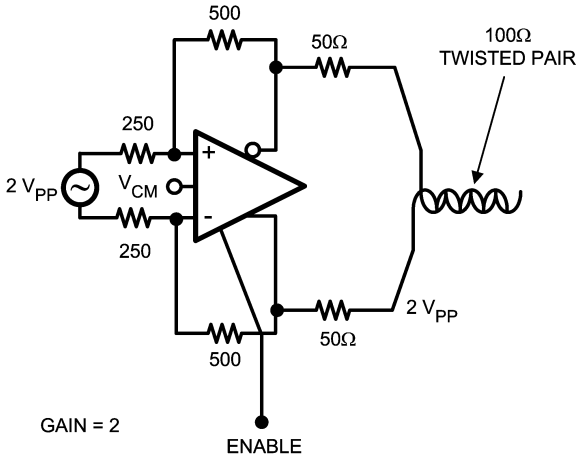
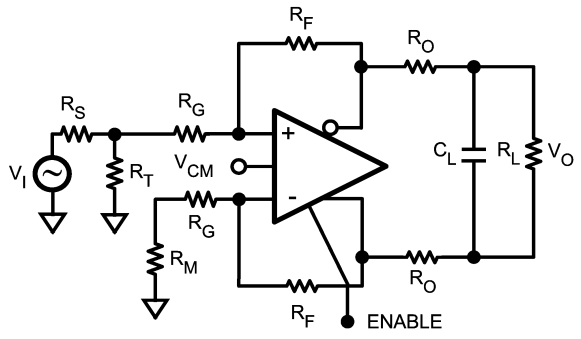


FIGURE 2. Fully Differential Cable Driver

With up to 15 V_{PP} differential output voltage swing and 80 mA of linear drive current the LMH6550 makes an excellent cable driver as shown in *Figure 2*. The LMH6550 is also suitable for driving differential cables from a single ended source.



$$\text{SET } R_M = R_T || R_S$$

$$\text{SET } R_T = \frac{1}{\left(\frac{1}{R_S} - \frac{1}{R_{IN}}\right)} \qquad R_{IN} = \frac{R_G}{1 - \left(\frac{R_F}{2^* (R_F + R_G)}\right)}$$

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FIGURE 3. Single Ended in Differential Out

Application Section (Continued)

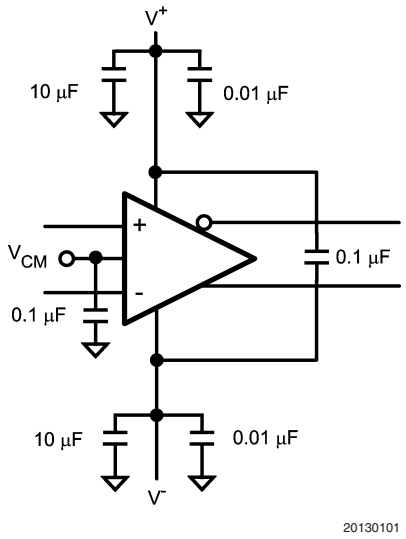

FIGURE 4. Split Supply Bypassing Capacitors

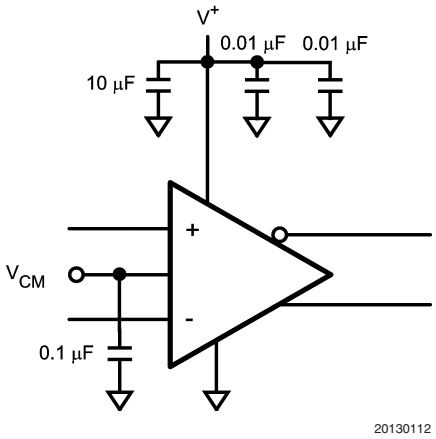

FIGURE 5. Single Supply Bypassing Capacitors

The LMH6550 requires supply bypassing capacitors as shown in *Figure 4* and *Figure 5*. The 0.01 µF and 0.1 µF capacitors should be leadless SMT ceramic capacitors and should be no more than 3 mm from the supply pins. The SMT capacitors should be connected directly to a ground plane. Thin traces or small vias will reduce the effectiveness of bypass capacitors. Also shown in both figures is a capacitor from the V_{CM} pin to ground. The V_{CM} pin is a high impedance input to a buffer which sets the output common mode voltage. Any noise on this input is transferred directly to the output. Output common mode noise will result in loss of dynamic range, degraded CMRR, degraded Balance and higher distortion. The V_{CM} pin should be bypassed even if the pin in not used. There is an internal resistive divider on chip to set the output common mode voltage to the mid point of the supply pins. The impedance looking into this pin is approximately 25kΩ. If a different output common mode voltage is desired drive this pin with a clean, accurate voltage reference.

Application Section (Continued)

SINGLE ENDED INPUT TO DIFFERENTIAL OUTPUT

The LMH6550 provides excellent performance as an active balun transformer. *Figure 3* shows a typical application where an LMH6550 is used to produce a differential signal from a single ended source. It should be noted that compared to differential input, using a single ended input will reduce gain by 1/2. So that the closed loop gain will be; Gain = Av = 0.5 * R_F/R_G.

In single ended input operation the output common mode voltage is set by the V_{CM}pin as in fully differential mode. Also, In this mode the common mode feedback circuit must recreate the signal that is not present on the unused differential input pin. The performance chart titled “Balance Error” is the measurement of the effectiveness of this process. The common mode feedback circuit is responsible for ensuring balanced output with a single ended input. Balance error is defined as the amount of input signal that couples into the output common mode. It is measured as a the undesired output common mode swing divided by the signal on the input. Balance error can be caused by either a channel to channel gain error, or phase error. Either condition will produce a common mode shift. The chart titled “Balance Error” measures the balance error with a single ended input as that is the most demanding mode of operation for the amplifier.

Supply and V_{CM}pin bypassing are also critical in this mode of operation. See the above section on FULLY DIFFERENTIAL OPERATION for bypassing recommendations also see *Figure 4* and *Figure 5* for recommended supply bypassing configurations.

SINGLE SUPPLY OPERATION

The input stage of the LMH6550 has a built in offset of 0.7V towards the lower supply to accommodate single supply operation with single ended inputs. As shown in *Figure 6*, the input common mode voltage is less than the output common voltage. It is set by current flowing through the feedback network from the device output. The input common mode range of 0.4V to 3.2V places constraints on gain settings. Possible solutions to this limitation include AC coupling the input signal, using split power supplies and limiting stage gain. AC coupling with single supply is shown in *Figure 7*.

In *Figure 6* below closed loop gain = $A_V = R_F/R_G$. Please note that in single ended to differential operation V_{IN} is measured single ended while V_{OUT} is measured differentially. This means that gain is really 1/2 or 6 dB less when measured on either of the output pins separately.

V_{ICM}= Input common mode voltage = $(V^+_{IN}+V^-_{IN})/2$.

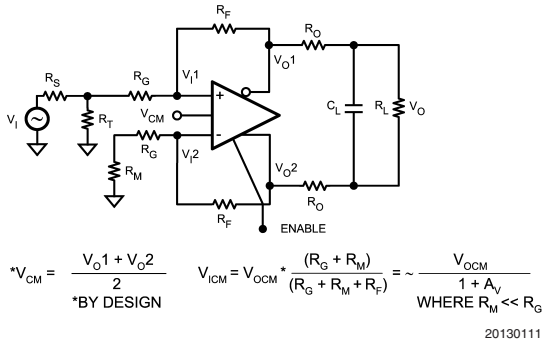

FIGURE 6. Relating $A_V$to Input/Output Common Mode Voltages

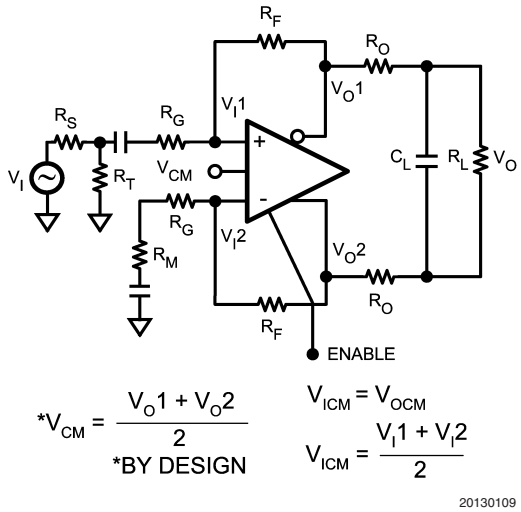

FIGURE 7. AC Coupled for Single Supply Operation

DRIVING ANALOG TO DIGITAL CONVERTERS

Analog to digital converters (ADC) present challenging load conditions. They typically have high impedance inputs with large and often variable capacitive components. As well, there are usually current spikes associated with switched capacitor or sample and hold circuits. *Figure 8* shows a typical circuit for driving an ADC. The two 56Ω resistors serve to isolate the capacitive loading of the ADC from the amplifier and ensure stability. In addition, the resistors form part of a low pass filter which helps to provide anti alias and noise reduction functions. The two 39 pF capacitors help to smooth the current spikes associated with the internal switching circuits of the ADC and also are a key component in the low pass filtering of the ADC input. In the circuit of *Figure 8*the cutoff frequency of the filter is 1/ (2*π*56Ω *(39 pF + 14pF)) = 53MHz (which is slightly less than the sampling frequency). Note that the ADC input capacitance must be factored into the frequency response of the input filter, and that being a differential input the effective input capacitance is double. Also as shown in *Figure 8* the input capacitance to many ADCs is variable based on the clock cycle. See the data sheet for your particular ADC for details.

Application Section (Continued)

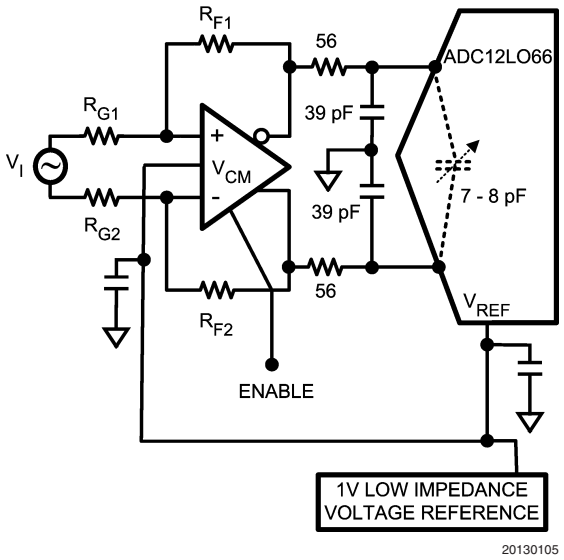

FIGURE 8. Driving an ADC

The amplifier and ADC should be located as closely together as possible. Both devices require that the filter components be in close proximity to them. The amplifier needs to have minimal parasitic loading on the output traces and the ADC is sensitive to high frequency noise that may couple in on its input lines. Some high performance ADCs have an input stage that has a bandwidth of several times its sample rate. The sampling process results in all input signals presented to the input stage mixing down into the Nyquist range (DC to Fs/2). See AN-236 for more details on the subsampling process and the requirements this imposes on the filtering necessary in your system.

USING TRANSFORMERS

Transformers are useful for impedance transformation as well as for single to differential, and differential to single ended conversion. A transformer can be used to step up the output voltage of the amplifier to drive very high impedance loads as shown in *Figure 9*. *Figure 11* shows the opposite case where the output voltage is stepped down to drive a low impedance load.

Transformers have limitations that must be considered before choosing to use one. Compared to a differential amplifier, the most serious limitations of a transformer are the inability to pass DC and balance error (which causes distortion and gain errors). For most applications the LMH6550 will have adequate output swing and drive current and a transformer will not be desirable. Transformers are used primarily to interface differential circuits to 50Ω single ended test equipment to simplify diagnostic testing.

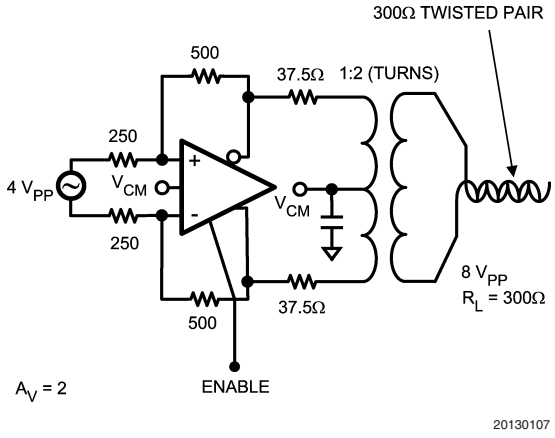

FIGURE 9. Transformer Out High Impedance Load

$$V_L = \frac{V_{IN} * A_V * N}{\left(\frac{2\,R_{OUT} * N^2}{R_L} + 1\right)}$$

WHERE V_{IN} = DIFFERENTIAL INPUT VOLTAGE

$$N = \text{TRANSFORMER TURNS RATIO} = \left(\frac{\text{SECONDARY}}{\text{PRIMARY}}\right)$$

A_V = CLOSED LOOP AMPLIFIER GAIN

R_{OUT} = SERIES OUTPUT MATCHING RESISTOR

R_L = LOAD RESISTOR

V_L = VOLTAGE ACROSS LOAD RESISTOR

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FIGURE 10. Calculating Transformer Circuit Net Gain

Application Section (Continued)

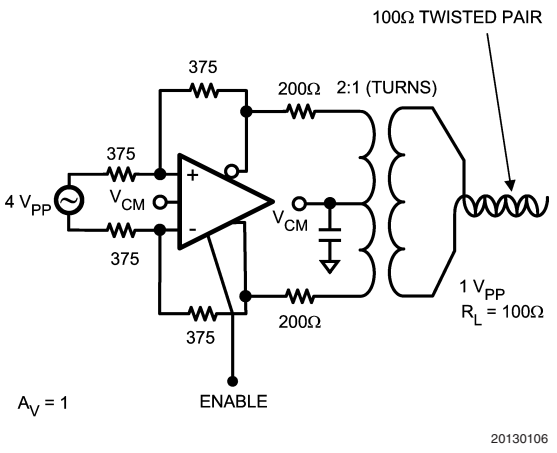


FIGURE 11. Transformer Out Low Impedance Load

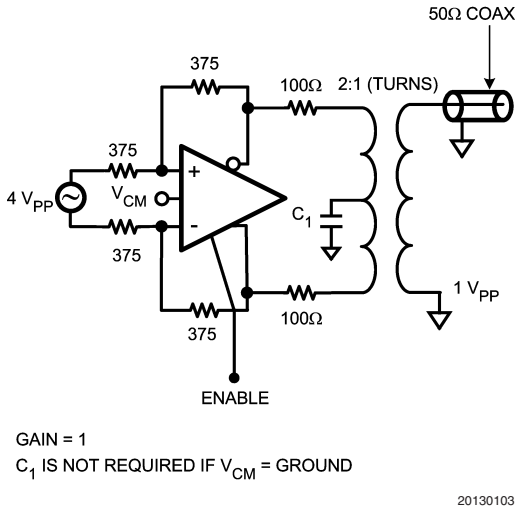


FIGURE 12. Driving 50Ω Test Equipment

CAPACITIVE DRIVE

As noted in the Driving ADC section, capacitive loads should be isolated from the amplifier output with small valued resistors. This is particularly the case when the load has a resistive component that is 500Ω or higher. A typical ADC has capacitive components of around 10 pF and the resistive component could be 1000Ω or higher. If driving a transmission line, such as 50Ω coaxial or 100Ω twisted pair, using matching resistors will be sufficient to isolate any subsequent capacitance. For other applications see the "Suggested Rout vs. Cap Load" charts in the Typical Performance Characteristics section.

POWER DISSIPATION

The LMH6550 is optimized for maximum speed and performance in the small form factor of the standard SOIC package, and is essentially a dual channel amplifier. To ensure maximum output drive and highest performance, thermal shutdown is not provided. Therefore, it is of utmost importance to make sure that the T_{JMAX} is never exceeded due to the overall power dissipation.

Follow these steps to determine the Maximum power dissipation for the LMH6550:

1. Calculate the quiescent (no-load) power: $P_{AMP} = I_{CC}^* (V_S)$, where $V_S = V^+ - V^-$. (Be sure to include any current through the feedback network if V_{OCM} is not mid rail.)
2. Calculate the RMS power dissipated in each of the output stages: P_D (rms) = rms $((V_S - V^+_{OUT}) * I^+_{OUT})$ + rms $((V_S - V^-_{OUT}) * I^-_{OUT})$, where V_{OUT} and I_{OUT} are the voltage and the current measured at the output pins of the differential amplifier as if they were single ended amplifiers and V_S is the total supply voltage.
3. Calculate the total RMS power: $P_T = P_{AMP} + P_D$.

The maximum power that the LMH6550 package can dissipate at a given temperature can be derived with the following equation:

$P_{MAX} = (150^\circ - T_{AMB})/ \theta_{JA}$, where T_{AMB} = Ambient temperature (°C) and θ_{JA} = Thermal resistance, from junction to ambient, for a given package (°C/W). For the SOIC package θ_{JA} is 150°C/W.

NOTE: If V_{CM} is not 0V then there will be quiescent current flowing in the feedback network. This current should be included in the thermal calculations and added into the quiescent power dissipation of the amplifier.

ESD PROTECTION

The LMH6550 is protected against electrostatic discharge (ESD) on all pins. The LMH6550 will survive 2000V Human Body model and 200V Machine model events. Under normal operation the ESD diodes have no effect on circuit performance. There are occasions, however, when the ESD diodes will be evident. If the LMH6550 is driven by a large signal while the device is powered down the ESD diodes will conduct . The current that flows through the ESD diodes will either exit the chip through the supply pins or will flow through the device, hence it is possible to power up a chip with a large signal applied to the input pins. Using the shutdown mode is one way to conserve power and still prevent unexpected operation.

BOARD LAYOUT

The LMH6550 is a very high performance amplifier. In order to get maximum benefit from the differential circuit architecture board layout and component selection is very critical. The circuit board should have low a inductance ground plane and well bypassed broad supply lines. External components should be leadless surface mount types. The feedback network and output matching resistors should be composed of short traces and precision resistors (0.1%). The output matching resistors should be placed within 3-4 mm of the amplifier as should the supply bypass capacitors. The LMH730154 evaluation board is an example of good layout techniques. Evaluation boards are available free of charge through the product folder on National's web site.

The LMH6550 is sensitive to parasitic capacitances on the amplifier inputs and to a lesser extent on the outputs as well. Ground and power plane metal should be removed from beneath the amplifier and from beneath R_F and R_G.

With any differential signal path symmetry is very important. Even small amounts of assymetery will contribute to distortion and balance errors.

Application Section (Continued)

EVALUATION BOARD

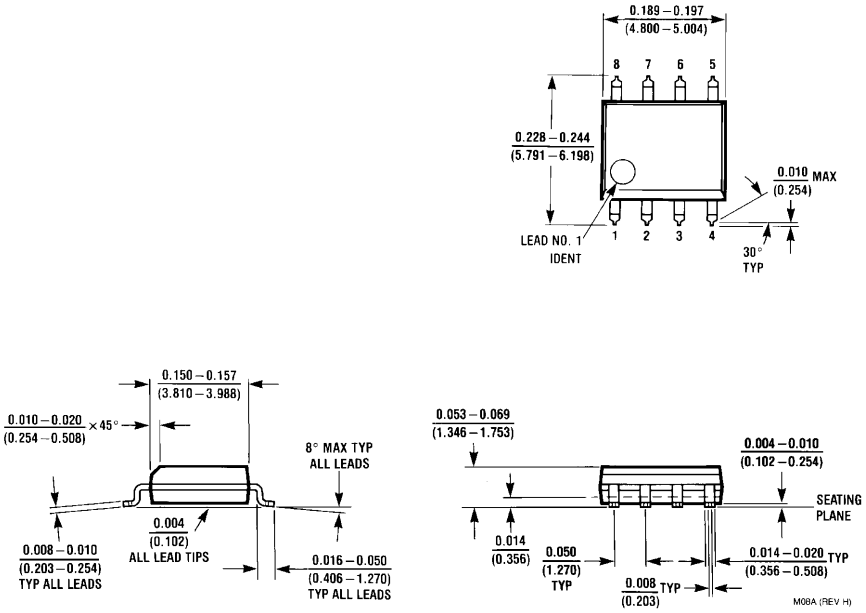
Generally, a good high frequency layout will keep power supply and ground traces away from the inverting input and output pins. Parasitic capacitances on these nodes to ground will cause frequency response peaking and possible circuit oscillations (see Application Note OA-15 for more information). National Semiconductor suggests the following evaluation boards as a guide for high frequency layout and as an aid in device testing and characterization:

Device	Package	Evaluation Board Part Number
LMH6550MA	SOIC	LMH730154

These evaluation boards can be shipped when a device sample request is placed with National Semiconductor.

Physical Dimensions inches (millimeters)

unless otherwise noted



8-Pin SOIC
NS Package Number M08A

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