National Semiconductor

ADVANCE INFORMATION

September 4, 2008

LMH4345, LMH4045, LMH4075
3 Gbps, HD, SD, DVB-ASI SDI Dual Serializer / Deserializer (SER/DES) with Loopthrough and LVDS Interface

General Description

The Dual SER/DES 5:1 Serializer and 1:5 De-serializer provides four independent high-speed Serial Digital Interface (SDI) links, two RX and two TX links, compliant with SMPTE 259M C, SMPTE 292M or SMPTE 424M at datarates of 270 Mbps, 1.5 Gbps or 3 Gbps as applicable. The channels also will support DVB_ASI interfaces, with internal 8b10b coding/decoding. Built-in programmable serializer and deserializer signal conditioning blocks improve signal integrity performance and allow flexible board layout. The input and output of the Dual Serdes are designed to interface easily to FPGA/ASIC devices. Each input or output channel is supported by 5 pairs of high-speed LVDS connections to reduce FPGA pin count as well as provide better signal integrity and EMI performance. The serializer outputs have integrated cable drivers which support SMPTE 259M (270 Mb/s), SMPTE 292M, and SMPTE 424M standards with excellent output jitter performance. Each Deserializer channel has a reclocked loopthrough output which also has an integrated cable driver. When paired with a host FPGA the LMH4345 deserializers automatically detect the incoming data rate and decode the raw 5-bit data words compliant to any of the supported standards. The interface between the LMH4345 and the host FPGA consists of four 5-bit wide LVDS buses (two input and two output), an LVDS clock per channel and an SMBus interface. No external VCOs or clocks are required. The LMH4345 receivers detect the frequency from the incoming data stream, generate a clean clock and transmit both clock and data to the host FPGA. Refer to table 1 for a listing of the variants of this product offered. National Semiconductor also offers single serializers and single deserializers as a part of the FPGA-Attach SER/DES product family.

The FPGA-Attach SER/DES product family is supported by a suite of IP which allows the design engineer to quickly develop video applications using the SER/DES products. The product is packaged in a 100 pin TQFP package.

Key Specifications

- Output compliant with SMPTE 259M-C, SMPTE 292M, SMPTE 424M and DVB-ASI
- Typical power dissipation: TBD mW (loopthrough disabled, 3G datarate)
- Jitter Tolerance (Deserializer) 0.6UI
- Output Jitter (Serializers) 0.1 UI

Features

- Two Independent Serializers and Two Independent Deserializers
- No external VCO or clocks required
- Reclocked serial loopthrough with Cable Driver
- Integrated Cable Drivers
- Powerdown Mode
- 3.3V SMBus configuration interface
- Small 100 Pin TQFP package
- Industrial Temperature range:-40°C to +85°C

Applications

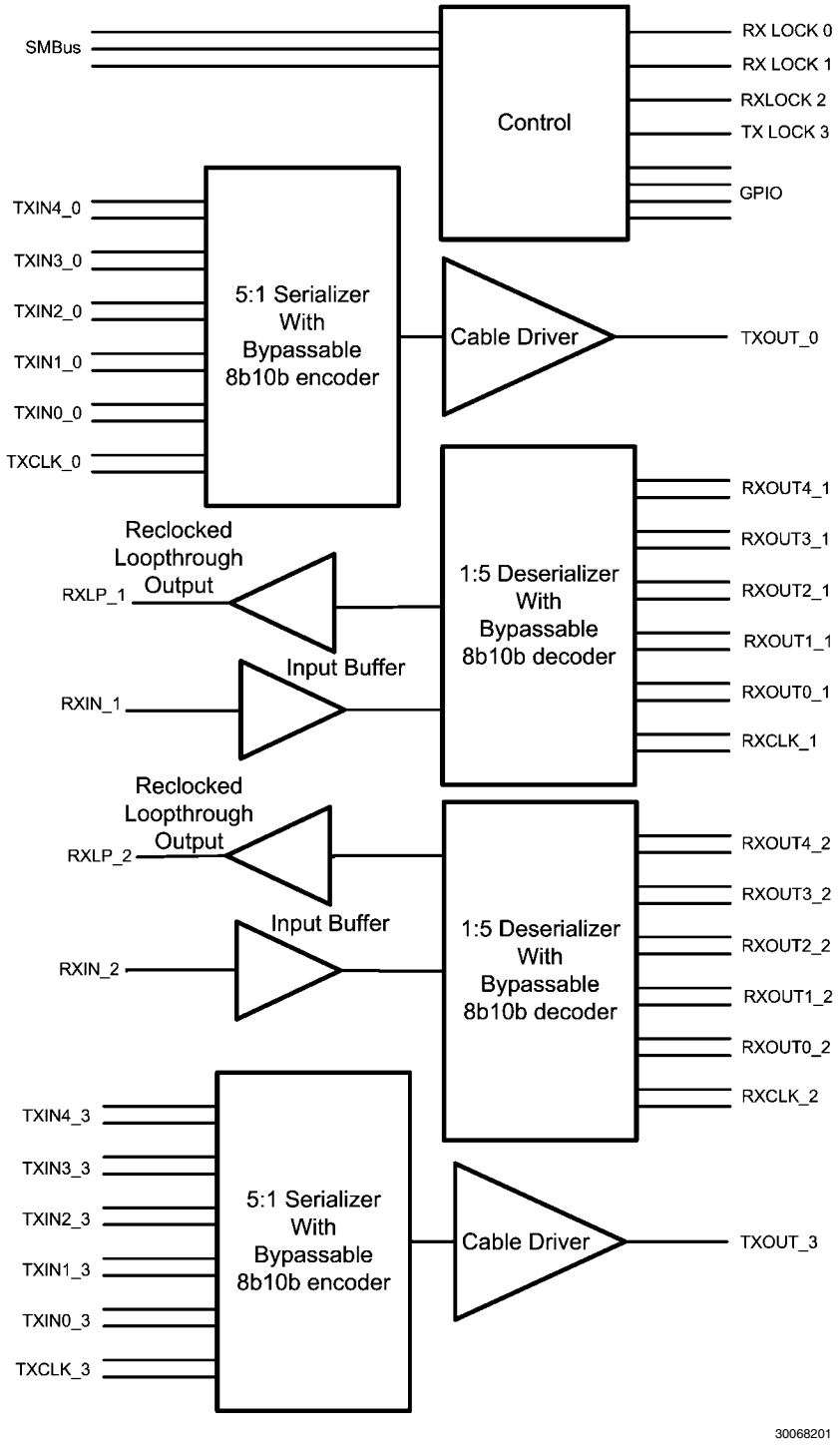
- SDI interfaces for:
  - Video Cameras
  - DVRs
  - Video Switchers
  - Video Editing Systems

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General Block Diagram



Pin Descriptions

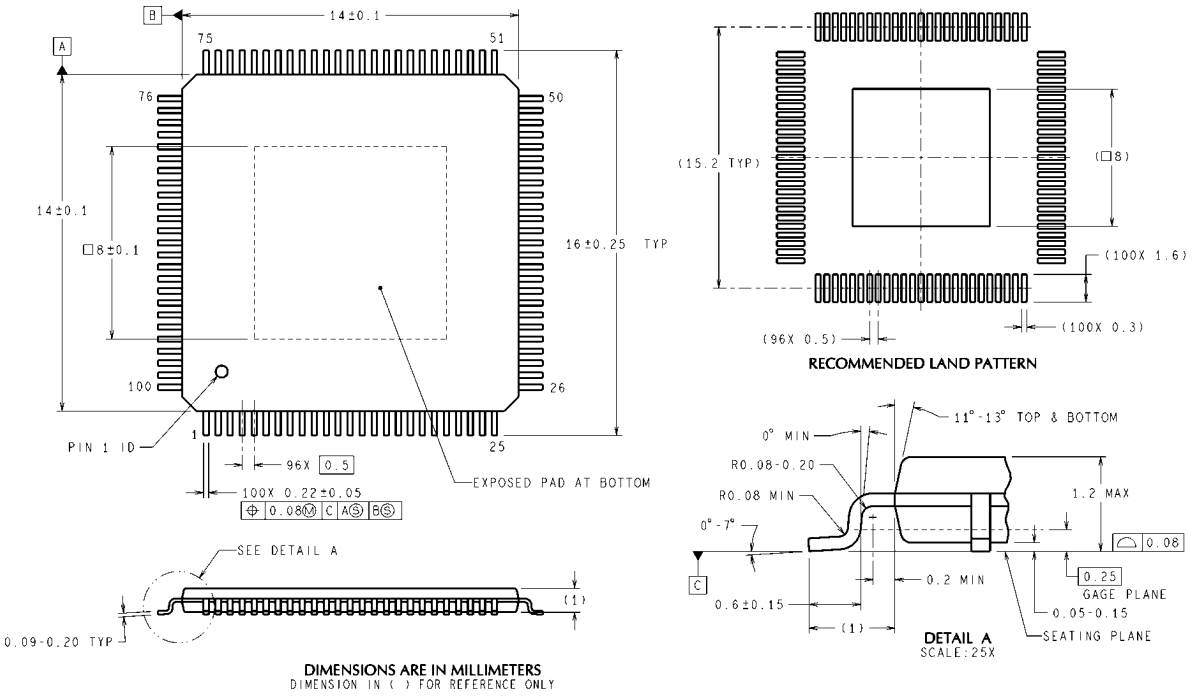
Pin Name	Type	Description
LVDS HOST Interface		
RXOUT[4:0]_1± RXOUT[4:0]_2±	Output, LVDS	LVDS Data Output Pins Two, Five channel wide DDR interfaces.
RXCLK_1± RXCLK_2±	Output, LVDS	LVDS Clock Output Pins DDR Interfaces.
TXIN[4:0]_0± TXIN[4:0]_3±	Input, LVDS	LVDS Data Input Pins Five bit wide DDR interfaces, internal 100Ω termination.
TXCLK_0± TXCLK_3±	Input, LVDS	LVDS Clock Input Pins DDR Interface, Internal 100Ω termination.
Serial Data Inputs		
$RXIN_1$±	Input, Differential	Serial differential input Pins Channel 1
$RXIN_2$±	Input, Differential	Serial differential input Pins Channel 2
Serial Data Outputs		
TXOUT_0±	Serializer output, channel 0	Serial Differential Output Pins Channel 0
TXOUT_3±	Serializer output, channel 3	Serial Differential Output Pins Channel 3
RXLP_1±	Deserializer output, channel 1	Differential Reclocked Loopthrough output channel 1
RXLP_2±	Deserializer output, channel 2	Differential Reclocked Loopthrough output channel 2
SMBus Interface		
SDA	I/O, LVCMOS	SMBus Data I/O Pin
SCK	Input, LVCMOS	SMBus Clock Input Pin
SMB_CS	Input, LVCMOS	SMBus Chip Select Input Pin Device is selected when High.
Control and Configuration Pins		
$\overline{\text{RESET}}$	Input, LVCMOS	Reset Input Pin H = normal mode L = device in RESET
$\overline{\text{LOCK0}}$, $\overline{\text{LOCK1}}$, $\overline{\text{LOCK2}}$, $\overline{\text{LOCK3}}$	Output, LVCMOS	PLL LOCK Status Output H = unlock condition L = PLL is Locked Each Lock pin corresponds to one channel.
GPIO[3:0]	I/O, LVCMOS	General Purpose Input / Output Software configurable I/O pins.
RSVD_L	Input, LVCMOS	Configuration Input – **Must tie Low** Connect to GND for normal operation

Pin Name	Type	Description
Analog Inputs		
R_{SET}	Input	SDI Output Amplitude Control Resistor connected from this pin to ground to set the signal amplitude for all four SDI outputs. Nominally 8.06kΩ for 800mV output (SMPTE Compliant).
LF_CP0, LF_CP1, LF_CP2, LF_CP3	Input	Loop Filter Connection
LF_REF0, LF_REF1, LF_REF2, LF_REF3		Loop Filter Reference
Power Supply and Ground		
V_{DD3V3}	Power	3.3V Power Supply connection
V_{DDPLL}	Power	3.3V PLL Power Supply connection
V_{DD2V5}	Power	2.5V Power Supply connection
V_{DD2V5A}	Power	Analog 2.5V Power Supply connection
GND	Ground	Ground connection – The DAP (large center pad) is the primary GND connection for the device and must be connected to Ground along with the GND pins.

TABLE 1. Feature Table

Device	SMPTE 424M Support	SMPTE 292M Support	SMPTE 259M Support	DVB-ASI Support
LMH4345	×	×	×	×
LMH4045		×	×	×
LMH4075			×	×

Physical Dimensions inches (millimeters) unless otherwise noted



VXF100A (Rev A)

100-Lead TQFP Package
NS Package Number VXF100A

Notes

For more National Semiconductor product information and proven design tools, visit the following Web sites at:

Products		Design Support	
Amplifiers	www.national.com/amplifiers	WEBENCH	www.national.com/webench
Audio	www.national.com/audio	Analog University	www.national.com/AU
Clock Conditioners	www.national.com/timing	App Notes	www.national.com/appnotes
Data Converters	www.national.com/adc	Distributors	www.national.com/contacts
Displays	www.national.com/displays	Green Compliance	www.national.com/quality/green
Ethernet	www.national.com/ethernet	Packaging	www.national.com/packaging
Interface	www.national.com/interface	Quality and Reliability	www.national.com/quality
LVDS	www.national.com/lvds	Reference Designs	www.national.com/refdesigns
Power Management	www.national.com/power	Feedback	www.national.com/feedback
Switching Regulators	www.national.com/switchers		
LDOs	www.national.com/ldo		
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PowerWise	www.national.com/powerwise		
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Wireless (PLL/VCO)	www.national.com/wireless		

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