LMC6001-MIL Ultra, Ultra-Low Input Current Amplifier

1 Features

- (Maximum Limit, 25°C Unless Otherwise Noted)
- Input Current (100% Tested): 25 fA
- Input Current Over Temperature: 2 pA
- Low Power: 750 µA
- Low V_{OS}: 350 µV
- Low Noise: 22 nV/√Hz at 1 kHz Typical

2 Applications

- Electrometer Amplifiers
- Photodiode Preamplifiers
- Ion Detectors
- A.T.E. Leakage Testing

3 Description

Featuring 100% tested input currents of 25 fA maximum, low operating power, and ESD protection of 2000 V, the LMC6001-MIL device achieves a new industry benchmark for low input current operational amplifiers. By tightly controlling the molding compound, Texas Instruments is able to offer this ultra-low input current in a lower cost molded package.

To avoid long turnon settling times common in other low input current op amps, the LMC6001A is tested three times in the first minute of operation. Even units that meet the 25-fA limit are rejected if they drift.

Because of the ultra-low input current noise of 0.13 fA/√Hz, the LMC6001-MIL can provide almost noiseless amplification of high resistance signal sources. Adding only 1 dB at 100 kΩ, 0.1 dB at 1 MΩ and 0.01 dB or less from 10 MΩ to 2,000 MΩ, the LMC6001-MIL is an almost noiseless amplifier.

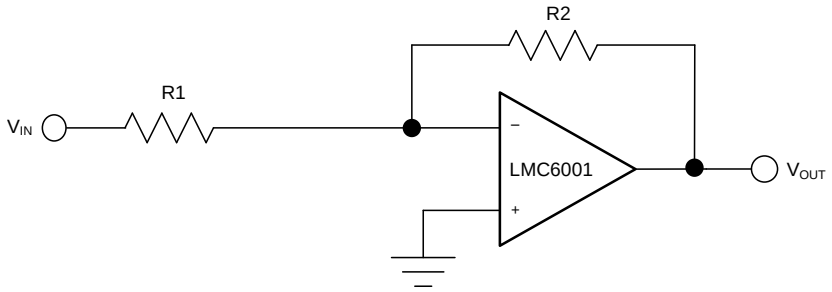
The LMC6001-MIL is ideally suited for electrometer applications requiring ultra-low input leakage such as sensitive photodetection transimpedance amplifiers and sensor amplifiers. Because input referred noise is only 22 nV/√Hz, the LMC6001-MIL can achieve higher signal to noise ratio than JFET input type electrometer amplifiers. Other applications of the LMC6001-MIL include long interval integrators, ultra-high input impedance instrumentation amplifiers, and sensitive electrical-field measurement circuits.

Device Information(1)

PART NUMBER	PACKAGE	BODY SIZE (NOM)
LMC6001-MIL	PDIP (8)	9.81 mm × 6.35 mm
	TO-99 (8)	9.08 mm × 9.08 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.

Simplified Schematic



An IMPORTANT NOTICE at the end of this data sheet addresses availability, warranty, changes, use in safety-critical applications, intellectual property matters and other important disclaimers. PRODUCTION DATA.

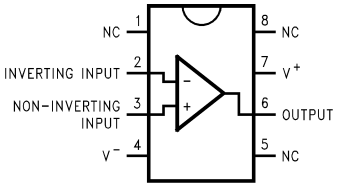
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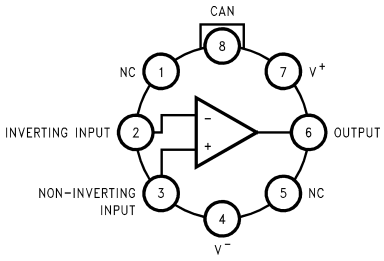
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4 Pin Configuration and Functions

P Package
8-Pin PDIP
Top View



LMC Package
8-Pin TO-99
Top View



Pin Functions

PIN			I/O	DESCRIPTION
NAME	PDIP NO.	TO-99 NO.		
CAN	—	8	—	No internal connection; connected to the external casing.
+IN	3	3	I	Noninverting Input
–IN	2	2	I	Inverting Input
NC	1, 5, 8	1, 5	—	No connection
OUTPUT	6	6	O	Output
V+	7	7	—	Positive (higher) power supply
V–	4	4	—	Negative (lower) power supply

5 Specifications

5.1 Absolute Maximum Ratings

Over operating free-air temperature range (unless otherwise noted)(1)(2)

	MIN	MAX	Unit
Differential Input Voltage	±Supply Voltage		
Voltage at Input/Output Pin	(V^+) + 0.3	(V^-) − 0.3	V
Supply Voltage $(V^+ - V^-)$	−0.3	+16	V
Output Short Circuit to V^+	See (3)(4)		
Output Short Circuit to V^-	See (3)		
Lead Temperature (Soldering, 10 Sec.)	260		°C
Junction Temperature	150		°C
Current at Input Pin	±10		mA
Current at Output Pin	±30		mA
Current at Power Supply Pin	40		mA
Storage Temperature, T_{stg}	−65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) If Military/Aerospace specified devices are required, please contact the Texas Instruments Sales Office/ Distributors for availability and specifications.
(3) Applies to both single supply and split supply operation. Continuous short circuit operation at elevated ambient temperature can result in exceeding the maximum allowed junction temperature of 150°C. Output currents in excess of ±30 mA over long term may adversely affect reliability.
(4) Do not connect the output to V^+, when V^+ is greater than 13 V or reliability will be adversely affected.

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5.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001 (1) (2)	±2000	V

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) Human body model, 1.5 kΩ in series with 100 pF.

5.3 Recommended Operating Conditions

Over operating free-air temperature range (unless otherwise noted).

		MIN	MAX	UNIT
V_{SS}	Supply input voltage	4.5	15.5	V
T_J	Operating junction temperature	–40	85	°C

5.4 Thermal Information

THERMAL METRIC (1)		LMC6001-MIL		UNIT
		P (PDIP)	LMC (TO-99)	
		8 PINS	8 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	100	145	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	—	45	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report, SPRA953.

5.5 DC Electrical Characteristics for LMC6001AI

Limits are ensured for T_J = 25°C unless otherwise specified. Unless otherwise specified, V^+ = 5 V, V^- = 0 V, V_{CM} = 1.5 V, and R_L > 1 M.

PARAMETER		TEST CONDITIONS		LMC6001AI			UNIT
				MIN (1)	TYP (2)	MAX (1)	
I_B	Input Current	Either Input, V_{CM} = 0 V, V_S = ±5 V			10	25	fA
			At the temperature extremes			2000	
I_{OS}	Input Offset Current				5		
		At the temperature extremes				1000	
V_{OS}	Input Offset Voltage					0.7	mV
		At the temperature extremes				1	
		V_S = ±5 V, V_{CM} = 0 V				10	
			At the temperature extremes			1.35	
TCV_{OS}	Input Offset Voltage Drift				2.5		µV/°C
R_{IN}	Input Resistance				>1		TΩ
CMRR	Common Mode	0 V ≤ V_{CM} ≤ 7.5 V		75	83		dB
	Rejection Ratio	V^+ = 10 V	At the temperature extremes	72			
+PSRR	Positive Power Supply Rejection Ratio	5 V ≤ V^+ ≤ 15 V		73	83		
			At the temperature extremes	70			
−PSRR	Negative Power Supply Rejection Ratio	0 V ≥ V^- ≥ −10 V		80	94		
			At the temperature extremes	77			
A_V	Large Signal Voltage Gain	Sourcing, R_L = 2 kΩ (3)		400	1400		V/mV
				300			
		Sinking, R_L = 2 kΩ (3)		180	350		
			At the temperature extremes	100			

(1) All limits are specified by testing or statistical analysis.
(2) Typical values represent the most likely parametric norm.
(3) V^+ = 15 V, V_{CM} = 7.5 V and R_L connected to 7.5 V. For Sourcing tests, 7.5 V ≤ V_O ≤ 11.5 V. For Sinking tests, 2.5 V ≤ V_O ≤ 7.5 V.

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DC Electrical Characteristics for LMC6001AI (continued)

Limits are ensured for T_J = 25°C unless otherwise specified. Unless otherwise specified, V^+ = 5 V, V^- = 0 V, V_{CM} = 1.5 V, and R_L > 1 M.

PARAMETER		TEST CONDITIONS			LMC6001AI			UNIT
					MIN(1)	TYP(2)	MAX(1)	
V_{CM}	Input Common-Mode Voltage	V^+ = 5 V and 15 V For CMRR ≥ 60 dB	V_{CM} Low			–0.4	–0.1	V
				At the temperature extremes			0	
			V_{CM} High		V^+ − 2.3	V^+ − 1.9		
				At the temperature extremes	V^+ − 2.5			
V_O	Output Swing	V^+ = 15 V, R_L = 2 kΩ to 2.5 V	V_O Low			0.1	0.14	V
				At the temperature extremes			0.17	
			V_O High		4.8	4.87		
				At the temperature extremes	4.73			
		V^+ = 15 V, R_L = 2 kΩ to 7.5 V	V_O Low			0.26	0.35	
				At the temperature extremes			0.45	
			V_O High		14.5	14.63		
				At the temperature extremes	14.34			
I_O	Output Current	Sourcing, V^+ = 5 V, V_O = 0 V			16	22		mA
			At the temperature extremes		10			
		Sinking, V^+ = 5 V, V_O = 5 V			16	21		
			At the temperature extremes		13			
		Sourcing, V^+ = 15 V, V_O = 0 V			28	30		
			At the temperature extremes		22			
		Sinking, V^+ = 15 V, V_O = 13 V(4)			28	34		
			At the temperature extremes		22			
I_S	Supply Current	V^+ = 5 V, V_O = 1.5 V				450	750	µA
			At the temperature extremes				900	
		V^+ = 15 V, V_O = 7.5 V				550	850	
			At the temperature extremes				950	

(4) Do not connect the output to V + , when V + is greater than 13 V or reliability will be adversely affected.

5.6 Dissipation Ratings

	MIN	MAX	UNIT
Power Dissipation	See (1)		

(1) For operating at elevated temperatures the device must be derated based on the thermal resistance θ_{JA} with $P_D = (T_J - T_A)/\theta_{JA}$.

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5.7 Typical Characteristics

V_S = ±7.5 V, T_A = 25°C, unless otherwise specified

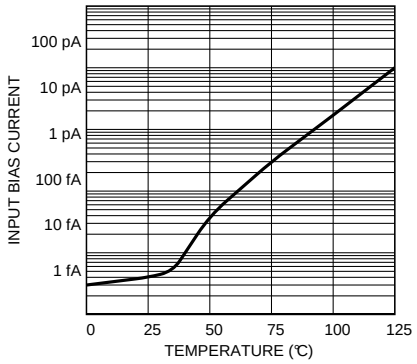
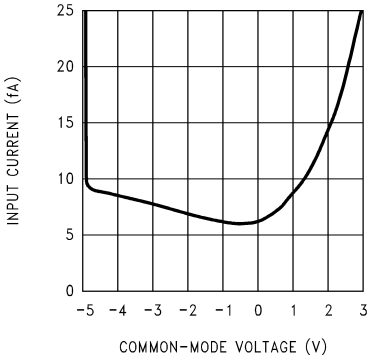


Figure 1. Input Current vs. Temperature



V_S = ±5 V

Figure 2. Input Current vs. V_{CM}

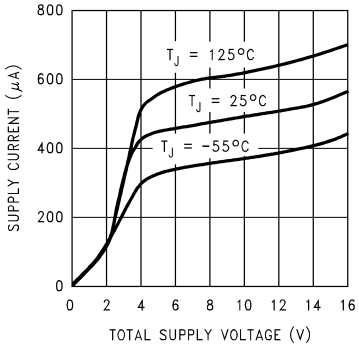


Figure 3. Supply Current vs. Supply Voltage

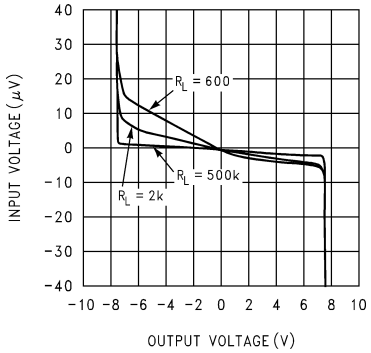


Figure 4. Input Voltage vs. Output Voltage

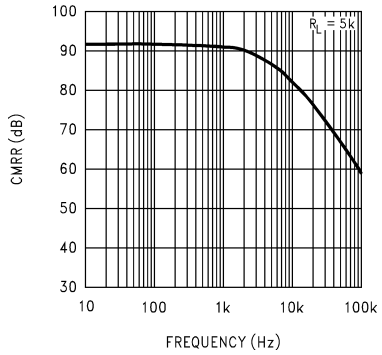


Figure 5. Common-Mode Rejection Ratio vs. Frequency

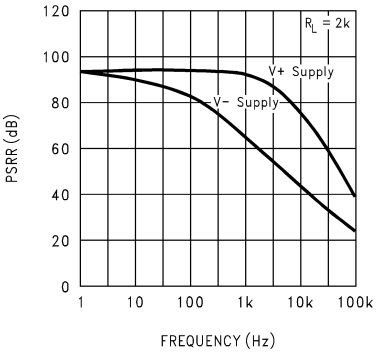


Figure 6. Power Supply Rejection Ratio vs. Frequency

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Typical Characteristics (continued)

V_S = ±7.5 V, T_A = 25°C, unless otherwise specified

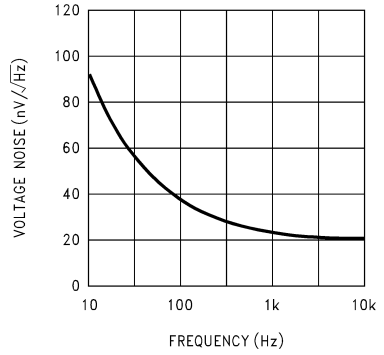


Figure 7. Input Voltage Noise vs. Frequency

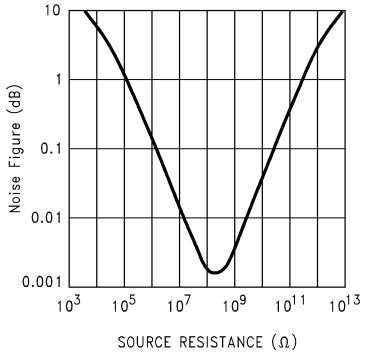


Figure 8. Noise Figure vs. Source Resistance

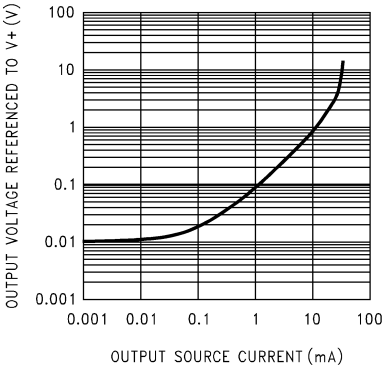


Figure 9. Output Characteristics Sourcing Current

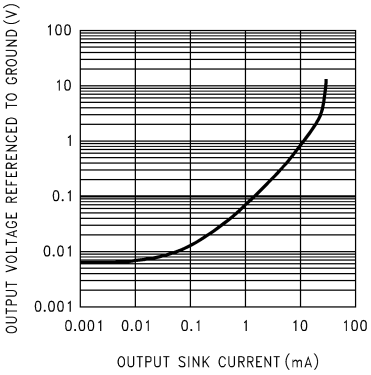


Figure 10. Output Characteristics Sinking Current

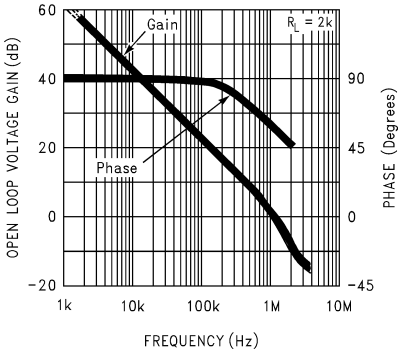
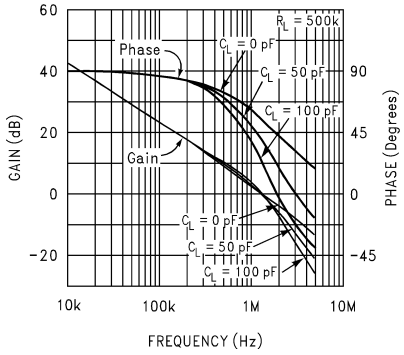


Figure 11. Gain and Phase Response vs. Temperature (−55°C to +125°C)



R_L = 500 kω

Figure 12. Gain and Phase Response vs. Capacitive Load

Typical Characteristics (continued)

V_S = ±7.5 V, T_A = 25°C, unless otherwise specified

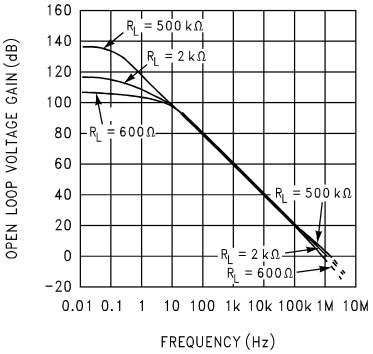


Figure 13. Open-Loop Frequency Response

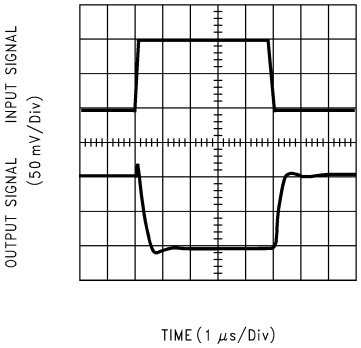


Figure 14. Inverting Small Signal Pulse Response

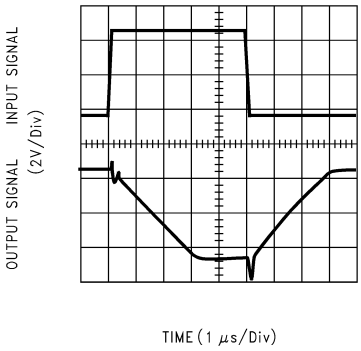


Figure 15. Inverting Large Signal Pulse Response

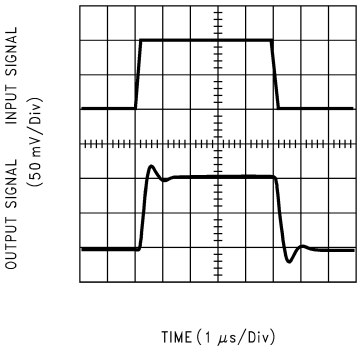


Figure 16. Noninverting Small Signal Pulse Response

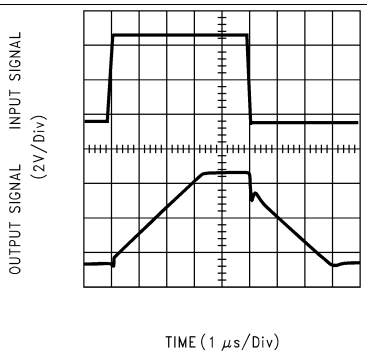


Figure 17. Noninverting Large Signal Pulse Response

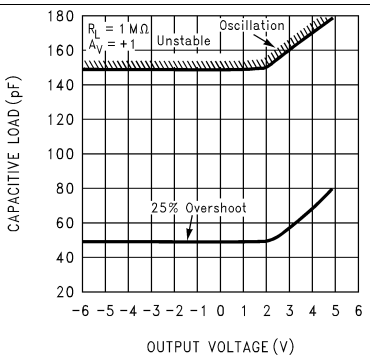


Figure 18. Stability vs. Capacitive Load

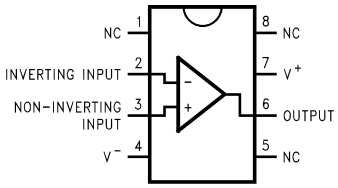
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6 Detailed Description

6.1 Overview

LMC6001-MIL has an extremely low input current of 25 fA. In addition, its ultra-low input current noise of 0.13 fA/√Hz allows almost noiseless amplification of high-resistance signal sources. LMC6001-MIL is ideally suited for electrometer applications requiring ultra-low input leakage current such as sensitive photodetection transimpedance amplifiers and sensor amplifiers.

6.2 Functional Block Diagram



6.3 Feature Description

6.3.1 Amplifier Topology

The LMC6001-MIL incorporates a novel op amp design topology that enables it to maintain rail-to-rail output swing even when driving a large load. Instead of relying on a push-pull unity gain output buffer stage, the output stage is taken directly from the internal integrator, which provides both low output impedance and large gain. Special feed-forward compensation design techniques are incorporated to maintain stability over a wider range of operating conditions than traditional op amps. These features make the LMC6001-MIL both easier to design with, and provide higher speed than products typically found in this low-power class.

6.3.2 Latch-up Prevention

CMOS devices tend to be susceptible to latch-up due to their internal parasitic SCR effects. The (I/O) input and output pins look similar to the gate of the SCR. There is a minimum current required to trigger the SCR gate lead. The LMC6001-MIL is designed to withstand 100-mA surge current on the I/O pins. Some resistive method should be used to isolate any capacitance from supplying excess current to the I/O pins. In addition, like an SCR, there is a minimum holding current for any latch-up mode. Limiting current to the supply pins will also inhibit latch-up susceptibility.

6.4 Device Functional Modes

The LMC6001-MIL has a single functional mode and operates according to the conditions listed in *Recommended Operating Conditions*.

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7 Applications and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

7.1 Application Information

7.1.1 Compensating for Input Capacitance

It is quite common to use large values of feedback resistance for amplifiers with ultra-low input current, like the LMC6001.

Although the LMC6001 is highly stable over a wide range of operating conditions, certain precautions must be met to achieve the desired pulse response when a large feedback resistor is used. Large feedback resistors with even small values of input capacitance, due to transducers, photodiodes, and printed-circuit-board parasitics, reduce phase margins.

When high input impedances are demanded, TI suggests guarding the LMC6001. Guarding input lines will not only reduce leakage, but lowers stray input capacitance as well. See *Printed-Circuit-Board Layout For High-Impedance Work*.

The effect of input capacitance can be compensated for by adding a capacitor, C_f, around the feedback resistors (as in Figure 19) such that:

$$\frac{1}{2\pi R_1 C_{IN}} \geq \frac{1}{2\pi R_2 C_f} \tag{1}$$

or

$$R_1 C_{IN} \leq R_2 C_f \tag{2}$$

Because it is often difficult to know the exact value of C_{IN}, C_f can be experimentally adjusted so that the desired pulse response is achieved. Refer to the LMC660 (SNOSBZ3) and LMC662 (SNOSC51) for a more detailed discussion on compensating for input capacitance.

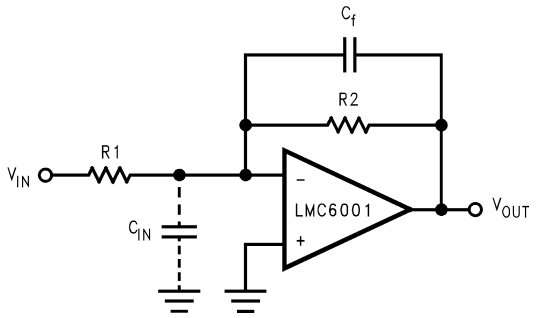


Figure 19. Cancelling the Effect of Input Capacitance

7.1.2 Capacitive Load Tolerance

All rail-to-rail output swing operational amplifiers have voltage gain in the output stage. A compensation capacitor is normally included in this integrator stage. The frequency location of the dominant pole is affected by the resistive load on the amplifier. Capacitive load driving capability can be optimized by using an appropriate resistive load in parallel with the capacitive load. See *Typical Characteristics*.

Direct capacitive loading will reduce the phase margin of many op amps. A pole in the feedback loop is created by the combination of the output impedance of the op amp and the capacitive load. This pole induces phase lag at the unity-gain crossover frequency of the amplifier resulting in either an oscillatory or underdamped pulse response. With a few external components, op amps can easily indirectly drive capacitive loads, as shown in Figure 20.

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Application Information (continued)

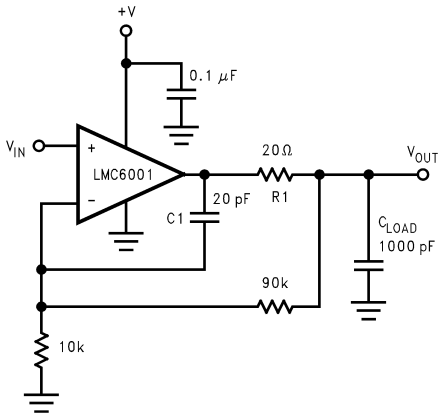


Figure 20. LMC6001 Noninverting Gain of 10 Amplifier, Compensated to Handle Capacitive Loads

In the circuit of Figure 20, R1 and C1 serve to counteract the loss of phase margin by feeding the high frequency component of the output signal back to the inverting input of the amplifier, thereby preserving phase margin in the overall feedback loop.

Capacitive load driving capability is enhanced by using a pullup resistor to V^+ (Figure 21). Typically a pullup resistor conducting 500 µA or more will significantly improve capacitive load responses. The value of the pullup resistor must be determined based on the current sinking capability of the amplifier with respect to the desired output swing. Open-loop gain of the amplifier can also be affected by the pullup resistor. See *DC Electrical Characteristics for LMC6001AI*.

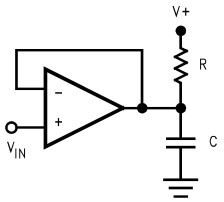


Figure 21. Compensating for Large Capacitive Loads with a Pullup Resistor

7.2 Typical Application

The extremely high input resistance, and low power consumption, of the LMC6001 make it ideal for applications that require battery-powered instrumentation amplifiers. Examples of these types of applications are hand-held pH probes, analytic medical instruments, electrostatic field detectors and gas chromotographs.

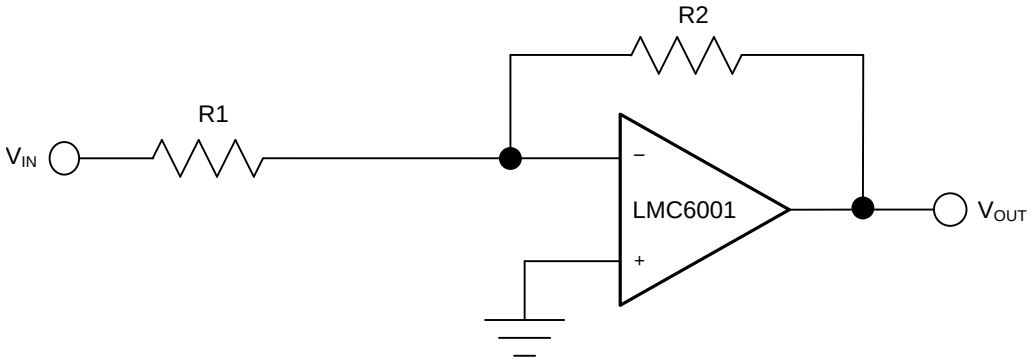


Figure 22. Typical Application Schematic, LMC6001

Typical Application (continued)

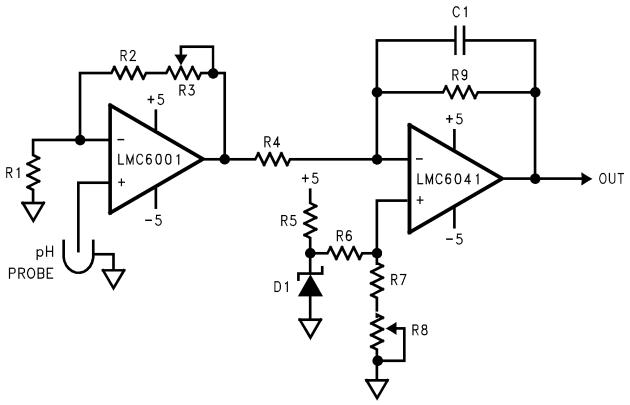
7.2.1 Two Op Amp, Temperature Compensated Ph Probe Amplifier

The signal from a pH probe has a typical resistance between 10 MΩ and 1000 MΩ. Because of this high value, it is very important that the amplifier input currents be as small as possible. The LMC6001 with less than 25-fA input current is an ideal choice for this application.

The LMC6001 amplifies the probe output providing a scaled voltage of ±100 mV/pH from a pH of 7. The second op amp, a micropower LMC6041 provides phase inversion and offset so that the output is directly proportional to pH, over the full range of the probe. The pH reading can now be directly displayed on a low-cost, low-power digital panel meter. Total current consumption will be about 1 mA for the whole system.

The micropower dual-operational amplifier, LMC6042, would optimize power consumption but not offer these advantages:

1. The LMC6001A ensures a 25-fA limit on input current at 25°C.
2. The input ESD protection diodes in the LMC6042 are only rated at 500 V while the LMC6001 has much more robust protection that is rated at 2000 V.



(1)

R1 100 k + 3500 ppm/°C

R2 68.1 k

R3, 8 5 k

R4, 9 100 k

R5 36.5 k

R6 619 k

R7 97.6 k

D1 LM4040D1Z-2.5

C1 2.2 µF

(2) µΩ style 137 or similar

Figure 23. Ph Probe Amplifier

7.2.1.1 Design Requirements

The theoretical output of the standard Ag/AgCl pH probe is 59.16 mV/pH at 25°C with 0 V out at a pH of 7.00. This output is proportional to absolute temperature. To compensate for this, a temperature-compensating resistor, R1, is placed in the feedback loop. This cancels the temperature dependence of the probe. This resistor must be mounted where it will be at the same temperature as the liquid being measured.

7.2.1.2 Detailed Design Procedure

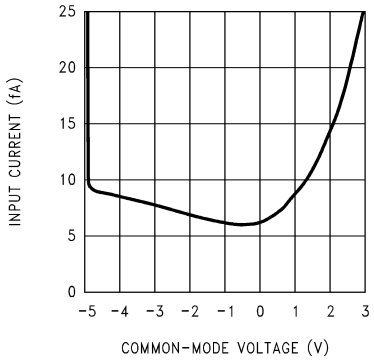
The set-up and calibration is simple with no interactions to cause problems.

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Typical Application (continued)

1. Disconnect the pH probe and with R3 set to about mid-range and the noninverting input of the LMC6001 grounded, adjust R8 until the output is 700 mV.
2. Apply −414.1 mV to the noninverting input of the LMC6001. Adjust R3 for and output of 1400 mV. This completes the calibration. As real pH probes may not perform exactly to theory, minor gain and offset adjustments should be made by trimming while measuring a precision buffer solution.

7.2.1.3 Application Curve



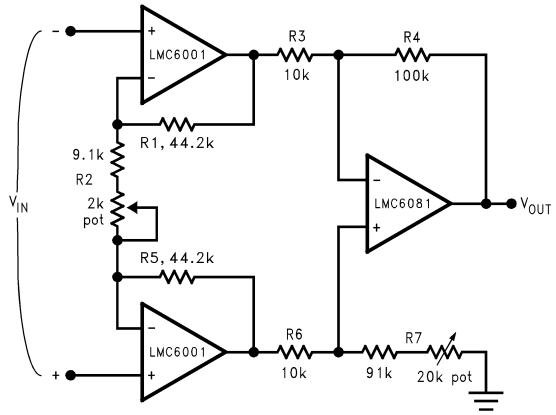
V_S = ±5 V

Figure 24. Input Current vs. V_{CM}

7.3 System Example

7.3.1 Ultra-Low Input Current Instrumentation Amplifier

Figure 25 shows an instrumentation amplifier that features high-differential and common-mode input resistance (>$10^{14}\Omega$), 0.01% gain accuracy at A_V = 1000, excellent CMRR with 1-MΩ imbalance in source resistance. Input current is less than 20 fA and offset drift is less than 2.5 µV/°C. R_2 provides a simple means of adjusting gain over a wide range without degrading CMRR. R_7 is an initial trim used to maximize CMRR without using super precision matched resistors. For good CMRR over temperature, low-drift resistors should be used.



If $R_1 = R_5$, $R_3 = R_6$, and $R_4 = R_7$; then

$$\frac{V_{OUT}}{V_{IN}} = \frac{R_2 + 2R_1}{R_2} \times \frac{R_4}{R_3}$$

$\therefore A_V \approx 100$ for circuit shown (R_2 = 9.85k).

Figure 25. Instrumentation Amplifier

8 Power Supply Recommendations

See the *Recommended Operating Conditions* for the minimum and maximum values for the supply input voltage and operating junction temperature.

9 Layout

9.1 Layout Guidelines

9.1.1 Printed-Circuit-Board Layout For High-Impedance Work

It is generally recognized that any circuit which must operate with less than 1000 pA of leakage current requires special layout of the PCB. When one wishes to take advantage of the ultra-low bias current of the LMC6001, typically less than 10 fA, it is essential to have an excellent layout. Fortunately, the techniques of obtaining low leakages are quite simple. First, the user must not ignore the surface leakage of the PCB, even though it may sometimes appear acceptably low, because under conditions of high humidity or dust or contamination, the surface leakage will be appreciable.

To minimize the effect of any surface leakage, lay out a ring of foil completely surrounding the inputs of the LMC6001 and the terminals of capacitors, diodes, conductors, resistors, relay terminals, and so forth, connected to the inputs of the op amp, as in Figure 30. To have a significant effect, guard rings must be placed on both the top and bottom of the PCB. This PC foil must then be connected to a voltage which is at the same voltage as the amplifier inputs, because no leakage current can flow between two points at the same potential. For example, a PCB trace-to-pad resistance of 10 TΩ, which is normally considered a very large resistance, could leak 5 pA if the trace were a 5-V bus adjacent to the pad of the input.

This would cause a 500 times degradation from the LMC6001's actual performance. If a guard ring is used and held within 1 mV of the inputs, then the same resistance of 10 TΩ will only cause 10 fA of leakage current. Even this small amount of leakage will degrade the extremely low input current performance of the LMC6001. See Figure 28 for typical connections of guard rings for standard op amp configurations.

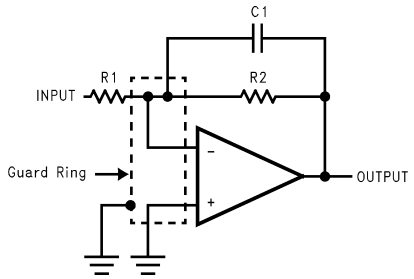


Figure 26. Inverting Amplifier

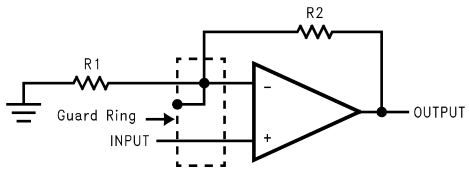


Figure 27. Noninverting Amplifier

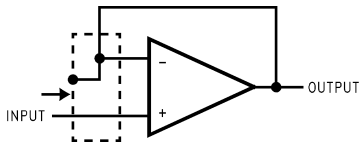
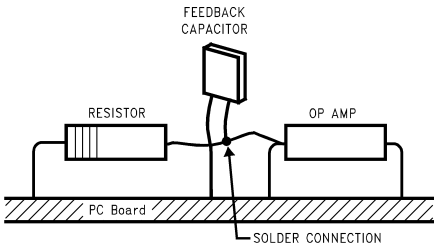


Figure 28. Typical Connections of Guard Rings

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Layout Guidelines (continued)

The designer should be aware that when it is inappropriate to lay out a PCB for the sake of just a few circuits, there is another technique which is even better than a guard ring on a PCB: Do not insert the input pin of the amplifier into the board at all, but bend it up in the air and use only air as an insulator. Air is an excellent insulator. In this case you may have to forego some of the advantages of PCB construction, but the advantages are sometimes well worth the effort of using point-to-point up-in-the-air wiring. See Figure 29.



(Input pins are lifted out of PCB and soldered directly to components. All other pins connected to PCB).

Figure 29. Air Wiring

Another potential source of leakage that might be overlooked is the device package. When the LMC6001 is manufactured, the device is always handled with conductive finger cots. This is to assure that salts and skin oils do not cause leakage paths on the surface of the package. We recommend that these same precautions be adhered to, during all phases of inspection, test and assembly.

9.2 Layout Example

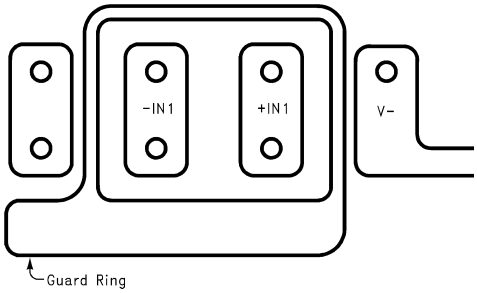


Figure 30. Examples of Guard Ring in PCB Layout

10 Device and Documentation Support

10.1 Documentation Support

10.1.1 Related Documentation

For related documentation, see the following:

- *LMC660 CMOS Quad Operational Amplifier*, SNOSBZ3
- *LMC662 CMOS Dual Operational Amplifier*, SNOSC51

10.2 Related Links

Table 1 lists quick access links. Categories include technical documents, support and community resources, tools and software, and quick access to sample or buy.

Table 1. Related Links

PARTS	PRODUCT FOLDER	SAMPLE & BUY	TECHNICAL DOCUMENTS	TOOLS & SOFTWARE	SUPPORT & COMMUNITY
LMC6001-MIL	Click here	Click here	Click here	Click here	Click here

10.3 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

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Design Support ***TI's Design Support*** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

10.4 Trademarks

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10.5 Electrostatic Discharge Caution



These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

10.6 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

11 Mechanical, Packaging, and Orderable Information

The following pages include mechanical packaging and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

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PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
LMC6001A MDC	ACTIVE	DIESALE	Y	0	270	Green (RoHS & no Sb/Br)	Call TI	Level-1-NA-UNLIM	-40 to 85		Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
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Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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