LM5575-Q1 Simple Switcher® 75-V, 1.5-A Step-Down Switching Regulator

1 Features

- LM5575-Q1 is an Automotive Grade Product That is AEC-Q100 Grade 0 Qualified
- -40°C to 150°C Operating Junction Temperature
- Integrated 75-V, 330-mΩ N-Channel MOSFET
- Ultra-Wide Input Voltage Range From 6 V to 75 V
- Adjustable Output Voltage as Low as 1.225 V
- 1.65% Feedback Reference Accuracy
- Operating Frequency Adjustable Between 50 kHz and 500 kHz With Single Resistor
- Master or Slave Frequency Synchronization
- Adjustable Soft-Start
- Emulated Current Mode Control Architecture
- Wide Bandwidth Error Amplifier
- Built-In Protection

2 Applications

- Automotive
- Industrial

3 Description

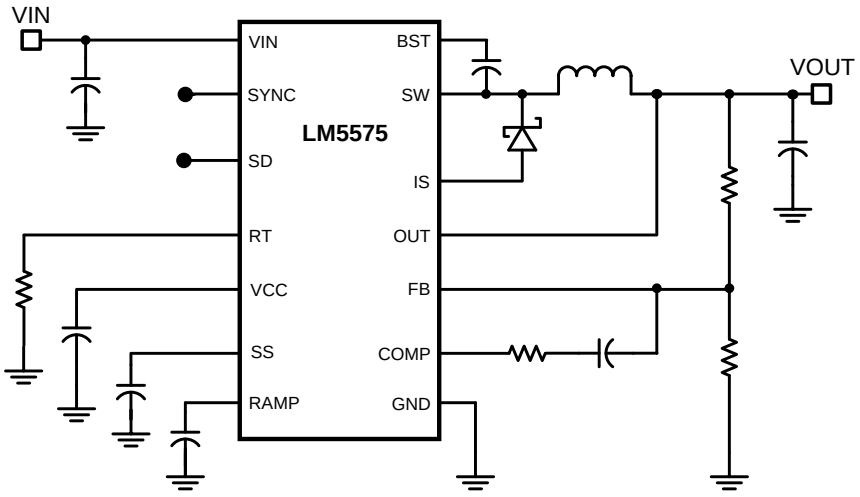
The LM5575-Q1 is an easy-to-use SIMPLE SWITCHER® buck regulator which allows design engineers to design and optimize a robust power supply using a minimum set of components. Operating with an input voltage range of 6 - 75 V, the LM5575-Q1 delivers 1.5 A of continuous output current with an integrated 330-mΩ N-Channel MOSFET. The regulator utilizes an Emulated Current Mode architecture which provides inherent line regulation, tight load transient response, and ease-of-loop compensation without the usual limitation of low-duty cycles associated with current mode regulators. The operating frequency is adjustable from 50 kHz to 500 kHz to allow optimization of size and efficiency. To reduce EMI, a frequency synchronization pin allows multiple IC's from the LM(2)557x devices to self-synchronize or to synchronize to an external clock. The LM5575-Q1 ensures robustness with cycle-by-cycle current limit, short-circuit protection, thermal shutdown, and remote shutdown. The device is available in a power enhanced TSSOP-16 package featuring an exposed die attach pad for thermal dissipation. The LM5575-Q1 is supported by the full suite of WEBENCH® On-Line design tools.

Device Information(1)

PART NUMBER	PACKAGE	BODY SIZE (NOM)
LM5575-Q1	HTSSOP (16)	5.00 mm × 4.40 mm

(1) For all available packages, see the orderable addendum at the end of the datasheet.

4 Simplified Schematic



An IMPORTANT NOTICE at the end of this data sheet addresses availability, warranty, changes, use in safety-critical applications, intellectual property matters and other important disclaimers. PRODUCTION DATA.

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5 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision B (April 2013) to Revision C — **Page**

- Added *Pin Configuration and Functions* section, *Handling Rating* table, *Feature Description* section, *Device Functional Modes*, *Application and Implementation* section, *Power Supply Recommendations* section, *Layout* section, *Device and Documentation Support* section, and *Mechanical, Packaging, and Orderable Information* section ... 1

Changes from Revision A (April 2013) to Revision B — **Page**

- Changed layout of National Data Sheet to TI format ... 25

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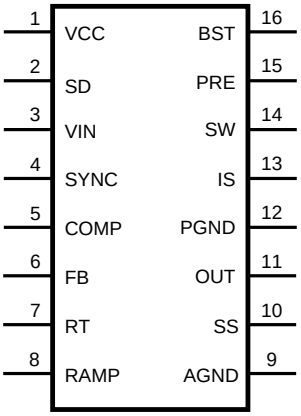
6 Pin Configuration and Functions

PWP Package
16-Pin HTSSOP With Exposed Thermal Pad
Top View



Pin Functions

PIN		I/O	DESCRIPTION	APPLICATION INFORMATION
NAME	NO.			
VCC	1	O	Output of the bias regulator	Vcc tracks Vin up to 9 V. Beyond 9 V, Vcc is regulated to 7 volts. A 0.1-uF to 1-uF ceramic decoupling capacitor is required. An external voltage (7.5 V – 14 V) can be applied to this pin to reduce internal power dissipation.
SD	2	I	Shutdown or UVLO input	If the SD pin voltage is below 0.7 V the regulator will be in a low power state. If the SD pin voltage is between 0.7 V and 1.225 V the regulator will be in standby mode. If the SD pin voltage is above 1.225 V the regulator will be operational. An external voltage divider can be used to set a line undervoltage shutdown threshold. If the SD pin is left open circuit, a 5µA pull-up current source configures the regulator fully operational.
Vin	3	I	Input supply voltage	Nominal operating range: 6 V to 75 V
SYNC	4	I	Oscillator synchronization input or output	The internal oscillator can be synchronized to an external clock with an external pull-down device. Multiple LM5575-Q1 devices can be synchronized together by connection of their SYNC pins.
COMP	5	O	Output of the internal error amplifier	The loop compensation network should be connected between this pin and the FB pin.
FB	6	I	Feedback signal from the regulated output	This pin is connected to the inverting input of the internal error amplifier. The regulation threshold is 1.225 V.
RT	7	I	Internal oscillator frequency set input	The internal oscillator is set with a single resistor, connected between this pin and the AGND pin.
RAMP	8	O	Ramp control signal	An external capacitor connected between this pin and the AGND pin sets the ramp slope used for current mode control. Recommended capacitor range 50 pF to 2000 pF.
AGND	9	Ground	Analog ground	Internal reference for the regulator control functions
SS	10	O	Soft-start	An external capacitor and an internal 10-µA current source set the time constant for the rise of the error amp reference. The SS pin is held low during standby, Vcc UVLO and thermal shutdown.
OUT	11	O	Output voltage connection	Connect directly to the regulated output voltage.
PGND	12	Ground	Power ground	Low side reference for the PRE switch and the IS sense resistor.
IS	13	I	Current sense	Current measurement connection for the re-circulating diode. An internal sense resistor and a sample/hold circuit sense the diode current near the conclusion of the off-time. This current measurement provides the DC level of the emulated current ramp.

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Pin Functions (continued)

PIN		I/O	DESCRIPTION	APPLICATION INFORMATION
NAME	NO.			
SW	14	O	Switching node	The source terminal of the internal buck switch. The SW pin should be connected to the external Schottky diode and to the buck inductor.
PRE	15	O	Pre-charge assist for the bootstrap capacitor	This open drain output can be connected to SW pin to aid charging the bootstrap capacitor during very light load conditions or in applications where the output may be pre-charged before the LM5575-Q1 is enabled. An internal pre-charge MOSFET is turned on for 250 ns each cycle just prior to the on-time interval of the buck switch.
BST	16	I	Boost input for bootstrap capacitor	An external capacitor is required between the BST and the SW pins. A 0.022-µF ceramic capacitor is recommended. The capacitor is charged from Vcc through an internal diode during the off-time of the buck switch.
EP	NA	--	Exposed Pad	Exposed metal pad on the underside of the device. It is recommended to connect this pad to the PWB ground plane, in order to aid in heat dissipation.

7 Specifications

7.1 Absolute Maximum Ratings

See (1)(2).

	MIN	MAX	UNIT
V_{IN} to GND		76	V
BST to GND		90	V
PRE to GND		76	V
SW to GND (Steady State)		−1.5	V
BST to V_{CC}		76	V
SD, V_{CC} to GND		14	V
BST to SW		14	V
OUT to GND		Limited to Vin	
SYNC, SS, FB, RAMP to GND		7	V

(1) *Absolute Maximum Ratings* are limits beyond which damage to the device may occur. *Recommended Operating Conditions* are conditions under which operation of the device is intended to be functional. For ensured specifications and test conditions, see the *Electrical Characteristics*.
(2) If Military/Aerospace specified devices are required, please contact the Texas Instruments Sales Office/ Distributors for availability and specifications.

7.2 Handling Ratings

			MIN	MAX	UNIT
T_{stg}	Storage temperature range		−65	150	°C
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per AEC Q100-002(1)		2000	V

(1) AEC Q100-002 indicates HBM stressing is done in accordance with the ANSI/ESDA/JEDEC JS-001 specification.

7.3 Recommended Operating Conditions(1)

over operating free-air temperature range (unless otherwise noted)

	MIN	MAX	UNIT
V_{IN}	6	75	V
Operation Junction Temperature	−40	150	°C

(1) *Absolute Maximum Ratings* are limits beyond which damage to the device may occur. *Recommended Operating Conditions* are conditions under which operation of the device is intended to be functional. For ensured specifications and test conditions, see the *Electrical Characteristics*.

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7.4 Thermal Information

THERMAL METRIC[1]		LM5575-Q1 PWP 16 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	50	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	14	

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, SPRA953.

7.5 Electrical Characteristics

Specifications with standard typeface are for T_J = 25°C. V_{IN} = 48V, R_T = 32.4 kΩ unless otherwise stated. (1)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
STARTUP REGULATOR						
VccReg	V_{CC} Regulator Output			7.15		V
		Over full Operating Junction Temperature range	6.85		7.5	
	V_{CC} LDO Mode turn-off			9		V
	V_{CC} Current Limit	V_{CC} = 0 V		25		mA
VCC SUPPLY						
	V_{CC} UVLO Threshold	(V_{CC} increasing)		5.35		V
		Over full Operating Junction Temperature range	5.01		5.69	
	V_{CC} Undervoltage Hysteresis			0.35		V
	Bias Current (Iin)	FB = 1.3 V		3.7		mA
		Over full Operating Junction Temperature range			4.5	
	Shutdown Current (Iin)	SD = 0 V		57		µA
		Over full Operating Junction Temperature range			85	
SHUTDOWN THRESHOLDS						
	Shutdown Threshold	(SD Increasing)		0.7		V
		Over full Operating Junction Temperature range	0.43		0.9	
	Shutdown Hysteresis			0.1		V
	Standby Threshold	(Standby Increasing)		1.225		V
		Over full Operating Junction Temperature range	1.15		1.30	
	Standby Hysteresis			0.1		V
	SD Pullup Current Source			5		µA
SWITCH CHARACTERISTICS						
	Buck Switch Rds(on)			330		mΩ
		Over full Operating Junction Temperature range			760	
	BOOST UVLO			4		V
	BOOST UVLO Hysteresis			0.56		V
	Pre-charge Switch Rds(on)			70		Ω
	Pre-charge Switch on-time			250		ns
CURRENT LIMIT						
	Cycle by Cycle Current Limit	RAMP = 0 V		2.1		A
		Over full Operating Junction Temperature range	1.8		2.7	

(1) Min and Max limits are 100% production tested at 25°C. Limits over the operating temperature range are ensured through correlation using Statistical Quality Control (SQC) methods. Limits are used to calculate Average Outgoing Quality Level (AOQL).

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Electrical Characteristics (continued)

Specifications with standard typeface are for T_J = 25°C. V_{IN} = 48V, R_T = 32.4 kΩ unless otherwise stated. (1)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
	Cycle by Cycle Current Limit Delay	RAMP = 2.5 V		85		ns
SOFT-START						
	SS Current Source			10		µA
		Over full Operating Junction Temperature range	7		14	
OSCILLATOR						
	Frequency1			200		kHz
		Over full Operating Junction Temperature range	180		220	
	Frequency2	R_T = 11 kΩ		485		kHz
		Over full Operating Junction Temperature range	425		545	
	SYNC Source Impedance			11		kΩ
	SYNC Sink Impedance			110		Ω
	SYNC Threshold (falling)			1.3		V
	SYNC Frequency	R_T = 11 kΩ				kHz
		Over full Operating Junction Temperature range	550			
	SYNC Pulse Width Minimum	Over full Operating Junction Temperature range	15			ns
RAMP GENERATOR						
	Ramp Current 1	Vin = 60 V, Vout=10 V		550		µA
		Over full Operating Junction Temperature range	467		633	
	Ramp Current 2	Vin = 10 V, Vout=10 V		50		µA
		Over full Operating Junction Temperature range	36		64	
PWM COMPARATOR						
	Forced Off-time			500		ns
		Over full Operating Junction Temperature range	390		590	
	Min On-time			80		ns
	COMP to PWM Comparator Offset			0.7		V
ERROR AMPLIFIER						
	Feedback Voltage	Vfb = COMP		1.225		V
		Over full Operating Junction Temperature range	1.205		1.245	
	FB Bias Current			17		nA
	DC Gain			70		dB
	COMP Sink / Source Current	Over full Operating Junction Temperature range	2.5			mA
	Unity Gain Bandwidth			3		MHz
DIODE SENSE RESISTANCE						
D_{SENSE}				83		mΩ
THERMAL SHUTDOWN						
Tsd	Thermal Shutdown Threshold			180		°C
	Thermal Shutdown Hysteresis			25		°C

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7.6 Typical Characteristics

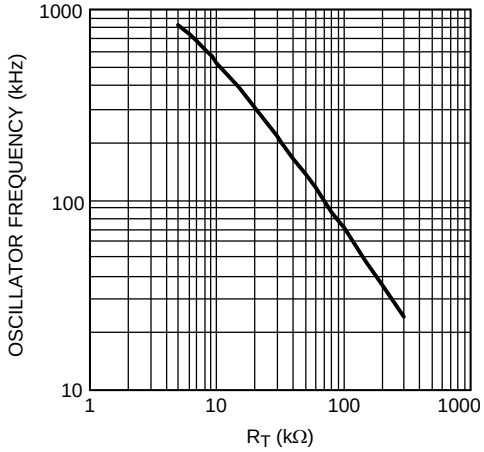

Figure 1. Oscillator Frequency vs R_T

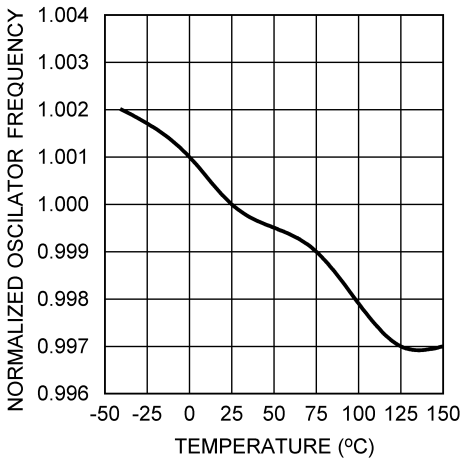

Figure 2. Oscillator Frequency vs Temperature F_{OSC} = 200 kHz

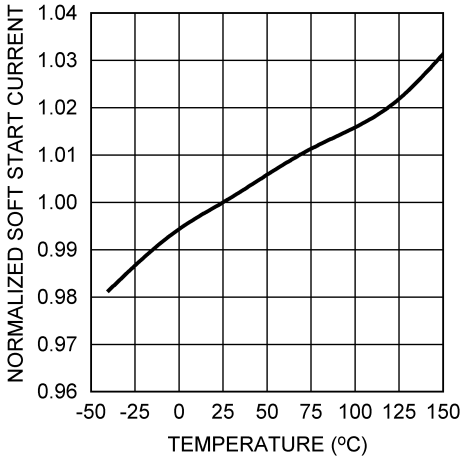

Figure 3. Soft-Start Current vs Temperature

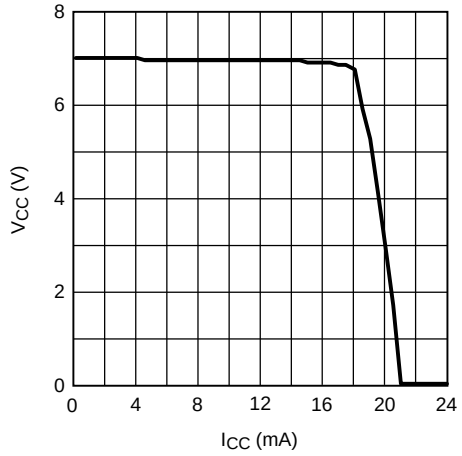

Figure 4. V_{CC} vs I_{CC} V_{IN} = 12 V

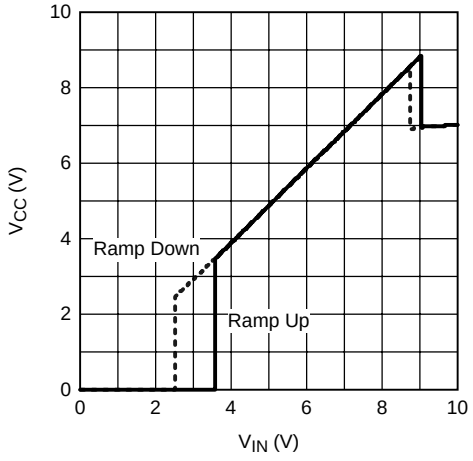

Figure 5. V_{CC} vs V_{IN} R_L = 7 kω

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Typical Characteristics (continued)

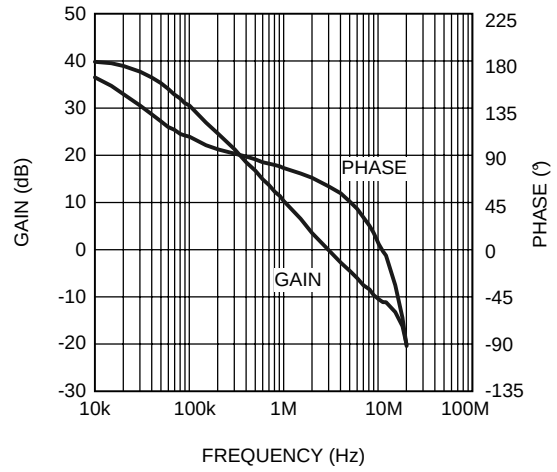

Figure 6. Error Amplifier Gain / Phase A_{VCL} = 101

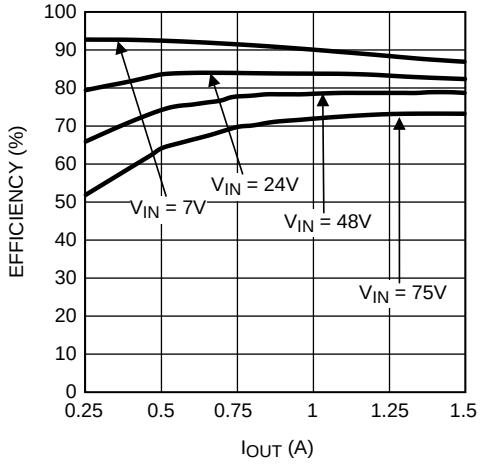

Figure 7. Demoboard Efficiency vs I_{OUT} and V_{IN}

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8 Detailed Description

8.1 Overview

The LM5575-Q1 switching regulator features all of the functions necessary to implement an efficient high-voltage buck regulator using a minimum of external components. This easy-to-use regulator integrates a 75-V N-Channel buck switch with an output current capability of 1.5 Amps. The regulator control method is based on current mode control utilizing an emulated current ramp. Peak current mode control provides inherent line voltage feed-forward, cycle-by-cycle current limiting, and ease-of-loop compensation. The use of an emulated control ramp reduces noise sensitivity of the pulse-width modulation circuit, allowing reliable processing of very small duty cycles necessary in high-input voltage applications. The operating frequency is user programmable from 50 kHz to 500 kHz. An oscillator synchronization pin allows multiple LM5575-Q1 regulators to self-synchronize or be synchronized to an external clock. The output voltage can be set as low as 1.225 V. Fault protection features include, current limiting, thermal shutdown and remote shutdown capability. The device is available in the TSSOP-16 package featuring an exposed pad to aid thermal dissipation.

8.2 Functional Block Diagram

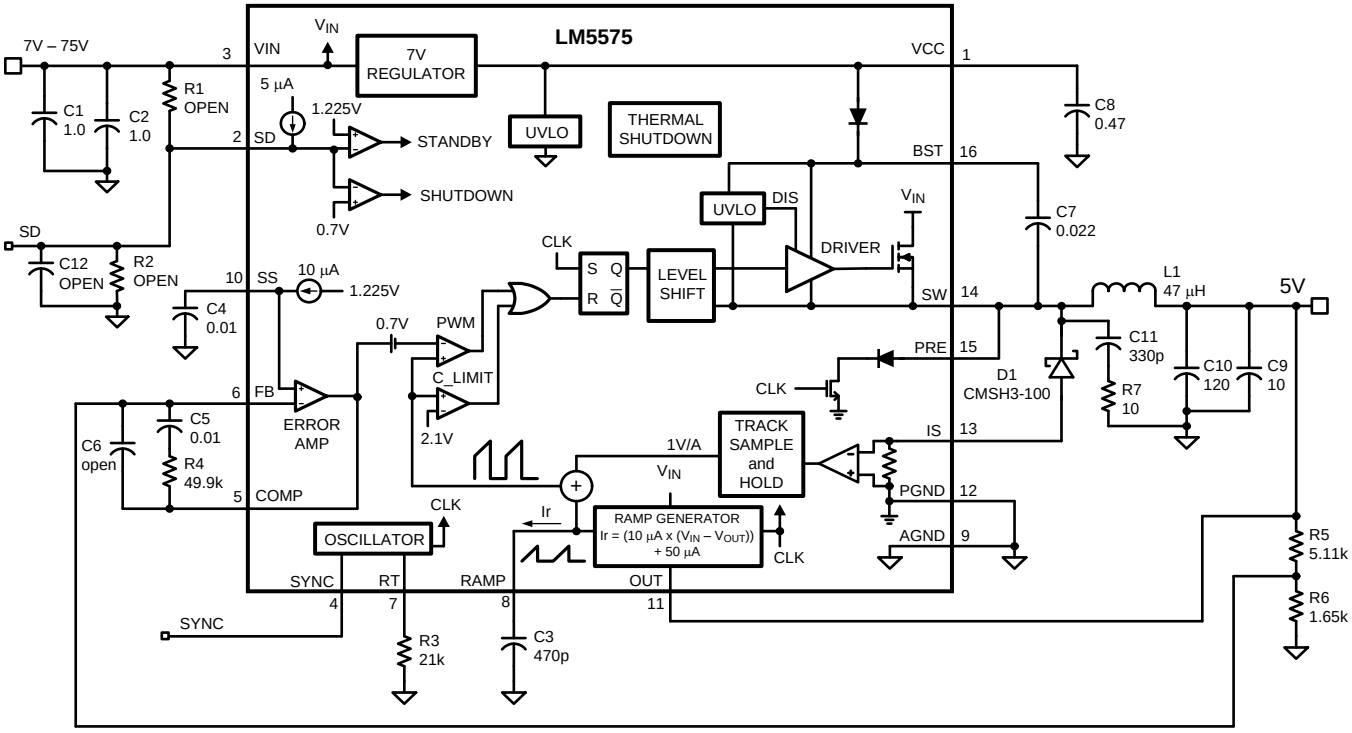

Figure 8. Typical Application Circuit and Block Diagram

The functional block diagram and typical application of the LM5575-Q1 are shown in Figure 8. The LM5575-Q1 can be applied in numerous applications to efficiently step-down a high, unregulated input voltage. The device is well suited for telecom, industrial and automotive power bus voltage ranges.

8.3 Feature Description

8.3.1 Shutdown and Standby

The LM5575-Q1 contains a dual-level Shutdown (SD) circuit. When the SD pin voltage is below 0.7 V, the regulator is in a low-current shutdown mode. When the SD pin voltage is greater than 0.7 V but less than 1.225 V, the regulator is in standby mode. In standby mode, the V_{CC} regulator is active but the output switch is disabled. When the SD pin voltage exceeds 1.225 V, the output switch is enabled and normal operation begins. An internal 5-µA pullup current source configures the regulator to be fully operational if the SD pin is left open.

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Feature Description (continued)

An external set-point voltage divider from VIN to GND can be used to set the operational input range of the regulator. The divider must be designed such that the voltage at the SD pin will be greater than 1.225 V when VIN is in the desired operating range. The internal 5-µA pullup current source must be included in calculations of the external set-point divider. Hysteresis of 0.1 V is included for both the shutdown and standby thresholds. The SD pin is internally clamped with a 1-kΩ resistor and an 8-V zener clamp. The voltage at the SD pin should never exceed 14 V. If the voltage at the SD pin exceeds 8 V, the bias current will increase at a rate of 1 mA/V.

The SD pin can also be used to implement various remote enable and disable functions. Pulling the SD pin below the 0.7-V threshold totally disables the controller. If the SD pin voltage is above 1.225 V, the regulator will be operational.

8.3.2 Current Limit

The LM5575-Q1 contains a unique current monitoring scheme for control and overcurrent protection. When set correctly, the emulated current sense signal provides a signal which is proportional to the buck switch current with a scale factor of 1.0 V/A. The emulated ramp signal is applied to the current limit comparator. If the emulated ramp signal exceeds 2.1 V (2.1 A) the present current cycle is terminated (cycle-by-cycle current limiting). In applications with small output inductance and high-input voltage, the switch current may overshoot due to the propagation delay of the current limit comparator. If an overshoot should occur, the diode current sampling circuit will detect the excess inductor current during the off-time of the buck switch. If the sample and hold DC level exceeds the 2.1-V current limit threshold, the buck switch will be disabled and skip pulses until the diode current sampling circuit detects the inductor current has decayed below the current limit threshold. This approach prevents current runaway conditions due to propagation delays or inductor saturation since the inductor current is forced to decay following any current overshoot.

8.3.3 Soft-Start

The soft-start feature allows the regulator to gradually reach the initial steady-state operating point, thus reducing start-up stresses and surges. The internal soft-start current source, set to 10 µA, gradually increases the voltage of an external soft-start capacitor connected to the SS pin. The soft-start capacitor voltage is connected to the reference input of the error amplifier. Various sequencing and tracking schemes can be implemented using external circuits that limit or clamp the voltage level of the SS pin.

In the event a fault is detected (overtemperature, Vcc UVLO, SD) the soft-start capacitor will be discharged. When the fault condition is no longer present, a new soft-start sequence will commence.

8.3.4 Thermal Protection

Internal Thermal Shutdown circuitry is provided to protect the integrated circuit in the event the maximum junction temperature is exceeded. When activated, typically at 180°C, the controller is forced into a low-power reset state, disabling the output driver and the bias regulator. This feature is provided to prevent catastrophic failures from accidental device overheating.

8.4 Device Functional Modes

8.4.1 High-Voltage Start-Up Regulator

The LM5575-Q1 contains a dual-mode internal high-voltage start-up regulator that provides the V_{CC} bias supply for the PWM controller and bootstrap MOSFET gate driver. The input pin (VIN) can be connected directly to the input voltage, as high as 75 volts. For input voltages below 9 V, a low dropout switch connects VCC directly to VIN. In this supply range, V_{CC} is approximately equal to V_{IN}. For V_{IN} voltage greater than 9 V, the low-dropout switch is disabled and the V_{CC} regulator is enabled to maintain V_{CC} at approximately 7 V. The wide operating range of 6 V to 75 V is achieved through the use of this dual-mode regulator.

The output of the V_{CC} regulator is current limited to 25 mA. Upon power-up, the regulator sources current into the capacitor connected to the VCC pin. When the voltage at the VCC pin exceeds the V_{CC} UVLO threshold of 5.35 V and the SD pin is greater than 1.225 V, the output switch is enabled and a soft-start sequence begins. The output switch remains enabled until V_{CC} falls below 5 V or the SD pin falls below 1.125 V.

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Device Functional Modes (continued)

An auxiliary supply voltage can be applied to the VCC pin to reduce the IC power dissipation. If the auxiliary voltage is greater than 7.3 V, the internal regulator will essentially shut off, reducing the IC power dissipation. The V_{CC} regulator series pass transistor includes a diode between VCC and VIN that should not be forward biased in normal operation. Therefore the auxiliary V_{CC} voltage should never exceed the V_{IN} voltage.

In high-voltage applications, take care to ensure the VIN pin does not exceed the absolute maximum voltage rating of 76 V. During line or load transients, voltage ringing on the VIN line that exceeds the Absolute Maximum Ratings can damage the IC. Both careful PC board layout and the use of quality bypass capacitors located close to the VIN and GND pins are essential.

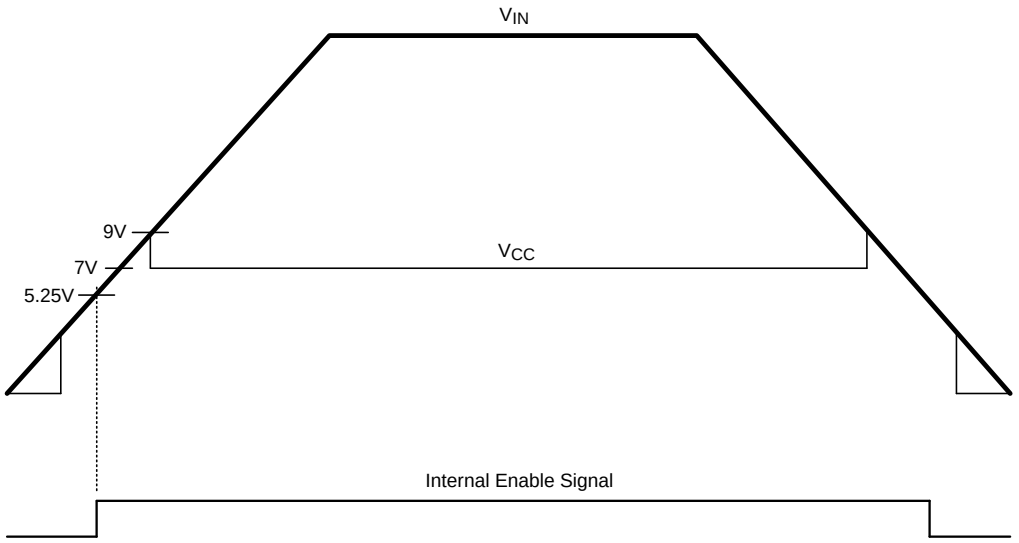

Figure 9. V_{IN} and V_{CC} Sequencing

8.4.2 Oscillator and Sync Capability

The LM5575-Q1 oscillator frequency is set by a single external resistor connected between the RT pin and the AGND pin. The R_T resistor should be located very close to the device and connected directly to the pins of the IC (RT and AGND).To set a desired oscillator frequency (F), the necessary value for the R_T resistor can be calculated from the following equation:

$$R_T = \frac{\frac{1}{F} - 580 \times 10^{-9}}{135 \times 10^{-12}} \quad (1)$$

The SYNC pin can be used to synchronize the internal oscillator to an external clock. The external clock must be of higher frequency than the free-running frequency set by the R_T resistor. A clock circuit with an open-drain output is the recommended interface from the external clock to the SYNC pin. The clock pulse duration should be greater than 15 ns.

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Device Functional Modes (continued)

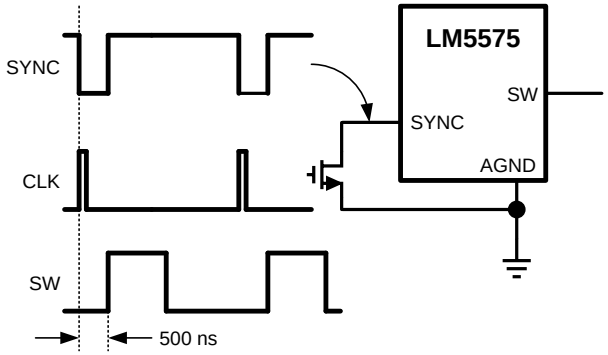

Figure 10. Sync from External Clock

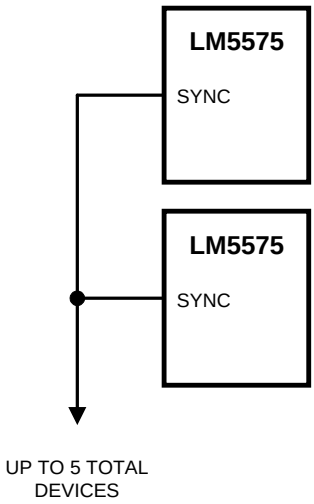

Figure 11. Sync from Multiple Devices

Multiple LM5575-Q1 devices can be synchronized together simply by connecting the SYNC pins together. In this configuration, all of the devices will be synchronized to the highest frequency device. The diagram in Figure 12 illustrates the SYNC input and output features of the LM5575-Q1. The internal oscillator circuit drives the SYNC pin with a strong pulldown and weak pullup inverter. When the SYNC pin is pulled low either by the internal oscillator or an external clock, the ramp cycle of the oscillator is terminated and a new oscillator cycle begins. Thus, if the SYNC pins of several LM5575-Q1 IC's are connected together, the IC with the highest internal clock frequency will pull the connected SYNC pins low first and terminate the oscillator ramp cycles of the other IC's. The LM5575-Q1 with the highest programmed clock frequency will serve as the master and control the switching frequency of the all the devices with lower oscillator frequency.

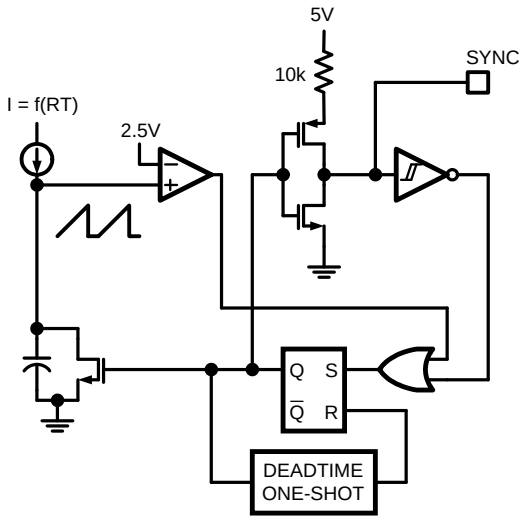

Figure 12. Simplified Oscillator Block Diagram and Sync I/O Circuit

8.4.3 Error Amplifier and PWM Comparator

The internal high-gain error amplifier generates an error signal proportional to the difference between the regulated output voltage and an internal precision reference (1.225 V). The output of the error amplifier is connected to the COMP pin, allowing the user to provide loop compensation components, generally a type II network, as illustrated in Figure 8. This network creates a pole at DC, a zero and a noise-reducing, high-frequency pole. The PWM comparator compares the emulated current sense signal from the RAMP generator to the error amplifier output voltage at the COMP pin.

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Device Functional Modes (continued)

8.4.4 Ramp Generator

The ramp signal used in the pulsewidth modulator for current mode control is typically derived directly from the buck switch current. This switch current corresponds to the positive slope portion of the output inductor current. Using this signal for the PWM ramp simplifies the control loop transfer function to a single pole response and provides inherent input voltage feed-forward compensation. The disadvantage of using the buck switch current signal for PWM control is the large leading edge spike due to circuit parasitics that must be filtered or blanked. Also, the current measurement may introduce significant propagation delays. The filtering, blanking time and propagation delay limit the minimum achievable pulsewidth. In applications where the input voltage may be relatively large in comparison to the output voltage, controlling small pulsewidths and duty cycles is necessary for regulation. The LM5575-Q1 utilizes a unique ramp generator, which does not actually measure the buck switch current but rather reconstructs the signal. Reconstructing or emulating the inductor current provides a ramp signal to the PWM comparator that is free of leading edge spikes and measurement or filtering delays. The current reconstruction is comprised of two elements; a sample and hold DC level and an emulated current ramp.

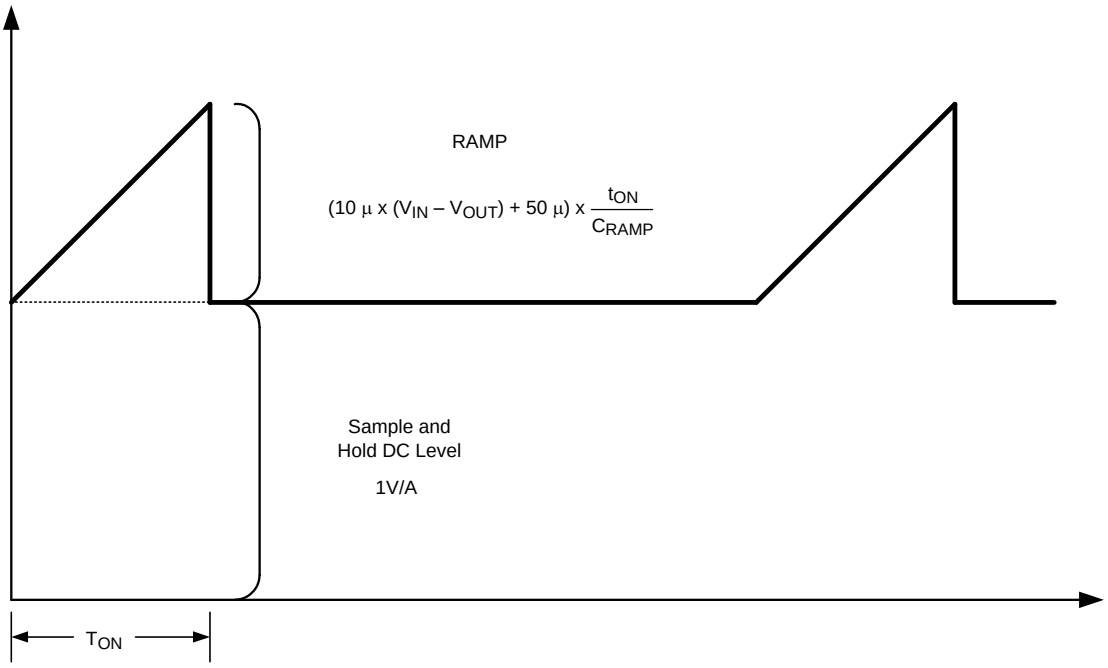

Figure 13. Composition of Current Sense Signal

The sample and hold DC level illustrated in Figure 13 is derived from a measurement of the re-circulating Schottky diode anode current. The re-circulating diode anode should be connected to the IS pin. The diode current flows through an internal current sense resistor between the IS and PGND pins. The voltage level across the sense resistor is sampled and held just prior to the onset of the next conduction interval of the buck switch. The diode current sensing and sample & hold provide the DC level of the reconstructed current signal. The positive slope inductor current ramp is emulated by an external capacitor connected from the RAMP pin to AGND and an internal voltage controlled current source. The ramp current source that emulates the inductor current is a function of the V_{IN} and V_{OUT} voltages per the following equation:

$$I_{RAMP} = (10\mu \times (Vin - Vout)) + 50\mu A \quad (2)$$

Proper selection of the RAMP capacitor depends upon the selected value of the output inductor. The value of C_{RAMP} can be selected from:

$$C_{RAMP} = L \times 10^{-5} \quad (3)$$

where

- L is the value of the output inductor in Henrys

Device Functional Modes (continued)

With this value, the scale factor of the emulated current ramp will be approximately equal to the scale factor of the DC level sample and hold (1.0 V/A). The C_{RAMP} capacitor should be located very close to the device and connected directly to the pins of the IC (RAMP and AGND).

For duty cycles greater than 50%, peak current mode control circuits are subject to sub-harmonic oscillation. Sub-harmonic oscillation is normally characterized by observing alternating wide and narrow pulses at the switch node. Adding a fixed slope voltage ramp (slope compensation) to the current sense signal prevents this oscillation. The 50 µA of offset current provided from the emulated current source adds some fixed slope to the ramp signal. In some high-output voltage, high duty cycle applications, additional slope may be required. In these applications, a pullup resistor may be added between the V_{CC} and RAMP pins to increase the ramp slope compensation.

For V_{OUT} > 7.5V:

Calculate optimal slope current, $I_{OS} = V_{OUT}$ x 10 µA/V.

For example, at V_{OUT} = 10 V, I_{OS} = 100 µA.

Install a resistor from the RAMP pin to V_{CC}:

$$R_{RAMP} = V_{CC} / (I_{OS} - 50\mu A) \quad (4)$$

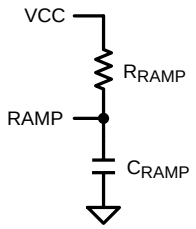

Figure 14. R_{RAMP} to V_{CC} for V_{OUT} > 7.5 V

8.4.5 Boost Pin

The LM5575-Q1 integrates an N-Channel buck switch and associated floating high-voltage level shift and gate driver. This gate driver circuit works in conjunction with an internal diode and an external bootstrap capacitor. A 0.022-µF ceramic capacitor, connected with short traces between the BST pin and SW pin, is recommended. During the off-time of the buck switch, the SW pin voltage is approximately –0.5 V and the bootstrap capacitor is charged from V_{CC} through the internal bootstrap diode. When operating with a high PWM duty cycle, the buck switch will be forced off each cycle for 500 ns to ensure that the bootstrap capacitor is recharged.

Under very light-load conditions or when the output voltage is pre-charged, the SW voltage will not remain low during the off-time of the buck switch. If the inductor current falls to zero and the SW pin rises, the bootstrap capacitor will not receive sufficient voltage to operate the buck switch gate driver. For these applications, the PRE pin can be connected to the SW pin to pre-charge the bootstrap capacitor. The internal pre-charge MOSFET and diode connected between the PRE pin and PGND turns on each cycle for 250 ns just prior to the onset of a new switching cycle. If the SW pin is at a normal negative voltage level (continuous conduction mode), then no current will flow through the pre-charge MOSFET/diode.

8.4.6 Maximum Duty Cycle and Input Drop-Out Voltage

There is a forced off-time of 500 ns implemented each cycle to ensure sufficient time for the diode current to be sampled. This forced off-time limits the maximum duty cycle of the buck switch. The maximum duty cycle will vary with the operating frequency.

$$D_{MAX} = 1 - Fs \times 500ns$$

where

- Fs is the oscillator frequency. (5)

Limiting the maximum duty cycle will raise the input dropout voltage. The input dropout voltage is the lowest input voltage required to maintain regulation of the output voltage. An approximation of the input dropout voltage is:

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Device Functional Modes (continued)

$$Vin_{MIN} = \frac{Vout + V_D}{1 - Fs \times 500\ ns} \quad (6)$$

where

- V_D is the voltage drop across the re-circulatory diode.

Operating at high switching frequency raises the minimum input voltage necessary to maintain regulation.

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9 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

9.1 Application Information

9.1.1 Bias Power Dissipation Reduction

Buck regulators operating with high input voltage can dissipate an appreciable amount of power for the bias of the IC. The V_{CC} regulator must step down the input voltage V_{IN} to a nominal V_{CC} level of 7 V. The large voltage drop across the V_{CC} regulator translates into a large power dissipation within the V_{CC} regulator. There are several techniques that can significantly reduce this bias regulator power dissipation. Figure 15 and Figure 16 depict two methods to bias the IC from the output voltage. In each case, the internal V_{CC} regulator is used to initially bias the VCC pin. After the output voltage is established, the VCC pin potential is raised above the nominal 7-V regulation level, which effectively disables the internal V_{CC} regulator. The voltage applied to the VCC pin should never exceed 14 V. The V_{CC} voltage should never be larger than the V_{IN} voltage.

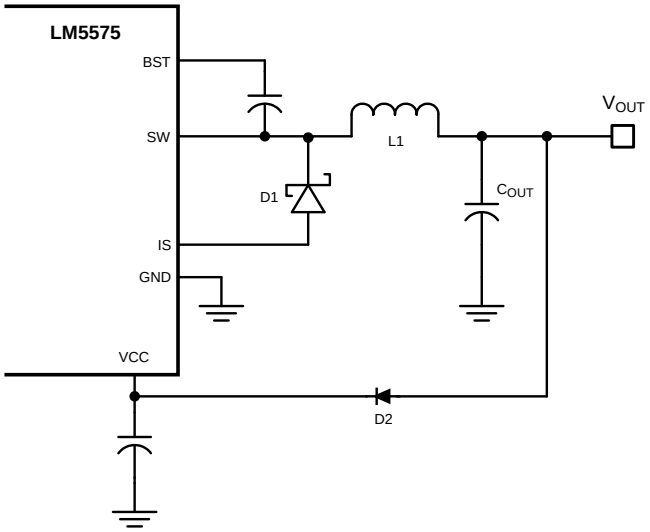

Figure 15. V_{CC} Bias from V_{OUT} for 8 V < V_{OUT} < 14 V

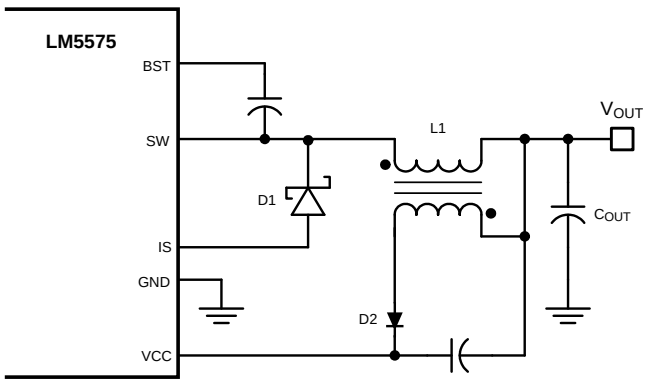

Figure 16. Vcc Bias With Additional Winding on the Output Inductor

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9.2 Typical Application

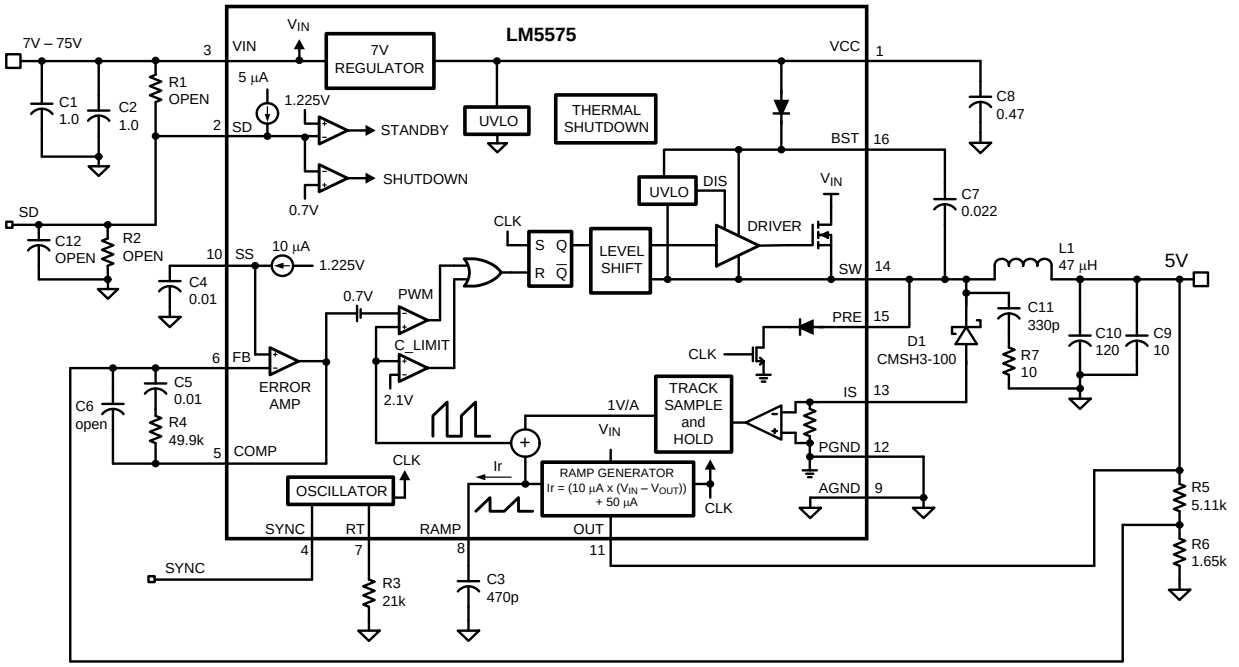

Figure 17. Typical Application Circuit

9.2.1 Design Requirements

The circuit shown in Figure 8 is configured for the following specifications:

- V_{OUT} = 5 V
- V_{IN} = 7 V to 75 V
- Fs = 300 kHz
- Minimum load current (for CCM) = 200 mA
- Maximum load current = 1.5 A

9.2.2 Detailed Design Procedure

9.2.2.1 External Components

The procedure for calculating the external components is illustrated with the following design example.

9.2.2.2 R3 (R_T)

R_T sets the oscillator switching frequency. Generally, higher-frequency applications are smaller but have higher losses. Operation at 300 kHz was selected for this example as a reasonable compromise for both small size and high efficiency. The value of R_T for 300-kHz switching frequency can be calculated as follows:

$$R_T = \frac{[(1 / 300 \times 10^3) - 580 \times 10^{-9}]}{135 \times 10^{-12}} \quad (7)$$

The nearest standard value of 21 kΩ was chosen for R_T.

9.2.2.3 L1

The inductor value is determined based on the operating frequency, load current, ripple current, and the minimum and maximum input voltage ($V_{IN(min)}$, $V_{IN(max)}$).

Typical Application (continued)

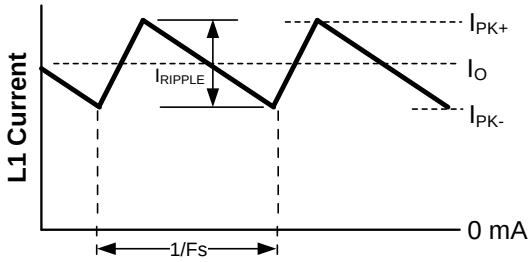

Figure 18. Inductor Current Waveform

To keep the circuit in continuous conduction mode (CCM), the maximum ripple current I_{RIPPLE} should be less than twice the minimum load current, or 0.4 Ap-p. Using this value of ripple current, the value of inductor (L1) is calculated using the following:

$$L1 = \frac{V_{OUT} \times (V_{IN(max)} - V_{OUT})}{I_{RIPPLE} \times F_S \times V_{IN(max)}} \quad (8)$$

$$L1 = \frac{5V \times (75V - 5V)}{0.4A \times 300\ kHz \times 75V} = 39\ \mu H \quad (9)$$

This procedure provides a guide to select the value of L1. The nearest standard value (47 µH) will be used. L1 must be rated for the peak current (I_{PK+}) to prevent saturation. During normal loading conditions, the peak current occurs at maximum load current plus maximum ripple. During an overload condition, the peak current is limited to 2.1 A nominal (2.5 A maximum). The selected inductor has a conservative 3.25 Amp saturation current rating. For this manufacturer, the saturation rating is defined as the current necessary for the inductance to reduce by 30%, at 20°C.

9.2.2.4 C3 (C_{RAMP})

With the inductor value selected, the value of C3 (C_{RAMP}) necessary for the emulation ramp circuit is:

$$C_{RAMP} = L \times 10^{-5}$$

where

- L is in Henrys. (10)

With L1 selected for 47 µH, the recommended value for C3 is 470 pF.

9.2.2.5 C9, C10

The output capacitors, C9 and C10, smooth the inductor ripple current and provide a source of charge for transient loading conditions. For this design a 10-µF ceramic capacitor and a 120-µF AL organic capacitor were selected. The ceramic capacitor provides ultra low ESR to reduce the output ripple voltage and noise spikes, while the AL capacitor provides a large bulk capacitance in a small volume for transient loading conditions. An approximation for the output ripple voltage is:

$$\Delta V_{OUT} = \Delta I_L \times \left(ESR + \frac{1}{8 \times F_S \times C_{OUT}} \right) \quad (11)$$

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Typical Application (continued)

9.2.2.6 D1

A Schottky type re-circulating diode is required for all LM5575-Q1 applications. Ultra-fast diodes are not recommended and may result in damage to the IC due to reverse recovery current transients. The near ideal reverse recovery characteristics and low-forward voltage drop are particularly important diode characteristics for high-input voltage and low-output voltage applications common to the LM5575-Q1. The reverse recovery characteristic determines how long the current surge lasts each cycle when the buck switch is turned on. The reverse recovery characteristics of Schottky diodes minimize the peak instantaneous power in the buck switch occurring during turn-on each cycle. The resulting switching losses of the buck switch are significantly reduced when using a Schottky diode. The reverse breakdown rating should be selected for the maximum V_{IN}, plus some safety margin.

The forward voltage drop has a significant impact on the conversion efficiency, especially for applications with a low output voltage. *Rated* current for diodes vary widely from various manufacturers. The worst case is to assume a short circuit load condition. In this case the diode will carry the output current almost continuously. For the LM5575-Q1 this current can be as high as 2.1 A. Assuming a worst case 1-V drop across the diode, the maximum diode power dissipation can be as high as 2.1 W. For the reference design a 100-V Schottky in a SMC package was selected.

9.2.2.7 C1, C2

The regulator supply voltage has a large source impedance at the switching frequency. Good-quality input capacitors are necessary to limit the ripple voltage at the VIN pin while supplying most of the switch current during the on-time. When the buck switch turns on, the current into the VIN pin steps to the lower peak of the inductor current waveform, ramps up to the peak value, then drops to zero at turn-off. The average current into VIN during the on-time is the load current. The input capacitance should be selected for RMS current rating and minimum ripple voltage. A good approximation for the required ripple current rating necessary is $I_{RMS} > I_{OUT} / 2$.

Quality ceramic capacitors with a low ESR should be selected for the input filter. To allow for capacitor tolerances and voltage effects, two 1.0-µF, 100-V ceramic capacitors will be used. If step input voltage transients are expected near the maximum rating of the LM5575-Q1, a careful evaluation of ringing and possible spikes at the device VIN pin should be completed. An additional damping network or input voltage clamp may be required in these cases.

9.2.2.8 C8

The capacitor at the VCC pin provides noise filtering and stability for the V_{CC} regulator. The recommended value of C8 should be no smaller than 0.1 µF, and should be a good-quality, low-ESR, ceramic capacitor. A value of 0.47 µF was selected for this design.

9.2.2.9 C7

The bootstrap capacitor between the BST and the SW pins supplies the gate current to charge the buck switch gate at turn-on. The recommended value of C7 is 0.022 µF, and should be a good-quality, low-ESR, ceramic capacitor.

9.2.2.10 C4

The capacitor at the SS pin determines the soft-start time, i.e. the time for the reference voltage and the output voltage, to reach the final regulated value. The time is determined from:

$$t_{ss} = \frac{C4 \times 1.225V}{10\ \mu A} \quad (12)$$

For this application, a C4 value of 0.01 µF was chosen which corresponds to a soft-start time of 1 ms.

9.2.2.11 R5, R6

R5 and R6 set the output voltage level, the ratio of these resistors is calculated from:

$$R5/R6 = (V_{OUT} / 1.225V) - 1 \quad (13)$$

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Typical Application (continued)

For a 5-V output, the R5/R6 ratio calculates to 3.082. The resistors should be chosen from standard value resistors, a good starting point is selection in the range of 1.0 kΩ - 10 kΩ. Values of 5.11 kΩ for R5, and 1.65 kΩ for R6 were selected.

9.2.2.12 R1, R2, C12

A voltage divider can be connected to the SD pin to set a minimum operating voltage $V_{IN(min)}$ for the regulator. If this feature is required, the easiest approach to select the divider resistor values is to select a value for R1 (between 10 kΩ and 100 kΩ recommended) then calculate R2 from:

$$R2 = 1.225 \times \left(\frac{R1}{V_{IN(min)} + (5 \times 10^{-6} \times R1) - 1.225} \right) \quad (14)$$

Capacitor C12 provides filtering for the divider. The voltage at the SD pin should never exceed 8 V, when using an external set-point divider it may be necessary to clamp the SD pin at high input voltage conditions. The reference design utilizes the full range of the LM5575-Q1 (6 V to 75 V); therefore these components can be omitted. With the SD pin open circuit the LM5575-Q1 responds once the V_{CC} UVLO threshold is satisfied.

9.2.2.13 R7, C11

A snubber network across the power diode reduces ringing and spikes at the switching node. Excessive ringing and spikes can cause erratic operation and couple spikes and noise to the output. Voltage spikes beyond the rating of the LM5575-Q1 or the re-circulating diode can damage these devices. Selecting the values for the snubber is best accomplished through empirical methods. First, make sure the lead lengths for the snubber connections are very short. For the current levels typical for the LM5575-Q1 a resistor value between 5 and 20 Ohms is adequate. Increasing the value of the snubber capacitor results in more damping but higher losses. Select a minimum value of C11 that provides adequate damping of the SW pin waveform at high load.

9.2.2.14 R4, C5, C6

These components configure the error amplifier gain characteristics to accomplish a stable overall loop gain. One advantage of current mode control is the ability to close the loop with only two feedback components, R4 and C5. The overall loop gain is the product of the modulator gain and the error amplifier gain. The DC modulator gain of the LM5575-Q1 is as follows:

$$\text{DC Gain}_{(MOD)} = G_{m(MOD)} \times R_{LOAD} = 1 \times R_{LOAD} \quad (15)$$

The dominant low frequency pole of the modulator is determined by the load resistance (R_{LOAD},) and output capacitance (C_{OUT}). The corner frequency of this pole is:

$$f_{p(MOD)} = 1 / (2\pi R_{LOAD} C_{OUT}) \quad (16)$$

For R_{LOAD} = 5 Ω and C_{OUT} = 130 µF then $f_{p(MOD)}$ = 245 Hz

$\text{DC Gain}_{(MOD)}$ = 1 x 5 = 14 dB

For the design example of Figure 8 the following modulator gain vs. frequency characteristic was measured as shown in Figure 19.

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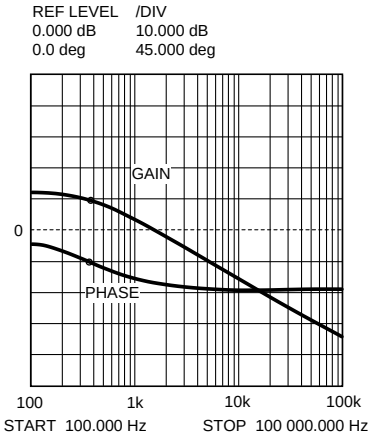
Typical Application (continued)



R_{LOAD} = 5 Ohms

C_{OUT} = 130 µF

Figure 19. Gain and Phase of Modulator

Components R4 and C5 configure the error amplifier as a type II configuration which has a pole at DC and a zero at f_Z = 1 / (2πR4C5). The error amplifier zero cancels the modulator pole leaving a single pole response at the crossover frequency of the loop gain. A single pole response at the crossover frequency yields a very stable loop with 90 degrees of phase margin.

For the design example, a target loop bandwidth (crossover frequency) of 15 kHz was selected. The compensation network zero (f_Z) should be selected at least an order of magnitude less than the target crossover frequency. This constrains the product of R4 and C5 for a desired compensation network zero 1 / (2π R4 C5) to be less than 2 kHz. Increasing R4, while proportionally decreasing C5, increases the error amp gain. Conversely, decreasing R4 while proportionally increasing C5, decreases the error amp gain. For the design example C5 was selected for 0.01 µF and R4 was selected for 49.9 kΩ. These values configure the compensation network zero at 320 Hz. The error amp gain at frequencies greater than f_Z is: R4 / R5, which is approximately 10 (20 dB).

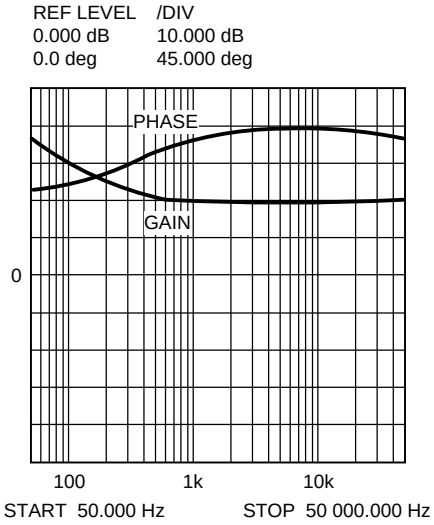


Figure 20. Error Amplifier Gain and Phase

The overall loop can be predicted as the sum (in dB) of the modulator gain and the error amp gain.

Typical Application (continued)

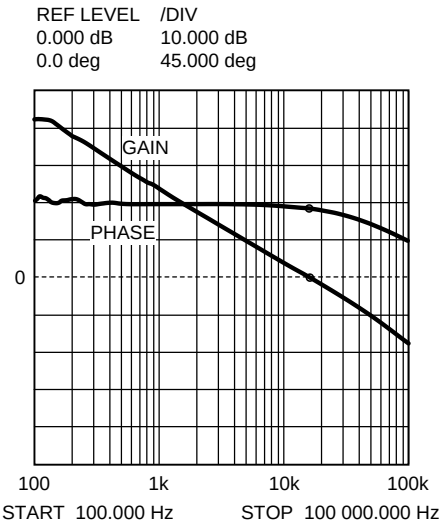


Figure 21. Overall Loop Gain and Phase

If a network analyzer is available, the modulator gain can be measured and the error amplifier gain can be configured for the desired loop transfer function. If a network analyzer is not available, the error amplifier compensation components can be designed with the guidelines given. Step-load transient tests can be performed to verify acceptable performance. The step-load goal is minimum overshoot with a damped response. C6 can be added to the compensation network to decrease noise susceptibility of the error amplifier. The value of C6 must be sufficiently small since the addition of this capacitor adds a pole in the error amplifier transfer function. This pole must be well beyond the loop crossover frequency. A good approximation of the location of the pole added by C6 is: f_{p2} = fz × C5 / C6.

9.2.3 Application Curves

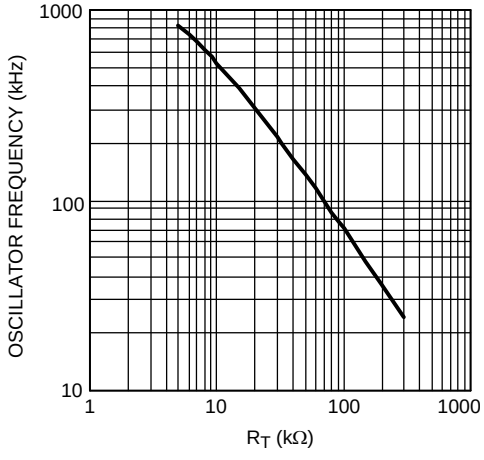


Figure 22. Oscillator Frequency vs R_T

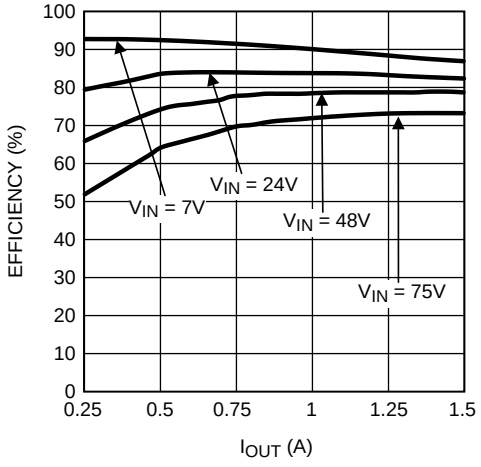


Figure 23. Demoboard Efficiency vs I_{OUT} and V_{IN}

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10 Power Supply Recommendations

The LM5575-Q1 is designed to operate from an input voltage supply range between 6 V and 75 V. This input supply should be able to withstand the maximum input current and maintain a voltage above 6 V. The resistance of the input supply rail should be low enough that an input current transient does not cause a high enough drop at the LM5575-Q1 supply voltage that can cause a false UVLO fault triggering and system reset. If the input supply is located more than a few inches from the LM5575-Q1 additional bulk capacitance may be required in addition to the ceramic bypass capacitors. The amount of bulk capacitance is not critical, but a 47-µF or 100-µF electrolytic capacitor is a typical choice.

11 Layout

11.1 Layout Guidelines

The circuit in Figure 8 serves as both a block diagram of the LM5575-Q1 and a typical application board schematic for the LM5575-Q1. In a buck regulator, there are two loops where currents are switched very fast. The first loop starts from the input capacitors, to the regulator VIN pin, to the regulator SW pin, to the inductor then out to the load. The second loop starts from the output capacitor ground, to the regulator PGND pins, to the regulator IS pins, to the diode anode, to the inductor and then out to the load. Minimizing the loop area of these two loops reduces the stray inductance and minimizes noise and possible erratic operation. A ground plane in the PC board is recommended as a means to connect the input filter capacitors to the output filter capacitors and the PGND pins of the regulator. Connect all of the low-power ground connections (C_{SS}, R_T, C_{RAMP}) directly to the regulator AGND pin. Connect the AGND and PGND pins together through the top-side copper area covering the entire underside of the device. Place several vias in this underside copper area to the ground plane.

The two highest power-dissipating components are the re-circulating diode and the LM5575-Q1 regulator IC. The easiest method to determine the power dissipated within the LM5575-Q1 is to measure the total conversion losses (Pin – Pout) then subtract the power losses in the Schottky diode, output inductor and snubber resistor.

An approximation for the Schottky diode loss is:

$$P = (1-D) \times Iout \times Vfwd \quad (17)$$

An approximation for the output inductor power is:

$$P = I_{OUT}^2 \times R \times 1.1 \quad (18)$$

where

- R is the DC resistance of the inductor and the 1.1 factor is an approximation for the AC losses

If a snubber is used, an approximation for the damping resistor power dissipation is:

$$P = Vin^2 \times Fsw \times Csnub \quad (19)$$

where

- Fsw is the switching frequency and Csnub is the snubber capacitor

The regulator has an exposed thermal pad to aid power dissipation. Adding several vias under the device to the ground plane will greatly reduce the regulator junction temperature. Selecting a diode with an exposed pad will aid the power dissipation of the diode.

The most significant variables that affect the power dissipated by the LM5575-Q1 are the output current, input voltage and operating frequency. The power dissipated while operating near the maximum output current and maximum input volatge can be appreciable. The operating frequency of the LM5575-Q1 evaluation board has been designed for 300 kHz. When operating at 1.5-A output current with a 70-V input the power dissipation of the LM5575-Q1 regulator is approximately 1.25 W.

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11.2 Layout Example

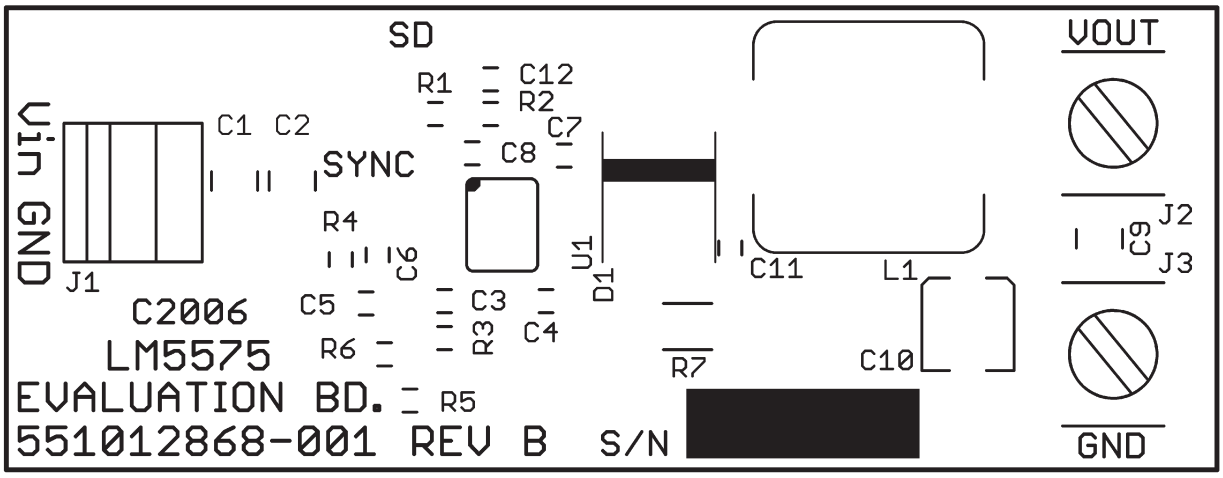

Figure 24. Silkscreen

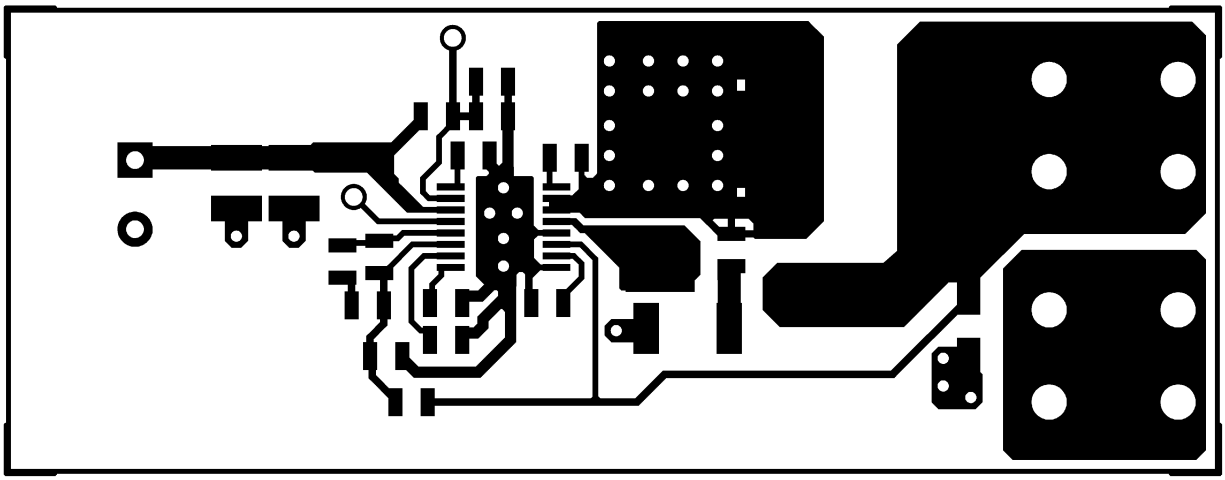

Figure 25. Component Side

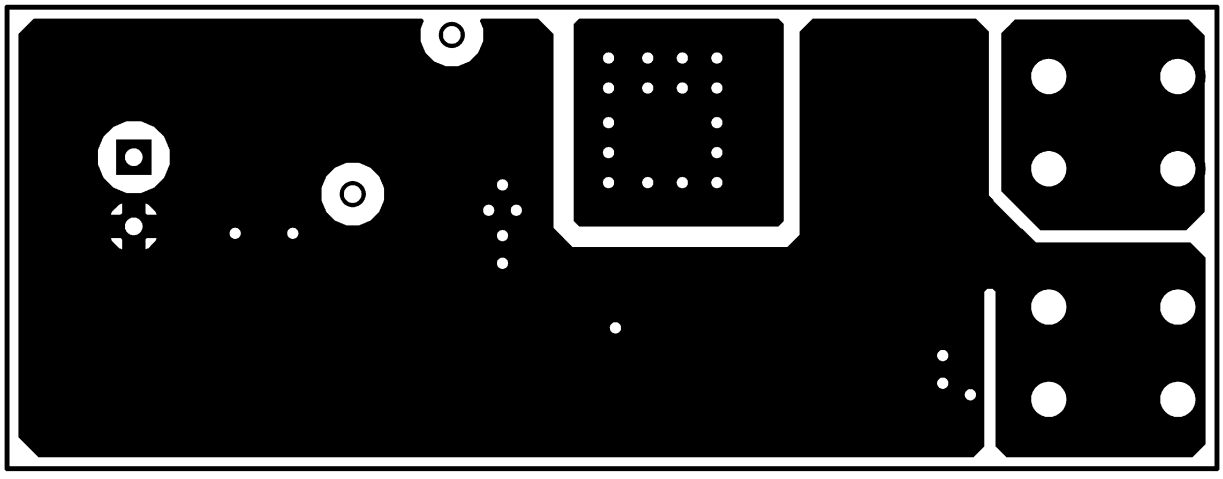

Figure 26. Solder Side

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11.3 Thermal Considerations

The junction-to-ambient thermal resistance of the LM5575-Q1 will vary with the application. The most significant variables are the area of copper in the PC board, the number of vias under the IC exposed pad and the amount of forced air cooling provided. Referring to the evaluation board artwork, the area under the LM5575-Q1 (component side) is covered with copper and there are 5 connection vias to the solder-side ground plane. Additional vias under the IC will have diminishing value as more vias are added. The integrity of the solder connection from the IC exposed pad to the PC board is critical. Excessive voids will greatly diminish the thermal dissipation capacity. The junction-to-ambient thermal resistance of the LM5575-Q1 mounted in the evaluation board varies from 50°C/W with no airflow to 28°C/W with 900 LFM (Linear Feet per Minute). With a 25°C ambient temperature and no airflow, the predicted junction temperature for the LM5575-Q1 will be 25 + (50 × 1.25) = 88°C. If the evaluation board is operated at 1.5-A output current, 70-V input voltage and high-ambient temperature for a prolonged period of time the thermal shutdown protection within the IC may activate. The IC will turn off allowing the junction to cool, followed by restart with the soft-start capacitor reset to zero.

12 Device and Documentation Support

12.1 Trademarks

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12.2 Electrostatic Discharge Caution



These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

12.3 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

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PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
LM5575Q0MH/NOPB	ACTIVE	HTSSOP	PWP	16	92	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 125	LM5575 Q0MH	Samples
LM5575Q0MHX/NOPB	PREVIEW	HTSSOP	PWP	16	2500	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 125	LM5575 Q0MH	
LM5575QMH/NOPB	ACTIVE	HTSSOP	PWP	16	92	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 125	LM5575 QMH	Samples
LM5575QMHX/NOPB	ACTIVE	HTSSOP	PWP	16	2500	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 125	LM5575 QMH	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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OTHER QUALIFIED VERSIONS OF LM5575-Q1 :

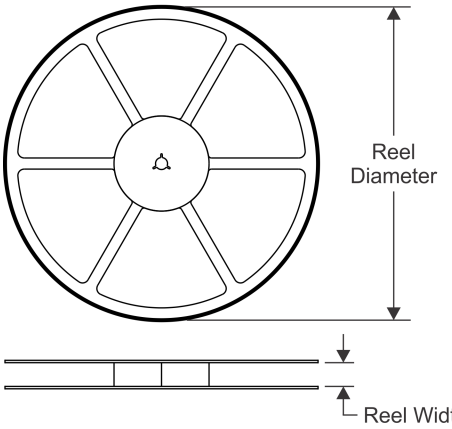
- Catalog: LM5575

NOTE: Qualified Version Definitions:

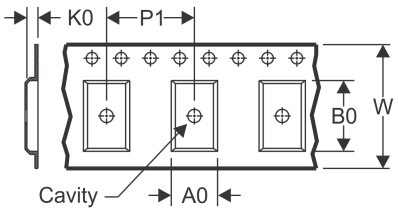
- Catalog - TI's standard catalog product

TAPE AND REEL INFORMATION

REEL DIMENSIONS

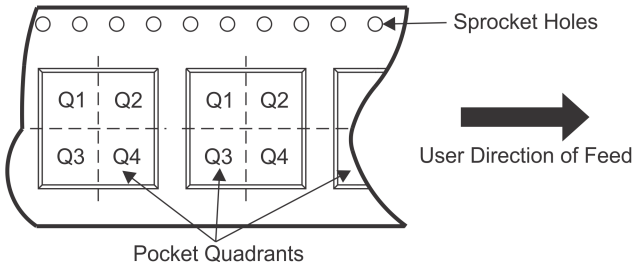


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

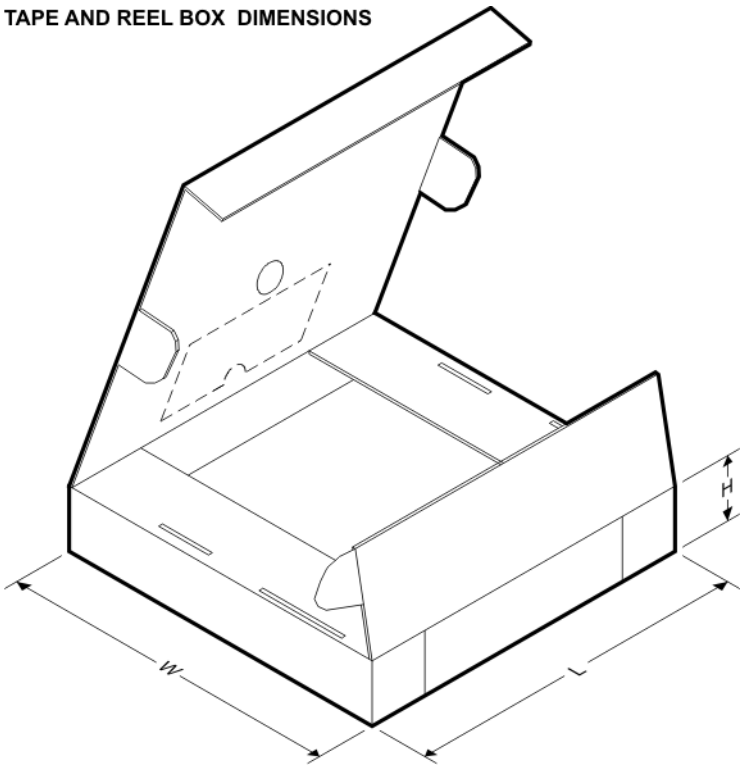
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

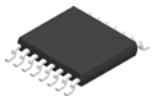
Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
LM5575QMHX/NOPB	HTSSOP	PWP	16	2500	330.0	12.4	6.95	5.6	1.6	8.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
LM5575QMHX/NOPB	HTSSOP	PWP	16	2500	367.0	367.0	35.0

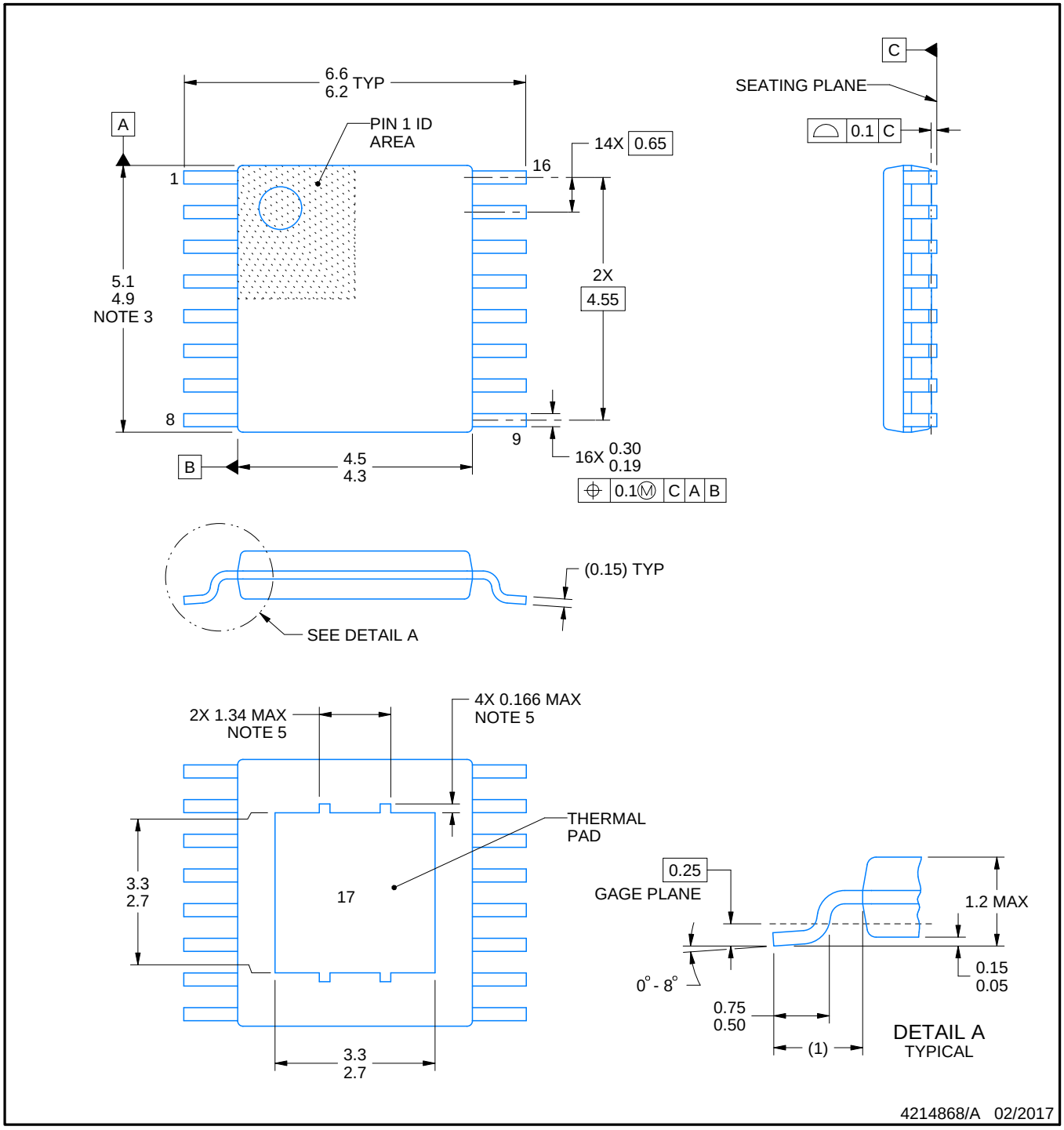


PACKAGE OUTLINE

PWP0016A

PowerPAD ™ HTSSOP - 1.2 mm max height

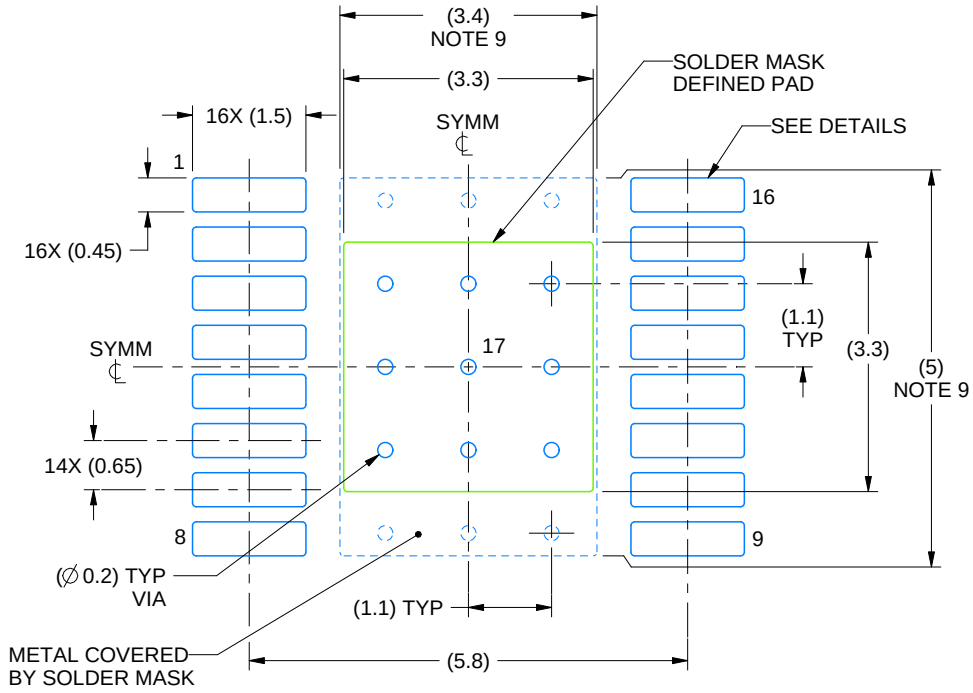
PLASTIC SMALL OUTLINE



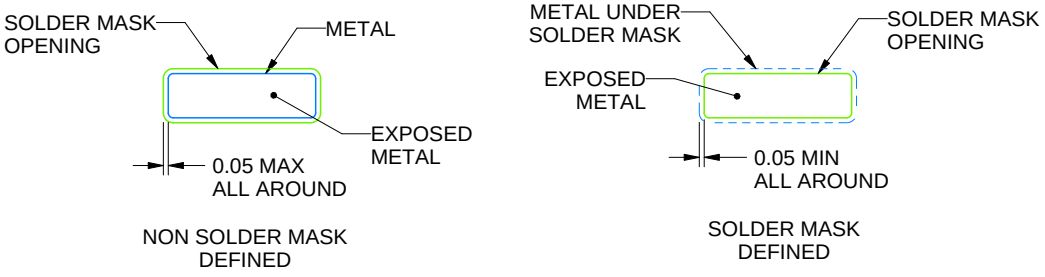
PowerPAD is a trademark of Texas Instruments.

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. Reference JEDEC registration MO-153.
5. Features may not be present.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:10X



SOLDER MASK DETAILS
PADS 1-16

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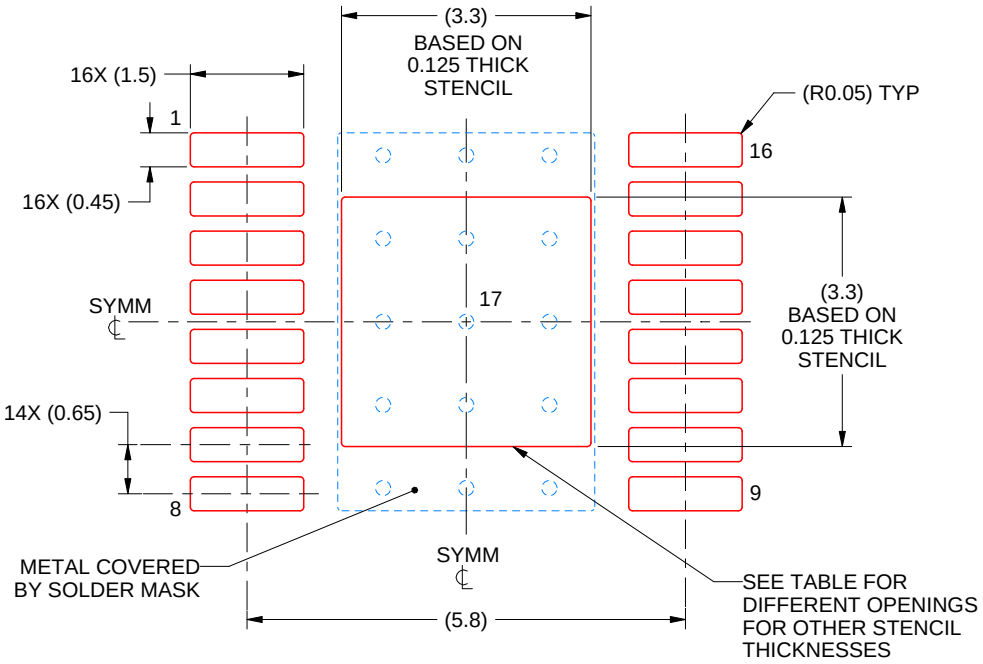
NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
8. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature numbers SLMA002 (www.ti.com/lit/slma002) and SLMA004 (www.ti.com/lit/slma004).
9. Size of metal pad may vary due to creepage requirement.



SOLDER PASTE EXAMPLE
EXPOSED PAD
100% PRINTED SOLDER COVERAGE BY AREA
SCALE:10X

STENCIL THICKNESS	SOLDER STENCIL OPENING
0.1	3.69 X 3.69
0.125	3.3 X 3.3 (SHOWN)
0.15	3.01 X 3.01
0.175	2.79 X 2.79

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NOTES: (continued)

10. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
11. Board assembly site may have different recommendations for stencil design.

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