LM5106 100-V Half-Bridge Gate Driver With Programmable Dead-Time

1 Features

- Drives Both a High-Side and Low-Side N-Channel MOSFET
- 1.8-A Peak Output Sink Current
- 1.2-A Peak Output Source Current
- Bootstrap Supply Voltage Range up to 118-V DC
- Single TTL Compatible Input
- Programmable Turnon Delays (Dead-Time)
- Enable Input Pin
- Fast Turnoff Propagation Delays (32 ns Typical)
- Drives 1000 pF With 15-ns Rise and 10-ns Fall Time
- Supply Rail Undervoltage Lockout
- Low Power Consumption
- 10-Pin WSON Package (4 mm × 4 mm) and 10-Pin VSSOP Package

2 Applications

- Solid-State Motor Drives
- Half-Bridge and Full-Bridge Power Converters
- Two Switch Forward Power Converters

3 Description

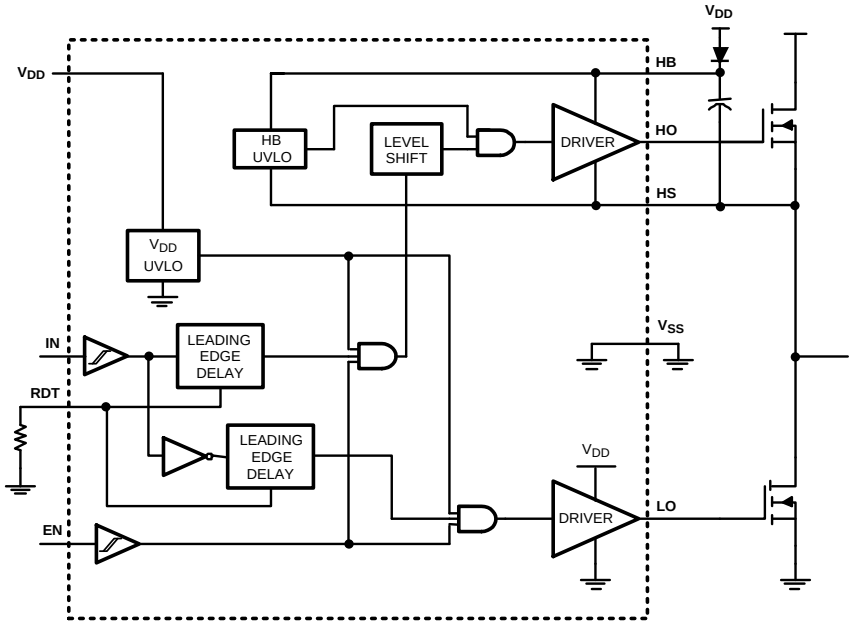
The LM5106 is a high-voltage gate driver designed to drive both the high-side and low-side N-channel MOSFETs in a synchronous buck or half-bridge configuration. The floating high-side driver can work with rail voltages up to 100 V. The single control input is compatible with TTL signal levels and a single external resistor programs the switching transition dead-time through tightly matched turnon delay circuits. The robust level shift technology operates at high speed while consuming low power and provides clean output transitions. Undervoltage lockout (UVLO) disables the gate driver when either the low side or the bootstrapped high-side supply voltage is below the operating threshold. The LM5106 is offered in the 10-pin VSSOP or the thermally enhanced 10-pin WSON plastic package.

Device Information(1)

PART NUMBER	PACKAGE	BODY SIZE (NOM)
LM5106	VSSOP (10)	3.00 mm × 3.00 mm
	WSON (10)	4.00 mm × 4.00 mm

(1) For all available packages, see the orderable addendum at the end of the datasheet.

Simplified Block Diagram



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4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision C (March 2013) to Revision D **Page**

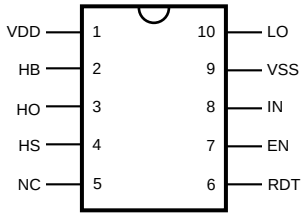
- Added *Pin Configuration and Functions* section, *ESD Ratings* table, *Feature Description* section, *Device Functional Modes*, *Application and Implementation* section, *Power Supply Recommendations* section, *Layout* section, *Device and Documentation Support* section, and *Mechanical, Packaging, and Orderable Information* section ... 1

Changes from Revision B (March 2013) to Revision C **Page**

- Changed layout of National Data Sheet to TI format ... 12

5 Pin Configuration and Functions

10-Pin
VSSOP (DGS), WSON (DPR)
Top View



Pin Functions

PIN		DESCRIPTION	APPLICATION INFORMATION
NO.	NAME		
1	VDD	Positive gate drive supply	Decouple VDD to VSS using a low ESR/ESL capacitor, placed as close to the IC as possible.
2	HB	High-side gate driver bootstrap rail	Connect the positive terminal of bootstrap capacitor to the HB pin and connect negative terminal to HS. The Bootstrap capacitor should be placed as close to IC as possible.
3	HO	High-side gate driver output	Connect to the gate of high-side N-MOS device through a short, low inductance path.
4	HS	High-side MOSFET source connection	Connect to the negative terminal of the bootststrap capacitor and to the source of the high-side N-MOS device.
5	NC	Not connected	
6	RDT	Dead-time programming pin	A resistor from RDT to VSS programs the turnon delay of both the high- and low-side MOSFETs. The resistor should be placed close to the IC to minimize noise coupling from adjacent PC board traces.
7	EN	Logic input for driver Disable/Enable	TTL compatible threshold with hysteresis. LO and HO are held in the low state when EN is low.
8	IN	Logic input for gate driver	TTL compatible threshold with hysteresis. The high-side MOSFET is turned on and the low-side MOSFET turned off when IN is high.
9	VSS	Ground return	All signals are referenced to this ground.
10	LO	Low-side gate driver output	Connect to the gate of the low-side N-MOS device with a short, low inductance path.
—	EP	Exposed Pad	The exposed pad has no electrical contact. Connect to system ground plane for reduced thermal resistance.

6 Specifications

6.1 Absolute Maximum Ratings[1][2]

	MIN	MAX	UNIT
V_{DD} to V_{SS}	–0.3	18	V
HB to HS	–0.3	18	V
IN and EN to V_{SS}	–0.3	V_{DD} + 0.3	V
LO to V_{SS}	–0.3	V_{DD} + 0.3	V
HO to V_{SS}	HS – 0.3	HB + 0.3	V
HS to V_{SS}[3]		100	V
HB to V_{SS}		118	V
RDT to V_{SS}	–0.3	5	V
Junction Temperature		150	°C
Storage temperature range, T_{stg}	–55	150	°C

(1) Absolute Maximum Ratings indicate limits beyond which damage to the component may occur. *Recommended Operating Conditions* are conditions under which operation of the device is ensured. Operating Ratings do not imply ensured performance limits. For ensured performance limits and associated test conditions, see the *Electrical Characteristics*.
(2) If Military/Aerospace specified devices are required, please contact the Texas Instruments Sales Office/Distributors for availability and specifications.
(3) In the application the HS node is clamped by the body diode of the external lower N-MOSFET, therefore the HS voltage will generally not exceed –1 V. However in some applications, board resistance and inductance may result in the HS node exceeding this stated voltage transiently. If negative transients occur on HS, the HS voltage must never be more negative than V_{DD} - 15 V. For example, if V_{DD} = 10 V, the negative transients at HS must not exceed –5 V.

6.2 ESD Ratings

		VALUE	UNIT
$V_{(ESD)}$ Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001[1]	±1500	V

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

	MIN	MAX	UNIT
V_{DD}	8	14	V
HS[1]	–1	100	V
HB	HS + 8	HS + 14	V
HS Slew Rate		< 50	V/ns
Junction Temperature	–40	125	°C

(1) In the application the HS node is clamped by the body diode of the external lower N-MOSFET, therefore the HS voltage will generally not exceed –1 V. However in some applications, board resistance and inductance may result in the HS node exceeding this stated voltage transiently. If negative transients occur on HS, the HS voltage must never be more negative than V_{DD} - 15 V. For example, if V_{DD} = 10 V, the negative transients at HS must not exceed –5 V.

6.4 Thermal Information

THERMAL METRIC[1]		LM5102		UNIT
		DGS	DPR[2]	
		10 PINS	10 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	165.3	37.9	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	58.9	38.1	
$R_{\theta JB}$	Junction-to-board thermal resistance	54.4	14.9	
ψ_{JT}	Junction-to-top characterization parameter	6.2	0.4	
ψ_{JB}	Junction-to-board characterization parameter	83.6	15.2	
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	N/A	4.4	

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report (SPRA953).
(2) Four-layer board with Cu finished thickness 1.5 oz, 1 oz, 1 oz, 1.5 oz. Maximum die size used. 5x body length of Cu trace on PCB top. 50-mm × 50-mm ground and power planes embedded in PCB. See Application Note *AN-1187 Leadless Leadframe Package (LLP)* (SNOA401).

6.5 Electrical Characteristics

MIN and MAX limits apply over the full operating junction temperature range. Unless otherwise specified, T_J = +25°C, V_{DD} = HB = 12 V, V_{SS} = HS = 0 V, EN = 5 V. No load on LO or HO. RDT= 100kΩ[1].

SYMBOL	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
SUPPLY CURRENTS						
I_{DD}	V_{DD} Quiescent Current	IN = EN = 0 V		0.34	0.6	mA
I_{DDO}	V_{DD} Operating Current	f = 500 kHz		2.1	3.5	mA
I_{HB}	Total HB Quiescent Current	IN = EN = 0 V		0.06	0.2	mA
I_{HBO}	Total HB Operating Current	f = 500 kHz		1.5	3	mA
I_{HBS}	HB to V_{SS} Current, Quiescent	HS = HB = 100 V		0.1	10	µA
I_{HBSO}	HB to V_{SS} Current, Operating	f = 500 kHz		0.5		mA
INPUT IN and EN						
V_{IL}	Low Level Input Voltage Threshold		0.8	1.8		V
V_{IH}	High Level Input Voltage Threshold			1.8	2.2	V
R_{pd}	Input Pulldown Resistance Pin IN and EN		100	200	500	kΩ
DEAD-TIME CONTROLS						
VRDT	Nominal Voltage at RDT		2.7	3	3.3	V
IRDT	RDT Pin Current Limit	RDT = 0 V	0.75	1.5	2.25	mA
UNDERVOLTAGE PROTECTION						
V_{DDR}	V_{DD} Rising Threshold		6.2	6.9	7.6	V
V_{DDH}	V_{DD} Threshold Hysteresis			0.5		V
V_{HBR}	HB Rising Threshold		5.9	6.6	7.3	V
V_{HBH}	HB Threshold Hysteresis			0.4		V
LO GATE DRIVER						
V_{OLL}	Low-Level Output Voltage	I_{LO} = 100 mA		0.21	0.4	V
V_{OHL}	High-Level Output Voltage	I_{LO} = –100 mA, $V_{OHL} = V_{DD} - V_{LO}$		0.5	0.85	V
I_{OHL}	Peak Pullup Current	LO = 0 V		1.2		A
I_{OLL}	Peak Pulldown Current	LO = 12 V		1.8		A
HO GATE DRIVER						
V_{OLH}	Low-Level Output Voltage	I_{HO} = 100 mA		0.21	0.4	V
V_{OHH}	High-Level Output Voltage	I_{HO} = –100 mA, $V_{OHH} = HB - HO$		0.5	0.85	V

(1) Min and Max limits are 100% production tested at 25°C. Limits over the operating temperature range are ensured through correlation using Statistical Quality Control (SQC) methods. Limits are used to calculate Average Outgoing Quality Level (AOQL).

Electrical Characteristics (continued)

MIN and MAX limits apply over the full operating junction temperature range. Unless otherwise specified, T_J = +25°C, V_{DD} = HB = 12 V, V_{SS} = HS = 0 V, EN = 5 V. No load on LO or HO. RDT= 100kΩ(1).

SYMBOL	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
I_{OHH}	Peak Pullup Current	HO = 0 V		1.2		A
I_{OLH}	Peak Pulldown Current	HO = 12 V		1.8		A
THERMAL RESISTANCE						
θ_{JA}	Junction to Ambient	See(2)(3)		40		°C/W

(2) Four-layer board with Cu finished thickness 1.5/1.0/1.0/1.5 oz. Maximum die size used. 5x body length of Cu trace on PCB top. 50-mm × 50-mm ground and power planes embedded in PCB. See *AN-1187 Leadless Leadframe Package (LLP)*, SNOA401.
(3) The θ_{JA} is not a constant for the package and depends on the printed circuit board design and the operating conditions.

6.6 Switching Characteristics

MIN and MAX limits apply over the full operating junction temperature range. Unless otherwise specified, T_J = +25°C, V_{DD} = HB = 12 V, V_{SS} = HS = 0 V, No Load on LO or HO(1).

SYMBOL	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{LPHL}	Lower Turn-Off Propagation Delay			32	56	ns
t_{HPHL}	Upper Turn-Off Propagation Delay			32	56	
t_{LPLH}	Lower Turn-On Propagation Delay	RDT = 100k	400	520	640	
t_{HPLH}	Upper Turn-On Propagation Delay	RDT = 100k	450	570	690	
t_{LPLH}	Lower Turn-On Propagation Delay	RDT = 10k	85	115	160	
t_{HPLH}	Upper Turn-On Propagation Delay	RDT = 10k	85	115	160	
t_{en}, t_{sd}	Enable and Shutdown propagation delay			36		
DT1, DT2	Dead-time LO OFF to HO ON & HO OFF to LO ON	RDT = 100k		510		
		RDT = 10k		86		
MDT	Dead-time matching	RDT = 100k		50		
t_R	Either Output Rise Time	C_L = 1000pF		15		
t_F	Either Output Fall Time	C_L = 1000pF		10		

(1) Min and Max limits are 100% production tested at 25°C. Limits over the operating temperature range are ensured through correlation using Statistical Quality Control (SQC) methods. Limits are used to calculate Average Outgoing Quality Level (AOQL).

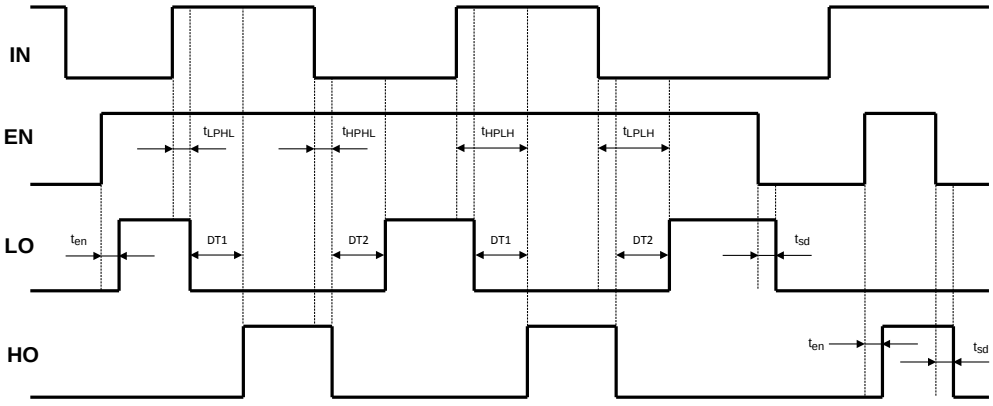


Figure 1. LM5106 Input - Output Waveforms

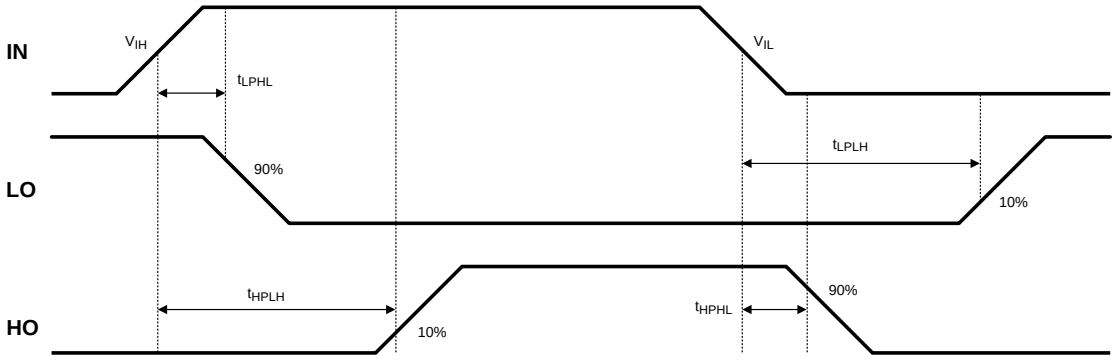


Figure 2. LM5106 Switching Time Definitions: t_{LPLH}, t_{LPHL}, t_{HPLH}, t_{HPHL}

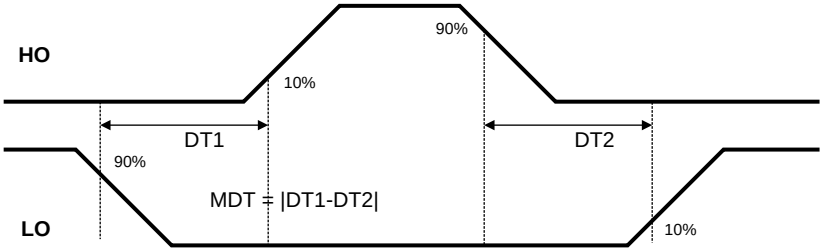


Figure 3. LM5106 Dead-time: DT

6.7 Typical Characteristics

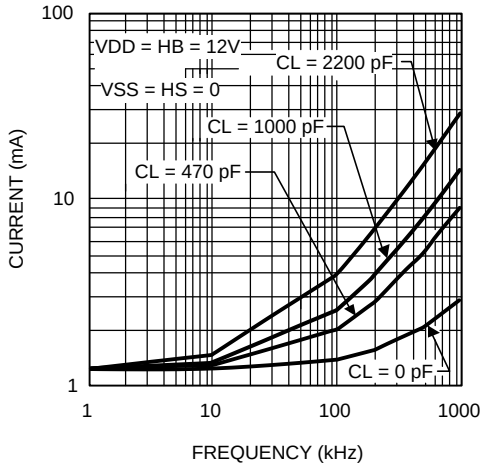


Figure 4. V_{DD} Operating Current vs Frequency

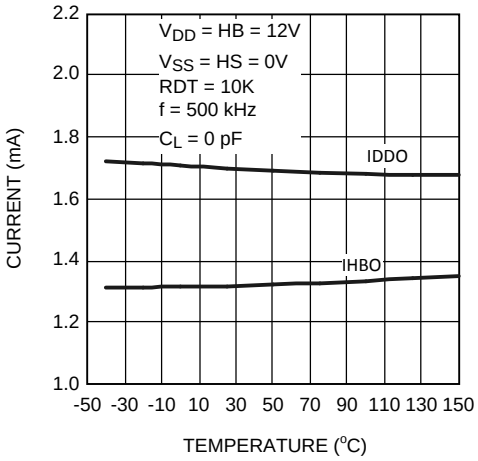


Figure 5. Operating Current vs Temperature

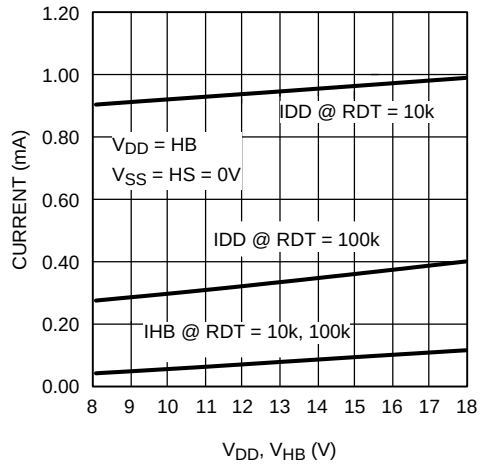


Figure 6. Quiescent Current vs Supply Voltage

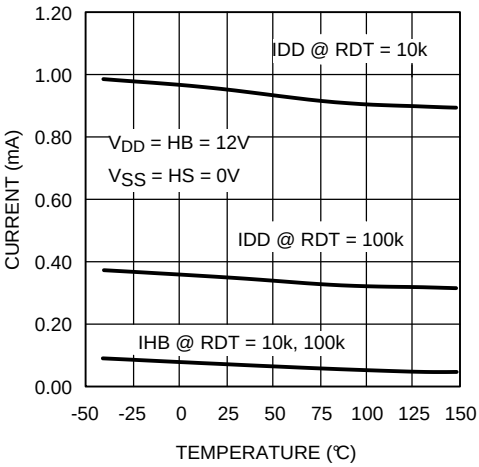


Figure 7. Quiescent Current vs Temperature

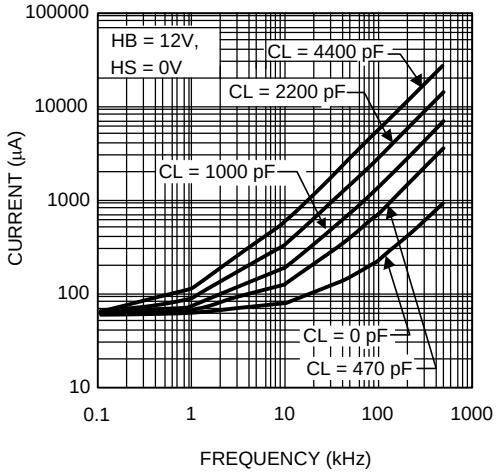


Figure 8. HB Operating Current vs Frequency

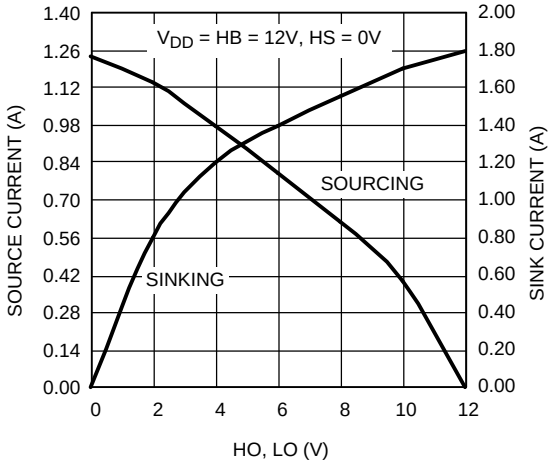


Figure 9. HO and LO Peak Output Current vs Output Voltage

Typical Characteristics (continued)

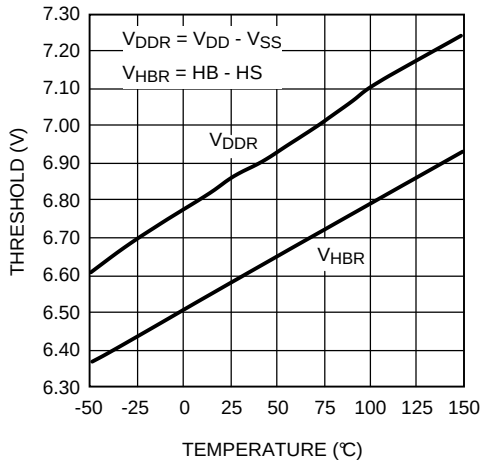


Figure 10. Undervoltage Rising Threshold vs Temperature

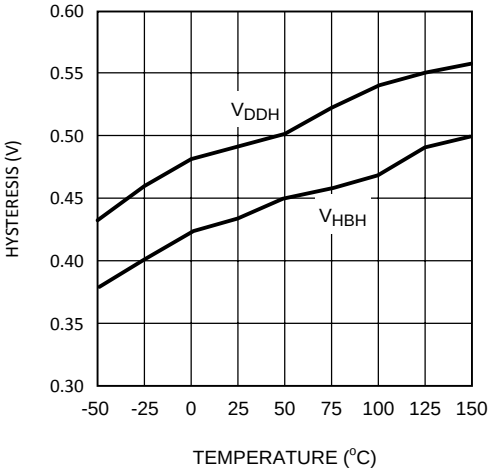


Figure 11. Undervoltage Hysteresis vs Temperature

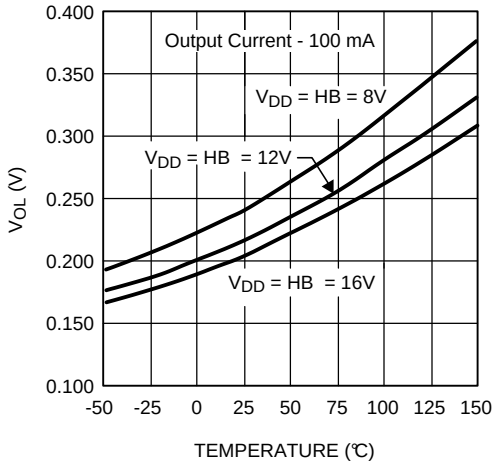


Figure 12. LO and HO - Low-Level Output Voltage vs Temperature

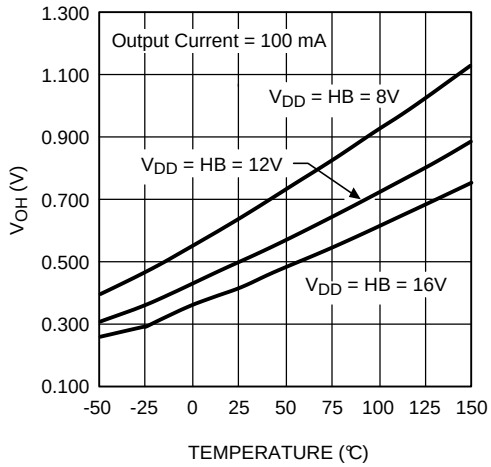


Figure 13. LO and HO - High-Level Output Voltage vs Temperature

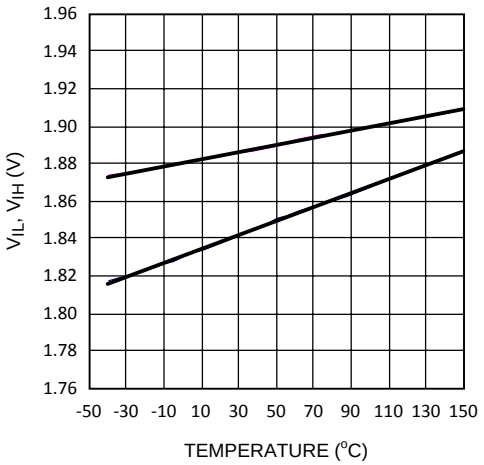


Figure 14. Input Threshold vs Temperature

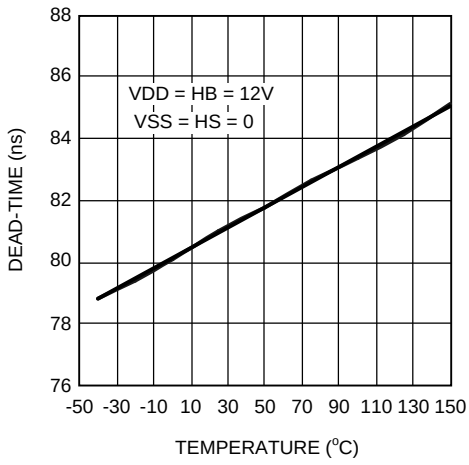


Figure 15. Dead-Time vs Temperature (RT = 10k)

Typical Characteristics (continued)

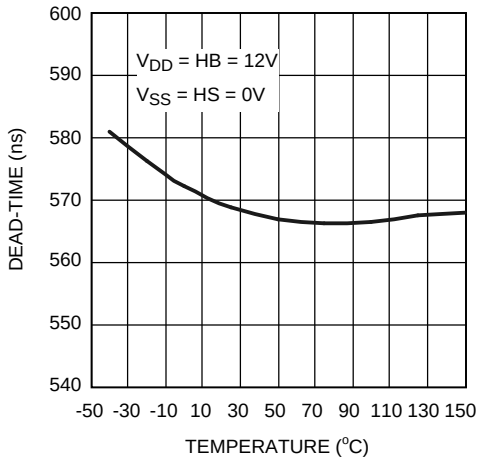


Figure 16. Dead-Time vs Temperature (RT = 100k)

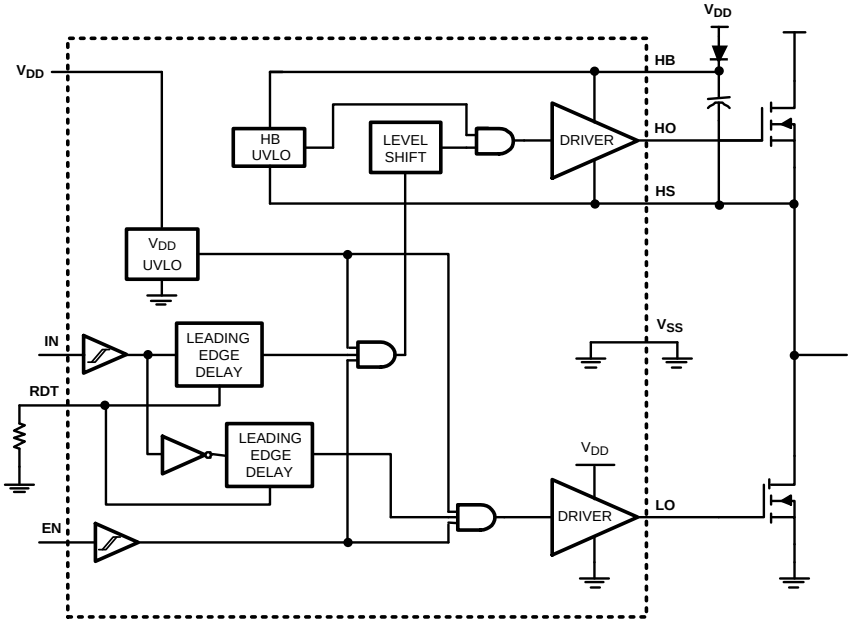
7 Detailed Description

7.1 Overview

The LM5106 is a single PWM input gate driver with Enable that offers a programmable dead-time. The dead-time is set with a resistor at the RDT pin and can be adjusted from 100 ns to 600 ns. The wide dead-time programming range provides the flexibility to optimize drive signal timing for a wide range of MOSFETs and applications.

The RDT pin is biased at 3 V and current limited to 1 mA maximum programming current. The time delay generator will accommodate resistor values from 5k to 100k with a dead-time time that is proportional to the RDT resistance. Grounding the RDT pin programs the LM5106 to drive both outputs with minimum dead-time.

7.2 Functional Block Diagram



7.3 Feature Description

7.3.1 Start-up and UVLO

Both top and bottom drivers include undervoltage lockout (UVLO) protection circuitry which monitors the supply voltage (V_{DD}) and bootstrap capacitor voltage (HB – HS) independently. The UVLO circuit inhibits each driver until sufficient supply voltage is available to turn on the external MOSFETs, and the UVLO hysteresis prevents chattering during supply voltage transitions. When the supply voltage is applied to the V_{DD} pin of the LM5106, the top and bottom gates are held low until V_{DD} exceeds the UVLO threshold, typically about 6.9 V. Any UVLO condition on the bootstrap capacitor will disable only the high-side output (HO).

7.4 Device Functional Modes

EN	IN Pin	LO Pin	HO Pin
L	Any	L	L
H	H	L	H
H	L	H	L

8 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

8.1 Application Information

The LM5106 is one of the latest generation of high-voltage gate drivers which are designed to drive both the high-side and low-side N-channel MOSFETs in a half-bridge/full bridge configuration or in a synchronous buck circuit. The floating high-side driver can operate with supply voltages up to 110 V. This allows for N-channel MOSFET control in half-bridge, full-bridge, push-pull, two switch forward and active clamp topologies.

The outputs of the LM5106 are controlled from a single input. The rising edge of each output can be delayed with a programming resistor.

Table 1. Highlights

FEATURE	BENEFIT
Programmable Turnon Delay	Allows optimization of gate drive timings in bridge topologies
Enable Pin	Reduces operating current when disabled to improved power system standby power
Low Power Consumption	Improves light load efficiency figures of the power stage.

8.2 Typical Application

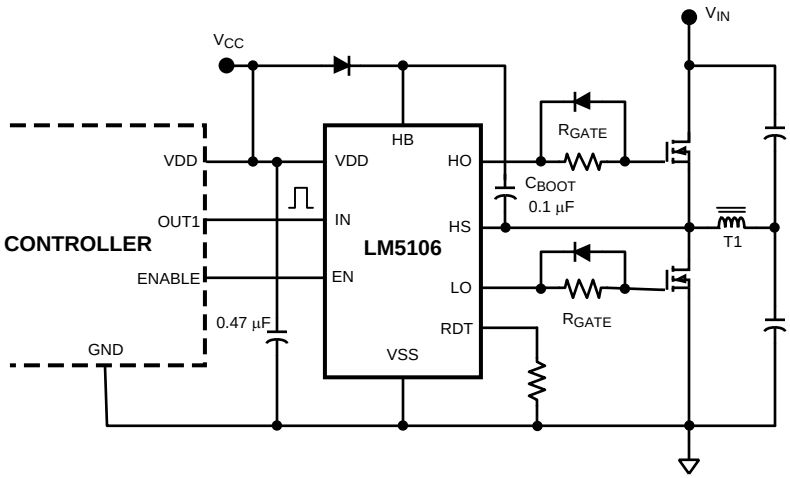


Figure 17. LM5106 Driving MOSFETs Connected in Half-Bridge Configuration

Typical Application (continued)

8.2.1 Design Requirements

PARAMETERS	VALUES
Gate Drive IC	LM5102
Mosfet	CSD18531Q5A
V_{DD}	10 V
Q_{gmax}	43 nC
F_{sw}	100 kHz
D_{Max}	95%
I_{HBO}	10 µA
V_{DH}	1.1 V
V_{HBR}	7.3 V
V_{HBH}	0.4 V

8.2.2 Detailed Design Procedure

8.2.2.1 Detailed Design Procedure

$\Delta V_{HB} = V_{DD} - V_{DH} - V_{HBL}$

where

- V_{DD} = Supply voltage of the gate drive IC
- V_{DH} = Bootstrap diode forward voltage drop
- V_{gsmin} = Minimum gate source threshold voltage (1)

$$C_{BOOT} = \frac{Q_{TOTAL}}{\Delta V_{HB}} \quad (2)$$

$$Q_{TOTAL} = Q_{gmax} + I_{HBO} \times \frac{D_{Max}}{F_{SW}} \quad (3)$$

The quiescent current of the bootstrap circuit is 10 µA which is negligible compared to the Qgs of the MOSFET.

$$Q_{TOTAL} = 43nC + 10\mu A \times \frac{0.95}{100kHz} \quad (4)$$

Q_{TOTAL} = 43.01 nC (5)

In practice the value for the C_{BOOT} capacitor should be greater than that calculated to allow for situations where the power stage may skip pulse due to load transients. In this circumstance the boot capacitor must maintain the HB pin voltage above the UVLO voltage for the HB circuit.

As a general rule the local V_{DD} bypass capacitor should be 10 times greater than the value of C_{BOOT}.

$V_{HBL} = V_{HBR} - V_{HBH}$ (6)

V_{HBL} = 6.9 V (7)

ΔV_{HB} = 10 V – 1.1 V – 6.9 V (8)

ΔV_{HB} = 2.0 V (9)

C_{BOOT} = 43.01nc / 2 V (10)

C_{BOOT} = 21.5 nF (11)

The bootstrap and bias capacitors should be ceramic types with X7R dielectric. The voltage rating should be twice that of the maximum VDD to allow for loss of capacitance once the devices have a DC bias voltage across them and to ensure long-term reliability of the devices.

The resistor values, RT, for setting turnon delay can be found in Figure 19.

8.2.3 Application Curves

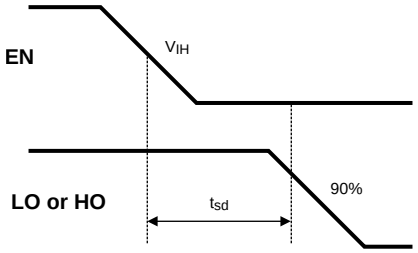


Figure 18. LM5106 Enable: t_{sd}

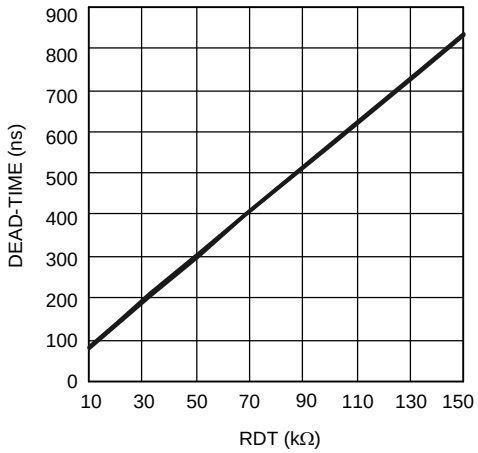


Figure 19. Dead-Time vs RT Resistor Value

9 Power Supply Recommendations

9.1 Power Dissipation Considerations

The total IC power dissipation is the sum of the gate driver losses and the bootstrap diode losses. The gate driver losses are related to the switching frequency (f), output load capacitance on LO and HO (C_L), and supply voltage (V_{DD}) and can be roughly calculated as:

$$P_{DGATES} = 2 \bullet f \bullet C_L \bullet V_{DD}^2 \quad (12)$$

There are some additional losses in the gate drivers due to the internal CMOS stages used to buffer the LO and HO outputs. Figure 20 shows the measured gate driver power dissipation versus frequency and load capacitance. At higher frequencies and load capacitance values, the power dissipation is dominated by the power losses driving the output loads and agrees well with the Equation 12. This plot can be used to approximate the power losses due to the gate drivers.

Power Dissipation Considerations (continued)

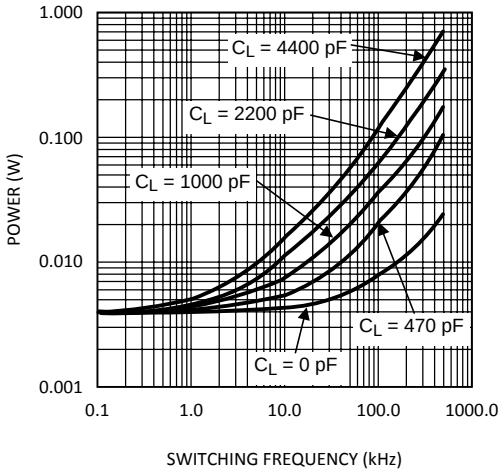


Figure 20. Gate Driver Power Dissipation (LO + HO)
V_{CC} = 12 V

10 Layout

10.1 Layout Guidelines

The optimum performance of high- and low-side gate drivers cannot be achieved without taking due considerations during circuit board layout. The following points are emphasized:

1. Low ESR / ESL capacitors must be connected close to the IC between VDD and VSS pins and between HB and HS pins to support high peak currents being drawn from VDD and HB during the turnon of the external MOSFETs.
2. To prevent large voltage transients at the drain of the top MOSFET, a low ESR electrolytic capacitor and a good quality ceramic capacitor must be connected between the MOSFET drain and ground (VSS).
3. To avoid large negative transients on the switch node (HS) pin, the parasitic inductances between the source of the top MOSFET and the drain of the bottom MOSFET (synchronous rectifier) must be minimized.
4. Grounding considerations:
   – The first priority in designing grounding connections is to confine the high peak currents that charge and discharge the MOSFET gates to a minimal physical area. This will decrease the loop inductance and minimize noise issues on the gate terminals of the MOSFETs. The gate driver should be placed as close as possible to the MOSFETs.
   – The second consideration is the high current path that includes the bootstrap capacitor, the bootstrap diode, the local ground referenced bypass capacitor, and the low-side MOSFET body diode. The bootstrap capacitor is recharged on a cycle-by-cycle basis through the bootstrap diode from the ground referenced VDD bypass capacitor. The recharging occurs in a short time interval and involves high peak current. Minimizing this loop length and area on the circuit board is important to ensure reliable operation.
5. The resistor on the RDT pin must be placed very close to the IC and separated from the high current paths to avoid noise coupling to the time delay generator which could disrupt timer operation.

10.1.1 HS Transient Voltages Below Ground

The HS node will always be clamped by the body diode of the lower external FET. In some situations, board resistances and inductances can cause the HS node to transiently swing several volts below ground. The HS node can swing below ground provided:

1. HS must always be at a lower potential than HO. Pulling HO more than –0.3 V below HS can activate parasitic transistors resulting in excessive current flow from the HB supply, possibly resulting in damage to the IC. The same relationship is true with LO and VSS. If necessary, a Schottky diode can be placed

Layout Guidelines (continued)

externally between HO and HS or LO and GND to protect the IC from this type of transient. The diode must be placed as close to the IC pins as possible in order to be effective.

2. HB to HS operating voltage should be 15 V or less. Hence, if the HS pin transient voltage is –5 V, VDD should be ideally limited to 10V to keep HB to HS below 15 V.
3. Low ESR bypass capacitors from HB to HS and from VCC to VSS are essential for proper operation. The capacitor should be located at the leads of the IC to minimize series inductance. The peak currents from LO and HO can be quite large. Any inductances in series with the bypass capacitor will cause voltage ringing at the leads of the IC which must be avoided for reliable operation.

10.2 Layout Example

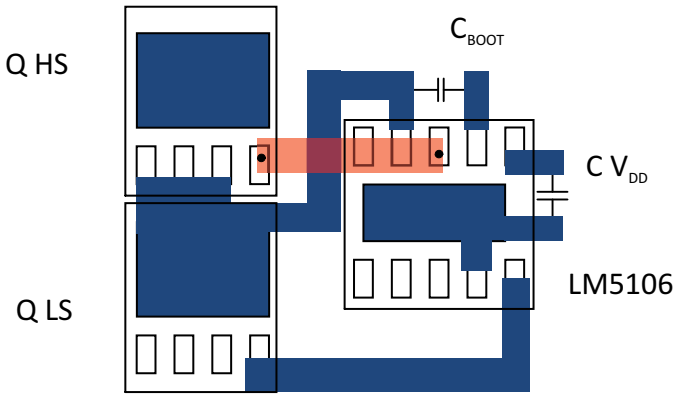


Figure 21. LM5106 Component Placement

11 Device and Documentation Support

11.1 Trademarks

All trademarks are the property of their respective owners.

11.2 Electrostatic Discharge Caution

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

11.3 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
LM5106MM/NOPB	ACTIVE	VSSOP	DGS	10	1000	Green (RoHS & no Sb/Br)	SN	Level-1-260C-UNLIM	-40 to 125	5106	Samples
LM5106MMX/NOPB	ACTIVE	VSSOP	DGS	10	3500	Green (RoHS & no Sb/Br)	SN	Level-1-260C-UNLIM	-40 to 125	5106	Samples
LM5106SD/NOPB	ACTIVE	WSON	DPR	10	1000	Green (RoHS & no Sb/Br)	NIPDAU | SN	Level-1-260C-UNLIM	-40 to 125	L5106SD	Samples
LM5106SDX/NOPB	ACTIVE	WSON	DPR	10	4500	Green (RoHS & no Sb/Br)	NIPDAU | SN	Level-1-260C-UNLIM	-40 to 125	L5106SD	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals.
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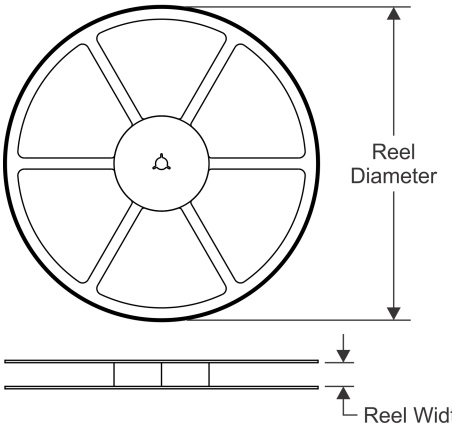
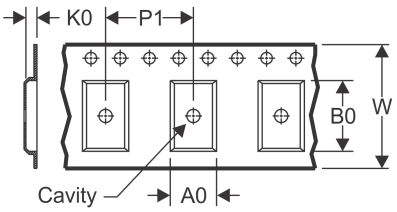
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

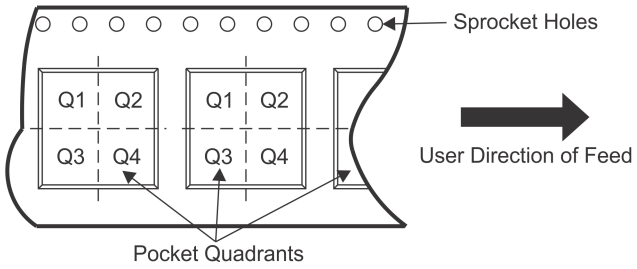


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

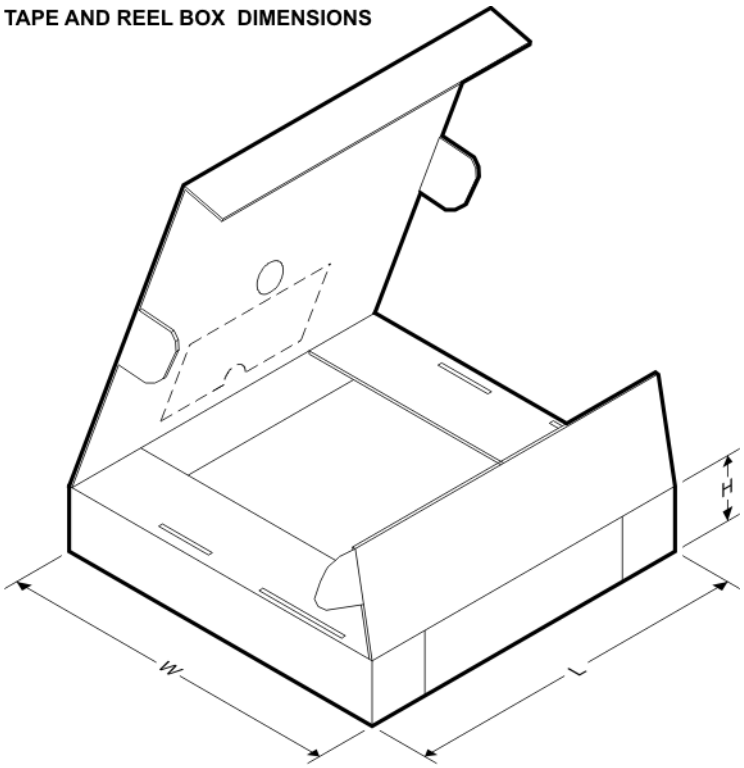
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
LM5106MM/NOPB	VSSOP	DGS	10	1000	178.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
LM5106MMX/NOPB	VSSOP	DGS	10	3500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
LM5106SD/NOPB	WSON	DPR	10	1000	180.0	12.4	4.3	4.3	1.1	8.0	12.0	Q1
LM5106SDX/NOPB	WSON	DPR	10	4500	330.0	12.4	4.3	4.3	1.3	8.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

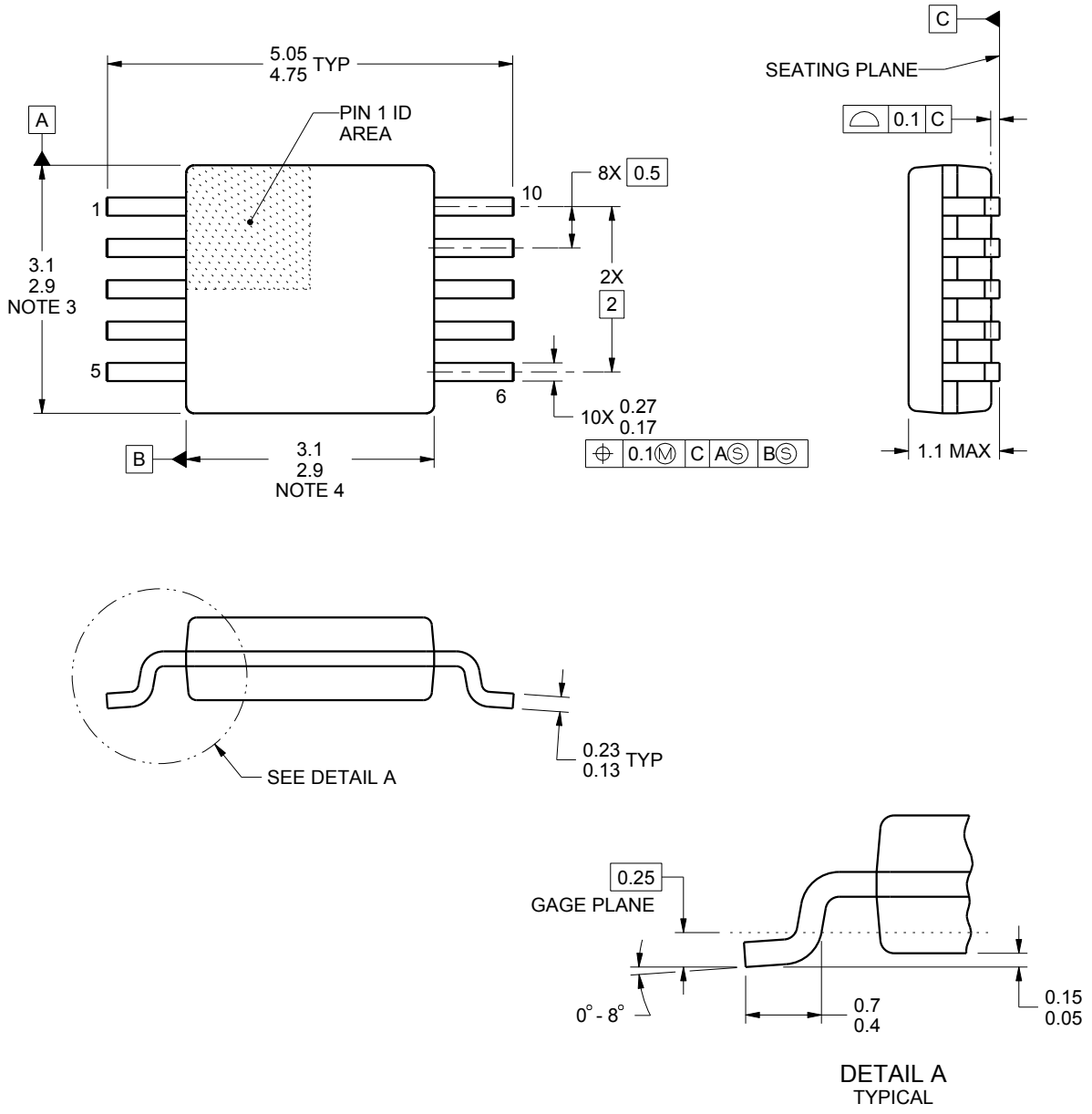
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
LM5106MM/NOPB	VSSOP	DGS	10	1000	210.0	185.0	35.0
LM5106MMX/NOPB	VSSOP	DGS	10	3500	367.0	367.0	35.0
LM5106SD/NOPB	WSON	DPR	10	1000	203.0	203.0	35.0
LM5106SDX/NOPB	WSON	DPR	10	4500	367.0	367.0	35.0

PACKAGE OUTLINE

DGS0010A

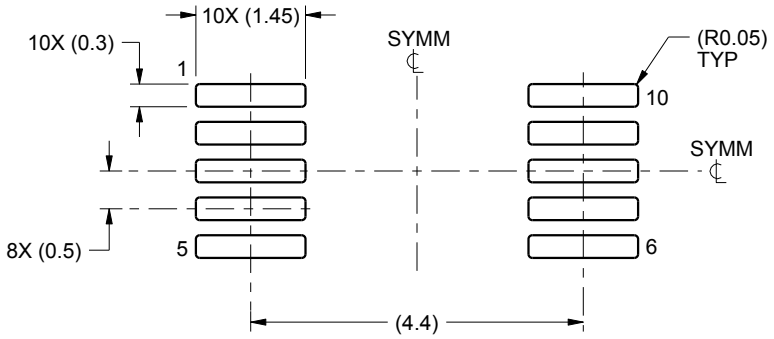
VSSOP - 1.1 mm max height

SMALL OUTLINE PACKAGE

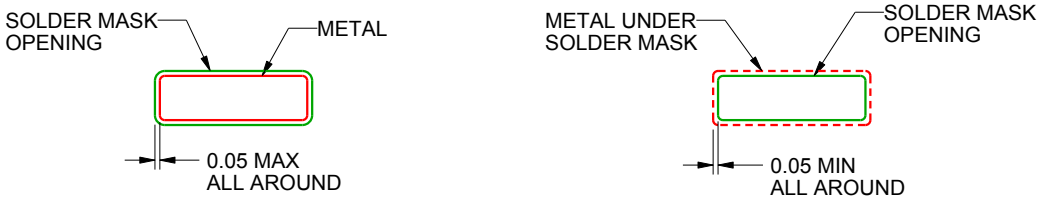


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-187, variation BA.



LAND PATTERN EXAMPLE
SCALE:10X

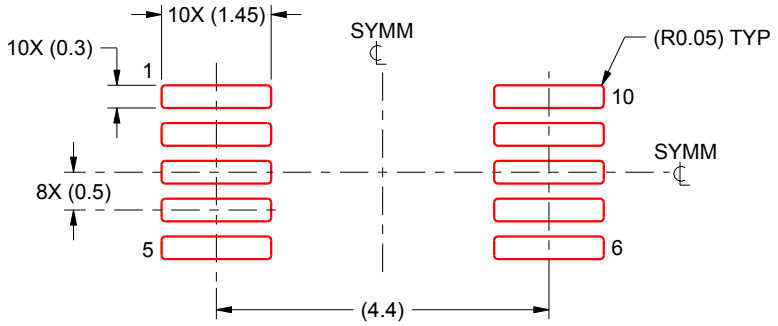


SOLDER MASK DETAILS
NOT TO SCALE

4221984/A 05/2015

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:10X

4221984/A 05/2015

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

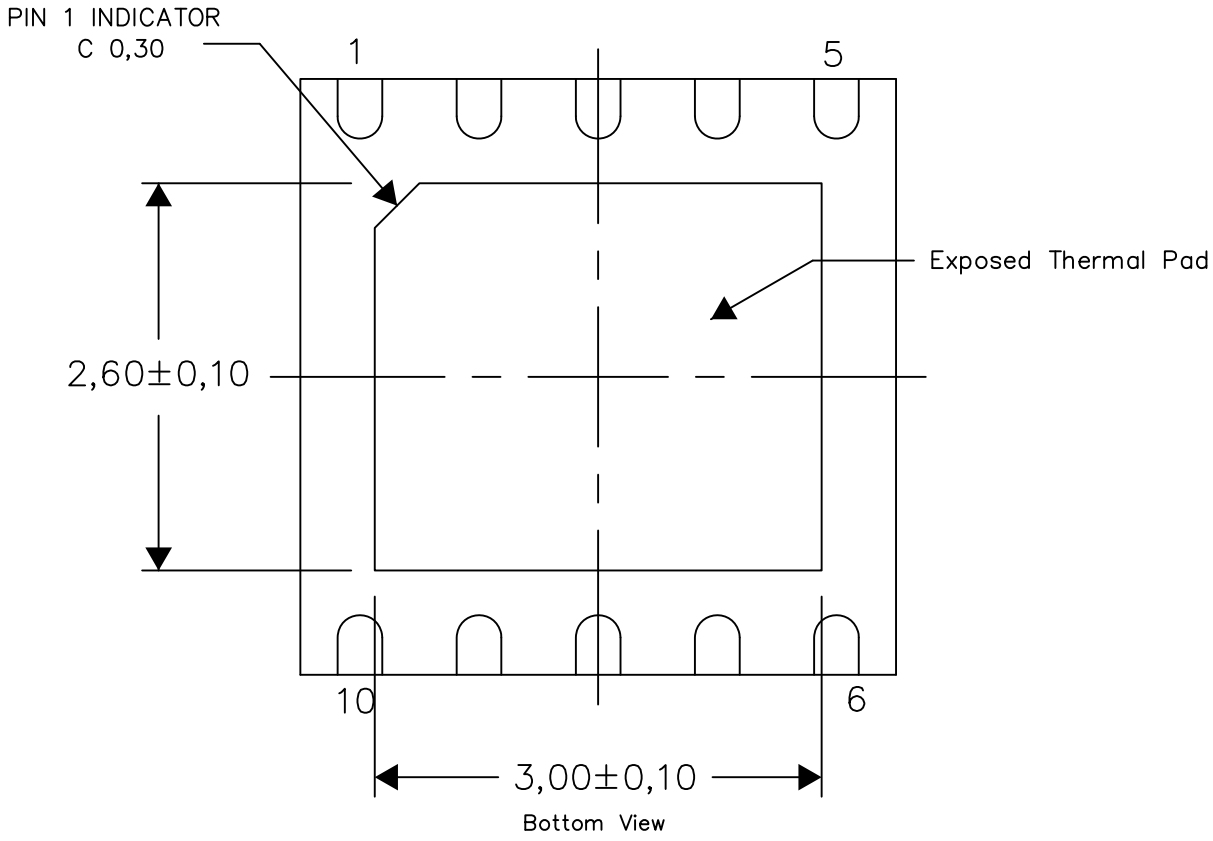
DPR (S–PWSON–N10) PLASTIC SMALL OUTLINE NO–LEAD

THERMAL INFORMATION

This package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. The thermal pad must be soldered directly to the printed circuit board (PCB). After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For information on the Quad Flatpack No–Lead (QFN) package and its advantages, refer to Application Report, QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271. This document is available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.

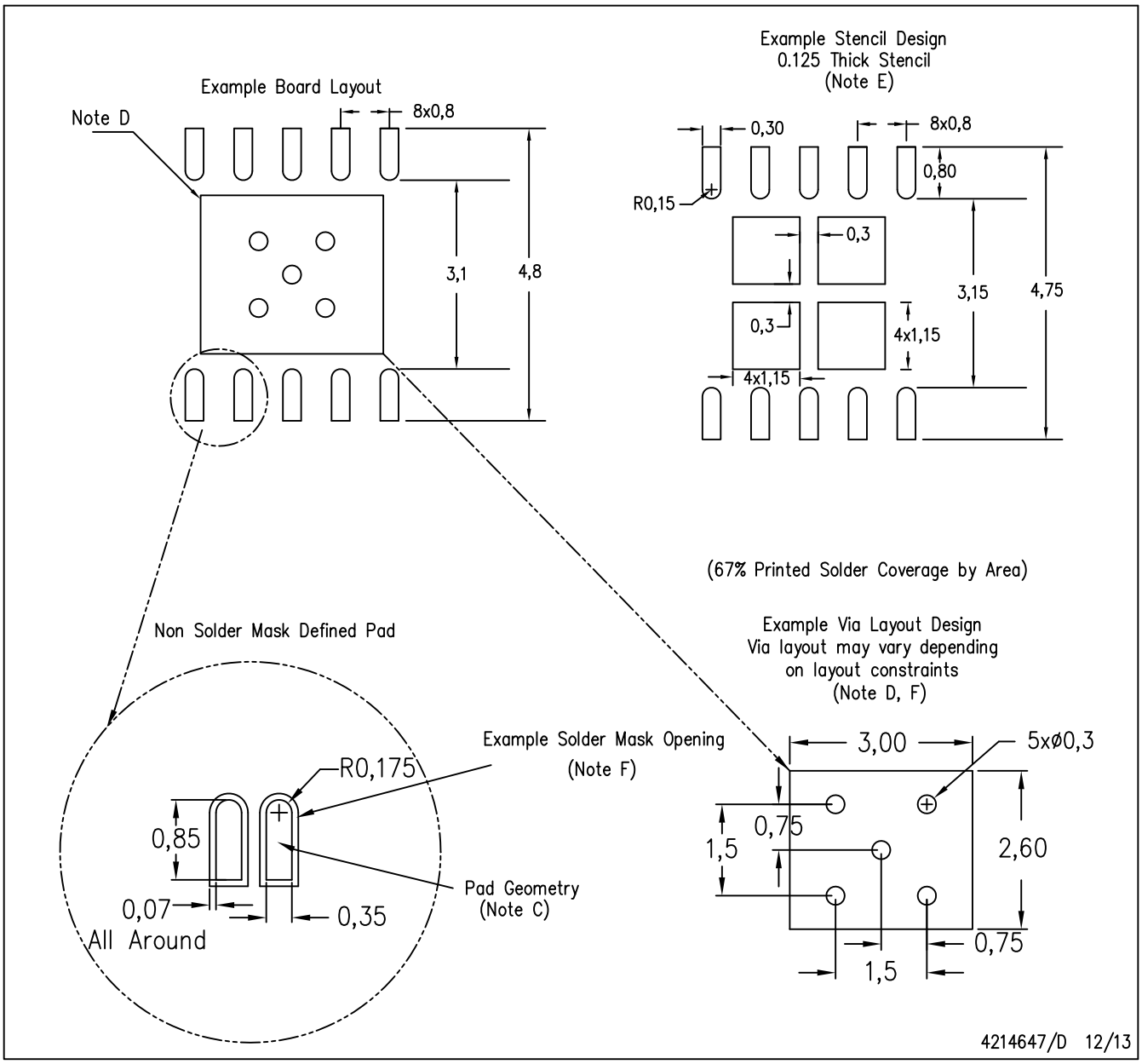


Exposed Thermal Pad Dimensions

4211551/C 12/13

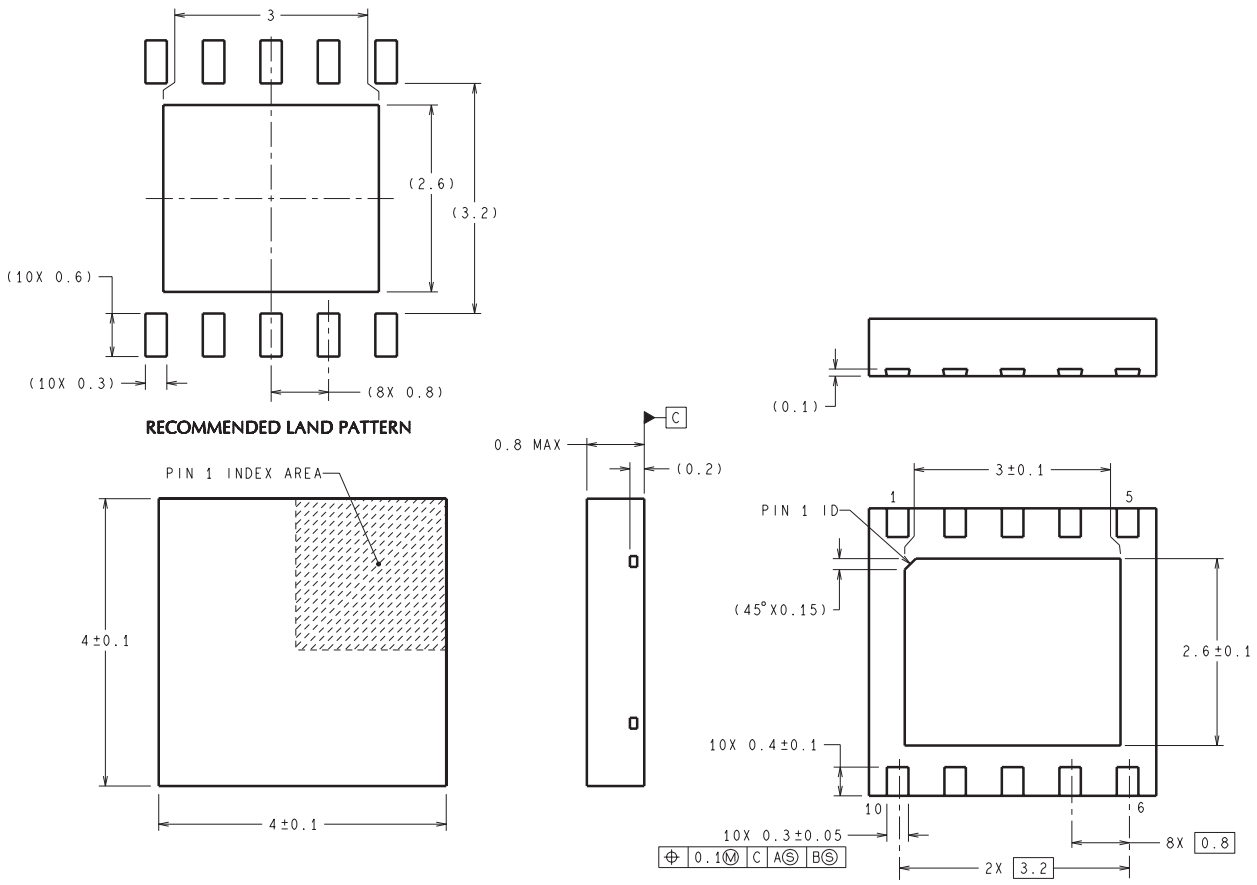
NOTES: All linear dimensions are in millimeters

DPR (S–PWSON–N10) PLASTIC SMALL OUTLINE NO–LEAD



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. This package is designed to be soldered to a thermal pad on the board. Refer to Application Note, Quad Flat–Pack Packages, Texas Instruments Literature No. SLUA271, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com <http://www.ti.com>.
E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
F. Customers should contact their board fabrication site for recommended solder mask tolerances and via tenting recommendations for vias placed in the thermal pad.

DPR0010A



DIMENSIONS ARE IN MILLIMETERS

SDC10A (Rev A)

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