LM5105 100V Half Bridge Gate Driver With Programmable Dead-Time

1 Features

- Drives Both a High Side and Low Side N-Channel MOSFET
- 1.8A Peak Gate Drive Current
- Bootstrap Supply Voltage Range up to 118V DC
- Integrated Bootstrap Diode
- Single TTL Compatible Input
- Programmable Turn-On Delays (Dead-Time)
- Enable Input Pin
- Fast Turn-Off Propagation Delays (26ns Typical)
- Drives 1000pF with 15ns Rise and Fall Time
- Supply Rail Under-Voltage Lockout
- Low Power Consumption
- Package: WSON-10 (4 mm x 4 mm)

2 Applications

- Solid State motor drives
- Half and Full Bridge power converters

3 Description

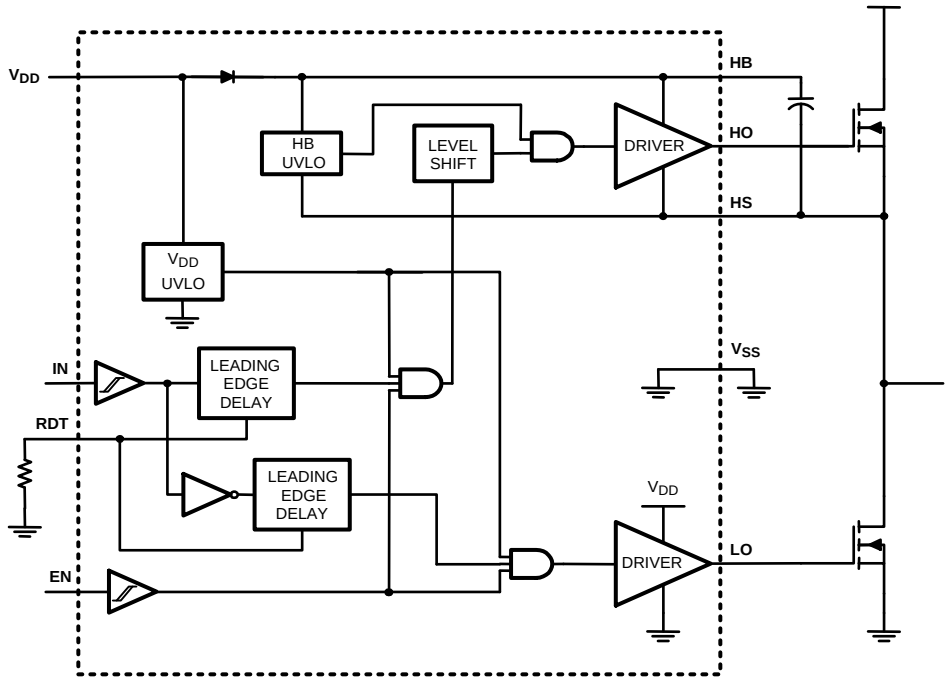
The LM5105 is a high voltage gate driver designed to drive both the high side and low side N–Channel MOSFETs in a synchronous buck or half bridge configuration. The floating high-side driver is capable of working with rail voltages up to 100V. The single control input is compatible with TTL signal levels and a single external resistor programs the switching transition dead-time through tightly matched turn-on delay circuits. A high voltage diode is provided to charge the high side gate drive bootstrap capacitor. The robust level shift technology operates at high speed while consuming low power and provides clean output transitions. Under-voltage lockout disables the gate driver when either the low side or the bootstrapped high side supply voltage is below the operating threshold. The LM5105 is offered in the thermally enhanced WSON plastic package.

Device Information(1)

PART NUMBER	PACKAGE	BODY SIZE (NOM)
LM5105	WSON (10)	4.00 mm × 4.00 mm

(1) For all available packages, see the orderable addendum at the end of the datasheet.

Simplified Application Diagram



An IMPORTANT NOTICE at the end of this data sheet addresses availability, warranty, changes, use in safety-critical applications, intellectual property matters and other important disclaimers. PRODUCTION DATA.

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4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision C (March 2013) to Revision D	Page
• Added *Device Information* table, *ESD Ratings*, *Detailed Description* section, *Application and Implementation* section, *Layout* section, *Device and Documentation Support* section, and *Mechanical, Packaging, and Orderable Information* section.	1

Changes from Revision B (March 2013) to Revision C	Page
• Changed layout of National Data Sheet to TI format	12

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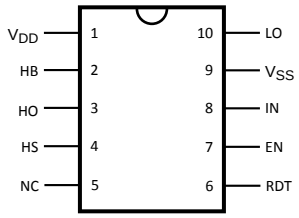
5 Pin Configuration and Functions

10-Lead WSON



Pin Functions

PIN		DESCRIPTION
NAME	NO.	
V_{DD}	1	Positive gate drive supply.Decouple VDD to VSS using a low ESR/ESL capacitor, placed as close to the IC as possible.
HB	2	High-side gate driver bootstrap rail. Connect the positive terminal of bootstrap capacitor to the HB pin and connect negative terminal to HS. The Bootstrap capacitor should be placed as close to IC as possible.
HO	3	High-side gate driver output. Connect to the gate of high side N-MOS device through a short, low inductance path.
HS	4	High-side MOSFET source connection. Connect to the negative terminal of the bootststrap capacitor and to the source of the high side N-MOS device.
NC	5	Not connected.
RDT	6	Dead-time programming pin. A resistor from RDT to VSS programs the turn-on delay of both the high and low side MOSFETs. The resistor should be placed close to the IC to minimize noise coupling from adjacent PC board traces.
EN	7	Logic input for driver disable or enable. TTL compatible threshold with hysteresis. LO and HO are held in the low state when EN is low.
IN	8	Logic input for gate driver. TTL compatible threshold with hysteresis. The high side MOSFET is turned on and the low side MOSFET turned off when IN is high.
V_{SS}	9	Ground return. All signals are referenced to this ground.
LO	10	Low-side gate driver output. Connect to the gate of the low side N-MOS device with a short, low inductance path.
Exposed Pad	It is recommended that the exposed pad on the bottom of the package be soldered to ground plane on the PC board to aid thermal dissipation.	

6 Specifications

6.1 Absolute Maximum Ratings

See [1][2]

V_{DD} to V_{SS}	–0.3V to +18V
HB to HS	–0.3V to +18V
IN and EN to V_{SS}	–0.3V to V_{DD} + 0.3V
LO to V_{SS}	–0.3V to V_{DD} + 0.3V
HO to V_{SS}	HS – 0.3V to HB + 0.3V
HS to V_{SS} [3]	−5V to +100V
HB to V_{SS}	118V
RDT to V_{SS}	–0.3V to 5V
Junction Temperature	+150°C
Storage Temperature Range	–55°C to +150°C

(1) Absolute Maximum Ratings indicate limits beyond which damage to the component may occur. Operating Ratings are conditions under which operation of the device is specified. Operating Ratings do not imply performance limits. For performance limits and associated test conditions, see the Electrical Characteristics.
(2) If Military/Aerospace specified devices are required, please contact the Texas Instruments Sales Office/Distributors for availability and specifications.
(3) In the application the HS node is clamped by the body diode of the external lower N-MOSFET, therefore the HS voltage will generally not exceed -1V. However in some applications, board resistance and inductance may result in the HS node exceeding this stated voltage transiently. If negative transients occur on HS, the HS voltage must never be more negative than V_{DD} - 15V. For example, if V_{DD} = 10V, the negative transients at HS must not exceed -5V.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM) [1]	±2000	V

(1) The human body model is a 100 pF capacitor discharged through a 1.5kΩ resistor into each pin. Pin 2, Pin 3 and Pin 4 are rated at 500V.

6.3 Recommended Operating Conditions

V_{DD}	+8V to +14V
HS [1]	–1V to 100V
HB	HS + 8V to HS + 14V
HS Slew Rate	<50V/ns
Junction Temperature	–40°C to +125°C

(1) In the application the HS node is clamped by the body diode of the external lower N-MOSFET, therefore the HS voltage will generally not exceed -1V. However in some applications, board resistance and inductance may result in the HS node exceeding this stated voltage transiently. If negative transients occur on HS, the HS voltage must never be more negative than V_{DD} - 15V. For example, if V_{DD} = 10V, the negative transients at HS must not exceed -5V.

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6.4 Electrical Characteristics

Specifications in standard typeface are for T_J = +25°C, and those in **boldface type** apply over the full **operating junction temperature range**. Unless otherwise specified, V_{DD} = HB = 12V, V_{SS} = HS = 0V, EN = 5V. No load on LO or HO. RDT= 100kΩ(1).

Symbol	Parameter	Conditions	Min	Typ	Max	Units
SUPPLY CURRENTS						
I_{DD}	V_{DD} Quiescent Current	IN = EN = 0V		0.34	**0.6**	mA
I_{DDO}	V_{DD} Operating Current	f = 500 kHz		1.65	**3**	mA
I_{HB}	Total HB Quiescent Current	IN = EN = 0V		0.06	**0.2**	mA
I_{HBO}	Total HB Operating Current	f = 500 kHz		1.3	**3**	mA
I_{HBS}	HB to V_{SS} Current, Quiescent	HS = HB = 100V		0.05	**10**	µA
I_{HBSO}	HB to V_{SS} Current, Operating	f = 500 kHz		0.1		mA
INPUT IN and EN						
V_{IL}	Low Level Input Voltage Threshold		**0.8**	1.8		V
V_{IH}	High Level Input Voltage Threshold			1.8	**2.2**	V
R_{pd}	Input Pulldown Resistance Pin IN and EN		**100**	200	**500**	kΩ
DEAD-TIME CONTROLS						
VRDT	Nominal Voltage at RDT		**2.7**	3	**3.3**	V
IRDT	RDT Pin Current Limit	RDT = 0V	**0.75**	1.5	**2.25**	mA
UNDER VOLTAGE PROTECTION						
V_{DDR}	V_{DD} Rising Threshold		**6.0**	6.9	**7.4**	V
V_{DDH}	V_{DD} Threshold Hysteresis			0.5		V
V_{HBR}	HB Rising Threshold		**5.7**	6.6	**7.1**	V
V_{HBH}	HB Threshold Hysteresis			0.4		V
BOOT STRAP DIODE						
V_{DL}	Low-Current Forward Voltage	I_{VDD-HB} = 100 µA		0.6	**0.9**	V
V_{DH}	High-Current Forward Voltage	I_{VDD-HB} = 100 mA		0.85	**1.1**	V
R_D	Dynamic Resistance	I_{VDD-HB} = 100 mA		0.8	**1.5**	Ω
LO GATE DRIVER						
V_{OLL}	Low-Level Output Voltage	I_{LO} = 100 mA		0.25	**0.4**	V
V_{OHL}	High-Level Output Voltage	I_{LO} = –100 mA, $V_{OHL} = V_{DD} – V_{LO}$		0.35	**0.55**	V
I_{OHL}	Peak Pullup Current	LO = 0V		1.8		A
I_{OLL}	Peak Pulldown Current	LO = 12V		1.6		A
HO GATE DRIVER						
V_{OLH}	Low-Level Output Voltage	I_{HO} = 100 mA		0.25	**0.4**	V
V_{OHH}	High-Level Output Voltage	I_{HO} = –100 mA, V_{OHH} = HB – HO		0.35	**0.55**	V
I_{OHH}	Peak Pullup Current	HO = 0V		1.8		A
I_{OLH}	Peak Pulldown Current	HO = 12V		1.6		A
THERMAL RESISTANCE						
θ_{JA}	Junction to Ambient	See(2)(3)		40		°C/W

(1) Min and Max limits are 100% production tested at 25°C. Limits over the operating temperature range are specified through correlation using Statistical Quality Control (SQC) methods. Limits are used to calculate Average Outgoing Quality Level (AOQL).
(2) 4 layer board with Cu finished thickness 1.5/1.0/1.0/1.5 oz. Maximum die size used. 5x body length of Cu trace on PCB top. 50 x 50mm ground and power planes embedded in PCB. See Application Note AN-1187.
(3) The θ_{JA} is not a constant for the package and depends on the printed circuit board design and the operating conditions.

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6.5 Switching Characteristics

Specifications in standard typeface are for T_J = +25°C, and those in **boldface type** apply over the full **operating junction temperature range**. Unless otherwise specified, V_{DD} = HB = 12V, V_{SS} = HS = 0V, No Load on LO or HO(1).

Symbol	Parameter	Conditions	Min	Typ	Max	Units
t_{LPHL}	Lower Turn-Off Propagation Delay			26	**56**	ns
t_{HPHL}	Upper Turn-Off Propagation Delay			26	**56**	ns
t_{LPLH}	Lower Turn-On Propagation Delay	RDT = 100k	**485**	595	**705**	ns
t_{HPLH}	Upper Turn-On Propagation Delay	RDT = 100k	**485**	595	**705**	ns
t_{LPLH}	Lower Turn-On Propagation Delay	RDT = 10k	**75**	105	**150**	ns
t_{HPLH}	Upper Turn-On Propagation Delay	RDT = 10k	**75**	105	**150**	ns
t_{en}, t_{sd}	Enable and Shutdown propagation delay			28		ns
DT1, DT2	Dead-Time LO OFF to HO ON & HO OFF to LO ON	RDT = 100k		570		ns
		RDT = 10k		80		ns
MDT	Dead-Time Matching	RDT = 100k		50		ns
t_R, t_F	Either Output Rise/Fall Time	C_L = 1000pF		15		ns
t_{BS}	Bootstrap Diode Turn-On or Turn-Off Time	I_F = 20 mA, I_R = 200 mA		50		ns

(1) Min and Max limits are 100% production tested at 25°C. Limits over the operating temperature range are specified through correlation using Statistical Quality Control (SQC) methods. Limits are used to calculate Average Outgoing Quality Level (AOQL).

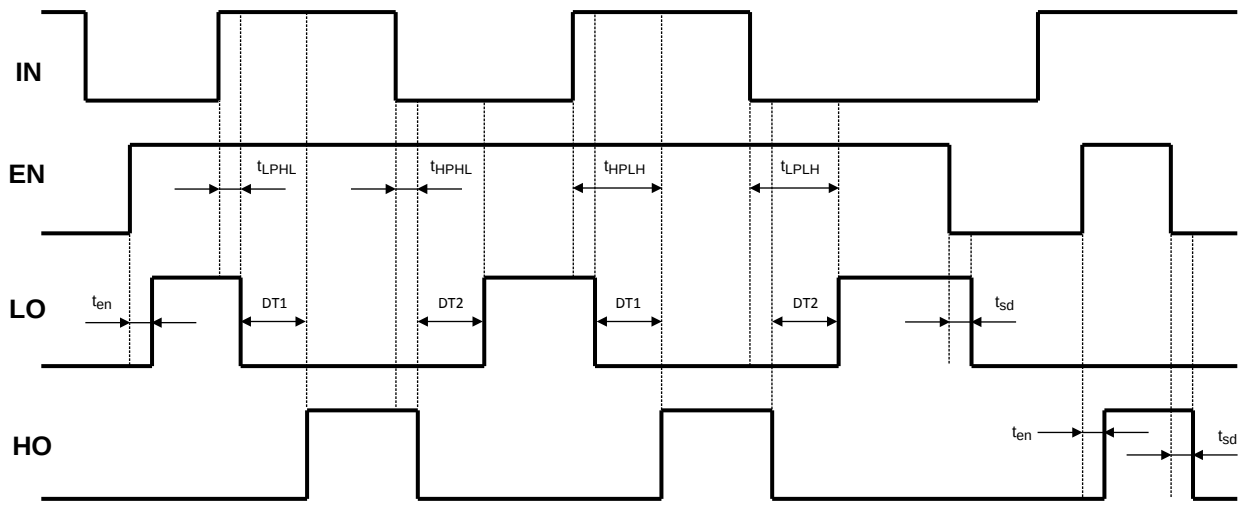

Figure 1. LM5105 Input - Output Waveforms

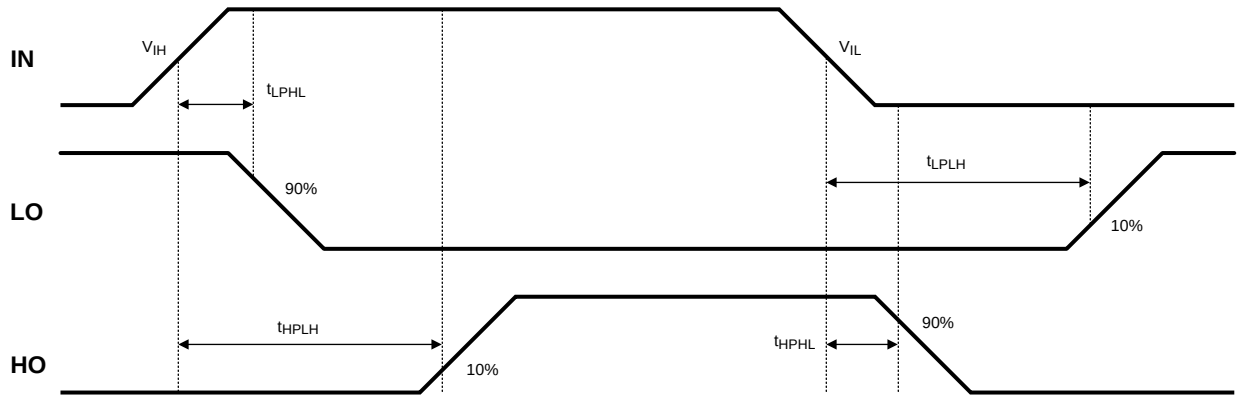

Figure 2. LM5105 Switching Time Definitions: T_{LPLH}, T_{LPHL}, T_{HPLH}, T_{HPHL}

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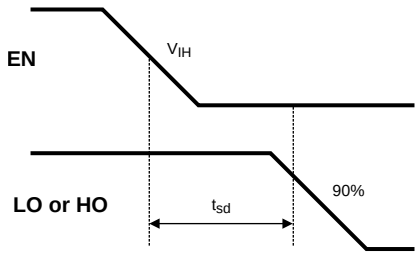

Figure 3. LM5105 Enable: T_{sd}

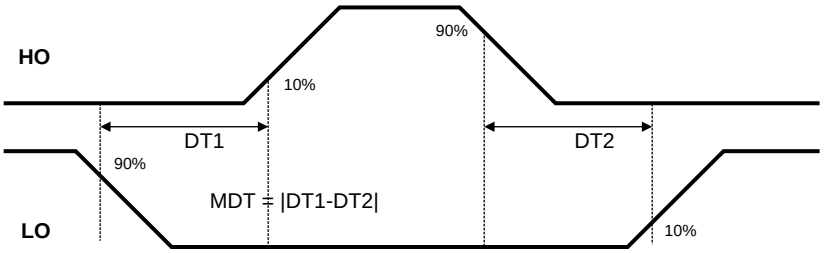

Figure 4. LM5105 Dead-Time: DT

6.6 Typical Performance Characteristics

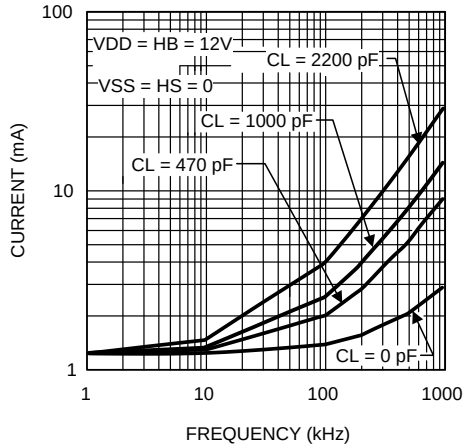

Figure 5. V_{DD} Operating Current vs Frequency

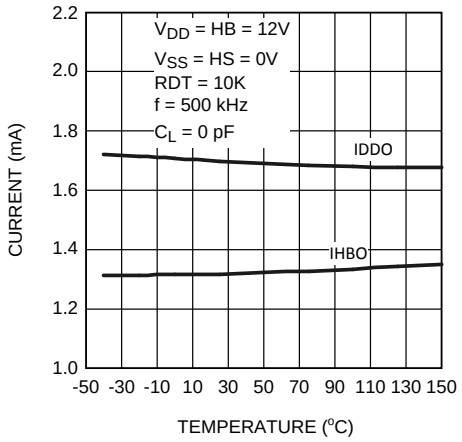

Figure 6. Operating Current vs Temperature

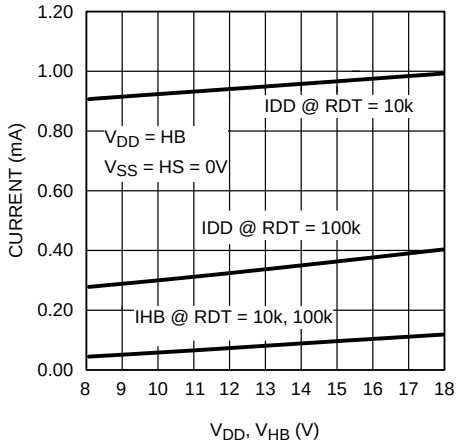

Figure 7. Quiescent Current vs Supply Voltage

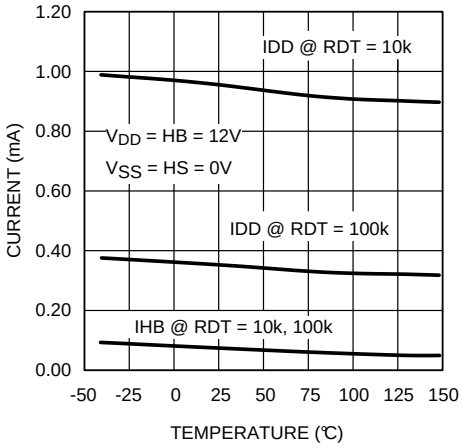

Figure 8. Quiescent Current vs Temperature

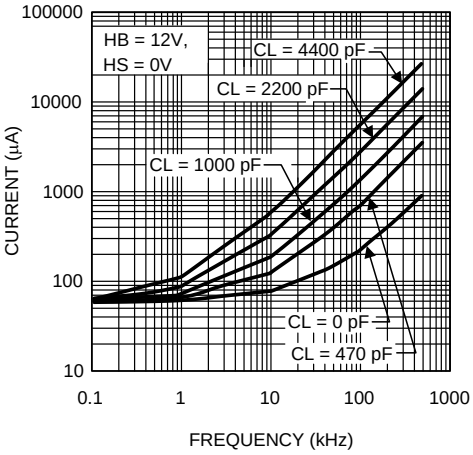

Figure 9. HB Operating Current vs Frequency

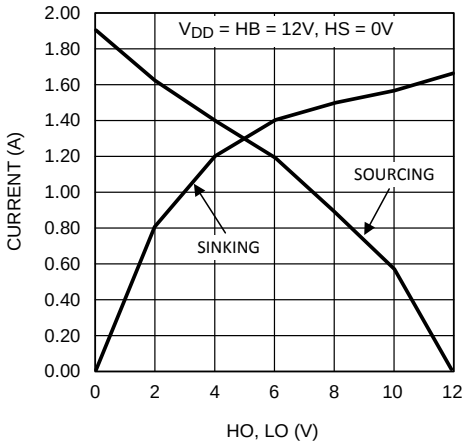

Figure 10. HO & LO Peak Output Current vs Output Voltage

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Typical Performance Characteristics (continued)

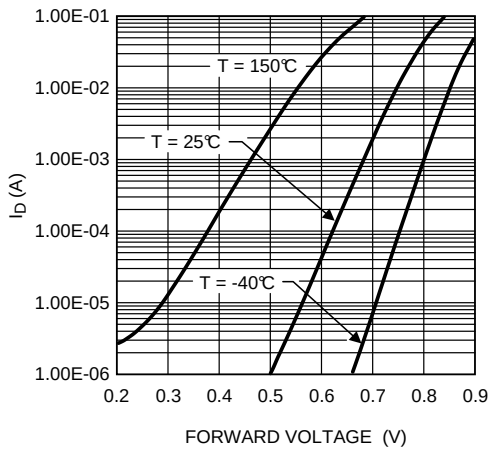

Figure 11. Diode Forward Voltage

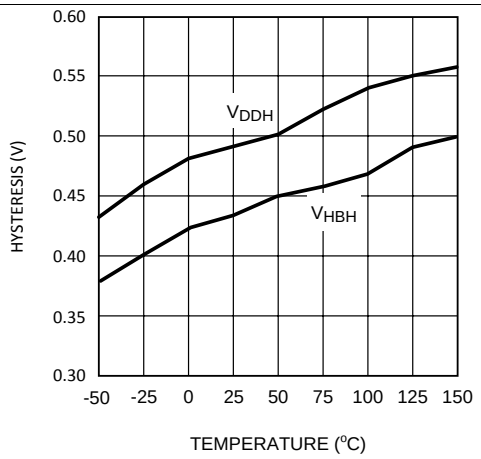

Figure 12. Undervoltage Hysteresis vs Temperature

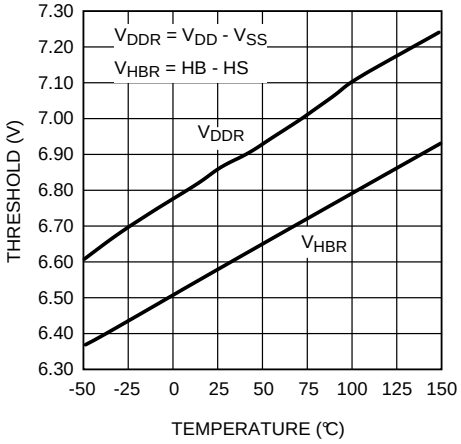

Figure 13. Undervoltage Rising Threshold vs Temperature

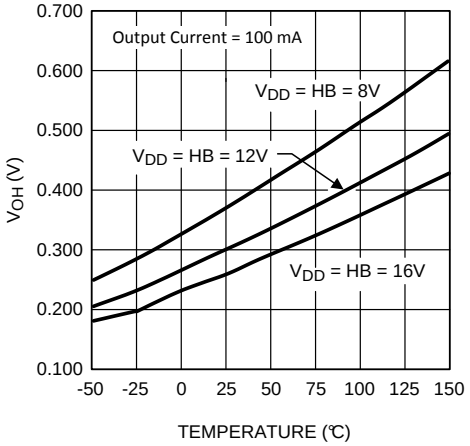

Figure 14. LO & HO - High Level Output Voltage vs Temperature

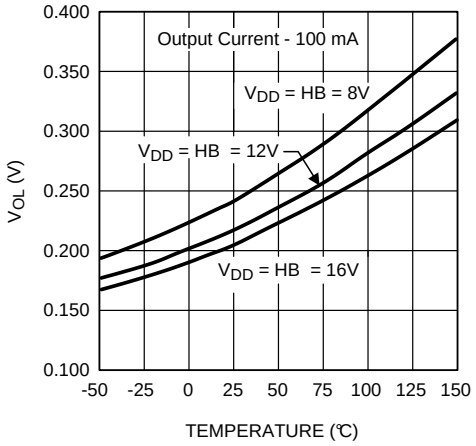

Figure 15. LO & HO - Low Level Output Voltage vs Temperature

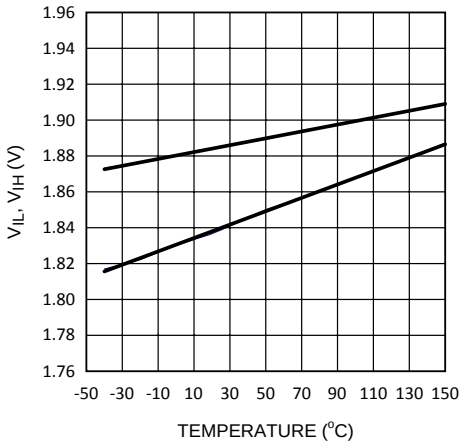

Figure 16. Input Threshold vs Temperature

Typical Performance Characteristics (continued)

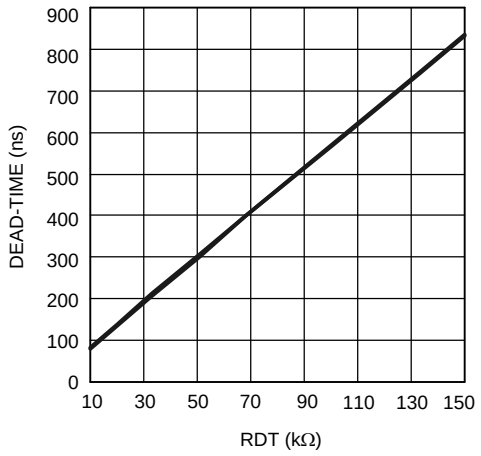

Figure 17. Dead-Time vs RT Resistor Value

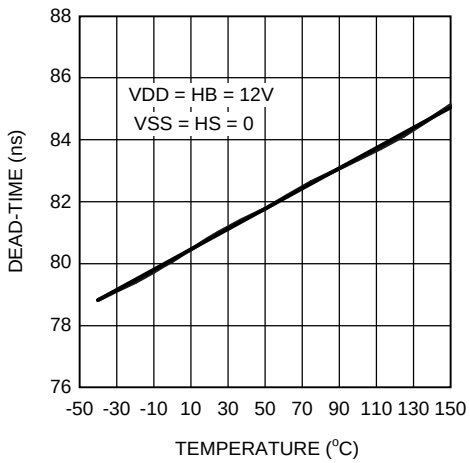

Figure 18. Dead-Time vs Temperature (RT = 10k)

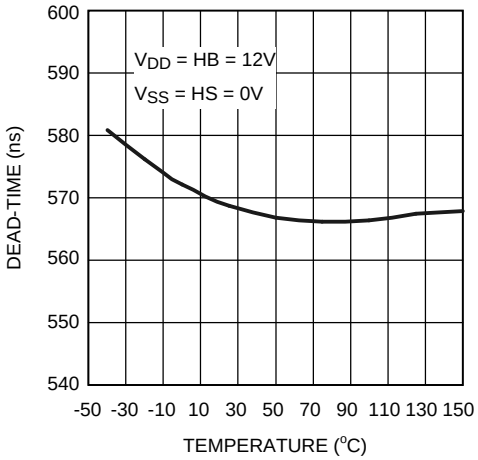

Figure 19. Dead-Time vs Temperature (RT = 100k)

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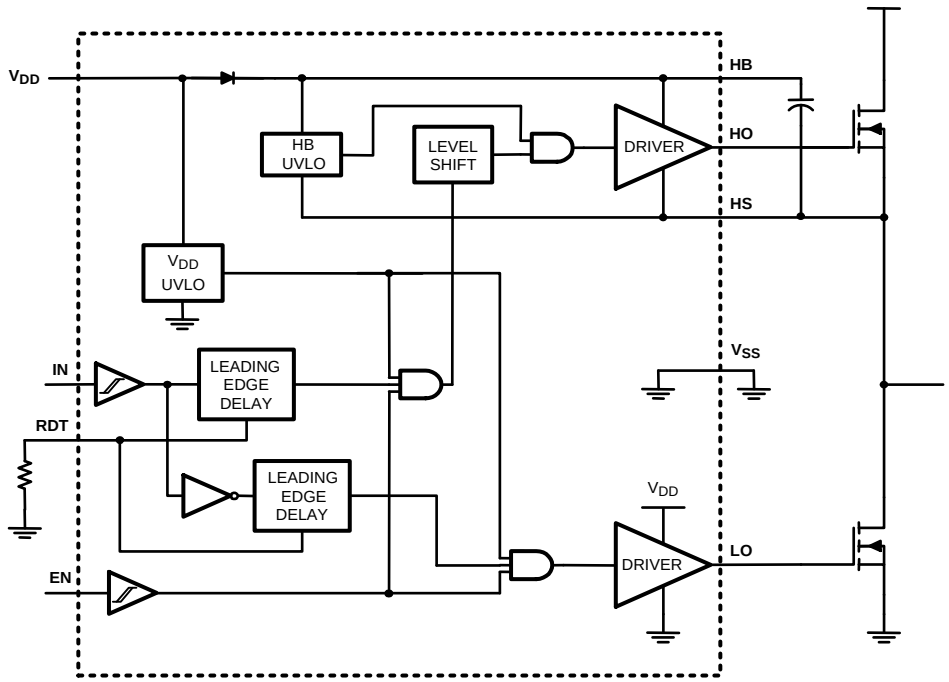
7 Detailed Description

7.1 Overview

The LM5105 is a single PWM input Gate Driver with Enable that offers a programmable dead-time. The dead-time is set with a resistor at the RDT pin and can be adjusted from 100ns to 600ns. The wide dead-time programming range provides the flexibility to optimize drive signal timing for a wide range of MOSFETS and applications.

The RDT pin is biased at 3V and current limited to 1 mA maximum programming current. The time delay generator will accommodate resistor values from 5k to 100k with a dead-time time that is proportional to the RDT resistance. Grounding the RDT pin programs the LM5105 to drive both outputs with minimum dead-time.

7.2 Functional Block Diagram



7.3 Feature Description

7.3.1 Startup and UVLO

Both top and bottom drivers include under-voltage lockout (UVLO) protection circuitry which monitors the supply voltage (V_{DD}) and bootstrap capacitor voltage (HB – HS) independently. The UVLO circuit inhibits each driver until sufficient supply voltage is available to turn-on the external MOSFETs, and the UVLO hysteresis prevents chattering during supply voltage transitions. When the supply voltage is applied to the V_{DD} pin of LM5105, the top and bottom gates are held low until V_{DD} exceeds the UVLO threshold, typically about 6.9V. Any UVLO condition on the bootstrap capacitor will disable only the high side output (HO).

8 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

8.1 Application Information

8.1.1 HS Transient Voltages Below Ground

The HS node will always be clamped by the body diode of the lower external FET. In some situations, board resistances and inductances can cause the HS node to transiently swing several volts below ground. The HS node can swing below ground provided:

1. HS must always be at a lower potential than HO. Pulling HO more than -0.3V below HS can activate parasitic transistors resulting in excessive current to flow from the HB supply possibly resulting in damage to the IC. The same relationship is true with LO and VSS. If necessary, a Schottky diode can be placed externally between HO and HS or LO and GND to protect the IC from this type of transient. The diode must be placed as close to the IC pins as possible in order to be effective.
2. HB to HS operating voltage should be 15V or less . Hence, if the HS pin transient voltage is -5V, VDD should be ideally limited to 10V to keep HB to HS below 15V.
3. A low ESR bypass capacitor between HB to HS as well as VCC to VSS is essential for proper operation. The capacitor should be located at the leads of the IC to minimize series inductance. The peak currents from LO and HO can be quite large. Any series inductances with the bypass capacitor will cause voltage ringing at the leads of the IC which must be avoided for reliable operation.

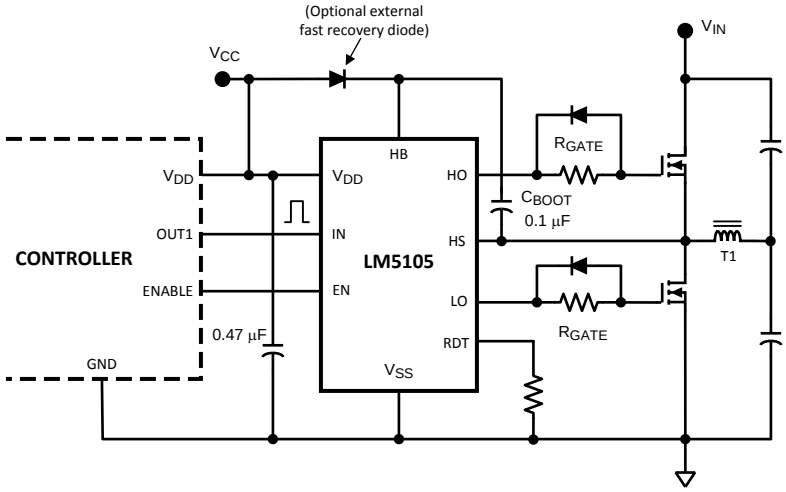


Figure 20. LM5105 Driving MOSFETS Connected In Half-Bridge Configuration

8.1.2 Power Dissipation Considerations

The total IC power dissipation is the sum of the gate driver losses and the bootstrap diode losses. The gate driver losses are related to the switching frequency (f), output load capacitance on LO and HO (C_L), and supply voltage (V_{DD}) and can be roughly calculated as:

$$P_{DGATES} = 2 \cdot f \cdot C_L \cdot V_{DD}^2 \quad (1)$$

There are some additional losses in the gate drivers due to the internal CMOS stages used to buffer the LO and HO outputs. The following plot shows the measured gate driver power dissipation versus frequency and load capacitance. At higher frequencies and load capacitance values, the power dissipation is dominated by the power losses driving the output loads and agrees well with the above equation. This plot can be used to approximate the power losses due to the gate drivers.

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Application Information (continued)

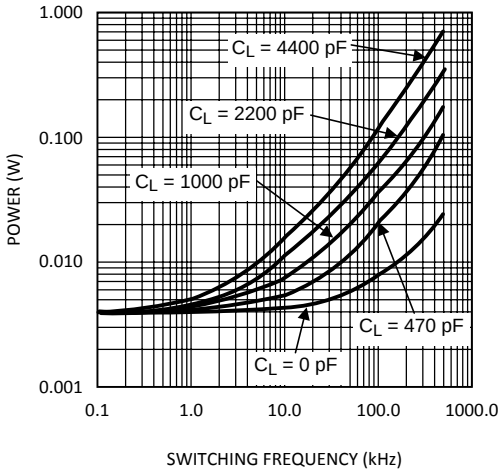

Figure 21. Gate Driver Power Dissipation (Lo + Ho)
V_{CC} = 12v, Neglecting Diode Losses

The bootstrap diode power loss is the sum of the forward bias power loss that occurs while charging the bootstrap capacitor and the reverse bias power loss that occurs during reverse recovery. Since each of these events happens once per cycle, the diode power loss is proportional to frequency. Larger capacitive loads require more current to recharge the bootstrap capacitor resulting in more losses. Higher input voltages (V_{IN}) to the half bridge result in higher reverse recovery losses. The following plot was generated based on calculations and lab measurements of the diode recovery time and current under several operating conditions. This can be useful for approximating the diode power dissipation.

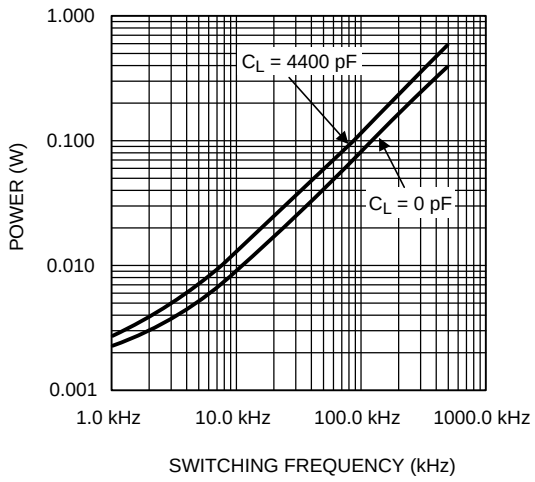

Figure 22. Diode Power Dissipation V_{IN} = 80v

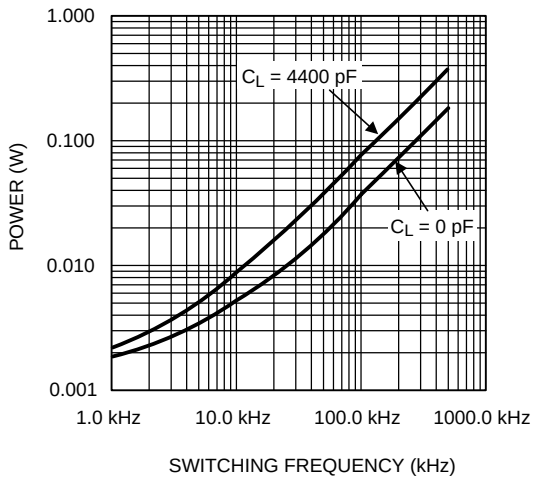

Figure 23. Diode Power Dissipation V_{IN} = 40v

The total IC power dissipation can be estimated from the above plots by summing the gate drive losses with the bootstrap diode losses for the intended application. Because the diode losses can be significant, an external diode placed in parallel with the internal bootstrap diode (refer to Figure 20) and can be helpful in removing power from the IC. For this to be effective, the external diode must be placed close to the IC to minimize series inductance and have a significantly lower forward voltage drop than the internal diode.

9 Layout

9.1 Layout Guidelines

The optimum performance of high and low side gate drivers cannot be achieved without taking due considerations during circuit board layout. Following points are emphasized.

1. A low ESR/ESL capacitor must be connected close to the IC, and between V_{DD} and V_{SS} pins and between HB and HS pins to support high peak currents being drawn from V_{DD} during turn-on of the external MOSFET.
2. To prevent large voltage transients at the drain of the top MOSFET, a low ESR electrolytic capacitor must be connected between MOSFET drain and ground (V_{SS}).
3. In order to avoid large negative transients on the switch node (HS) pin, the parasitic inductances in the source of top MOSFET and in the drain of the bottom MOSFET (synchronous rectifier) must be minimized.
4. Grounding considerations:
   - The first priority in designing grounding connections is to confine the high peak currents from charging and discharging the MOSFET gate in a minimal physical area. This will decrease the loop inductance and minimize noise issues on the gate terminal of the MOSFET. The MOSFETs should be placed as close as possible to the gate driver.
   - The second high current path includes the bootstrap capacitor, the bootstrap diode, the local ground referenced bypass capacitor and low side MOSFET body diode. The bootstrap capacitor is recharged on the cycle-by-cycle basis through the bootstrap diode from the ground referenced V_{DD} bypass capacitor. The recharging occurs in a short time interval and involves high peak current. Minimizing this loop length and area on the circuit board is important to ensure reliable operation.
5. The resistor on the RDT pin must be placed very close to the IC and separated from high current paths to avoid noise coupling to the time delay generator which could disrupt timer operation.

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10 Device and Documentation Support

10.1 Community Resource

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

TI E2E™ Online Community ***TI's Engineer-to-Engineer (E2E) Community.*** Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support ***TI's Design Support*** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

10.2 Trademarks

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10.3 Electrostatic Discharge Caution

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

10.4 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

11 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
LM5105SD/NOPB	ACTIVE	WSON	DPR	10	1000	Green (RoHS & no Sb/Br)	CU NIPDAU | CU SN	Level-1-260C-UNLIM	-40 to 125	L5105SD	Samples
LM5105SDX/NOPB	ACTIVE	WSON	DPR	10	4500	Green (RoHS & no Sb/Br)	CU NIPDAU | CU SN	Level-1-260C-UNLIM	-40 to 125	L5105SD	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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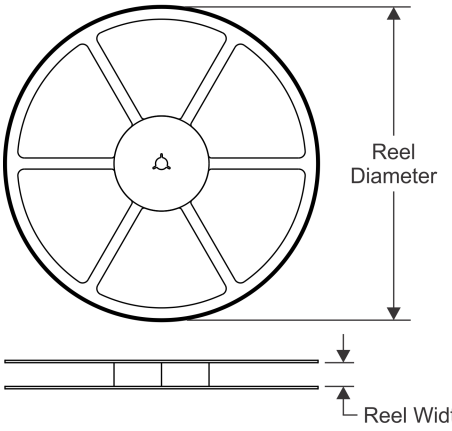
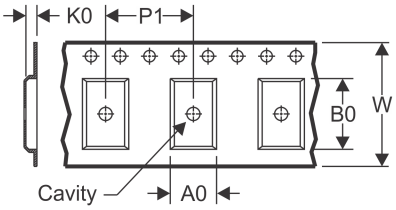
TAPE AND REEL INFORMATION

REEL DIMENSIONS

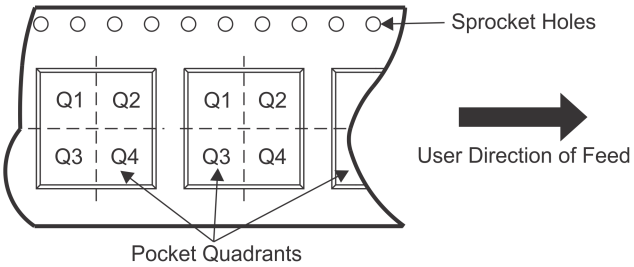


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

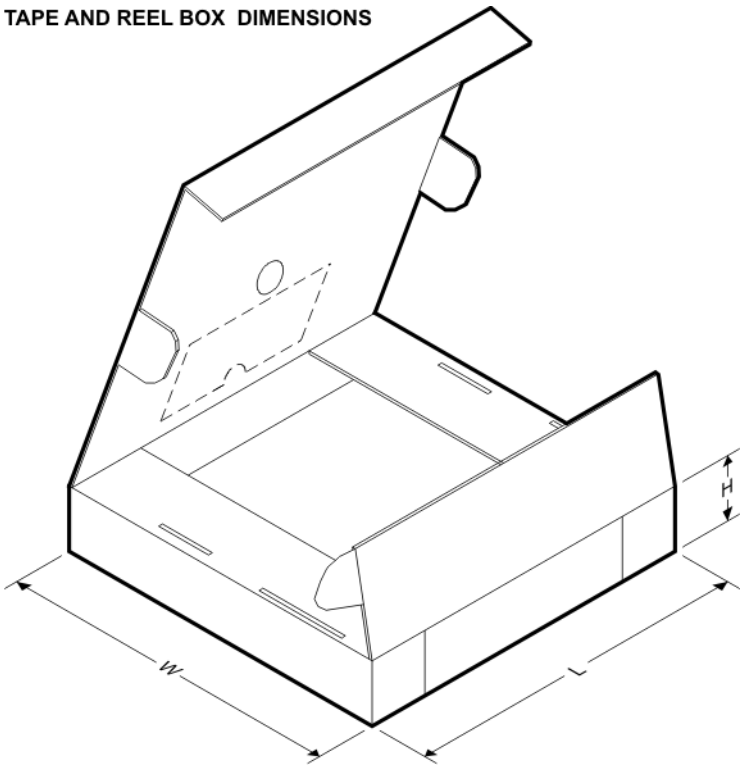
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
LM5105SD/NOPB	WSON	DPR	10	1000	180.0	12.4	4.3	4.3	1.1	8.0	12.0	Q1
LM5105SDX/NOPB	WSON	DPR	10	4500	330.0	12.4	4.3	4.3	1.1	8.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
LM5105SD/NOPB	WSON	DPR	10	1000	203.0	203.0	35.0
LM5105SDX/NOPB	WSON	DPR	10	4500	346.0	346.0	35.0

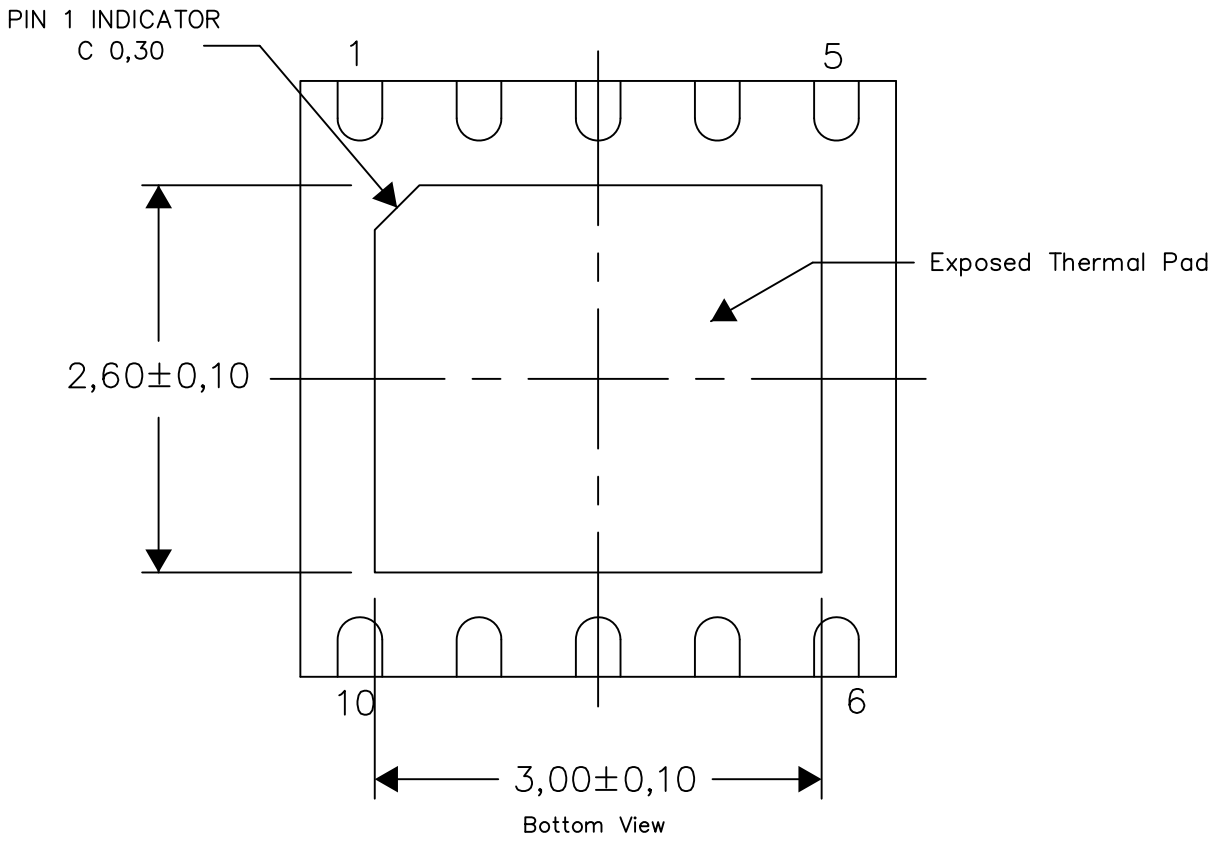
DPR (S–PWSON–N10) PLASTIC SMALL OUTLINE NO–LEAD

THERMAL INFORMATION

This package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. The thermal pad must be soldered directly to the printed circuit board (PCB). After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For information on the Quad Flatpack No–Lead (QFN) package and its advantages, refer to Application Report, QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271. This document is available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.

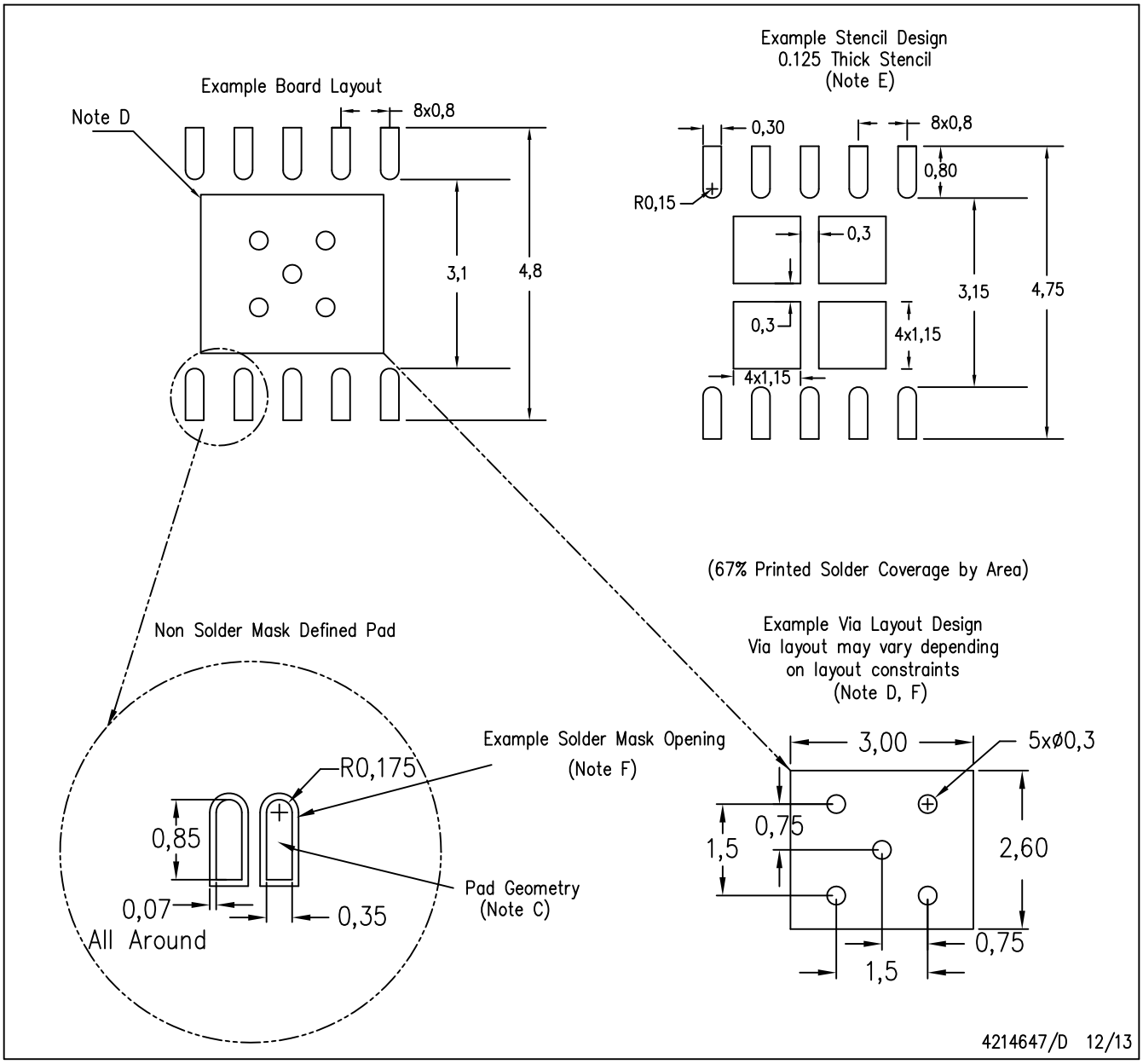


Exposed Thermal Pad Dimensions

4211551/C 12/13

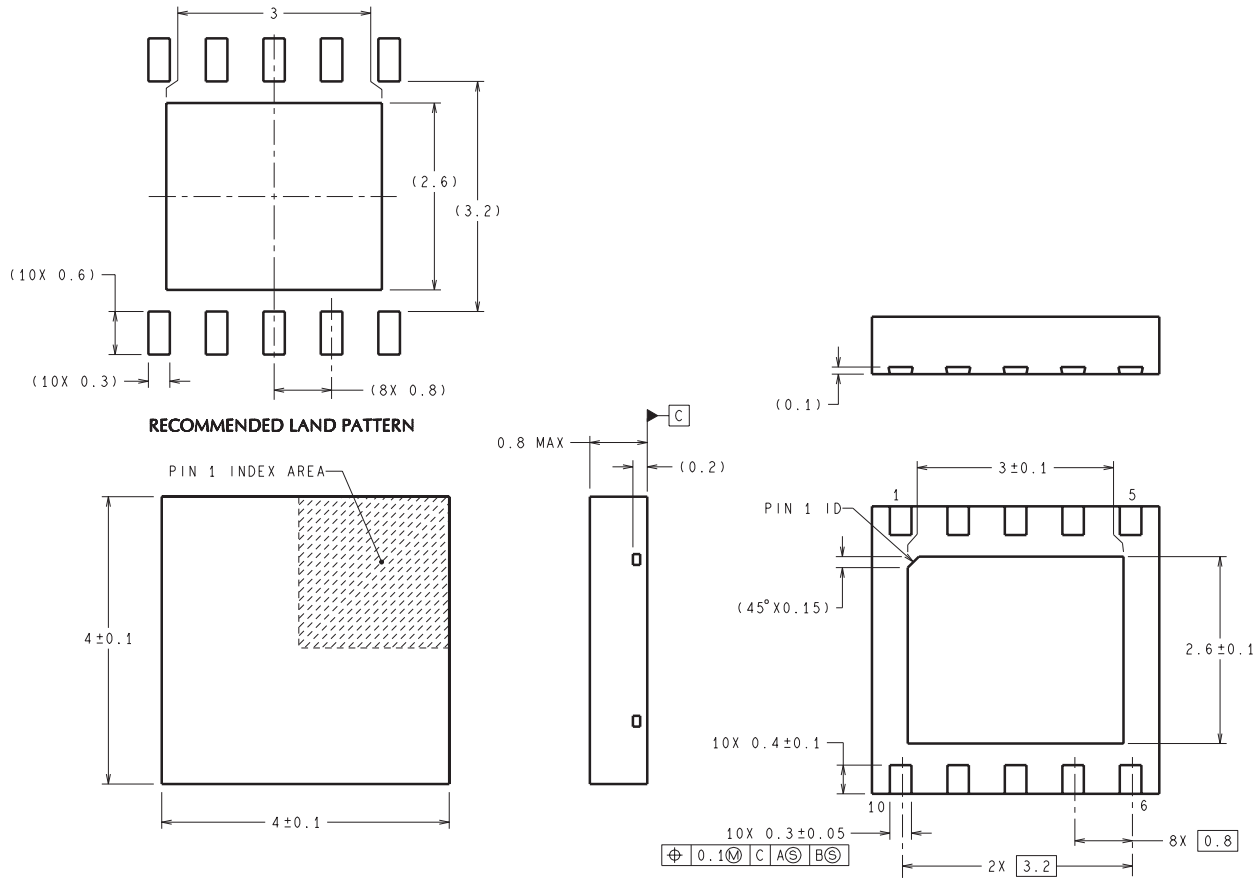
NOTES: All linear dimensions are in millimeters

DPR (S–PWSON–N10) PLASTIC SMALL OUTLINE NO–LEAD



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. This package is designed to be soldered to a thermal pad on the board. Refer to Application Note, Quad Flat–Pack Packages, Texas Instruments Literature No. SLUA271, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com <http://www.ti.com>.
E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
F. Customers should contact their board fabrication site for recommended solder mask tolerances and via tenting recommendations for vias placed in the thermal pad.

DPR0010A


3
(2.6)
(3.2)
(10X 0.6)
(10X 0.3)
(8X 0.8)
RECOMMENDED LAND PATTERN
PIN 1 INDEX AREA
4±0.1
4±0.1
0.8 MAX
C
(0.2)
(0.1)
3±0.1
PIN 1 ID
1
5
(45°X0.15)
2.6±0.1
10X 0.4±0.1
10
6
10X 0.3±0.05
0.1Ⓜ C AⓈ BⓈ
8X 0.8
2X 3.2
DIMENSIONS ARE IN MILLIMETERS
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