LM5066IEVM-626 Evaluation Module (EVM)

This user's guide describes the LM5066I EVM (LM5066IEVM-626). LM5066IEVM-626 contains evaluation and reference circuitry for the LM5066I. The LM5066I device combines a high performance hot swap controller with a PMBus™ compliant SMBus/I²C interface to accurately measure, protect, and control the electrical operating conditions of systems connected to a backplane power bus.

Contents

1 Introduction 3
1.1 Features 3
1.2 Applications 3
1.3 Electrical Specifications 3
2 Schematic 4
3 General Configuration and Description 5
3.1 Physical Access 5
3.2 Equipment Setup 6
4 Operation 6
5 Test Results 7
6 Getting Started 11
6.1 Hardware Setup Steps 11
6.2 Device Evaluation 11
6.3 GUI Event Log 13
6.4 Plotting Telemetry Data 14
6.5 Configuring the LM5066I Device 14
6.6 Customizing the Design 16
7 Layout Guidelines 18
8 Board Layout 20
9 Bill of Materials 23

List of Figures

1 Startup Waveform 7
2 Startup into Short Performance 7
3 Overvoltage Performance 8
4 Undervoltage Waveform 8
5 Overload Performance 9
6 Load Transient into Overload Performance 9
7 Hot Short on Vout (Zoomed Out) 10
8 Hot Short on Vout (Zoomed In) 10
9 Device Selector 11
10 Initial GUI Screen 12
11 LM5066I Block-Level Representation 12
12 LM5066I Telemetry Display Options 13
13 LM5066I GUI With the Telemetry Plotting Tool Enabled 14
14 Device Configuration Panel 15
15 LM5066I Design Tool 16
16 Recommended Board Connector Design 18

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17 Sense Resistor Connections 19
18 Top Assembly 20
19 Top Layer 20
20 Internal Layer 1 21
21 Internal Layer 2 21
22 Bottom Layer 22

List of Tables

1 LM5066IEVM-626 Electrical and Performance Specifications at 25°C 3
2 Connector Functionality 5
3 Test Points 5
4 Switches 6
5 LM5066IEVM-626 BOM 23

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1 Introduction

The LM5066IEVM-626 evaluation board provides the design engineer with a fully functional intelligent monitoring and protection controller board designed for positive voltage systems. This user's guide describes the various functions of the board, how to test and evaluate it, and how to use the GUI design tool to change the components for a specific application. To use the advanced telemetry and monitoring capabilities of this device, the user must install the Intelligent Power Manager GUI; however, the LM5066I is capable of acting as a hot-swap and protection circuit without any software installation. For the latest software information, check the LM5066I High Voltage System Power Management and Protection IC with PMBus data sheet (SNVS950).

1.1 Features

- Programmable current limiting and power limiting for complete SOA protection
- Programmable fault timer to eliminate nuisance shutdowns
- Programmable undervoltage and overvoltage protection
- Programmable power good indicator
- Programmable auto-retry or latch options
- Fully Node Manager 2.0 and 2.5 compliant with I^2C/SMBus interface and PMBus compliant command structure
- Real-time monitoring of VIN, VOUT, IIN, PIN, and VAUX with 12-bit resolution and 1-kHz sampling rate

1.2 Applications

- Any live backplane insertion application
  - Servers
  - Telecommunications

1.3 Electrical Specifications

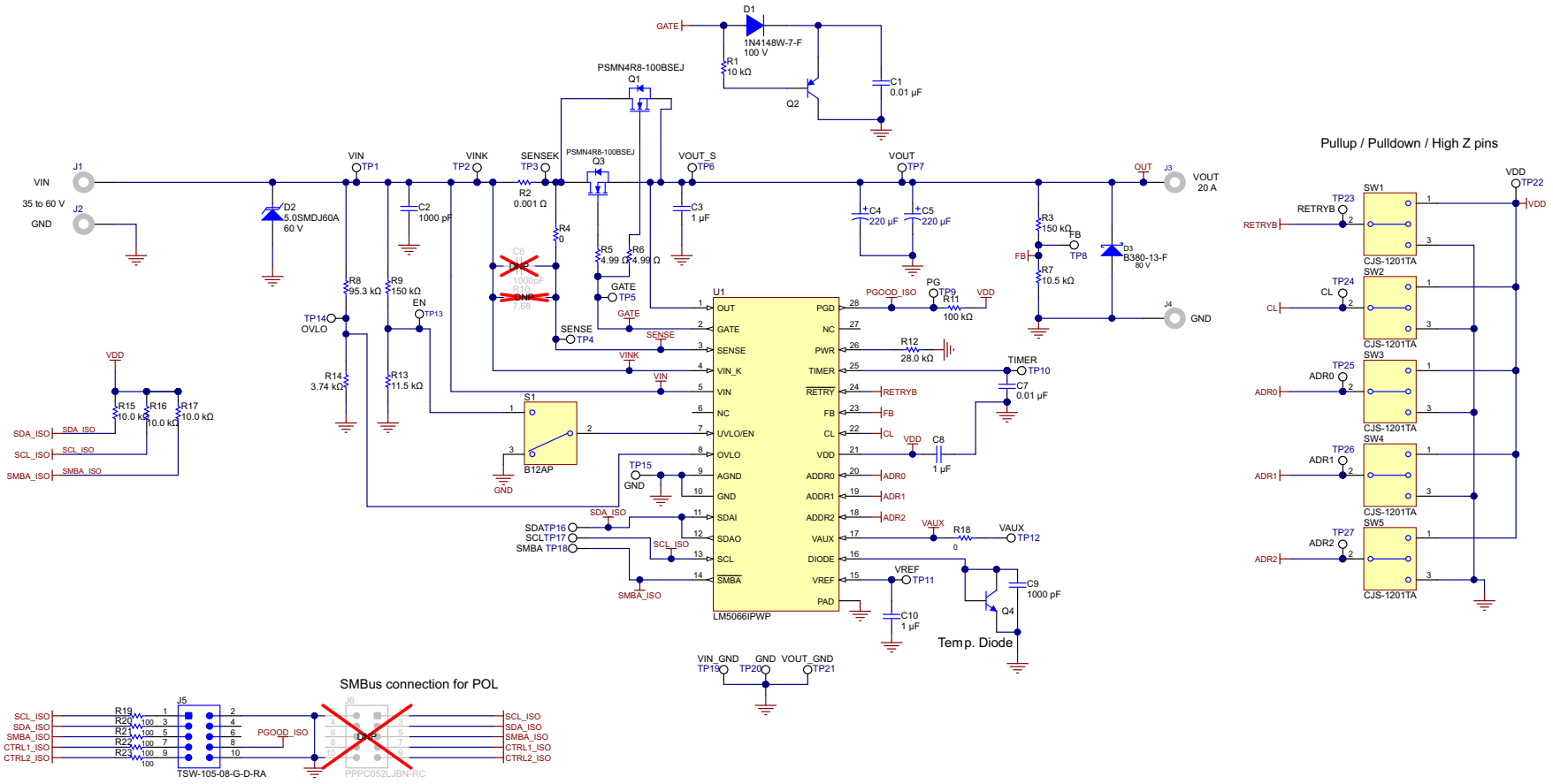
Table 1. LM5066IEVM-626 Electrical and Performance Specifications at 25°C

Characteristic	LM5066IEVM-626
Input voltage range (operating)	40 to 60 V
Current operating	20 A
Power limit (nom)	239 W
Current limit (nom)	26 A
Fault timer (nom)	520 µs
UVLO rising (nom)	38 V
UVLO falling (nom)	35 V
Overvoltage rising (nom)	65 V
Overvoltage falling (nom)	63 V
PG threshold – vout rising (nom)	38 V
PG threshold – vout falling (nom)	35 V
Pass "Hot-Short" on output	Yes
Pass "Start into short"?	Yes
Is the load off until PG asserted?	Yes
Can a hot board be plugged back in?	Yes

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2 Schematic



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3 General Configuration and Description

3.1 Physical Access

Table 2 lists the LM5066IEVM-626 connector and functionality, Table 3 describes the test point availability, and Table 4 describes the switch functionality.

Table 2. Connector Functionality

Connector	Label	Description
J1	VIN	Power bus input. Apply bus input voltage between J1 and J2.
J2	GND	Power bus input return connector. Apply bus input voltage between J1 and J2.
J3	VOUT	Switched bus output. Apply the load between J3 and J4.
J4	GND	Switch bus output return connector. Apply the load between J3 and J4.
J5		PMBus interface

Table 3. Test Points

Test Point	Label	Description
TP1	VIN	Positive supply input
TP2	VINK	Positive supply Kelvin sense pin on sense resistor
TP3	SENSEK	Sense Kelvin sense pin on sense resistor
TP4	SENSEK	Sense pin test point
TP5	GATE	Gate drive output
TP6	VOUT_S	Output voltage at the pass FET
TP7	VOUT	Output voltage at the load
TP8	FB	Power Good feedback
TP9	PG	Power Good indicator
TP10	TIMER	Timing capacitor voltage
TP11	VREF	Internal reference voltage
TP12	VAUX	Auxiliary ADC input
TP13	EN	UVLO/EN pin voltage
TP14	OVLO	OVLO pin voltage
TP15, TP19, TP20, TP21	GND	Circuit ground
TP16	SDA	SMBus input/output
TP17	SCL	SMBis clock
TP18	SMBA	SMBUS alert line (active low)
TP22	VDD	Internal sub-regulator 4.85-V output
TP23	RETRYB	Fault retry input
TP24	CL	Current limit range
TP25	ADR0	SMBus address line 0
TP26	ADR1	SMBus address line 1
TP27	ADR2	SMBus address line 2

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Table 4. Switches

Switch	Label	Description
S1	EN	Enable and disable of the hotswap
SW1	RETRY	Fault retry input
SW2	CL	Current limit range
SW3	ADR0	SMBus address line 0
SW4	ADR1	SMBus address line 1
SW5	ADR2	SMBus address line 2

3.2 Equipment Setup

1. Set the input power supply voltage to the desired operating input voltage.
2. Turn the power supply off.
3. Connect the positive voltage lead from the power supply to J1 (VIN). Connect the ground lead form the power supply to J2 (GND).
4. Place a voltmeter or oscilloscope probe across J3 and J4 (VOUT).

4 Operation

1. Turn on the power supply.
2. Enable S1 ON.
3. Vary the input voltage and add load current as necessary for test purposes.
4. Apply fault conditions to observe fault performance as necessary.

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5 Test Results

This section provides typical performance waveforms for the LM5066IEVM-626 with VIN = 48 V at no load (unless otherwise specified). Actual performance data is affected by measurement techniques and environmental variables; therefore, these curves are presented for reference and may differ from actual results obtained.

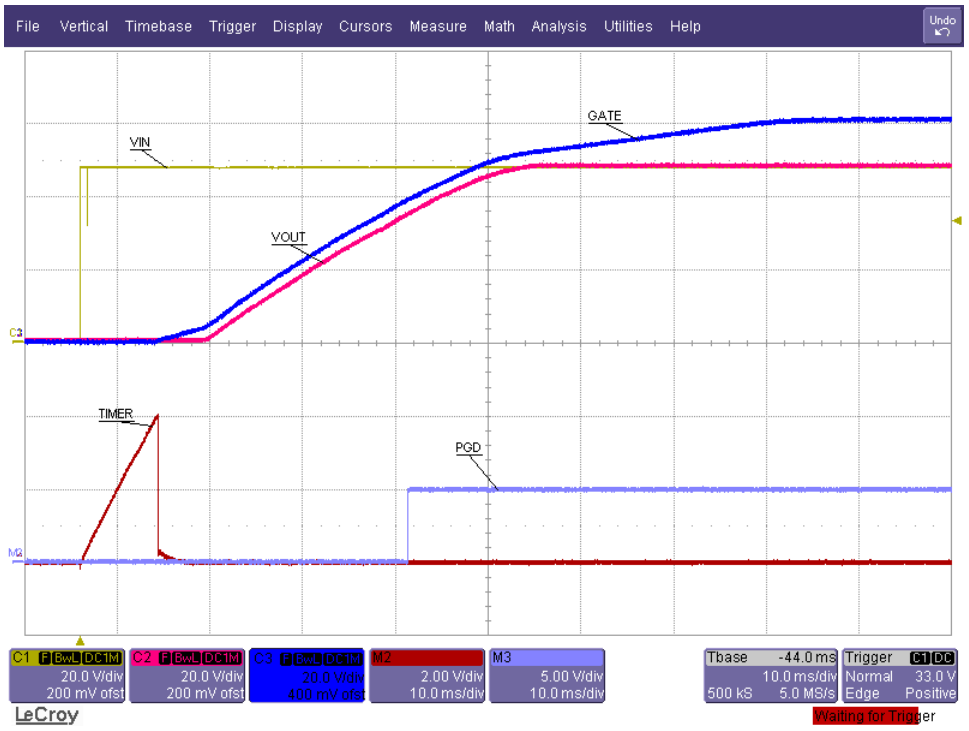


Figure 1. Startup Waveform



Figure 2. Startup into Short Performance

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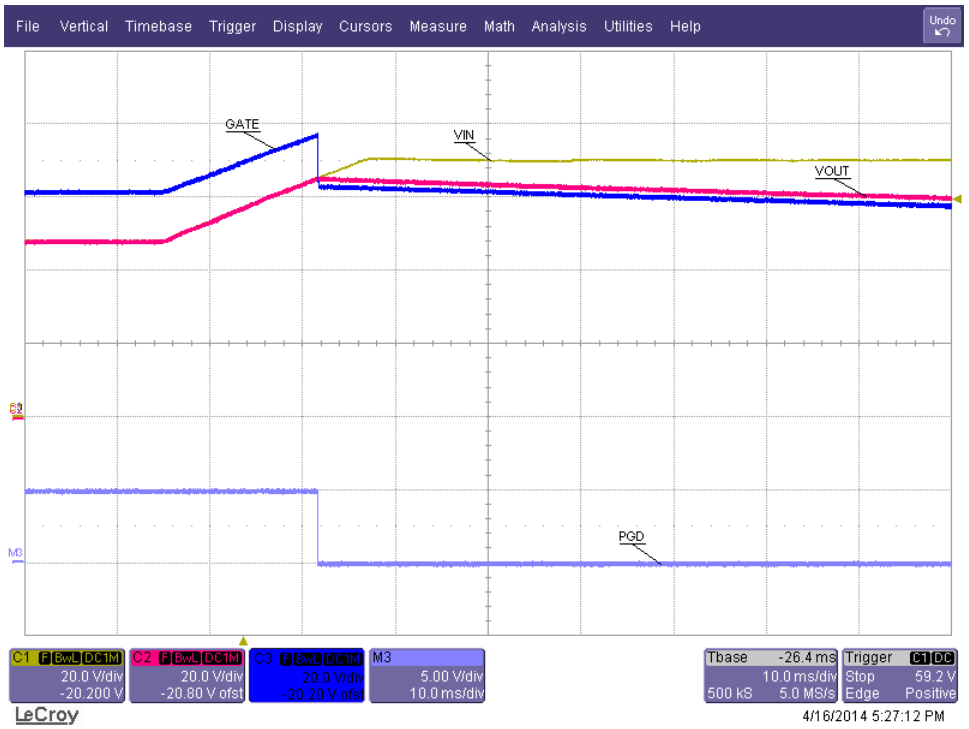


Figure 3. Overvoltage Performance

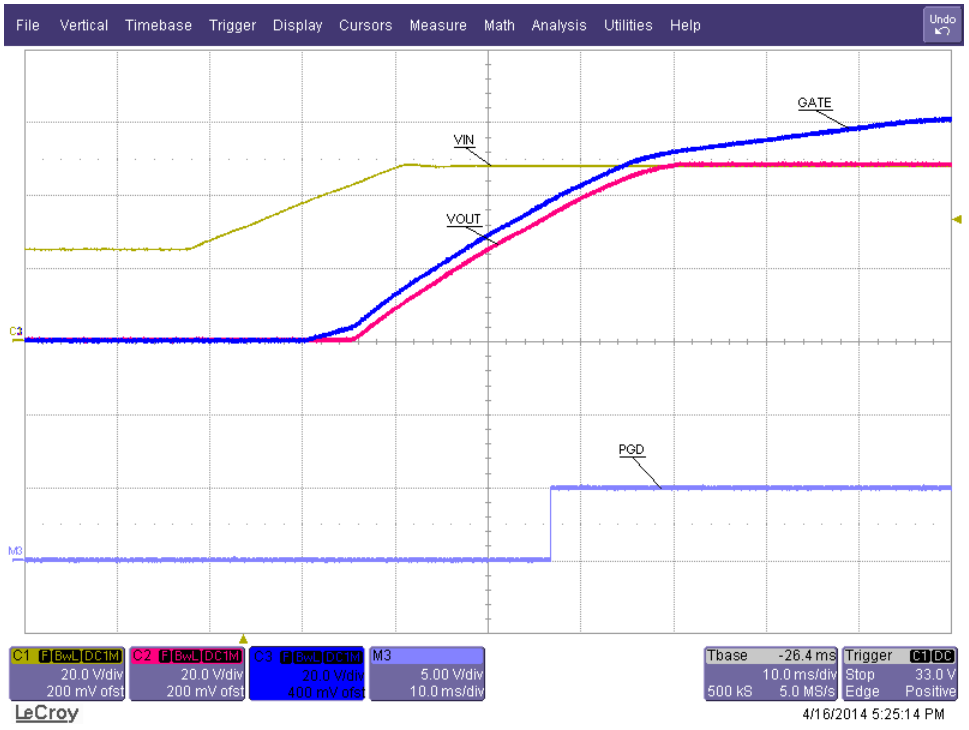


Figure 4. Undervoltage Waveform

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Figure 5. Overload Performance

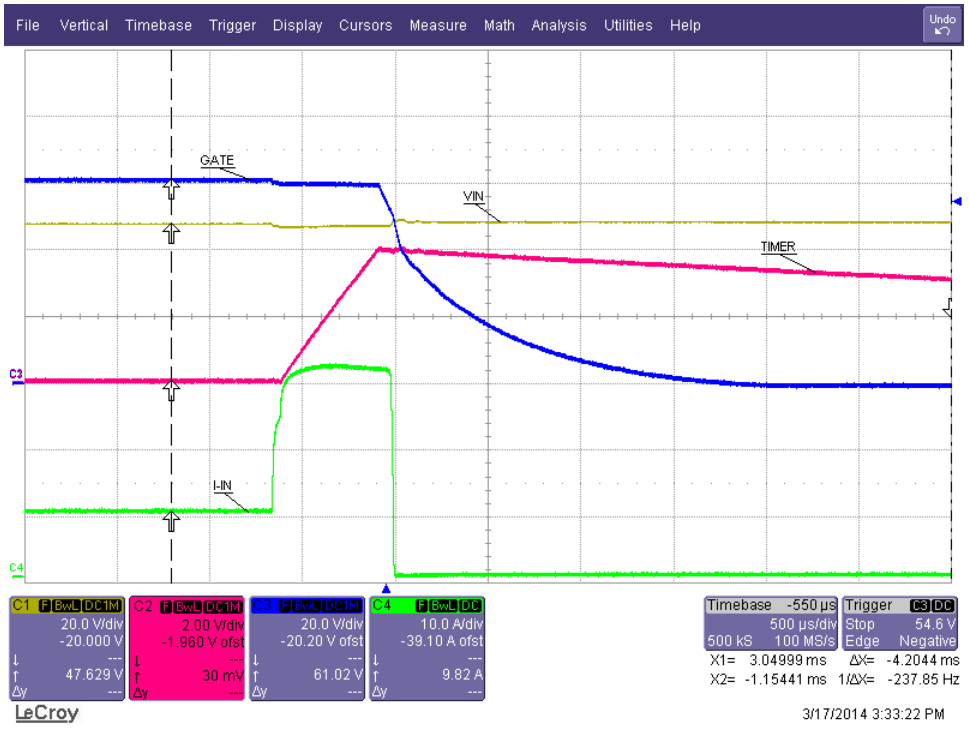


Figure 6. Load Transient into Overload Performance

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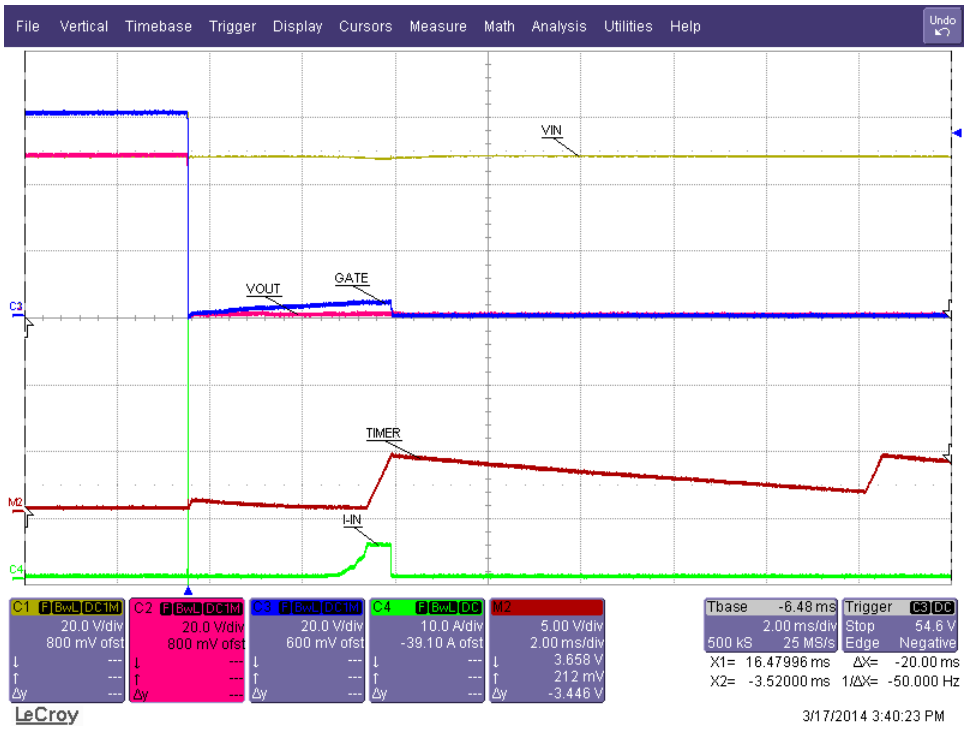


Figure 7. Hot Short on Vout (Zoomed Out)

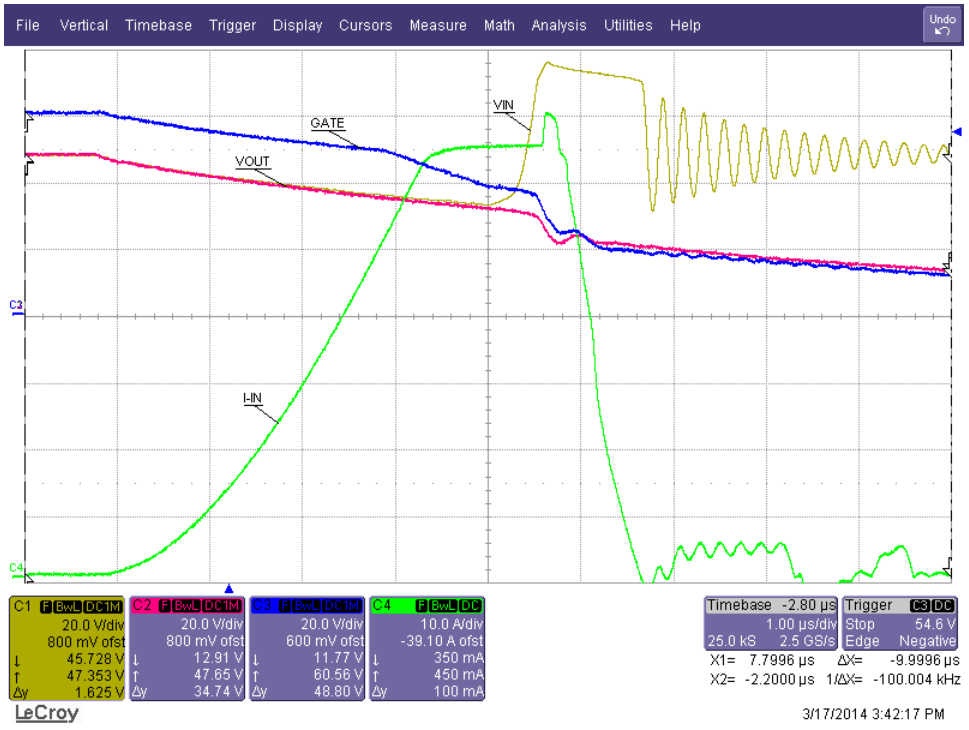


Figure 8. Hot Short on Vout (Zoomed In)

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6 Getting Started

The LM5066IEVM is supplied with the PMBus address set to 0x40 as dictated by the jumper configuration of the ADR0, ADR1, and ADR2 jumper connections.

The first step to evaluate the telemetry features of LM5066I is to install the GUI software. The software can be found under software on the product page. This file should be executed on a PC running Windows® XP or later to install the software.

6.1 Hardware Setup Steps

1. Connect the input supply to the VIN (J1) and GND (J2) banana plugs.
2. Connect the load to the VOUT (J3) and GND (J4) banana plugs.
3. Connect the FTDI Dongle to the 10-pin connector on the left side of the board to J5.
4. Connect the supplied mini USB cable from the FTDI dongle to an USB port on a PC.

When the FTDI dongle is connected for the first time, the user will be prompted to install the device drivers. For the most current driver installation procedure, refer to the README.TXT file in the installation directory.

For a hot swap circuit to function reliably, TI recommends a low inductance connection to the input supply. Its purpose is to minimize voltage transients which occur when the load current changes or is shut off. If the user is not careful, wiring inductance in the supply lines will generate a voltage transient at the input which can exceed the absolute maximum rating of the LM5066I, resulting in its destruction. To protect against such voltage transients, TVS device D2 is provided to clamp the voltage at the input to within safe operating limits. Likewise, Schottky diode D3 is provided on the output to clamp the output from going excessively negative during short circuit events.

6.2 Device Evaluation

After configuring the hardware connections, apply an input voltage of 48 V to the device. The current hardware configuration allows the LM5066I device to work from 40- to 60-V input supply voltage; however, this guide assumes an input voltage of 48 V. Launch the GUI by going to the Windows Start menu → All Programs → PMBManager-x.xxxxx → PMBusManager. A pulldown menu should come up with a list of devices populated. Select the "LM5066" option as shown in Figure 9.

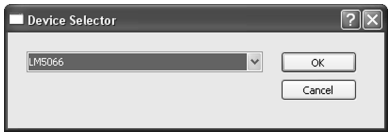


Figure 9. Device Selector

The device should be detected on the PMBus, and the initial load screen should appear as shown in Figure 10.

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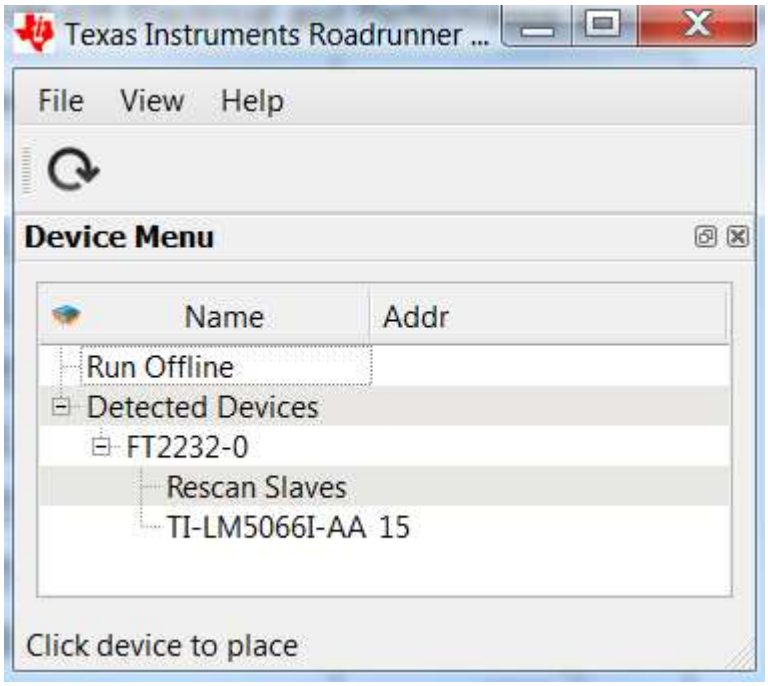


Figure 10. Initial GUI Screen

If a device is not detected, there is an option to rescan, ignore, or exit the GUI. If the hardware is intended to be connected, check the USB connection to the PCB, FTDI connection to the evaluation module, and verify that the power is present on the evaluation PCB by measuring the voltage between the V_{IN_S} and V_{IN_GND} test points. Ignoring the detection message allows use of the integrated design tool without the hardware connected.

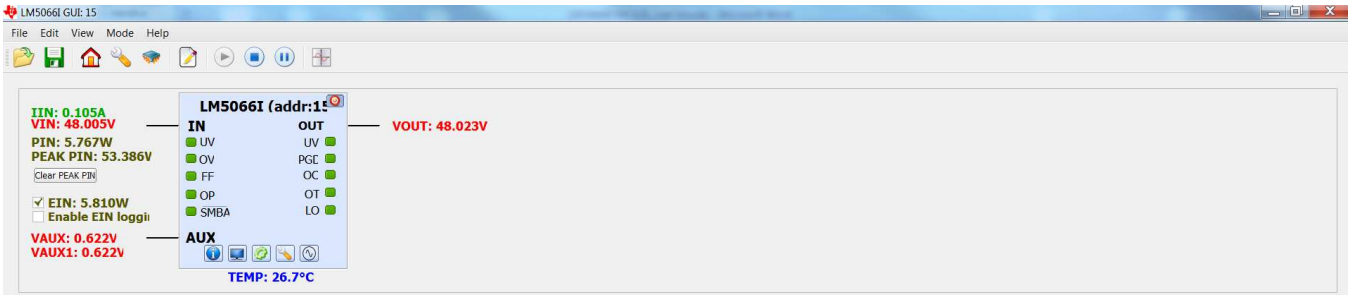


Figure 11. LM5066I Block-Level Representation

Click on the detected device ID (TI-LM5066I-AA) to display a block level representation of the device as shown in Figure 11. The block level view of the device provides a display of all the telemetry data as well as most of the faults and warnings supported by the device. The faults and warnings supported are generally associated with an invalid input or output condition.

The faults shown on the left side of the block representation are generally associated with the input. These include input under-voltage (UV), input over-voltage (OV), FET fail (FF), and input over-power (OP). The SMBus alert status, $\overline{\text{SMBA}}$, is also shown on the left side and will turn red during any warning or fault event. To facilitate the evaluation of the device, SMBus alerts are automatically cleared by the GUI.

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The faults shown on the right side of the block representation are associated with the output. These include output over-voltage (OV), power good status (PGD), output over-current (OC), and over-temperature (OT). There is also an indicator if the output is in the latched off state (LO). The device latches the output off after the number of user-programmable retries is exceeded. To clear the latched off condition, the output can be toggled off and on by the red power button located in the top right of the LM5066I block representation.

To show a repetitive update of the device telemetry and status, click the Play button at the top of the screen. The Play button starts an active telemetry log of the gathered data. Clicking the Stop button stops the telemetry collection and allows for the log file to be viewed and saved. The Pause button pauses both the displaying and logging of telemetry information.

To enable or disable specific telemetry, click the Display Options button on the block representation and choose the desired telemetry to display (see Figure 12).

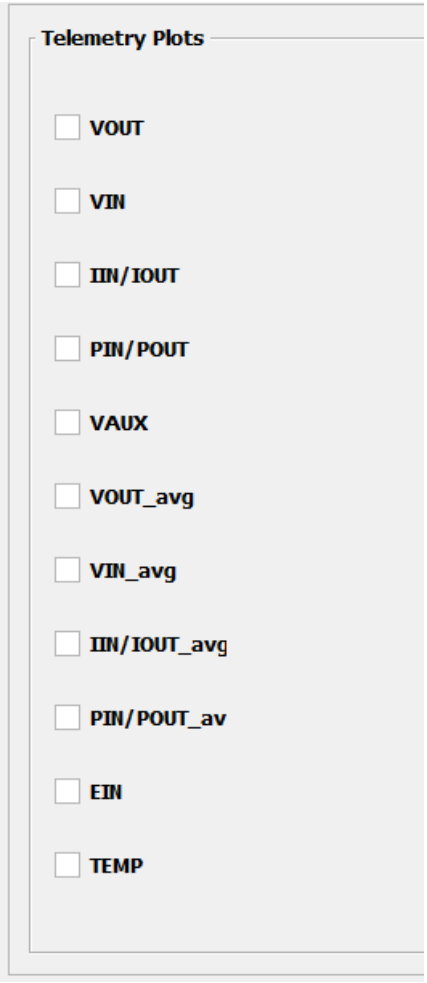


Figure 12. LM5066I Telemetry Display Options

Note that turning off the various warning options does not mask the faults from issuing an SMBus alert; by turning off warning options, the selected warnings are just not displayed if they occur. The device is capable of masking various faults, and this functionality can be setup in the device configuration panel.

6.3 GUI Event Log

A GUI event log is provided to keep track of GUI configuration changes and device fault events. To display the event log, select View from the main menu bar, then Telemetry Data Log. The event log appears on the left side of the main GUI window. The event log can be detached and expanded if desired by left clicking on the event log window and dragging the window with the mouse to the desired location.

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6.4 Plotting Telemetry Data

To enable telemetry data plots, click on the sine wave button located on the LM5066I block representation. After enabling the telemetry, a prompt appears requesting entry of the GUI sample interval, plot interval, and plot depth. For most cases, the default rates and depths are acceptable. The plotting tool allows the user to select the desired data to be plotted. Up to two different parameters can be plotted at the same time as shown in Figure 13.



Figure 13. LM5066I GUI With the Telemetry Plotting Tool Enabled

Telemetry data is plotted as a black line that continually updates as the device is queried. In addition to the telemetry data, the relevant warning and fault thresholds are also plotted. Warning thresholds are shown as orange lines while fault thresholds are shown in red and blue.

From the Plot menu option in the main menu bar, the user can disable the plotting grid and the warning and fault lines.

6.5 Configuring the LM5066I Device

Warning thresholds, temperature fault threshold, protection ranges, fault masking, and averaging can be configured in the Device Configuration panel. This panel, shown in Figure 14, is enabled by clicking View → Device Configuration.

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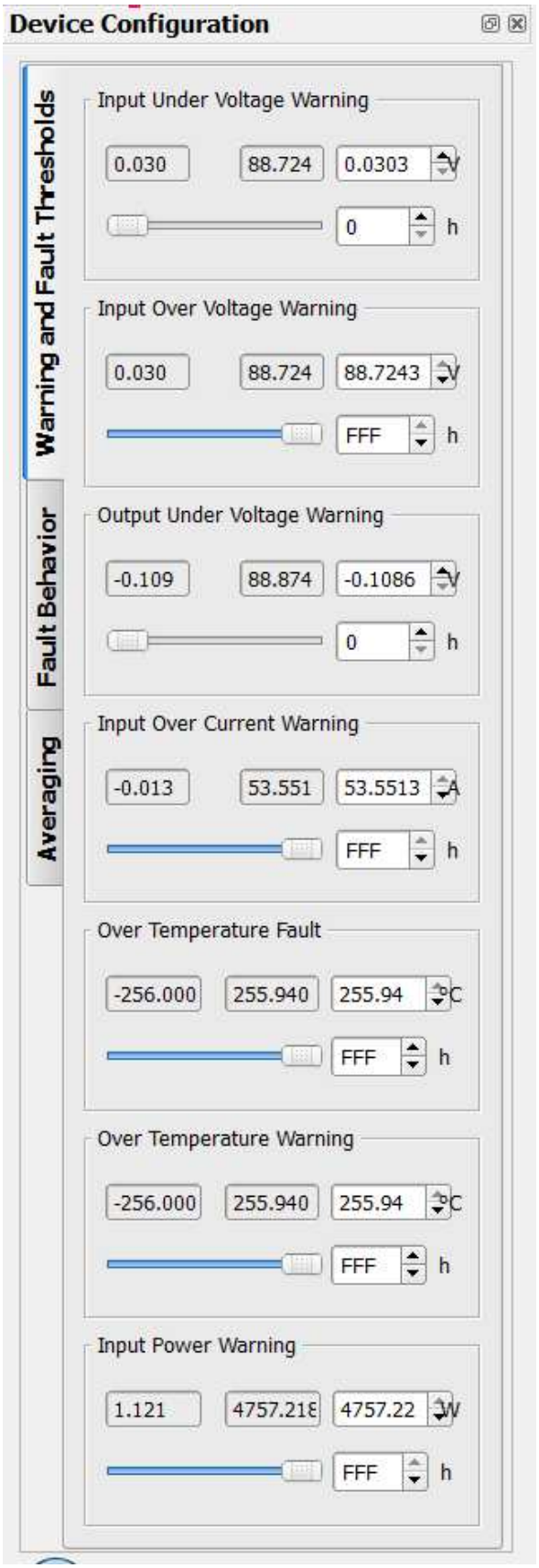


Figure 14. Device Configuration Panel

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The Warning and Fault Threshold tab allows configuration of the input undervoltage, input overvoltage, output undervoltage, input overcurrent, input power, and overtemperature warnings. This tab also allows adjustment of the overtemperature fault threshold. The hardware design sets the fault threshold for the input over-voltage and under-voltage, current limit, power limit, and power good. Decimal values for the thresholds are shown in the text box located to the right of the slider bar. The hexadecimal value of the setting is located above the decimal values setting, which can be useful when developing software for this device.

The fault behavior tab allows the user to set the device fault configuration and fault masking. The fault configuration section allows the user to set the number of retries, as well as the circuit breaker and current limit thresholds. The number of retries can be set by the $\overline{\text{RETRY}}$ pin to be infinite or latched off. Through software, the number of retries can be set to 0 (latch-off), 1, 2, 4, 8, 16, or infinite. The software settings are independent of the hardware settings; however, if the power is cycled, the device defaults to values dictated by the hardware. Current limit power-up values are also set by the hardware. The values for current limit can be set to either 26 mV (CL = VDD) or 50 mV (CL = GND). The circuit breaker threshold can also be set in software to either 1.9× or 3.9× the current limit value through the software. Fault masking is possible for many of the device fault conditions. Fault conditions allow masking of both the MOSFET response and the SMBus alert signal. Note that if a fault occurs repeatedly while the MOSFET is masked, damage to the MOSFET may result. This feature is allowed primarily for debug purposes. Faults that do not shut off the MOSFET and only issue a SMBus alert, also allow masking of the alert. Note the power-up default setting for the Power Good signal is to mask the SMBus alert, in order to ensure that SMBus alert is not asserted immediately after power-up.

For convenience, the Device Configuration panel can be undocked by holding down the left mouse button while the cursor is at the top of the panel and dragging it to the desired location.

6.6 Customizing the Design

The GUI assumes the hardware configuration is set to default LM5066I evaluation board configuration. If any of the components are changed, the device hardware configuration needs to be updated in the Design Tool section. To open the design tool, click the Wrench button located on the LM5066I block representation, which will open the window displayed in Figure 15.

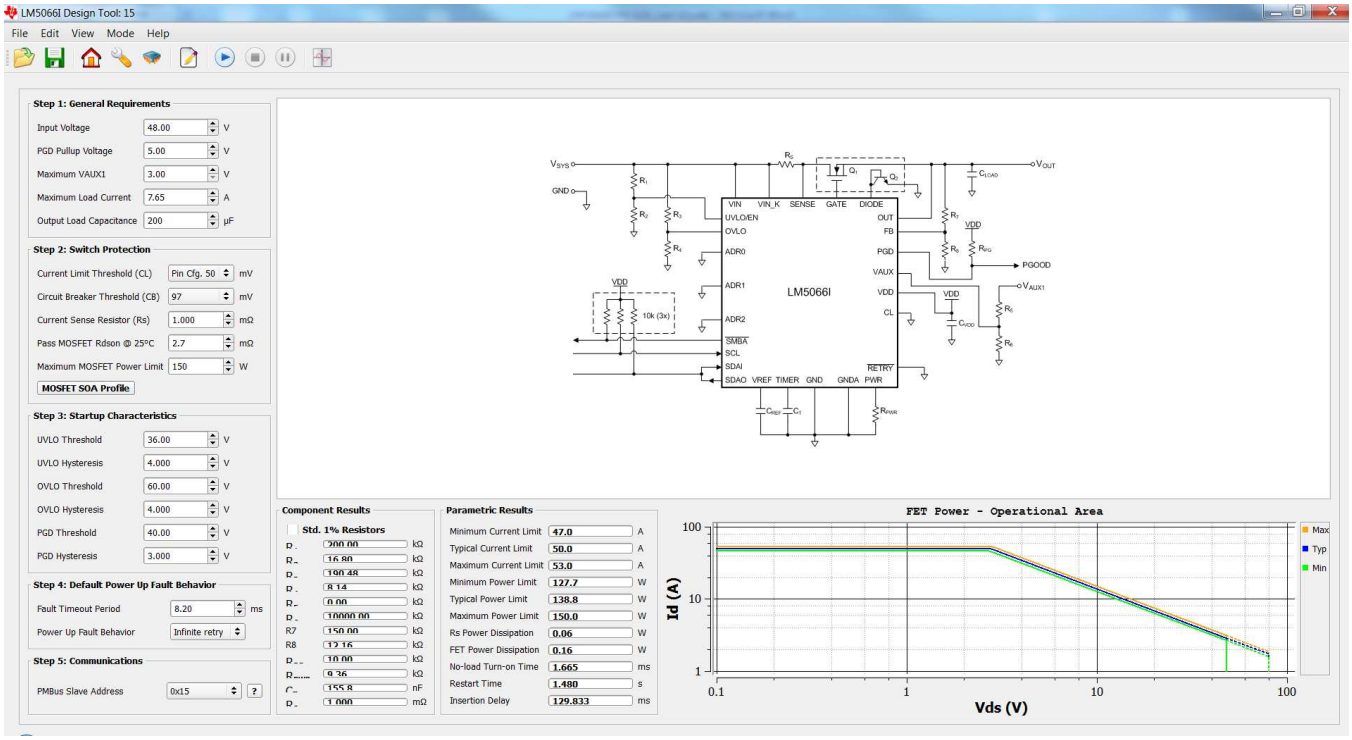


Figure 15. LM5066I Design Tool

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Design inputs are keyed in on the left side following steps 1 though 5.

1. Enter the general operating conditions in step 1 of the design tool. These inputs help set bounds on the startup time and application voltage ranges.
2. Step 2 allows the user to tailor the MOSFET protection features to be specific to the target application. Current limit is pin-configurable and software-configurable, and circuit breaker is software-configurable. If the CL switch is used to set the current limit, ensure the GUI selection matches the pin-configurable CL bit setting on the board. By clicking on the MOSFET SOA Profile button, the user can select SOA data from several popular MOSFETs or enter the SOA data for the desired MOSFET. The resistor R_{PWR} can then be calculated to keep Q_1 or Q_3, or both, within its SOA profile.
3. Step 3 allows the user to select the undervoltage lockout (UVLO) and overvoltage lockout (OVLO) values, and power good (PGD) thresholds. Note that with the correct values for R8, R9, R13, R14, and R3 and R7 installed, the LM5066I indicates a fault condition when the input or output voltages, or both, are outside of their programmed range.
4. Step 4 allows the user to set the fault time-out period and the fault response. The fault time-out should be set to be below the MOSFET SOA data for a given time. For example, if a design is done to adhere to the 10 ms pulsed MOSFET SOA data, the desired fault time-out must be less than 10 ms. The fault time-out time entered sets the value for C_T. It also sets the insertion delay and fault retry delay. The initial power-up retry behavior is also selected in this design step. Make sure to change the $\overline{\text{RETRY}}$ switch to match the design tool schematic when changing the default retry setting.
5. In step 5, the user enters the desired PMBus address. Note changing the PMBus address of the device in step 5 does not change the device address, but shows how the address pins of the device need to be configured to achieve a desired address. After the ADR pin switches are configured for a particular address, power to the device needs to be cycled and the GUI restarted in order for the new address to take effect.

When invalid or incorrect inputs are given to the design tool, text associated with the faulty input turns red. Positioning the mouse cursor over the red text gives additional information about any design conflict.

Component and parametric results are shown to the right as well as the LM5066I safe operational area (SOA) chart. The SOA chart shows the minimum, typical, and maximum SOA protection areas for a given design. For a robust design, the SOA of the MOSFET used should be above the max protection SOA line for all operating areas.

After a design is complete, the design should be saved by selecting the File menu, then Save. After the hardware is modified to match the design, the GUI should be restarted and the hardware configuration file loaded right after the device is detected and placed. If the values in the design tool are different than the values on the board, erroneous telemetry and fault data are reported by the GUI. To return to the block view of the device, press the Home button located at the far left in the menu bar.

The design tool is also useful to calculate the PMBus coefficients. With the correct value for current sense resistor (R2), the tool calculates the correct coefficients to scale the raw telemetry data. The coefficients can be viewed by selecting View from the main menu bar, and then selecting the PMBus Coefficient Editor. When the PMBus Coefficient Editor is opened, press the Get All button to show the currently used coefficients.

If desired, the results presented by the design tool can be calculated by hand using the equations provided in the data sheet. However, note the design tool calculates parameters factoring in worst-case tolerances, while the equations in the data sheet are based on typical thresholds.

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7 Layout Guidelines

The following guidelines should be followed when designing the PC board for the LM5066I:

1. Place the LM5066I close to the board's input connector to minimize trace inductance from the connector to the MOSFET.
2. Place a TVS, Z1, directly adjacent to the VIN and GND pins of the LM5066I to help minimize voltage transients which may occur on the input supply line. The TVS should be chosen such that the peak VIN is just lower the TVS reverse-bias voltage. Transients of ≥20 V over the nominal input voltage can easily occur when the load current is shut off. A small capacitor may be sufficient for low current sense applications (I <2 A). TI recommends to test the VIN input voltage transient performance of the circuit by current limiting or shorting the load and measuring the peak input voltage transient.
3. Place a 1-µF ceramic capacitor as close as possible to VREF pin.
4. Place a 1-µF ceramic capacitor as close as possible to VDD pin.
5.
6. The sense resistor (RS) should be placed close to the LM5066I. A trace should connect the VIN pad and Q1 pad of the sense resistor to VIN_K and SENSE pins, respectively. Connect RS using the Kelvin techniques shown in Figure 16.
7. The high-current path from the board's input to the load (through Q1), and the return path, should be parallel and close to each other to minimize loop inductance.
8. The AGND and GND connections should be connected at the pins of the device. The ground connections for the various components around the LM5066I should be connected directly to each other and to the LM5066I's GND and AGND pin connection, and then connected to the system ground at one point. Do not connect the various component grounds to each other through the high current ground line.
9. Provide adequate thermal sinking for the series-pass device (Q1) to help reduce stresses during turn-on and turn-off.
10. The board's edge connector can be designed such that the LM5066I detects through the UVLO/EN pin that the board is being removed, and responds by turning off the load before the supply voltage is disconnected. For example, in Figure 17, the voltage at the UVLO/EN pin goes to ground before VIN is removed from the LM5066I as a result of the shorter edge connector pin. When the board is inserted into the edge connector, the system voltage is applied to the LM5066I's VIN pin before the UVLO voltage is taken high, thereby allowing the LM5066I to turn on the output in a controlled fashion.

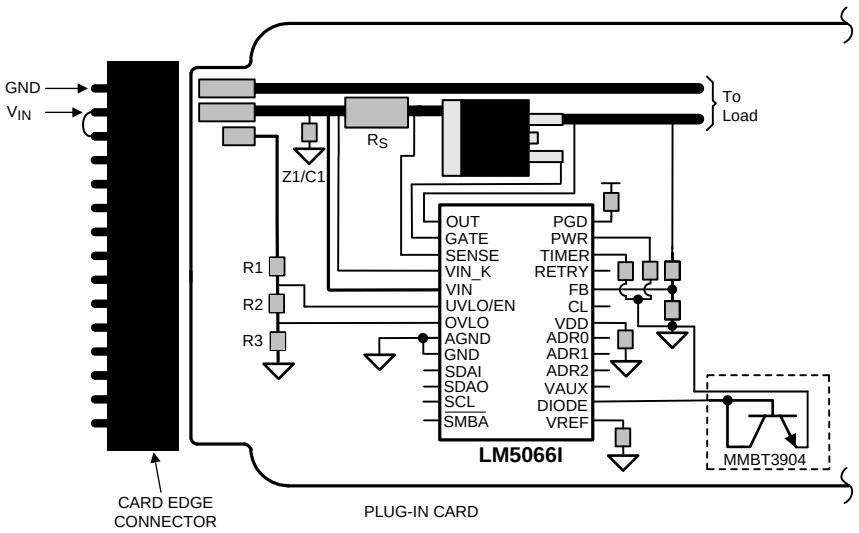


Figure 16. Recommended Board Connector Design

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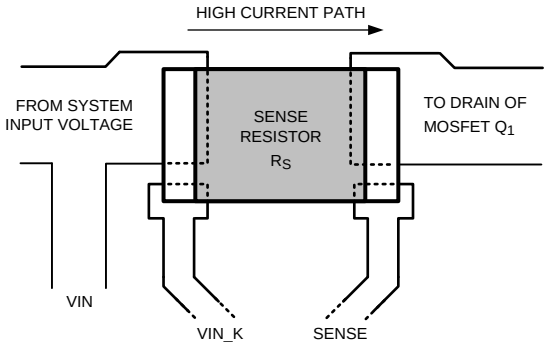


Figure 17. Sense Resistor Connections

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8 Board Layout

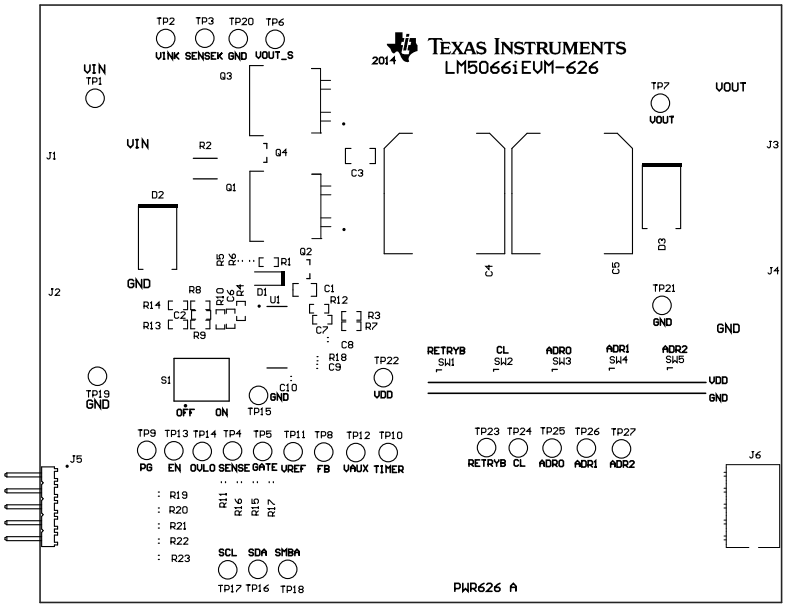


Figure 18. Top Assembly

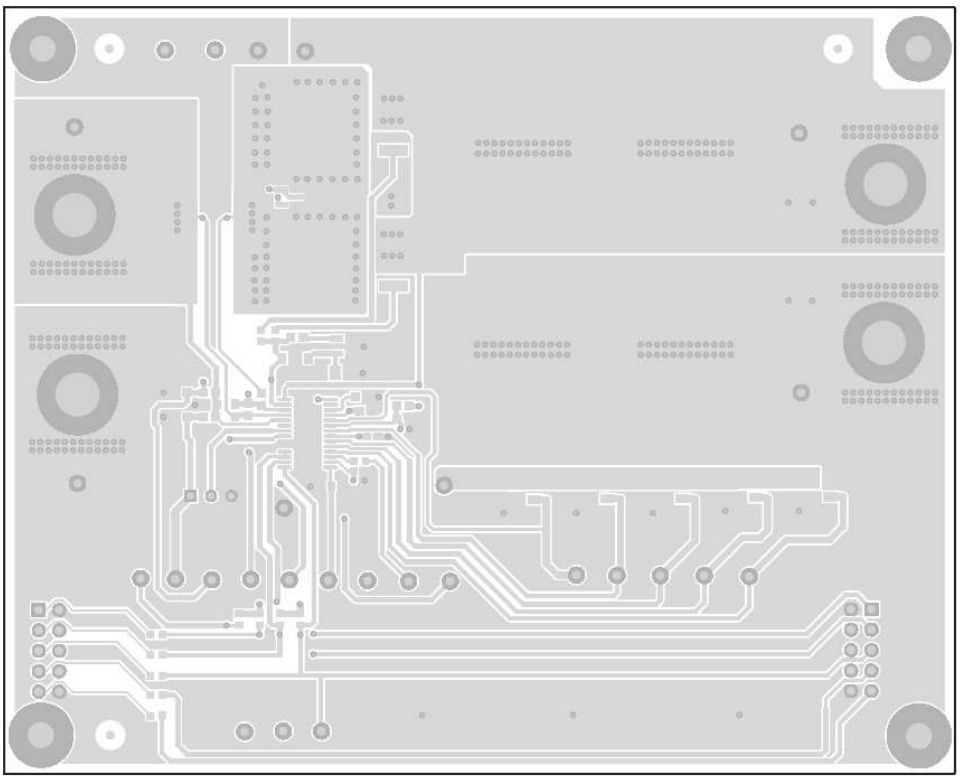


Figure 19. Top Layer

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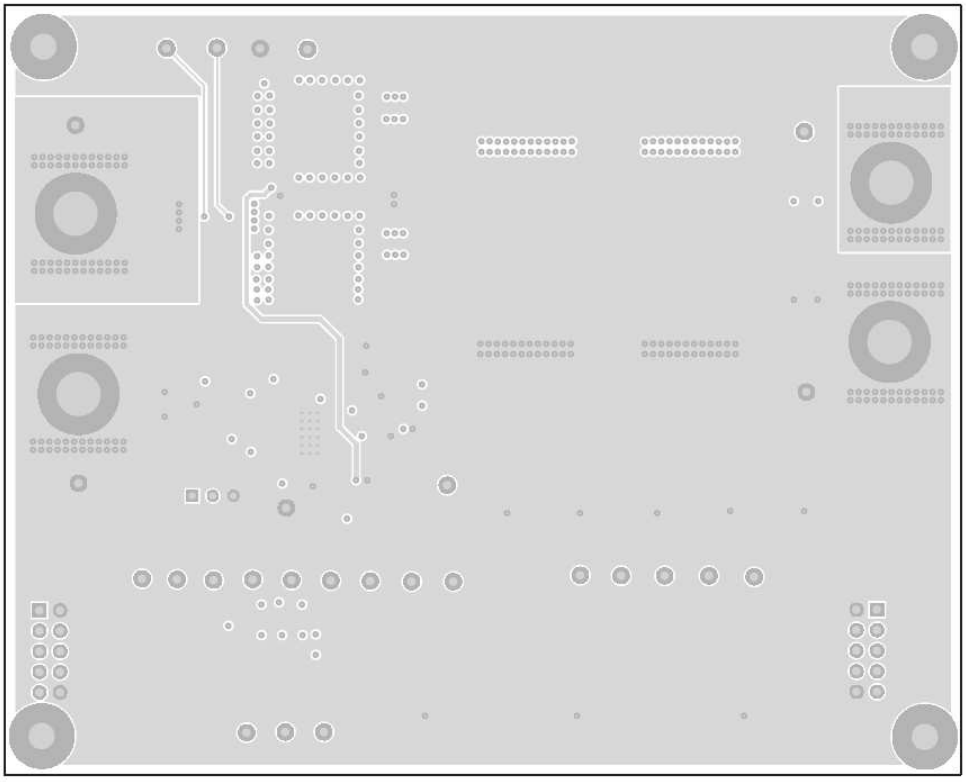


Figure 20. Internal Layer 1

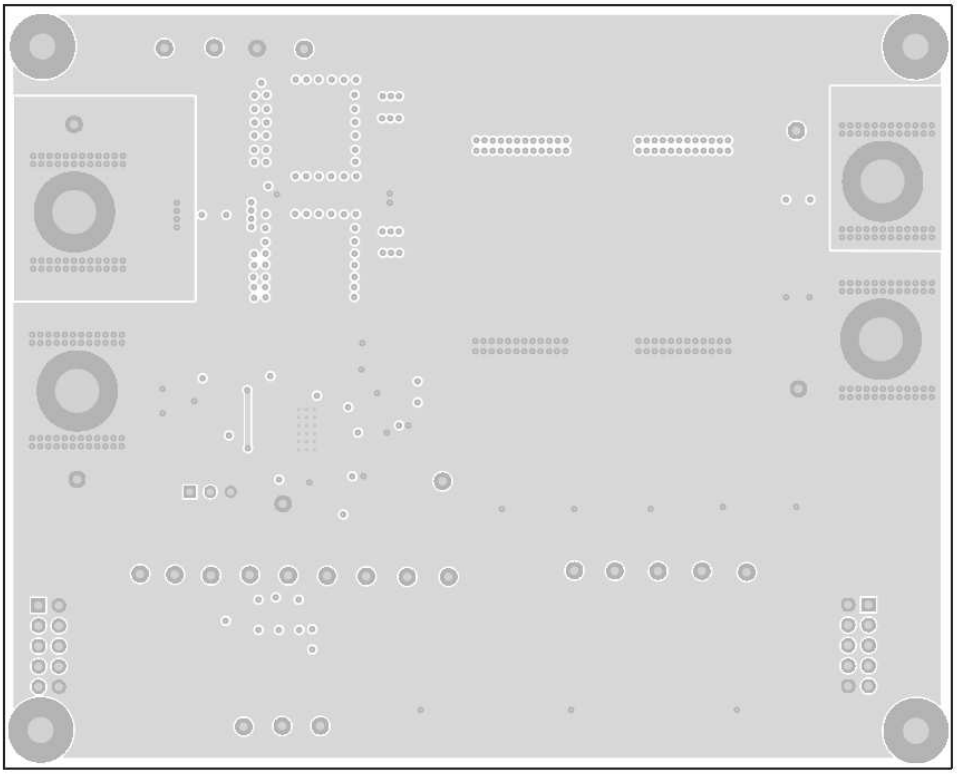


Figure 21. Internal Layer 2

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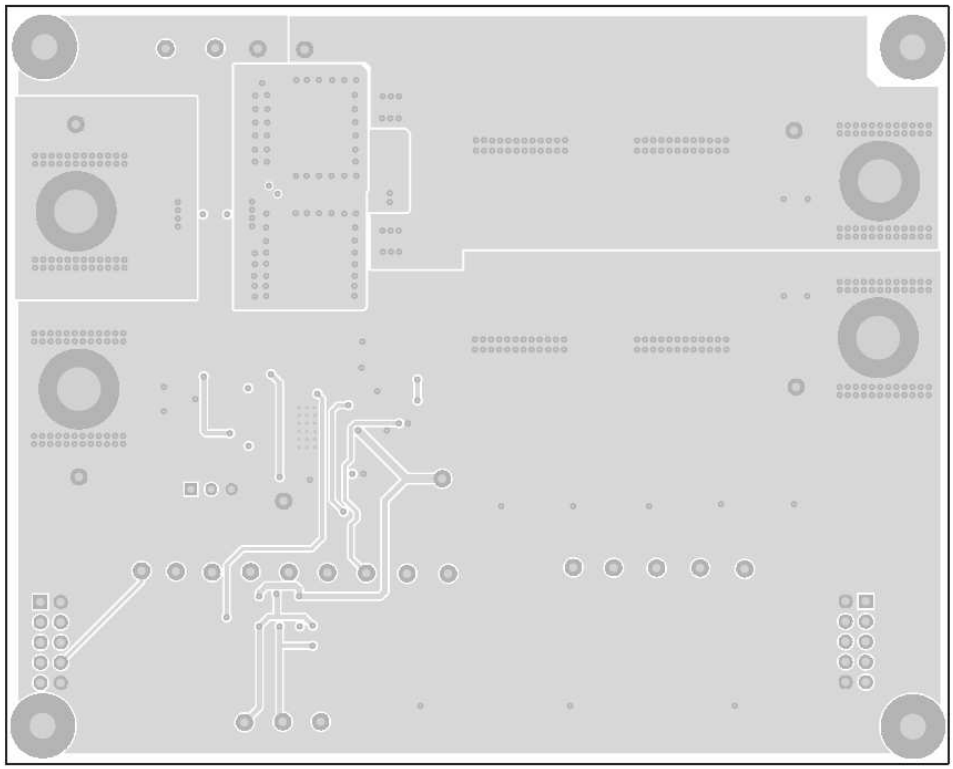


Figure 22. Bottom Layer

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9 Bill of Materials

Table 5. LM5066IEVM-626 BOM

Designator	Qty	Value	Description	Package Reference	PartNumber	Manufacturer
C1	1	0.01uF	CAP, CERM, 0.01uF, 100V, ±5%, X7R, 0805	0805	08051C103JAT2A	AVX
C2	1	1000pF	CAP, CERM, 1000pF, 100V, ±5%, X7R, 0603	0603	06031C102JAT2A	AVX
C3	1	1uF	CAP, CERM, 1uF, 100V, ±10%, X7R, 1206	1206	GRM31CR72A105KA01L	MuRata
C4, C5	2	220uF	CAP, AL, 220uF, 100V, ±20%, 0.16 ohm, SMD	MN0	EMVH101GDA221MMN0S	Nippon Chemi-Con
C7	1	0.01uF	CAP, CERM, 0.01uF, 25V, ±10%, X7R, 0603	0603	GRM188R71E103KA01D	MuRata
C8, C10	2	1uF	CAP, CERM, 1uF, 16V, ±10%, X5R, 0603	0603	C0603C105K4PACTU	Kemet
C9	1	1000pF	CAP, CERM, 1000pF, 50V, ±10%, X7R, 0603	0603	C1608X7R1H102K	TDK
D1	1	100V	Diode, Ultrafast, 100V, 0.15A, SOD-123	SOD-123	1N4148W-7-F	Diodes Inc.
D2	1	60V	Diode, TVS, Uni, 60V, 5000W, SMC	SMC	5.0SMDJ60A	Littelfuse
D3	1	80V	Diode, Schottky, 80V, 3A, SMC	SMC	B380-13-F	Diodes Inc.
H1, H2, H3, H4	4		Standoff, Hex, 0.5"L #4-40 Nylon	Standoff	1902C	Keystone
H5, H6, H7, H8	4		Machine Screw, Round, #4-40 x 1/4, Nylon, Philips panhead	Screw	NY PMS 440 0025 PH	B&F Fastener Supply
J1, J2, J3, J4	4		Standard Banana Jack, Uninsulated, 8.9mm		575-8	Keystone Electronics
J5	1		Header, 5x2, 100mil, R/A, TH	Header, 5x2, 100mil, R/A	TSW-105-08-G-D-RA	Samtec
Q1, Q3	2	100V	MOSFET, N-CH, 100V, 120A, DDPAK	DDPAK	PSMN4R8-100BSEJ	NXP Semiconductor
Q2	1	0.5V	Transistor, PNP, 150V, 0.5A, SOT-23	SOT-23	MMBT5401LT1G	ON Semiconductor
Q4	1	0.2V	Transistor, NPN, 40V, 0.2A, SOT-23	SOT-23	CMPT3904 LEAD FREE	Central Semiconductor
R1	1	10k	RES, 10k ohm, 5%, 0.1W, 0603	0603	CRCW060310K0JNEA	Vishay-Dale
R2	1	0.001	RES, 0.001 ohm, 1%, 1W, 2512	2512	ERJ-M1WTF1M0U	Panasonic
R3, R9	2	150k	RES, 150k ohm, 1%, 0.1W, 0603	0603	CRCW0603150KFKEA	Vishay-Dale
R4, R18	2	0	RES, 0 ohm, 5%, 0.1W, 0603	0603	CRCW06030000Z0EA	Vishay-Dale
R5, R6	2	4.99	RES, 4.99 ohm, 1%, 0.1W, 0603	0603	CRCW06034R99FKEA	Vishay-Dale
R7	1	10.5k	RES, 10.5k ohm, 1%, 0.1W, 0603	0603	CRCW060310K5FKEA	Vishay-Dale
R8	1	95.3k	RES, 95.3k ohm, 1%, 0.1W, 0603	0603	CRCW060395K3FKEA	Vishay-Dale
R11	1	100k	RES, 100k ohm, 5%, 0.1W, 0603	0603	CRCW0603100KJNEA	Vishay-Dale
R12	1	28.0k	RES, 28.0k ohm, 1%, 0.1W, 0603	0603	CRCW060328K0FKEA	Vishay-Dale
R13	1	11.5k	RES, 11.5k ohm, 1%, 0.1W, 0603	0603	CRCW060311K5FKEA	Vishay-Dale

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Table 5. LM5066IEVM-626 BOM (continued)

Designator	Qty	Value	Description	Package Reference	PartNumber	Manufacturer
R14	1	3.74k	RES, 3.74k ohm, 1%, 0.1W, 0603	0603	CRCW06033K74FKEA	Vishay-Dale
R15, R16, R17	3	10.0k	RES, 10.0k ohm, 1%, 0.1W, 0603	0603	CRCW060310K0FKEA	Vishay-Dale
R19, R20, R21, R22, R23	5	100	RES, 100 ohm, 1%, 0.1W, 0603	0603	CRCW0603100RFKEA	Vishay-Dale
S1	1		SWITCH TOGGLE SPDT 0.4VA 28V	6.8x23.1x8.8mm	B12AP	NKK Switches
SW1, SW2, SW3, SW4, SW5	5		Slide SW, SPDT 0.1A 50VDC	SW, 3.1x2.5x6 mm	CJS-1201TA	Copal Electronics
TP1, TP2, TP3, TP4, TP5, TP6, TP7, TP8, TP9, TP10, TP11, TP12, TP13, TP14, TP15, TP16, TP17, TP18, TP19, TP20, TP21, TP22, TP23, TP24, TP25, TP26, TP27	27	White	Test Point, TH, Miniature, White		5002	Keystone Electronics
U1	1		LM5066I/A High Voltage System Power Management and Protection IC with PMBus, PWP0028A	PWP0028A	LM5066IPWP	Texas Instruments
C6	0	1000pF	CAP, CERM, 1000pF, 100V, ±5%, X7R, 0603	0603	06031C102JAT2A	AVX
FID1, FID2, FID3	0		Fiducial mark. There is nothing to buy or mount.	Fiducial	N/A	N/A
J6	0		Connector, Receptacle, 100mil, 5x2, Gold plated, R/A, TH	5x2 R/A Header Receptacle	PPPC052LJBN-RC	Sullins Connector Solutions
R10	0	7.68	RES, 7.68 ohm, 1%, 0.1W, 0603	0603	CRCW06037R68FKEA	Vishay-Dale

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10. User has sole responsibility to ensure the safety of any activities to be conducted by it and its employees, affiliates, contractors or designees, with respect to handling and using EVMs. Further, user is responsible to ensure that any interfaces (electronic and/or mechanical) between EVMs and any human body are designed with suitable isolation and means to safely limit accessible leakage currents to minimize the risk of electrical shock hazard.
11. User shall employ reasonable safeguards to ensure that user's use of EVMs will not result in any property damage, injury or death, even if EVMs should fail to perform as described or expected.
12. User shall be solely responsible for proper disposal and recycling of EVMs consistent with all applicable federal, state, and local requirements.

Certain Instructions. User shall operate EVMs within TI's recommended specifications and environmental considerations per the user's guide, accompanying documentation, and any other applicable requirements. Exceeding the specified ratings (including but not limited to input and output voltage, current, power, and environmental ranges) for EVMs may cause property damage, personal injury or death. If there are questions concerning these ratings, user should contact a TI field representative prior to connecting interface electronics including input power and intended loads. Any loads applied outside of the specified output range may result in unintended and/or inaccurate operation and/or possible permanent damage to the EVM and/or interface electronics. Please consult the applicable EVM user's guide prior to connecting any load to the EVM output. If there is uncertainty as to the load specification, please contact a TI field representative. During normal operation, some circuit components may have case temperatures greater than 60°C as long as the input and output are maintained at a normal ambient operating temperature. These components include but are not limited to linear regulators, switching transistors, pass transistors, and current sense resistors which can be identified using EVMs' schematics located in the applicable EVM user's guide. When placing measurement probes near EVMs during normal operation, please be aware that EVMs may become very warm. As with all electronic evaluation tools, only qualified personnel knowledgeable in electronic measurement and diagnostics normally found in development environments should use EVMs.

Agreement to Defend, Indemnify and Hold Harmless. User agrees to defend, indemnify, and hold TI, its directors, officers, employees, agents, representatives, affiliates, licensors and their representatives harmless from and against any and all claims, damages, losses, expenses, costs and liabilities (collectively, "Claims") arising out of, or in connection with, any handling and/or use of EVMs. User's indemnity shall apply whether Claims arise under law of tort or contract or any other legal theory, and even if EVMs fail to perform as described or expected.

Safety-Critical or Life-Critical Applications. If user intends to use EVMs in evaluations of safety critical applications (such as life support), and a failure of a TI product considered for purchase by user for use in user's product would reasonably be expected to cause severe personal injury or death such as devices which are classified as FDA Class III or similar classification, then user must specifically notify TI of such intent and enter into a separate Assurance and Indemnity Agreement.

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General Statement for EVMs including a radio

User Power/Frequency Use Obligations: For EVMs including a radio, the radio included in such EVMs is intended for development and/or professional use only in legally allocated frequency and power limits. Any use of radio frequencies and/or power availability in such EVMs and their development application(s) must comply with local laws governing radio spectrum allocation and power limits for such EVMs. It is the user's sole responsibility to only operate this radio in legally acceptable frequency space and within legally mandated power limitations. Any exceptions to this are strictly prohibited and unauthorized by TI unless user has obtained appropriate experimental and/or development licenses from local regulatory authorities, which is the sole responsibility of the user, including its acceptable authorization.

U.S. Federal Communications Commission Compliance

For EVMs Annotated as FCC – FEDERAL COMMUNICATIONS COMMISSION Part 15 Compliant

Caution

This device complies with part 15 of the FCC Rules. Operation is subject to the following two conditions: (1) This device may not cause harmful interference, and (2) this device must accept any interference received, including interference that may cause undesired operation. Changes or modifications could void the user's authority to operate the equipment.

FCC Interference Statement for Class A EVM devices

This equipment has been tested and found to comply with the limits for a Class A digital device, pursuant to part 15 of the FCC Rules. These limits are designed to provide reasonable protection against harmful interference when the equipment is operated in a commercial environment. This equipment generates, uses, and can radiate radio frequency energy and, if not installed and used in accordance with the instruction manual, may cause harmful interference to radio communications. Operation of this equipment in a residential area is likely to cause harmful interference in which case the user will be required to correct the interference at its own expense.

FCC Interference Statement for Class B EVM devices

This equipment has been tested and found to comply with the limits for a Class B digital device, pursuant to part 15 of the FCC Rules. These limits are designed to provide reasonable protection against harmful interference in a residential installation. This equipment generates, uses and can radiate radio frequency energy and, if not installed and used in accordance with the instructions, may cause harmful interference to radio communications. However, there is no guarantee that interference will not occur in a particular installation. If this equipment does cause harmful interference to radio or television reception, which can be determined by turning the equipment off and on, the user is encouraged to try to correct the interference by one or more of the following measures:

- Reorient or relocate the receiving antenna.
- Increase the separation between the equipment and receiver.
- Connect the equipment into an outlet on a circuit different from that to which the receiver is connected.
- Consult the dealer or an experienced radio/TV technician for help.

Industry Canada Compliance (English)

For EVMs Annotated as IC – INDUSTRY CANADA Compliant:

This Class A or B digital apparatus complies with Canadian ICES-003.

Changes or modifications not expressly approved by the party responsible for compliance could void the user's authority to operate the equipment.

Concerning EVMs Including Radio Transmitters

This device complies with Industry Canada licence-exempt RSS standard(s). Operation is subject to the following two conditions: (1) this device may not cause interference, and (2) this device must accept any interference, including interference that may cause undesired operation of the device.

Concerning EVMs Including Detachable Antennas

Under Industry Canada regulations, this radio transmitter may only operate using an antenna of a type and maximum (or lesser) gain approved for the transmitter by Industry Canada. To reduce potential radio interference to other users, the antenna type and its gain should be so chosen that the equivalent isotropically radiated power (e.i.r.p.) is not more than that necessary for successful communication.

This radio transmitter has been approved by Industry Canada to operate with the antenna types listed in the user guide with the maximum permissible gain and required antenna impedance for each antenna type indicated. Antenna types not included in this list, having a gain greater than the maximum gain indicated for that type, are strictly prohibited for use with this device.

Canada Industry Canada Compliance (French)

Cet appareil numérique de la classe A ou B est conforme à la norme NMB-003 du Canada

Les changements ou les modifications pas expressément approuvés par la partie responsable de la conformité ont pu vider l'autorité de l'utilisateur pour actionner l'équipement.

Concernant les EVMs avec appareils radio

Le présent appareil est conforme aux CNR d'Industrie Canada applicables aux appareils radio exempts de licence. L'exploitation est autorisée aux deux conditions suivantes : (1) l'appareil ne doit pas produire de brouillage, et (2) l'utilisateur de l'appareil doit accepter tout brouillage radioélectrique subi, même si le brouillage est susceptible d'en compromettre le fonctionnement.

Concernant les EVMs avec antennes détachables

Conformément à la réglementation d'Industrie Canada, le présent émetteur radio peut fonctionner avec une antenne d'un type et d'un gain maximal (ou inférieur) approuvé pour l'émetteur par Industrie Canada. Dans le but de réduire les risques de brouillage radioélectrique à l'intention des autres utilisateurs, il faut choisir le type d'antenne et son gain de sorte que la puissance isotrope rayonnée équivalente (p.i.r.e.) ne dépasse pas l'intensité nécessaire à l'établissement d'une communication satisfaisante.

Le présent émetteur radio a été approuvé par Industrie Canada pour fonctionner avec les types d'antenne énumérés dans le manuel d'usage et ayant un gain admissible maximal et l'impédance requise pour chaque type d'antenne. Les types d'antenne non inclus dans cette liste, ou dont le gain est supérieur au gain maximal indiqué, sont strictement interdits pour l'exploitation de l'émetteur.

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EVMs entering Japan are NOT certified by TI as conforming to Technical Regulations of Radio Law of Japan.

If user uses EVMs in Japan, user is required by Radio Law of Japan to follow the instructions below with respect to EVMs:

1. Use EVMs in a shielded room or any other test facility as defined in the notification #173 issued by Ministry of Internal Affairs and Communications on March 28, 2006, based on Sub-section 1.1 of Article 6 of the Ministry's Rule for Enforcement of Radio Law of Japan,
2. Use EVMs only after user obtains the license of Test Radio Station as provided in Radio Law of Japan with respect to EVMs, or
3. Use of EVMs only after user obtains the Technical Regulations Conformity Certification as provided in Radio Law of Japan with respect to EVMs. Also, do not transfer EVMs, unless user gives the same notice above to the transferee. Please note that if user does not follow the instructions above, user will be subject to penalties of Radio Law of Japan.

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