AN-2160 LM5066 Evaluation Board

1 Introduction

The LM5066EVK evaluation board provides the design engineer with a fully functional intelligent monitoring and protection controller board designed for positive voltage systems. This application note describes the various functions of the board, how to test and evaluate it, and how to use the GUI design tool to change the components for a specific application. Use of the advanced telemetry and monitoring capabilities of this device requires the installation of the Intelligent Power Manager graphical user interface; however, the LM5066 is capable of acting as a hot-swap and protection circuit without any software installation. Please check the *LM5066 High Voltage System Power Management and Protection IC with PMBus* (SNVS655) data sheet for the latest software information.

2 PCB Features

- Input voltage range: 36V to 60V
- Programmable current limit: set to 16.7A (CL = GND or HIGH-Z) or 8.7A (CL = VDD)
- Q_1 power limit: 70W (typical)
- UVLO thresholds: 36V (rising) and 32V (falling)
- OVLO thresholds: 60V (rising) and 56V (falling)
- PGD thresholds: 40V (rising) and 37V (falling)
- Insertion delay: 128 ms (typical)
- Fault time-out period: 8.2 ms
- Restart time: 1.4 seconds
- PCB size: 2.3” x 3.4”

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3 Schematic

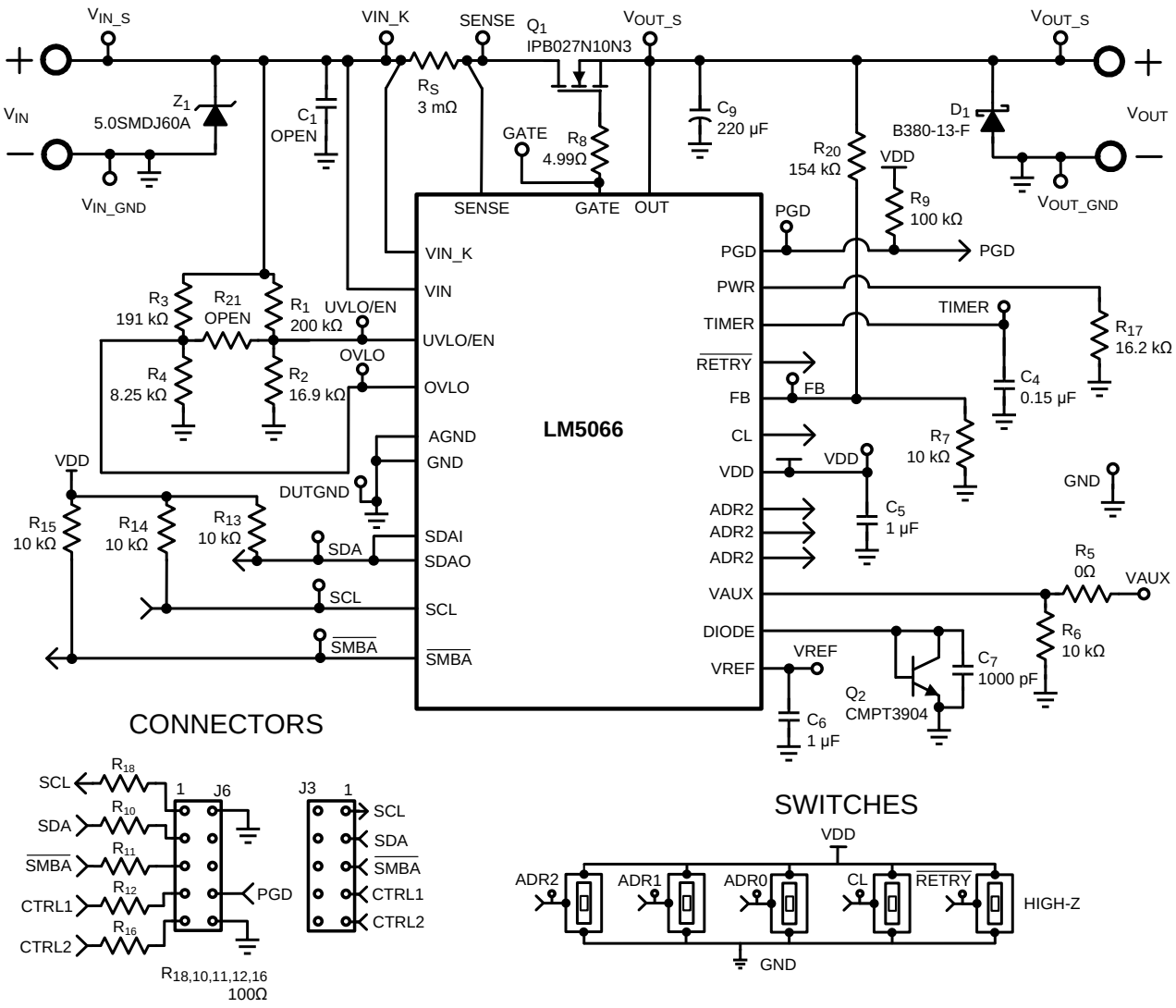


Figure 1. Evaluation Board Schematic

The schematic for the LM5066 evaluation board is shown in Figure 1. Connections to the PMBus™ interface are provided by J6. Banana connectors provide input and output connections. Pins ADR0, ADR1, and ADR2 are connected to switches that set the PMBus™ address of the device to one of 27 unique addresses. Pins $\overline{\text{RETRY}}$ and CL are also connected to switches, allowing for hardware programmability of the retry and current limit parameters, respectively. Test points are provided to connect to the input voltage, output voltage, VAUX, PGD, VREF, VDD, SENSE, GATE, FB, UVLO/EN, OVLO, SCL, SDA, $\overline{\text{SMBA}}$ and the TIMER pins.

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4 Getting Started

The LM5066 evaluation kit hardware is shown in Figure 2.

The LM5066EVK is supplied with the PMBus™ address set to 0x40 as dictated by the jumper configuration of the ADR0, ADR1, and ADR2 jumper connections.

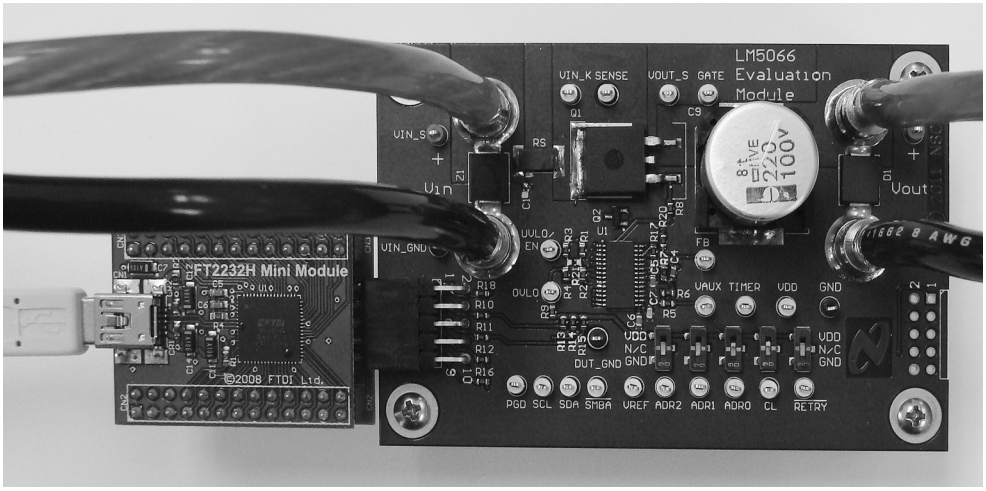


Figure 2. Connection Illustration

The first step to evaluate the telemetry features of LM5066 is to install the GUI software. The software is included on a CD in the evaluation kit and is titled PMBManager-x.x.x-xxxxxxxx.exe, where the x characters indicate the software version and build date. This file should be executed on a PC running Windows XP or later to install the software. Once the GUI software is installed the hardware should be configured as shown in Figure 2.

5 Hardware Setup Steps

1. Connect the input supply to the VIN+ and VIN- banana plugs.
2. Connect the load to the VOUT+ and VOUT- banana plugs.
3. Connect the FTDI Dongle to the 10 pin connector on the left side of the board.
4. Connect the supplied mini USB cable from the FTDI dongle to an USB port on a PC.

When the FTDI dongle is connected for the first time the user will be prompted to install the device drivers. For the most current driver installation procedure refer to the README.TXT file in the installation directory.

For a hot swap circuit to function reliably, a low inductance connection to the input supply is recommended. Its purpose is to minimize voltage transients which occur when the load current changes or is shut off. If not careful, wiring inductance in the supply lines will generate a voltage transient at the input which can exceed the absolute maximum rating of the LM5066, resulting in its destruction. To protect against such voltage transients, TVS device Z1 is provided to clamp the voltage at the input to within safe operating limits. Likewise, Schottky diode D1 is provided on the output to clamp the output from going excessively negative during short circuit events.

6 Device Evaluation

After configuring the hardware connections, apply an input voltage of 48V to the device. The current hardware configuration allows the LM5066 device to work from 36V to 60V input supply voltage; however, this guide will assume an input voltage of 48V. Launch the GUI by going to the Windows Start menu -> All Programs -> PMBManager-x.xxxxx -> PMBusManager. A pulldown menu should come up with a list of devices populated. Select the "LM5066" option as shown in Figure 3.

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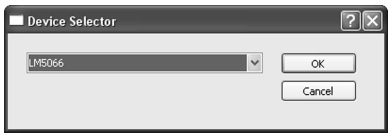


Figure 3. Device Selector

The device should be detected on the PMBus™ and the initial load screen should appear as shown in Figure 4.

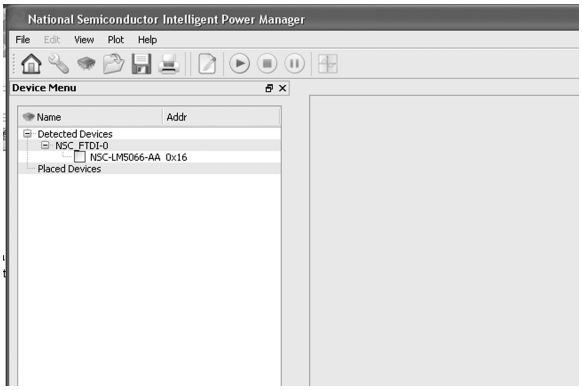


Figure 4. Initial GUI Screen

If a device is not detected, an option is provided to rescan, ignore, or exit the GUI. If the hardware is intended to be connected, check the USB connection to the PCB, FTDI connection to the evaluation module, and verify that the power is present on the evaluation PCB by measuring the voltage between the V_{IN_S} and V_{IN_GND} test points. Ignoring the detection message allows use of the integrated design tool without the hardware connected.

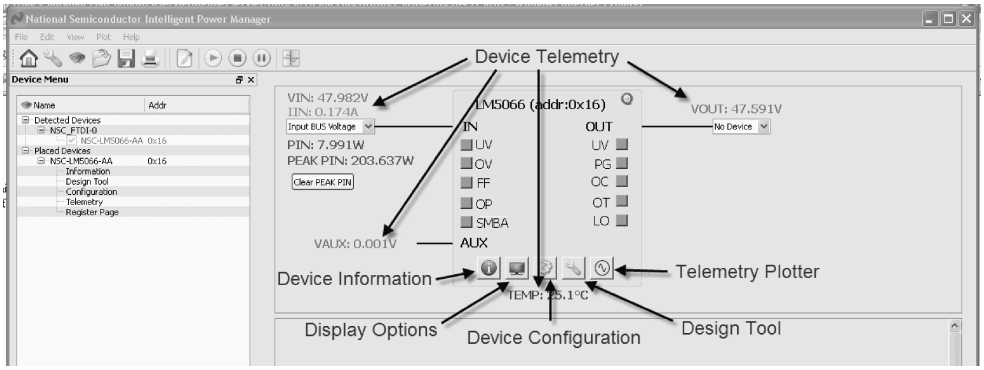


Figure 5. LM5066 Block Level Representation

Click on the detected device ID (NSC-LM5066-AA) to display a block level representation of the device as shown in Figure 5. The block level view of the device provides a display of all the telemetry data as well as most of the faults and warnings supported by the device. The faults and warnings supported are generally associated with an invalid input or output condition.

The faults shown on the left side of the block representation are generally associated with the input. These include input under-voltage (UV), input over-voltage (OV), FET Fail (FF), and input over-power (OP). The SMBus alert status, $\overline{\text{SMBA}}$, is also shown on the left side and will turn red during any warning or fault event. To facilitate the evaluation of the device, SMBus alerts are automatically cleared by the GUI.

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The faults shown on the right side of the block representation are associated with the output. These include output over-voltage (OV), power good status (PGD), output over-current (OC), and over-temperature (OT). There is also an indicator if the output is in the latched off state (LO). The device will latch the output off after the number of user programmable retries is exceeded. To clear the latched off condition, the output can be toggled off and on by the red power button located in the top right of the LM5066 block representation.

To show a repetitive update of the device telemetry and status click on the Play button at the top of the screen. The Play button starts an active telemetry log of the gathered data. Clicking the Stop button stops the telemetry collection and allows for the log file to be viewed and saved. The pause button pauses both the displaying and logging of telemetry information.

To enable/disable specific telemetry, click the Display Options button on the block representation and choose the desired telemetry to display (see Figure 6).

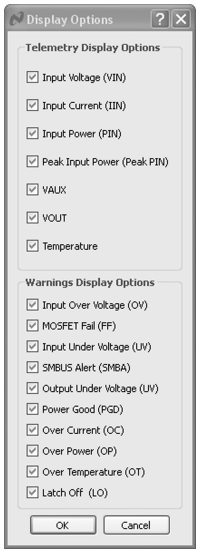


Figure 6. LM5066 Telemetry Display Options

Note that turning off the various warning options does not mask the faults from issuing an SMBus alert - it just does not display them if they occur. The device is capable of masking various faults and this functionality can be setup in the device configuration panel.

7 GUI Event Log

A GUI event log is provided to keep track of GUI configuration changes and device fault events. To display the event log select View from the main menu bar and then View Event Log. The event log will appear on the left side of the main GUI window. The event log can be detached and expanded if desired by left clicking on the event log window and dragging window with the mouse to the desired location.

8 Plotting Telemetry Data

To enable telemetry data plots click on the sine wave button located on the LM5066 block representation. After enabling the telemetry, a prompt will appear requesting entry of the GUI sample rate, plot rate, and plot depth. For most cases the default rates and depths will be acceptable. The plotting tool allows the user to select the desired data to be plotted. Up to 2 different parameters may be plotted at the same time as shown in Figure 7.

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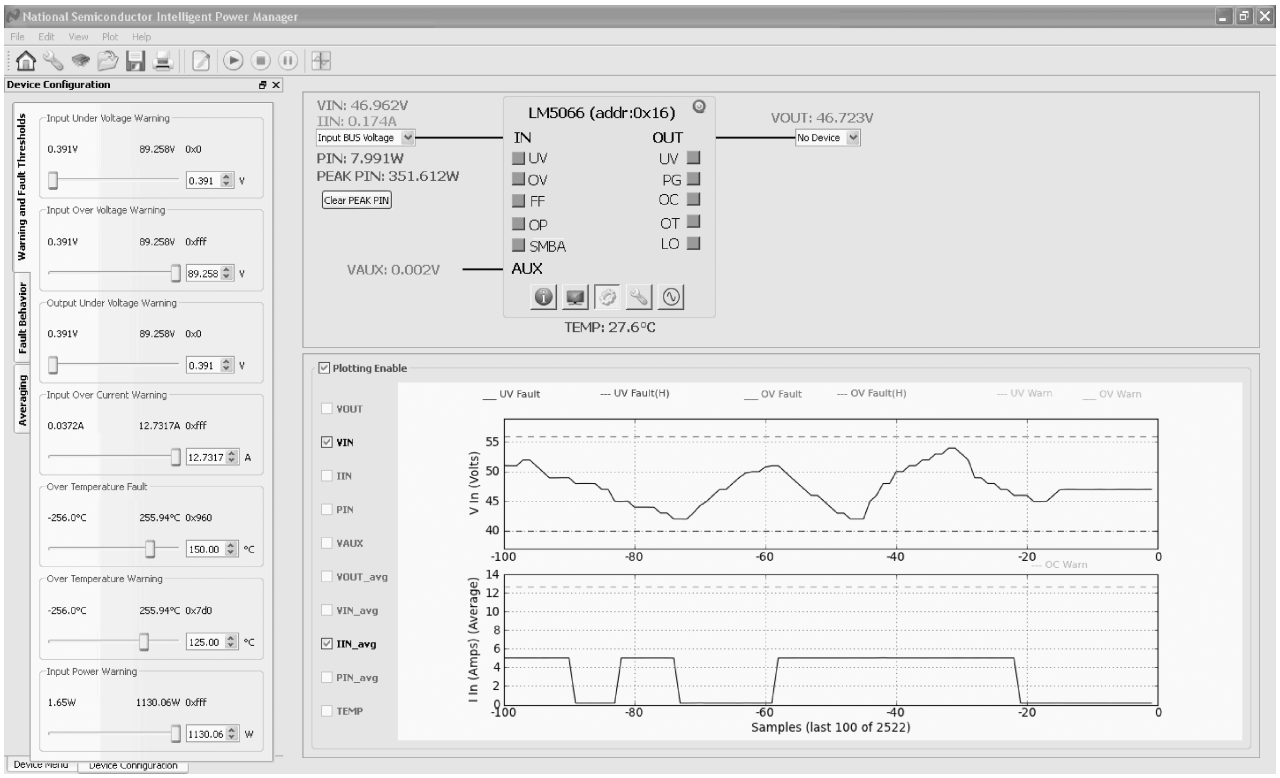


Figure 7. LM5066 GUI with Telemetry Plotting Tool Enabled

Telemetry data is plotted as a black line that continually updates as the device is queried. In addition to the telemetry data, the relevant warning and fault thresholds are also plotted. Warning thresholds are shown as orange lines while fault thresholds are shown in red and blue.

From the Plot menu option in the main menu bar, the user can disable the plotting grid as well as the warning and fault lines.

9 Configuring the LM5066 Device

Warning Thresholds, Temperature Fault Threshold, Protection Ranges, Fault Masking, and Averaging can be configured in the Device Configuration panel. This panel, shown in Figure 8, is enabled by clicking the gear button shown on the LM5066 block representation.

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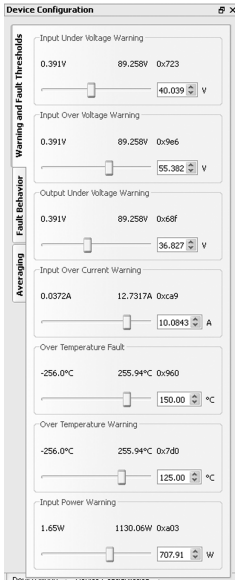


Figure 8. Device Configuration Panel

The Warning and Fault Threshold tab allows configuration of the input under-voltage, input over-voltage, output under-voltage, input over-current, input power, and over temperature warnings. This tab also allows adjustment of the over-temperature fault threshold. Fault threshold for the input over- and under-voltage, current limit, power limit, and power good are set by the hardware design. Decimal values for the thresholds are shown in the text box located to the right of the slider bar. Above the decimal values setting is the value of the setting in hexadecimal, which can be useful when developing software for this device.

The fault behavior tab allows the user to set the device fault configuration and fault masking. The fault configuration section allows the user to set the number of retries, as well as the circuit breaker and current limit thresholds. The number of retries can be set by the $\overline{\text{RETRY}}$ pin to be infinite or latched off. Through software, the number of retries can be set to 0 (latch-off), 1, 2, 4, 8, 16 or infinite. The software settings are independent of the hardware settings; however, if the power is cycled the device will default to values dictated by the hardware. Current limit power-up values are also set by the hardware. The values for current limit can be set to either 26 mV (CL = VDD) or 50 mV (CL = GND). The circuit breaker threshold can also be set in software to either 1.9 times or 3.9 times the current limit value through the software. Fault masking is possible for many of the device fault conditions. Fault conditions allow masking of both the MOSFET response and the SMBus alert signal. Note that if a fault occurs repeatedly while the MOSFET is masked, damage to the MOSFET may result. This feature is allowed primarily for debug purposes. Faults that do not shut off the MOSFET, and only issue a SMBus alert, will also allow masking of the alert. Note the power-up default setting for the Power Good signal is to mask the SMBus alert, in order to ensure that SMBus alert is not asserted immediately after power-up.

For convenience, the Device Configuration Panel can be undocked by holding down the left mouse button while the cursor is at the top of the panel and dragging it to where you would like it to be placed.

10 Customizing the Design

The GUI assumes the hardware configuration is set to default LM5066 evaluation board configuration. If any of the components are changed, the device hardware configuration needs to be updated in the Design Tool section. To open the design tool, click the Wrench button located on the LM5066 block representation which will open the window displayed in Figure 9.

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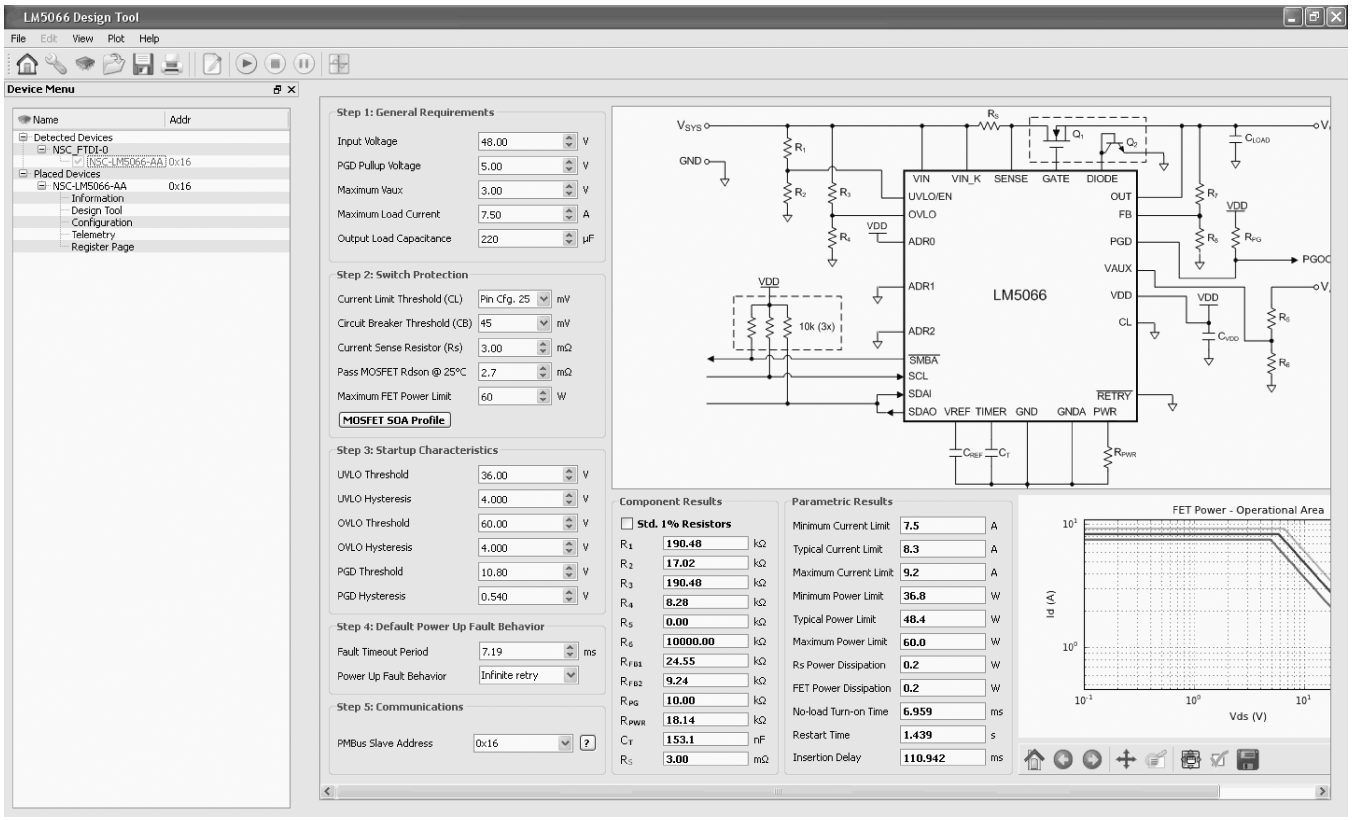


Figure 9. LM5066 Design Tool

Design inputs are keyed in on the left side following steps 1 though 5. General operating conditions should be entered in step 1 of the design tool. These inputs help set bounds on the startup time and application voltage ranges.

Step 2 allows the user to tailor the MOSFET protection features to be specific to the target application. Current limit is pin-configurable and software configurable, and circuit breaker is software-configurable. If CL switch is used to set the current limit, make sure the GUI selection matches the pin-configurable CL bit setting on the board. By clicking on the MOSFET SOA Profile button the user can select SOA data from several popular MOSFETs or enter the SOA data for the desired MOSFET. The resistor R_{PWR} can then be calculated to keep Q_1 within its SOA profile.

Step 3 allows the user to select the under- and over-voltage lockout values (UVLO/OVLO), and power good (PGD) thresholds. Note that with the correct values for R1 - R4, and RFB1 and RFB2 installed, the LM5066 will indicate a fault condition when the input and/or output voltages are outside of their programmed range.

Step 4 allows the user to set the fault time-out period and the fault response. The fault time-out should be set to be below the MOSFET SOA data for a given time. For example, if a design is done to adhere to the 10 ms pulsed MOSFET SOA data, the desired fault time-out must be less than 10ms. The fault time-out time entered will set the value for C_T. It also sets the insertion delay and fault retry delay. The initial power up retry behavior is also selected in this design step. Make sure to change the $\overline{\text{RETRY}}$ switch to match the design tool schematic when changing the default retry setting.

In Step 5 the user enters the desired PMBus address. Note changing the PMBus address of the device in step 5 does not change the device address, but shows how the address pins of the device need to be configured to achieve a desired address. Once the ADR pin switches are configured for a particular address, power to the device needs to be cycled and the GUI restarted in order for the new address to take affect.

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When invalid or incorrect inputs are given to the design tool, text associated with the faulty input will turn red. Positioning the mouse cursor over the red text will give additional information about any design conflict.

Component and parametric results are shown to the right as well as the LM5066 safe operational area (SOA) chart. The SOA chart shows the minimum, typical, and maximum SOA protection areas for a given design. For a robust design, the SOA of the MOSFET used should be above the MAX protection SOA line for all operating areas.

Once a design is complete, the design should be saved by selecting the File menu, and then Save. Once the hardware is modified to match the design the GUI should be restarted and the hardware configuration file loaded right after the device is detected and placed. If the values in the design tool are different than the values on the board, erroneous telemetry and fault data will be reported by the GUI. To return to the block view of the device, press the Home buttonlocated at the far left in the menu bar.

The design tool is also useful to calculate the PMBus coefficients. With the correct value for current sense resistor (R_S) the tool will calculate the correct coefficients to scale the raw telemetry data. The coefficients can be viewed by selecting View from the main menu bar, and then selecting the PMBus Coefficient Editor. When the PMBus Coefficient Editor is opened, press the Get All button to show the currently used coefficients.

If desired the results presented by the design tool can be calculated by hand using the equations provided in the datasheet. However, note the design tool calculates parameters factoring in worst case tolerances, while the equations in the datasheet are based on typical thresholds.

11 Theory of Operation

The LM5066 provides intelligent control of the power to a load from a live power source. The three primary functions of the device are to limit in-rush current during turn-on, monitor the load current for faults during normal operation, and to provide system telemetry for the following parameters: Input Voltage (VIN), Input Current (IIN), Input Power (PIN), Output Voltage (VOUT), Auxilliary Voltage (VAUX), and Temperature. Additional functions include under- and over-voltage lock-outs (UVLO/OVLO) to ensure voltage is supplied to the load only when the system input voltage is within a specified range, power limiting of the series pass MOSFET (Q_1) during turn-on, and a Power Good logic output (PGD) to indicate the output voltage status.

Upon applying the input voltage to the LM5066, Q_1 is initially held off for the insertion delay (128 ms) to allow ringing and transients on the input to subside. At the end of the insertion delay, if the input voltage at V_{IN} is above the UVLO threshold, Q_1 is turned on in a controlled manner to limit the in-rush current.

The LM5066 utilizes two methods to limit in-rush currents at startup. For the input voltage range and sense resistor on this board, the in-rush current will be limited by the MOSFET power limit method. The power limit method controls the input current such that a constant power is dissipated across Q_1 during startup. At the onset of the startup period, V_{IN} = 48V and V_{OUT} = 0V. Q_1's power dissipation is limited to a peak value set by R_{PWR} (70W) by monitoring its drain current (the voltage across R_S) and its drain-to-source voltage. Their product is maintained constant by controlling the drain current as the drain-to-source voltage decreases (as the output voltage increases). This is shown in the constant power portion of Figure 10 where the drain current is increasing to I_{LIM}.

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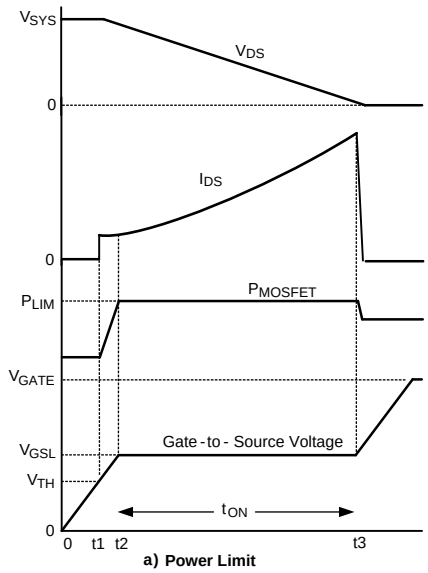


Figure 10. Power Up Using Power Limit

If the power across Q_1 does not exceed the programmed power limit, the LM5066 will also limit the drain current to the current limit value determined by the sense resistance and the selected current limit voltage threshold, 26 mV or 50 mV. The current limit will be maintained constant as the output voltage continues to increase. During the current limit period, the voltage at the TIMER pin will be rising. If the TIMER voltage reaches 3.9V before the current limit time has expired, the device will shut down and retry according to the programmed retry configuration. If the TIMER does not expire, the output voltage will rise and the drain current needed to charge the output capacitance will reduce. The output voltage will continue to rise towards the the input voltage (V_{DS} decreases to near zero), and the drain current then reduces to a value determined by the load. Q_1's gate-to-source voltage then increases to its final value. The circuit is now in normal operation mode.

Monitoring of the load current for faults during normal operation is accomplished using the current limit circuit described above. If the load current increases to 8.67 Amps (26 mV across R_S), Q_1's gate is controlled to prevent the current from increasing further. When current limiting takes effect, the fault timer limits the duration of the fault. At the end of the fault time-out period Q_1 is shut off, denying current to the load. The LM5066 then initiates a restart every 1.4 seconds. The restart consists of turning on Q_1 and monitoring the load current to determine if the fault is still present. After the fault is removed, the circuit powers up to normal operation at the next restart. If the retry setting is changed to a limited number of retrys, it will stop retrying after the programmed number of retrys occur, and keep Q_1 shut off until UVLO/EN is toggled, or the output is turned off, and then on via PMBus.

In a sudden overload condition (e.g. when the output is shorted to ground), it is possible the current could increase faster than the response time of the current limit circuit. In this case, the circuit breaker sensor shuts off Q_1's gate rapidly when the voltage across R_S reaches 50 mV. When the current reduces to the current limit threshold, the current limit circuitry then takes over.

The PGD logic level output is low during turn-on and switches high when the output voltage at OUT is above 40V. PGD switches low when the voltage at OUT is below 37V. The high level voltage at PGD can be any appropriate voltage up to +80V and can be higher or lower than the voltages at VIN and OUT.

The UVLO thresholds are set by resistors R1 and R2, the OVLO thresholds are set by R3 and R4, and the PGD thresholds are set by resistors RFB1 and RFB2 (R_{20} and R_7 on the board). Internal current sources at the UVLO, OVLO, and FB pins provide hysteresis for these thresholds.

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12 Fault Detection & Restart

If the load current increases to the fault level (the current limit threshold of 8.67A), an internal current source charges the timing capacitor at the TIMER pin. When the voltage at the TIMER pin reaches 3.9V, the fault time-out period is complete and the LM5066 shuts off Q_1. The restart sequence then begins, consisting of seven cycles at the TIMER pin between 3.9V and 1.1V, as shown in Figure 11. When the voltage at the TIMER pin reaches 0.3V during the eighth high-to-low ramp, Q_1 is turned on. If the fault is still present, the fault time-out period and the restart sequence repeat.

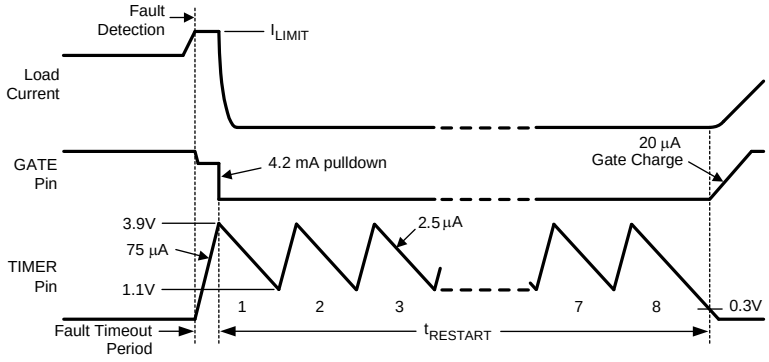


Figure 11. Fault Time-out and Restart Sequence

The waveform at the TIMER pin can be monitored at the TIMER test point. On this evaluation board, the initial fault time-out period is 8.2 ms and the restart time is 1.4 seconds.

13 UVLO and OVLO Input Voltage Threshold

Programming the UVLO threshold sets the minimum system voltage to enable Q_1. If VIN is below the UVLO thresholds, Q_1 is switched off, denying power to the load. Programmable hysteresis is adjustable by changing the value of R1.

The UVLO thresholds are set with two resistors (R1, R2) as shown in Figure 12 .

The OVLO threshold sets the maximum voltage that can be present on the input before the device turns off the series pass device. The OVLO threshold is set with the two resistors (R3, R4). The hysteresis voltage is set by the internal 21 µA current source and the value of R3.

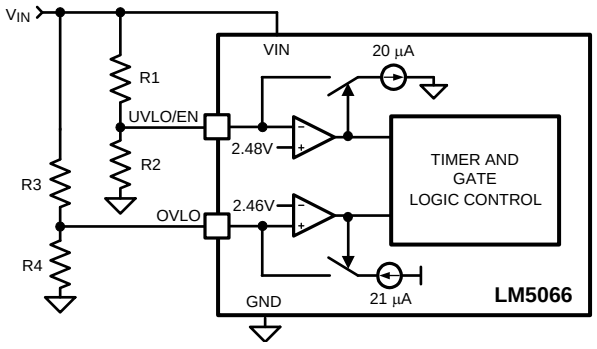


Figure 12. Programming the UVLO Threshold

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14 PGD and FB Pins

During turn-on, the Power Good pin (PGD) will not be able to pull low until the voltage at VIN increases above ≅1.6V. Pulling the PGD pin up to VDD will keep the PGD pin low during this region because VDD does not turn on until VIN increases above ≅7V. When the voltage at the board's output pin increases above 40V (typ), PGD switches high. PGD switches low when the output voltage decreases below 37V (typ). Additionally, PGD switches low if the UVLO/EN pin is taken below its threshold regardless of the output voltage.

The output voltage threshold for the PGD pin is set with two resistors (RFB1, RFB2 on the GUI, R_{20} and R_7 on the board) at the FB pin.

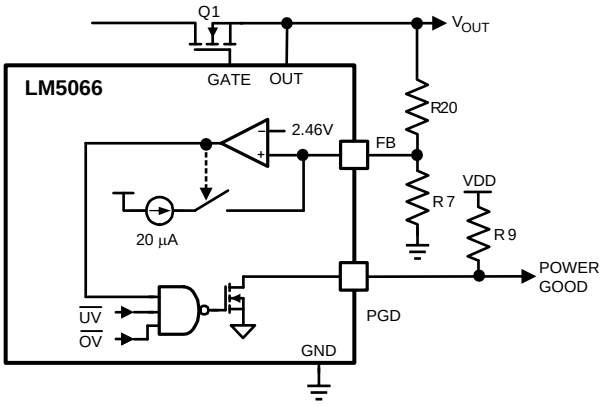


Figure 13. Programming the PGD Threshold

A pull-up voltage and pull-up resistor are required at PGD as shown in Figure 13. The pull-up voltage (VPGD) can be as high as 80V with transient capability to 100V and can be higher or lower than the voltages at VIN and OUT.

15 Shutdown

With the circuit in normal operation, the LM5066 can be shutdown by grounding the UVLO/EN pin or by clicking the ON/OFF button on the LM5066 block representation in the GUI.

16 Board Layout and Probing Cautions

Refer to the product datasheet for detailed layout guidelines. For most applications the layout of this evaluation module as detailed in the PC Board Layout section of this document should be sufficient to provide a working solution with accurate telemetry. The following should be kept in mind when the board is powered:

1. Use CAUTION when probing the circuit to prevent injury as well as possible damage to the circuit.
2. At maximum load current (16.7A), the wire size and length used to connect the power source and the load become very important. The wires connecting this evaluation board to the power source should be a heavy gauge and twisted together to minimize inductance in those leads. The same applies for the wires connecting this board to the load. This recommendation is made in order to minimize high voltage transients from occurring when the load current is shut off.
3. A 60V TVS diode located as close as possible to the LM5066 VIN and GND pins provides the critical function of clamping inevitable input voltage overshoot when Q_1 turns off at high currents. If operation above 60V is required, the TVS will need to be replaced with a TVS rated at a higher standoff voltage. Always verify the TVS by performing a worst-case current limit at the maximum input voltage and monitoring the resulting input voltage surge. The TVS should be able to clamp the input below 100V in all cases.
4. The ground points for the UVLO/EN, OVLO and FB resistor networks are tied directly to a via where the LM5066 is conneced to the ground plane. The ground for the temperature sensing transistor, Q2, is also tied back to the LM5066 ground.
5. Input capacitor, C1, local to the LM5066 is not populated due to the input current spike to charge this

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capacitor. Populating C1 will result in reduced VIN voltage slew rates at the expense of increased inrush current during a hot insertion.

17 Performance Characteristics

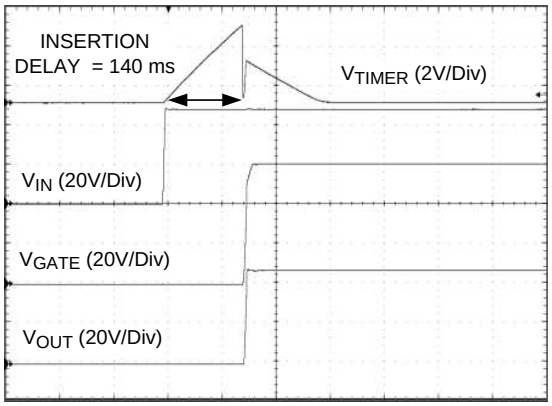


Figure 14. Insertion Time Delay (100 ms/DIV)

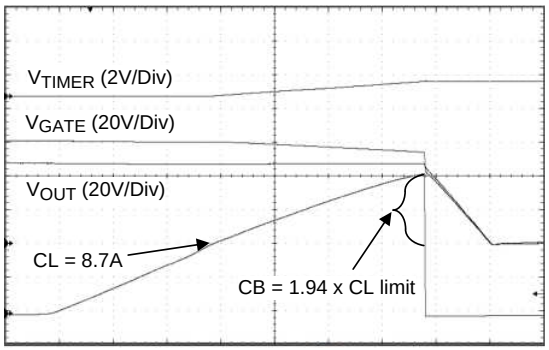


Figure 15. Circuit Breaker Response (500 µs/DIV)

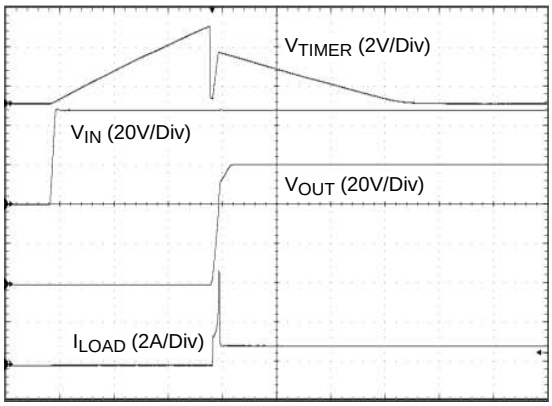


Figure 16. Turn-On Sequence into a 4Ω Load (50 ms/DIV)

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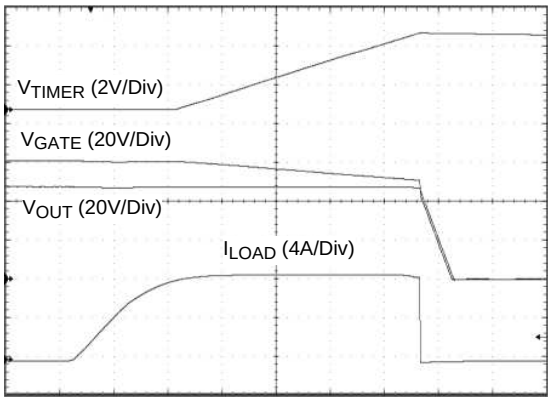


Figure 17. Initial Fault Timeout (2 ms/DIV)

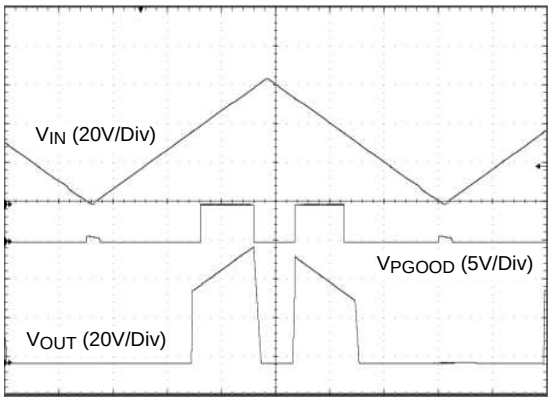


Figure 18. PGD Power up/Power down behavior (200 ms/DIV)

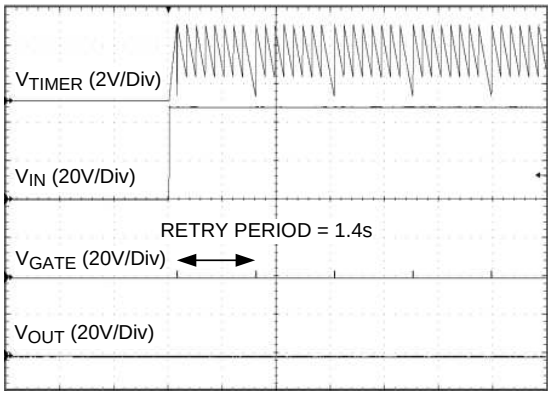


Figure 19. Restart Timing (1 s/DIV)

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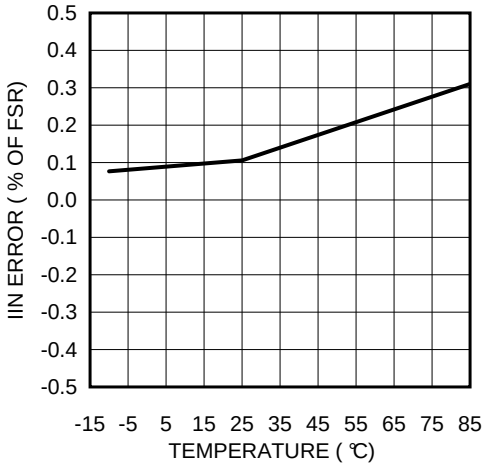


Figure 20. IIN Error vs Temperature

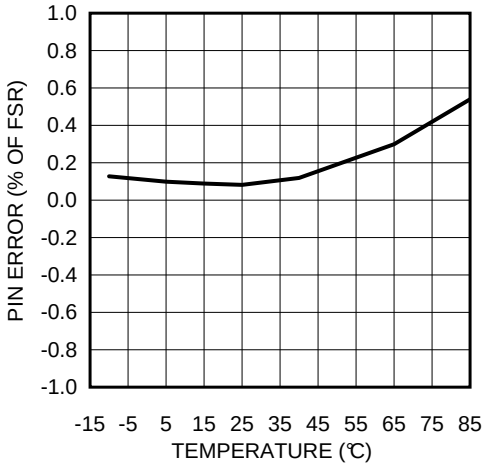


Figure 21. PIN Error vs Temperature

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18 Bill of Materials

Designator	Value	Description	Manufacturer	Part Number	Qty.
U1		HOT SWAP CONTROLLER	Texas Instruments	LM5066	1
C4	0.15 µF	CAP, CERM, 0.15uF, 10V, +/-10%, X7R, 0603	MuRata	GRM188R71A154KA01D	1
C5, C6	1 µF	CAP, CERM, 1uF, 16V, +/-10%, X5R, 0603	Kemet	C0603C105K4PACTU	2
C7	1000 pF	CAP, CERM, 1000pF, 50V, +/-10%, X7R, 0603	TDK	C1608X7R1H102K	1
C9	220 µF	CAP, AL, 220uF, 100V, +/-20%, SMD	Nippon Chemi-Con	EMVE101GDA221MLN0S	1
D1		Diode, Schottky, 80V, 3A, SMC	Diodes Inc.	B380-13-F	1
Q1		MOSFET N-CH 100V 120A TO263-3	Infineon Technologies	IPB027N10N3 G	1
Q2		Transistor, NPN, 40V, 0.2A, SOT-23	Central Semiconductor	CMPT3904 LEAD FREE	1
R1	200 kΩ	RES, 200k ohm, 1%, 0.1W, 0603	Vishay-Dale	CRCW0603200KFKEA	1
R3	191 kΩ	RES, 191k ohm, 1%, 0.1W, 0603	Vishay-Dale	CRCW0603191KFKEA	1
R2	16.9 kΩ	RES, 16.9k ohm, 1%, 0.1W, 0603	Vishay-Dale	CRCW060316K9FKEA	1
R4	8.25 kΩ	RES, 8.25k ohm, 1%, 0.1W, 0603	Vishay-Dale	CRCW06038K25FKEA	1
R5	0 Ω	RES, 0 ohm, 5%, 0.1W, 0603	Vishay-Dale	CRCW06030000Z0EA	1
R6,R7, R13, R14, R15	10.0 kΩ	RES, 10.0k ohm, 1%, 0.1W, 0603	Vishay-Dale	CRCW060310K0FKEA	5
R8	4.99 Ω	RES, 4.99 ohm, 1%, 0.1W, 0603	Vishay-Dale	CRCW06034R99FKEA	1
R9	100 kΩ	RES, 100k ohm, 5%, 0.1W, 0603	Vishay-Dale	CRCW0603100KJNEA	1
R10, R11, R12, R16, R18	100 Ω	RES, 100 ohm, 1%, 0.1W, 0603	Vishay-Dale	CRCW0603100RFKEA	5
R17	16.2 kΩ	RES, 16.2k ohm, 1%, 0.1W, 0603	Vishay-Dale	CRCW060316K2FKEA	1
R20	154 kΩ	RES, 154k ohm, 1%, 0.1W, 0603	Vishay-Dale	CRCW0603154KFKEA	1
RS	3 mΩ	RES .003 OHM 1W 1% 2512 SMD	Vishay-Dale	WSL25123L000FEA	1
SW1, SW2, SW3, SW4, SW5		SWITCH SLIDE SPDT SMD J-LEAD 50 V, 100 mA	Copal	CJS-1201TA	5
Z1		DIODE TVS 60V 5000W 5% UNI SMD	Littlefuse	5.0SMDJ60A	1

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19 PC Board Layout

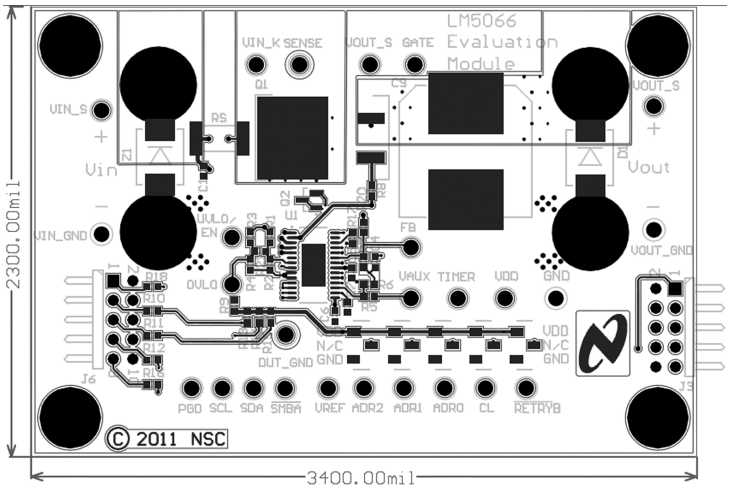


Figure 22. Board Top Layer (planes outlined in grey)

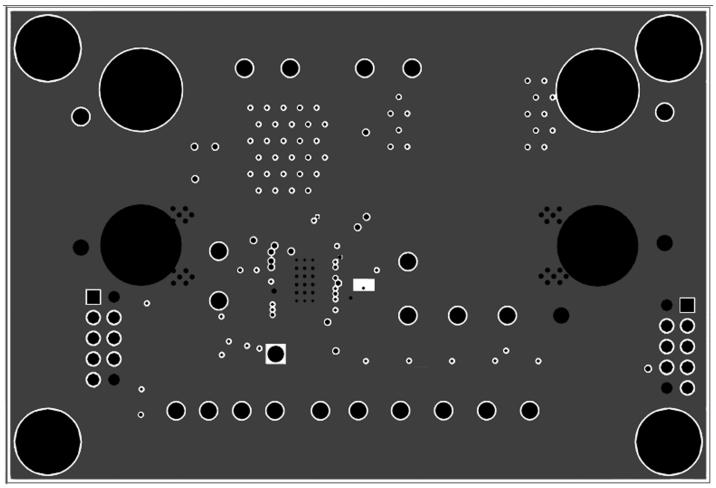


Figure 23. Board Mid Layer 1 (ground plane)

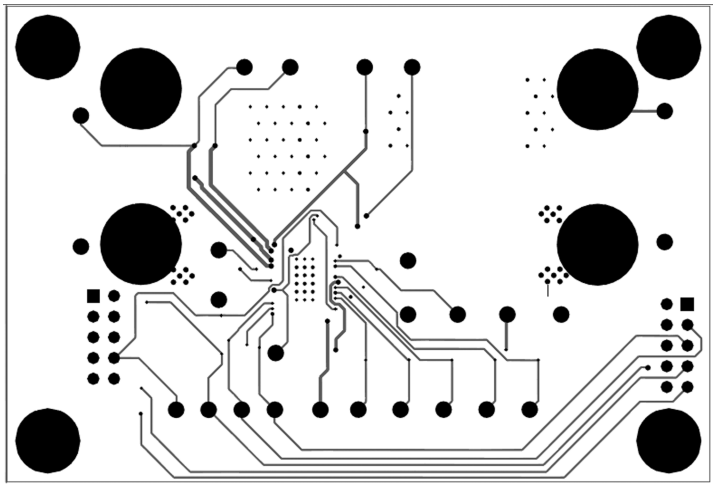


Figure 24. Board Mid Layer 2

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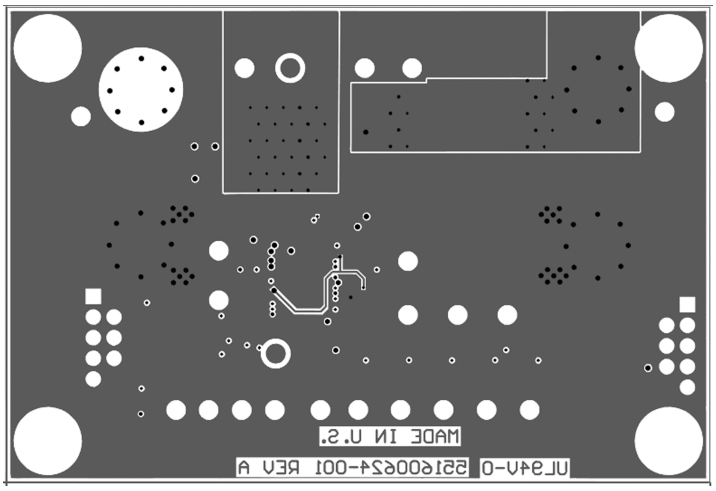


Figure 25. Board Bottom Layer (viewed from top)

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