LM5064 Negative Voltage System Power Management and Protection IC with PMBus

Check for Samples: LM5064

FEATURES

- **Input Voltage Range: -10V to -80V**
- **Programmable 26 mV or 50 mV Current Limit Threshold with Power Limiting (MOSFET Power Dissipation Limiting)**
- **Real Time Monitoring of V_{IN}, V_{OUT}, I_{IN}, P_{IN}, V_{AUX} with 12-Bit Resolution and 1 kHz Sampling Rate**
- **Configurable Circuit Breaker Protection for Hard Shorts**
- **Configurable Under-Voltage and Over-Voltage Protection**
- **Remote Temperature Sensing with Programmable Warning and Shutdown Thresholds**
- **Detection and Notification of Damaged MOSFET Condition**
- **Power Measurement Accuracy: ±4.5% Over Temperature**
- **True Input Power Averages Dynamic Power Readings**
- **Averaging of V_{IN}, I_{IN}, P_{IN}, and V_{OUT} Over Programmable Interval Ranging from 0.001 to 4 Seconds**
- **Programmable WARN and FAULT Thresholds with $\overline{\text{SMBA}}$ Notification**
- **Black Box Capture of Telemetry Measurements and Device Status Triggered by WARN or FAULT Condition**
- **I^2C/SMBus Interface and PMBus Compliant Command Structure**
- **Full Featured Application Development Software**
- **HTSSOP-28 Package**

APPLICATIONS

- **Base Station Power Distribution Systems**
- **Intelligent Solid State Circuit Breaker**
- **-24V/-48V Industrial Systems**

DESCRIPTION

The LM5064 combines a high performance hot swap controller with a PMBus™ compliant SMBus/I^2C interface to accurately measure, protect and control the electrical operating conditions of systems connected to a backplane power bus. The LM5064 continuously supplies real-time power, voltage, current, temperature and fault data to the system management host via the SMBus interface.

The LM5064 control block includes a unique hot swap architecture that provides current and power limiting to protect sensitive circuitry during insertion of boards into a live system backplane, or any other "hot" power source. A fast acting circuit breaker prevents damage in the event of a short circuit on the output. The input under-voltage and over-voltage levels and hysteresis are configurable, as well as the insertion delay time and fault detection time. A temperature monitoring block on the LM5064 interfaces with a low-cost external diode for monitoring the temperature of the external MOSFET or other thermally sensitive components. The PGD output provides a fast indicator when the input and/or output voltages are outside their programmed ranges.

The LM5064 monitoring circuit computes both the real-time and average values of subsystem operating parameters (V_{IN}, I_{IN}, P_{IN}, V_{OUT}) as well as the peak power. Accurate power averaging is accomplished by averaging the product of the input voltage and current. A black box (Telemetry/Fault Snapshot) function captures and stores telemetry data and device status in the event of a warning or a fault.

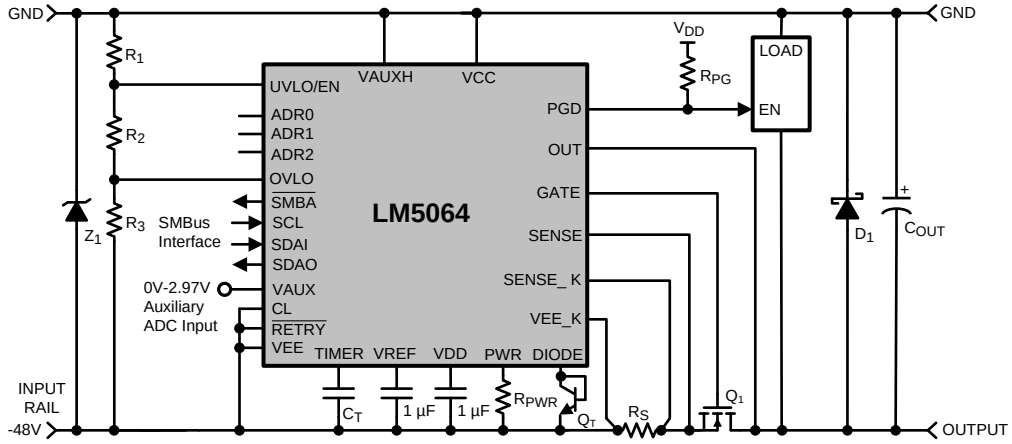
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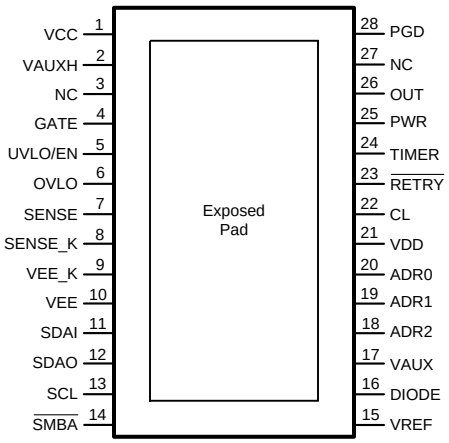
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Typical Application Circuit



Connection Diagram



Top View
28-Lead HTSSOP
9.7 mm × 4.4 mm × 0.9 mm
PWP0028A Package

PIN DESCRIPTIONS

Pin#	Name	Description
1	VCC	Positive supply input. Connect the VCC pin to the positive voltage rail.
2	VAUXH	High voltage auxiliary input. VCC with respect to VEE is measured by connecting the VAUXH pin to the VCC rail.
3	NC	No connect. This pin is not internally connected and should not be connected to any signal or power rail.
4	GATE	MOSFET gate control signal for fault control of the output. The GATE pin is clamped to VEE through a 12.6V internal zener diode.
5	UVLO/EN	Under-voltage lockout threshold input. Connecting the UVLO pin to a resistor divider from VCC to VEE will set the under-voltage lockout threshold. After the UVLO pin voltage falls below 2.48V, an internal 20 µA current source is switched to provide a user settable hysteresis. The UVLO pin can be toggled directly to act as a precision enable. After the UVLO threshold voltage is exceeded, the output voltage will begin to transition to V_{VEE} as the GATE pin supplies 52 µA to turn on the MOSFET.
6	OVLO	Over-voltage lockout threshold input. Connecting the OVLO pin to a resistor divider from VCC to VEE will set the over-voltage lockout threshold. After the OVLO pin voltage exceeds 2.47V, an internal 21 µA current source is switched to provide a user settable hysteresis. If the OVLO threshold is exceeded, the MOSFET will be immediately disabled to protect the output.

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PIN DESCRIPTIONS (continued)

Pin#	Name	Description
7	SENSE	Current limit and power limit sense input. SENSE provides a direct connection to the MOSFET source and current sense resistor voltage to detect current limit and power limit events. This unfiltered signal will allow the LM5064 to quickly respond during over-current or over-power events.
8	SENSE_K	Current telemetry Kelvin sense positive input. SENSE_K is the positive input to a precision differential current sense amplifier. Connecting SENSE_K to the positive terminal of the current sense resistor will provide an accurate current telemetry signal.
9	VEE_K	Current telemetry Kelvin sense negative input. The VEE_K pin is the negative input to a precision differential current sense amplifier. Connecting VEE_K to the negative terminal of the current sense resistor will provide an accurate current signal.
10	VEE	Negative supply input. Connect the VEE pin to the negative voltage supply rail. Use a small ceramic bypass capacitor (0.1 µF) from the VEE pin to the VCC pin to suppress transient current spikes when the load switch is turned off. The operational voltage range for the VEE pin is -10V to -80V. The VEE pin absolute maximum voltage is -100V.
11	SDAI	SMBus data input. The SDAI pin is designed to read PMBus commands using the SMBus communication protocol. SDAI can be connected to SDAO if desired.
12	SDAO	SMBus data output. The SDAO pin is designed to transmit PMBus commands using the SMBus communication protocol. SDAO can be connected to SDAI if desired.
13	SCL	SMBus clock input.
14	$\overline{\text{SMBA}}$	SMBus alert. This pin is connected to an open drain MOSFET which pulls the pin to VEE if a fault is detected.
15	VREF	Internal ADC reference output. Connect a 1 µF capacitor from the VREF pin to VEE to filter noise imposed on the internal reference output.
16	DIODE	Positive diode sense. The DIODE pin should be connected to the anode of a diode whose cathode is connected to VEE for temperature monitoring.
17	VAUX	Auxiliary pin allows voltage telemetry from an external source. Full scale input of 2.97V.
18	ADR2	Address pin 2. The address pins can be connected to VDD, VEE, or left open to set the PMBus address of the LM5064.
19	ADR1	Address pin 1 The address pins can be connected to VDD, VEE, or left open to set the PMBus address of the LM5064.
20	ADR0	Address pin 0. The address pins can be connected to VDD, VEE, or left open to set the PMBus address of the LM5064.
21	VDD	Internal 4.9V sub-regulator output. VDD must be connected and closely coupled to VEE through a 1 µF ceramic bypass capacitor.
22	CL	Current limit threshold input. The LM5064 detects current limit events by sensing the voltage across a series resistor. The current limit threshold is set to 26 mV by connecting CL to VDD and 50 mV when CL is connected to VEE.
23	$\overline{\text{RETRY}}$	Retry selction pin. Connecting $\overline{\text{RETRY}}$ to VDD sets the LM5064 to lockout after a fault condition is detected. Connecting $\overline{\text{RETRY}}$ to VEE sets the LM5064 to retry after a fault condition.
24	TIMER	Timing input. Set the insertion time delay and the fault timeout period by connecting a capacitor from the TIMER pin to VEE. The restart time is also set through the TIMER pin when in restart mode.
25	PWR	Power limit input. Connecting a resistor from PWR to VEE sets the maximum power dissipation allowed in the external MOSFET switch. Power is calculated using the current information through the current sense resistor and voltage sensed across the MOSFET.
26	OUT	Output voltage sense input. The OUT pin is used to sense the output voltage and calculate the power across the MOSFET switch.
27	NC	No connect. This pin is not internally connected and should not be connected to any signal or power rail.
28	PGD	Power good monitor output. Open-drain output pulls low during over-current, UVLO, and OVLO. An external pull-up resistor to VDD or external rail is required.
EP	EP	Exposed pad. Connect to PCB VEE plane using multiple thermal vias.



These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

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Absolute Maximum Ratings (1)

VCC, UVLO/EN, OUT, VAUXH, PGD to VEE	-0.3V to 100V
GATE to VEE	-0.3V to 16V
OVLO, TIMER, PWR to VEE	-0.3V to 7V
SENSE_K, SENSE, VEE_K to VEE	-0.3V to +0.3V
SCL, SDAI, SDAO, $\overline{\text{SMBA}}$, CL, ADR0, ADR1, ADR2, VDD, VAUX, DIODE, $\overline{\text{RETRY}}$, VREF to VEE	-0.3V to 6V
ESD Rating	
Human Body Model(2)	2 kV
Storage Temperature	-65°C to 150°C
Junction Temperature	150°C

(1) Absolute Maximum Ratings are limits beyond which damage to the device may occur. Operating Ratings are conditions under which operation of the device is intended to be functional. For specifications and test conditions, see the Electrical Characteristics.
(2) The human body model is a 100 pF capacitor discharged through a 1.5 kΩ resistor into each pin. 2 kV rating for all pins except GATE and PGD which are rated at 1.5 kV and 1 kV respectively.

Operating Ratings

VCC supply voltage above VEE	10V to +80V
OUT voltage above VEE	0V to +80V
PGD off voltage above VEE	0V to +80V
Junction temperature	−40°C to + 125°C

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Electrical Characteristics

Limits in standard type are for T_J = 25°C only; limits in boldface type apply over the junction temperature (T_J) range of -40°C to +125°C. Minimum and Maximum limits are specified through test, design, or statistical correlation. Typical values represent the most likely parametric norm at T_J = 25°C, and are provided for reference purposes only. Unless otherwise stated the following conditions apply: VCC-VEE = 48V. See (1) (2).

Symbol	Parameter	Conditions	Min	Typ	Max	Units
Input (VCC)						
I_{IN-EN}	Input current, enabled	VCC - VEE = 48V, UVLO/EN = 5V		6	**8**	mA
POR_{IT}	Threshold voltage to start insertion timer	VCC - VEE increasing		8	**9.2**	V
POR_{EN}	Threshold voltage to enable all functions	VCC - VEE increasing		8.7	**9.9**	V
POR_{EN-HYS}	POR_{EN} hysteresis	VCC - VEE decreasing		170		mV
Output (OUT)						
I_{OUT-EN}	OUT bias current, enabled	Enabled, OUT = VEE		-100		nA
$I_{OUT-DIS}$	OUT bias current, disabled (3)	Disabled, OUT = VEE + 48V		135		µA
OVLO/UVLO						
$UVLO_{TH}$	UVLO/EN threshold	UVLO/EN Falling	**2.41**	2.48	**2.55**	V
$UVLO_{HYS}$	UVLO/EN hysteresis current	UVLO/EN = VEE + 2V	**13**	20	**26**	µA
$UVLO_{DEL}$	UVLO delay	Delay to GATE high		9		µs
		Delay to GATE low		12		µs
$UVLO_{BIAS}$	UVLO/EN bias current	UVLO/EN = VEE + 5V			**1**	µA
$OVLO_{TH}$	OVLO threshold		**2.39**	2.47	**2.53**	V
$OVLO_{HYS}$	OVLO hysteresis current	OVLO = VEE + 2.8V	**-26**	-21	**-13**	µA
$OVLO_{DEL}$	OVLO delay	Delay to GATE high		10		µs
		Delay to GATE low		12		µs
$OVLO_{BIAS}$	OVLO bias current	OVLO = 2.3V			**1**	µA
Power Limit (PWR)						
PWR_{LIM-1}	Power limit sense voltage (OUT-SENSE)	OUT – SENSE = 48V, RPWR = 145 kΩ	**19.5**	24.5	**29.5**	mV
PWR_{LIM-2}		OUT - SENSE = 24V, RPWR = 75 kΩ		24.7		mV
I_{PWR}	PWR pin current	V_{PWR} = 2.5V		-18		µA
$R_{SAT(PWR)}$	PWR pin impedance when disabled	UVLO/EN = 2.0V		140		Ω
Gate Control (GATE)						
I_{GATE}	Source current	Normal Operation	**-72**	-52	**-32**	µA
	Sink current	UVLO/EN < VEE+2V	**3.4**	4.1	**5.3**	mA
		SENSE - VEE =150 mV, V_{GATE} =VEE+5V	**50**	111	**180**	mA
V_{GATE}	Gate output voltage in normal operation	GATE-VEE Voltage		12.6		V
Current Limit						
V_{CL}	Current limit threshold voltage	CL = VDD (4)	**23**	26	**30**	mV
V_{CL}	Current limit threshold voltage	CL = VEE or FLOAT (4)	**47**	50	**53**	mV
t_{CL}	Response time	SENSE-VEE stepped from 0 mV to 80 mV		54		µs
I_{SENSE}	SENSE input current	Enabled, OUT = VEE		-5		µA
		Disabled, OUT = VCC		-55		µA
I_{SENSE_K}	SENSE_K input current			-10		µA

(1) Absolute Maximum Ratings are limits beyond which damage to the device may occur. Operating Ratings are conditions under which operation of the device is intended to be functional. For specifications and test conditions, see the Electrical Characteristics.
(2) Current out of a pin is indicated as a negative value.
(3) OUT bias current (disabled) due to leakage current through an internal 1 MΩ resistance from SENSE to OUT.
(4) CL bit High or Low is set by either the CL pin on startup (if CL = VDD, then High, if CL = VEE or FLOAT, then Low) or by the current limit setting bit in the device setup register.

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Electrical Characteristics (continued)

Limits in standard type are for T_J = 25°C only; limits in boldface type apply over the junction temperature (T_J) range of -40°C to +125°C. Minimum and Maximum limits are specified through test, design, or statistical correlation. Typical values represent the most likely parametric norm at T_J = 25°C, and are provided for reference purposes only. Unless otherwise stated the following conditions apply: VCC-VEE = 48V. See (1) (2).

Symbol	Parameter	Conditions	Min	Typ	Max	Units
I_{VEE_K}	VEE_K input current			-10		µA
Circuit Breaker						
RT_{CB}	Circuit breaker to current limit ratio: $(V_{SENSE}-V_{VEE})/V_{CL}$	CB/CL ratio bit = 0, ILim = 50 mV	**1.45**	1.9	**2.22**	
		CB/CL ratio bit = 1, ILim = 50 mV	**2.8**	3.7	**4.9**	
		CB/CL ratio bit = 0, ILim = 26 mV		1.8		
		CB/CL ratio bit = 1, ILim = 26 mV		3.6		
V_{CB}	Circuit breaker threshold voltage: $(V_{SENSE}-V_{VEE})$	CB/CL ratio bit = 0, ILim = 50 mV	**72**	93	**116**	mV
		CB/CL ratio bit = 1, ILim = 50 mV	**144**	187	**230**	mV
		CB/CL ratio bit = 0, ILim = 26 mV	**37**	49	**59**	mV
		CB/CL ratio bit = 1, ILim = 26 mV	**72**	93	**116**	mV
t_{CB}	Circuit breaker response time	SENSE-VEE stepped from 0 mV to 150 mV, time to GATE = VEE		800		ns
Timer (TIMER)						
V_{TMRH}	Upper threshold		**3.74**	3.9	**4.07**	V
V_{TMRL}	Lower threshold	Restart cycles	**1.09**	1.2	**1.39**	V
		End of 8th cycle		0.3		V
		Re-enable threshold		0.3		V
I_{TIMER}	Insertion time current		**-5.9**	-4.8	**-3.3**	µA
	Sink current, end of insertion time	TIMER pin = VEE+2V	**1**	1.5	**2**	mA
	Fault detection current	SENSE-VEE=V_{CL}	**-95**	-74	**-50**	µA
	Fault sink current		**1.7**	2.4	**3.2**	µA
DC_{FAULT}	Fault restart duty cycle			0.5		%
t_{FAULT}	Fault to GATE = VEE delay	TIMER pin reaches the upper threshold		15		µs
Power Good (PGD)						
PGD_{TH}	Threshold measured at OUT - SENSE	OUT – SENSE Decreasing	**1.18**	1.24	**1.31**	V
		OUT – SENSE Increasing	**2.44**	2.5	**2.56**	V
PGD_{VOL}	Output low voltage	I_{SINK} = 2 mA		50	**150**	mV
PGD_{IOH}	Off leakage current	V_{PGD} = 80V			**5**	µA
ADC and MUX						
	Resolution			12		Bits
INL	Integral non-linearity	ADC only		±4		LSB
$t_{ACQUIRE}$	Acquisition + conversion time	Any Channel		100		µs
t_{RR}	Acquisition round robin time	Cycle all channels		1		ms
Internal Reference						
V_{REF}	Reference voltage		**2.93**	2.97	**3.02**	V
Telemetry Accuracy (5)						
IIN_{FSR}	Current input full scale range	CL= VEE (6)		74.9		mV
		CL = VDD (6)		38.1		mV
IIN_{LSB}	Current input LSB	CL= VEE (6)		18.3		µV
		CL = VDD (6)		9.3		µV
$VAUX_{FSR}$	VAUX input full scale range			2.96		V

(5) Full scale range depends on both the VREF value and the gain/attenuation of the current/voltage channel.
(6) CL bit High or Low is set by either the CL pin on startup (if CL = VDD, then High, if CL = VEE or FLOAT, then Low) or by the current limit setting bit in the device setup register.

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Electrical Characteristics (continued)

Limits in standard type are for T_J = 25°C only; limits in boldface type apply over the junction temperature (T_J) range of -40°C to +125°C. Minimum and Maximum limits are specified through test, design, or statistical correlation. Typical values represent the most likely parametric norm at T_J = 25°C, and are provided for reference purposes only. Unless otherwise stated the following conditions apply: VCC-VEE = 48V. See (1) (2).

Symbol	Parameter	Conditions	Min	Typ	Max	Units
$VAUX_{LSB}$	VAUX input LSB			724		µV
$VAUXH_{FSR}$	VAUXH input full scale range			88.9		V
$VAUXH_{LSB}$	VAUXH input LSB			21.7		mV
OUT_{LSB}	OUT pin LSB			21.7		mV
IIN_{ACC}	Input current accuracy	SENSE_K-VEE_K = 50 mV, CL = VEE (Note 6)	**-3.0**		**3.0**	%
V_{ACC}	VAUX, VAUXH, OUT	VAUXH-VEE=48V,OUT - VEE= 48V, VAUX = 2.8V	**-2.7**		**2.7**	%
PIN_{ACC}	Input power accuracy	VCC-VEE = 48V, SENSE_K-VEE_K = 50 mV, CL = VDD	**-4.5**		**4.5**	%
Diode Temperature Sensor						
T_{ACC}	Temperature accuracy using local diode	T_A = 25°C to 85°C		2		°C
	Remote diode resolution			9		bits
I_{DIODE}	External diode current source	High Level		250	**325**	µA
		Low Level		9.4		µA
	Diode current ratio			25.9		
VAUX						
I_{IN}	Input current	VAUX = 3V			**1**	µA
VDD Regulation						
VDD_{OUT}	VDD regulated output	IDD = 0 mA	**4.6**	4.9	**5.15**	V
		IDD = -10 mA		4.8		V
VDD_{ILIM}	VDD current limit	VDD = 0V	**-25**	-30	**-42**	mA
VDD_{POR}	VDD voltage reset threshold	VDD Rising		4.1		V
PMBus Pin Thresholds (SCL, SDAI/O, $\overline{SMBA}$) (7)						
V_{IL}	Data, clock input low voltage	With respect to VEE			**0.9**	V
V_{IH}	Data, clock input high voltage	With respect to VEE	**2.1**		**5.5**	V
V_{OL}	Data output low voltage	I_{SINK} = 3 mA	**0**		**0.4**	µA
I_{LEAK}	Input leakage current	SDAI, $\overline{SMBA}$, SCL = 5V above VEE			**1**	µA
Pin Strappable Thresholds (CL, $\overline{RETRY}$)						
V_{IH}	Input high voltage		**3**			V
I_{LEAK}	Input leakage current	CL,$\overline{RETRY}$ = 5V		5		µA
Thermal (8)						
θ_{JA}	Junction to ambient			30		°C/W
θ_{JC}	Junction to case			4		°C/W

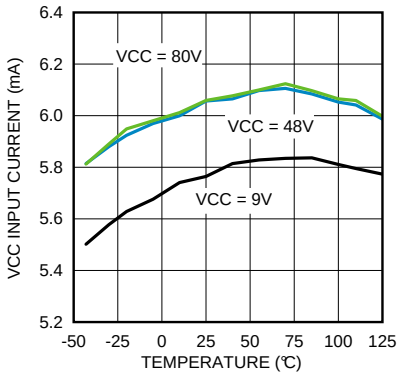
(7) PMBus communication clock rate at final test is 400 kHz.
(8) Junction to ambient thermal resistance is highly application and board layout dependent. Specified thermal resistance values for the package specified is based on a 4-layer, 4"x3", 2/1/1/2 oz. Cu board as per JEDEC standards is used. For detailed information on soldering plastic HTSSOP packages refer to the Packaging Data Book.

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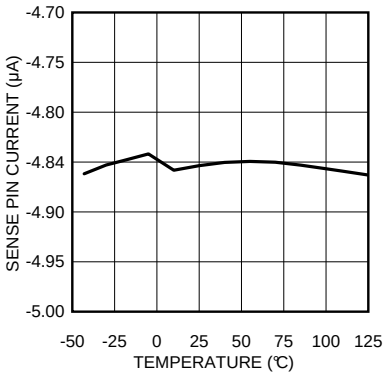
Typical Performance Characteristics

Unless otherwise specified the following conditions apply: T_J = 25°C, VCC-VEE = 48V.

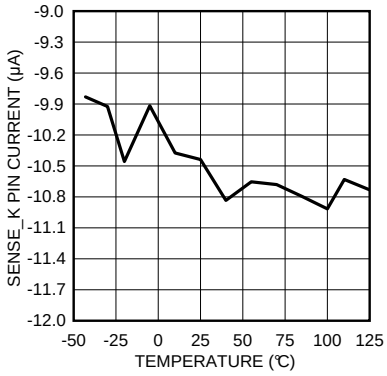
VCC Pin Current



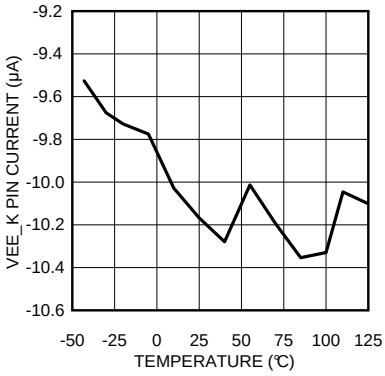
SENSE Pin Current



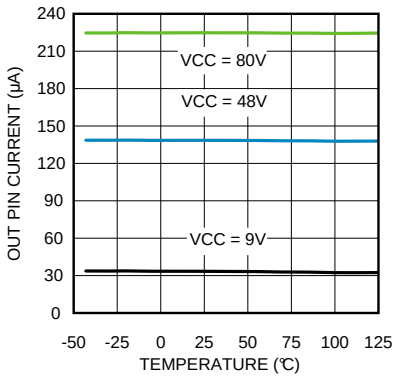
SENSE_K Pin Current (Enabled)



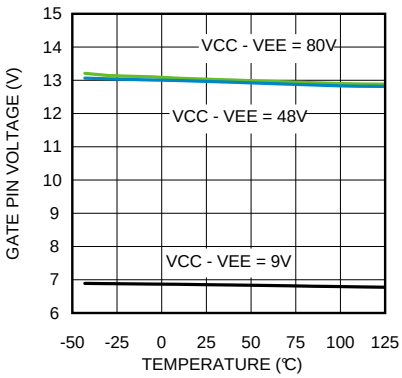
VEE_K Pin Current (Enabled)



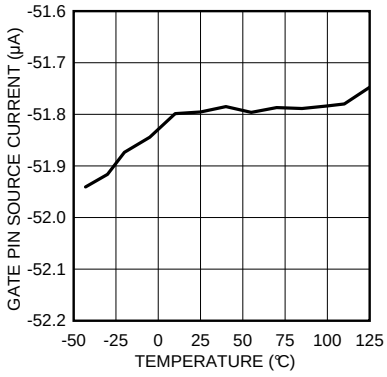
OUT Pin Current (Disabled)



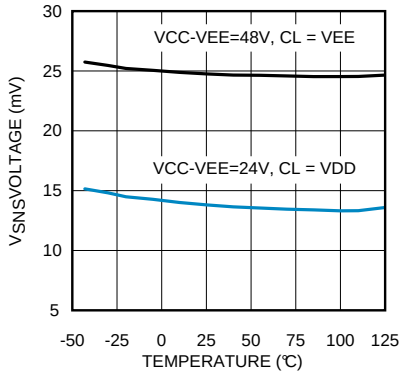
GATE Output Voltage (V_{GATE})



GATE Pin Source Current



V_{SNS} (SENSE_K-VEE_K) at Power Limit Threshold R_{PWR} = 75 kΩ

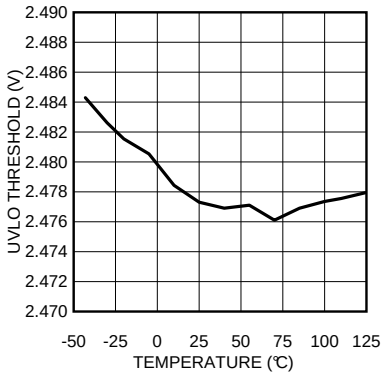


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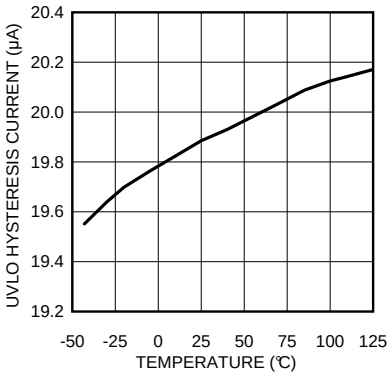
Typical Performance Characteristics (continued)

Unless otherwise specified the following conditions apply: T_J = 25°C, VCC-VEE = 48V.

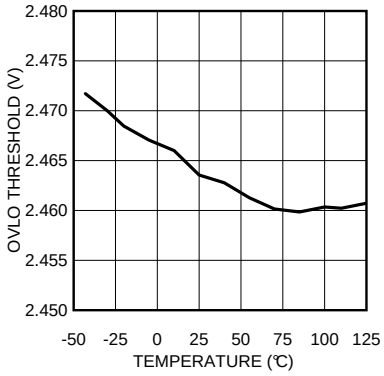
UVLO Threshold



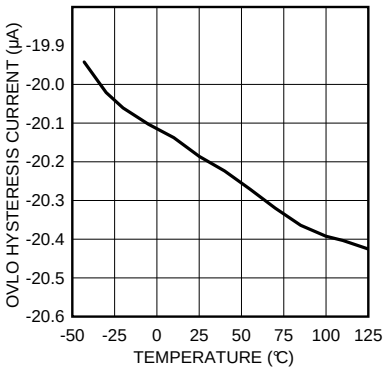
UVLO Hysteresis Current



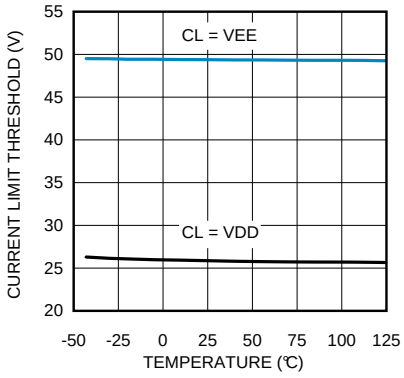
OVLO Threshold



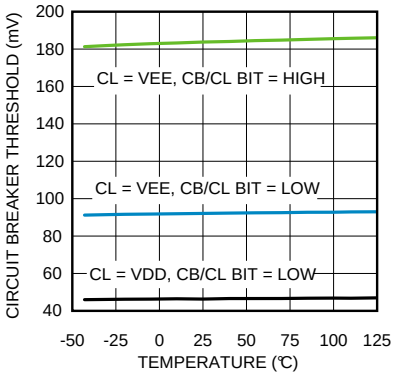
OVLO Hysteresis Current



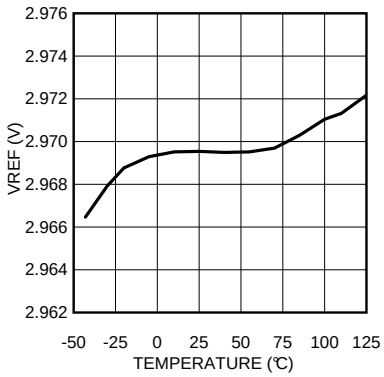
Current Limit Threshold



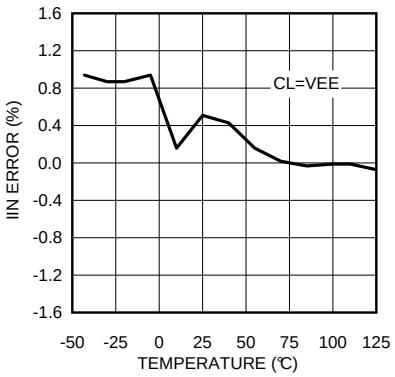
Circuit Breaker Threshold



Reference Voltage



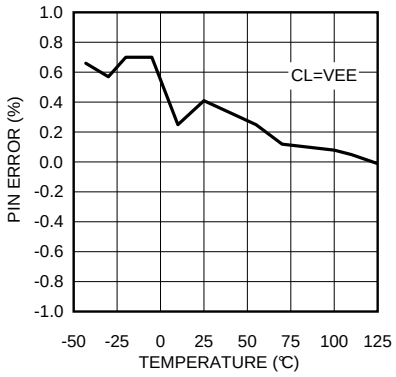
IIN Measurement Accuracy (SENSE_K-VEE_K = 50 mV)



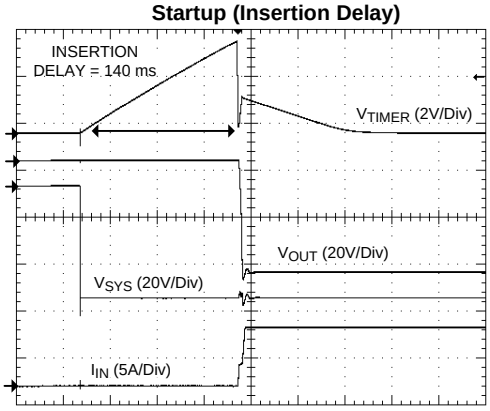
Typical Performance Characteristics (continued)

Unless otherwise specified the following conditions apply: T_J = 25°C, VCC-VEE = 48V.

PIN Measurement Accuracy (SENSE_K-VEE_K = 50 mV)

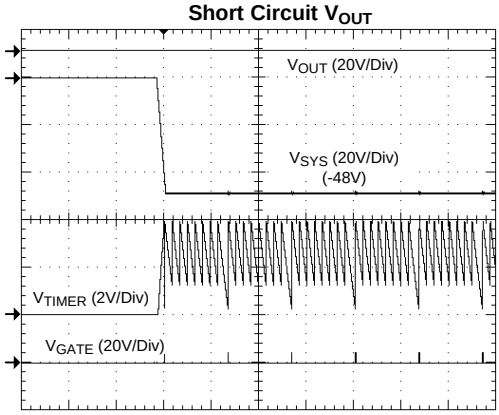


Startup (Insertion Delay)



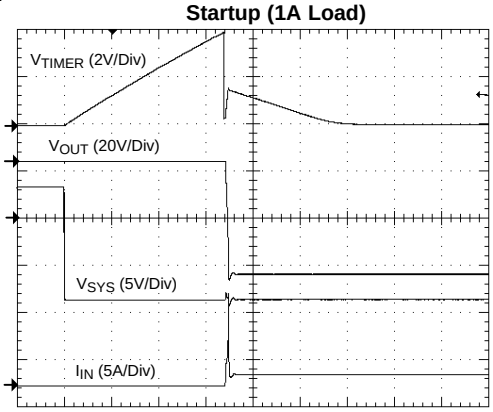
40 ms/div

Short Circuit V_{OUT}



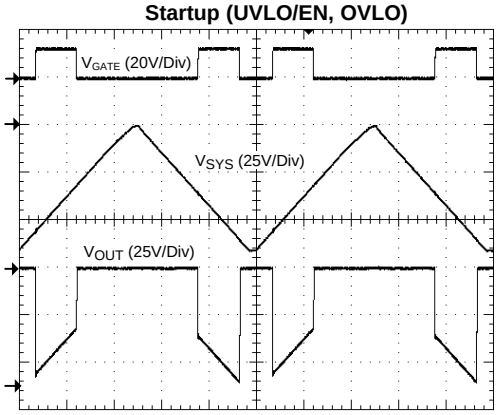
1s/div

Startup (1A Load)



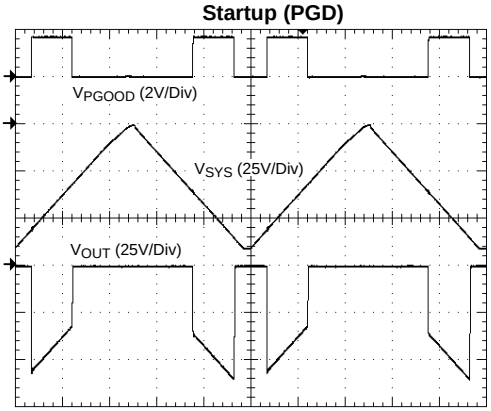
40 ms/div

Startup (UVLO/EN, OVLO)



400 ms/div

Startup (PGD)



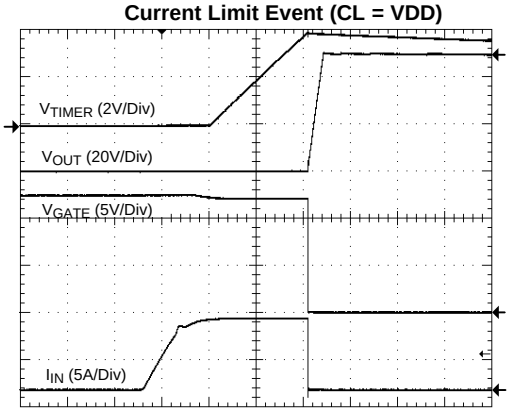
400 ms/div

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Typical Performance Characteristics (continued)

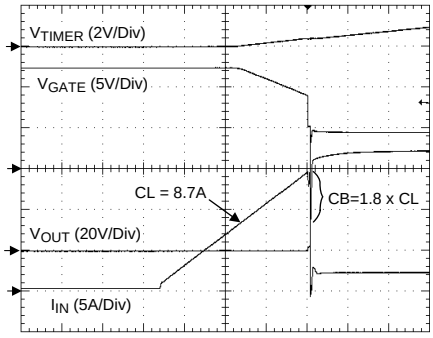
Unless otherwise specified the following conditions apply: T_J = 25°C, VCC-VEE = 48V.

Current Limit Event (CL = VDD)



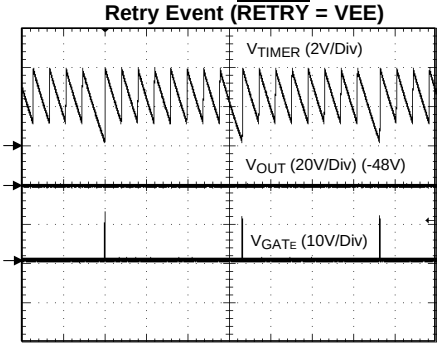
4 ms/div

Circuit Breaker Event (CL = VDD)



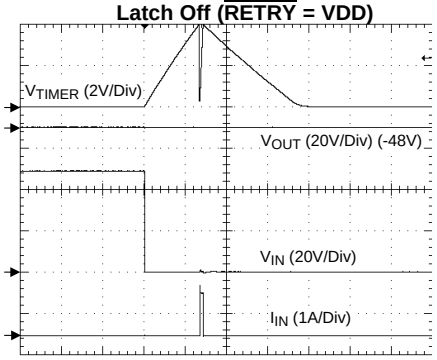
400 µs/div

Retry Event ($\overline{\text{RETRY}}$ = VEE)



400 ms/div

Latch Off ($\overline{\text{RETRY}}$ = VDD)



100 ms/div

BLOCK DIAGRAM

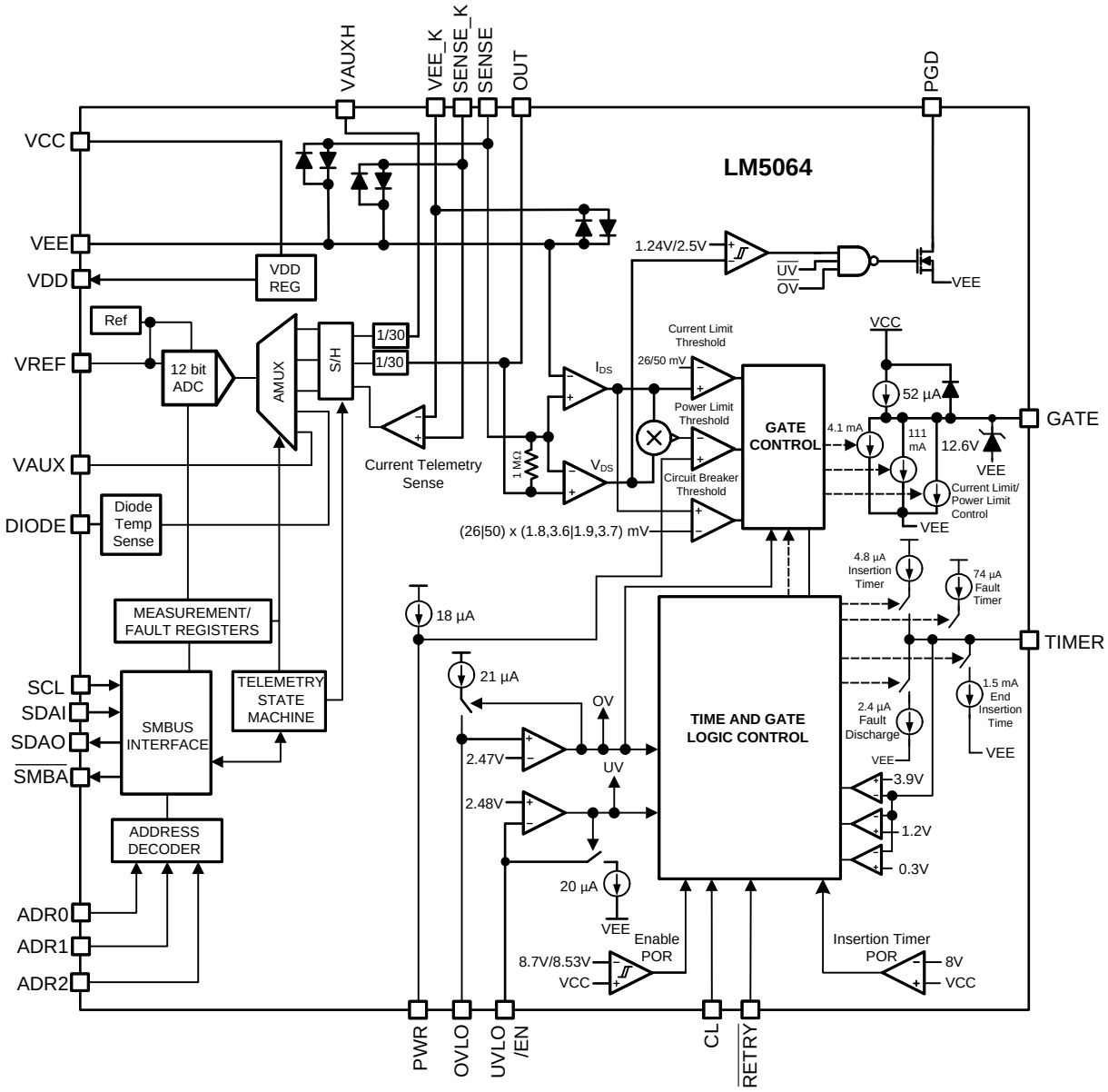


Figure 1. Block Diagram

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FUNCTIONAL DESCRIPTION

The LM5064 is designed to control the in-rush current to the load upon insertion of a circuit card into a live backplane or other "hot" power source, thereby limiting the voltage sag on the backplane's supply and the dv/dt of the voltage applied to the load. The effect from the insertion event on other circuits in the system is minimized, preventing possible unintended resets. A controlled shutdown when the circuit card is removed can also be implemented using the LM5064.

In addition to a programmable current limit, the LM5064 monitors and limits the maximum power dissipation in the series pass device (Q_1) to maintain operation within the device's Safe Operating Area (SOA). Either current limiting or power limiting for an extended period of time (user defined) results in the shutdown of the series pass device. In this event, the LM5064 can latch off or repetitively retry based on the hardware setting of the $\overline{\text{RETRY}}$ pin. Once started, the number of retries can be set to 0, 1, 2, 4, 8, 16, or infinite. The circuit breaker function quickly switches off the series pass device upon detection of a severe over-current condition. Programmable under-voltage lockout (UVLO) and over-voltage lockout (OVLO) circuits shut down the LM5064 when the system input voltage (V_{SYS}) is outside the desired operating range.

The telemetry capability of the LM5064 provides intelligent monitoring of the input voltage, output voltage, input current, input power, temperature, and an auxiliary input. The LM5064 also provides a peak capture of the input power and programmable hardware averaging of the input voltage, current, power, and output voltage. Warning thresholds which trigger the $\overline{\text{SMBA}}$ pin may be programmed for input and output voltage, current, power and temperature via the PMBus interface. Additionally, the LM5064 is capable of detecting damage to the external MOSFET, Q_1.

Operating Voltage

The LM5064 operating voltage is the voltage supplied between VCC and VEE (VCC-VEE) which has an operating range of 10V to 80V with a 100V transient capability. All signals to the IC are referenced to the VEE voltage which acts as the effective return path for the IC.

Power Up Sequence

Referring to Figure 2, as the system voltage (V_{SYS}) initially increases, the external N-channel MOSFET (Q_1) is held off by an internal 111 mA pull-down current at the GATE pin. The strong pull-down current at the GATE pin prevents an inadvertent turn on as the MOSFET's gate-to-drain (Miller) capacitance is charged. Additionally, the TIMER pin is initially held at VEE. When the operating voltage of the LM5064 (VCC - VEE) reaches the POR_{IT} threshold, the insertion time begins. During the insertion time, the capacitor at the TIMER pin (C_T) is charged by a 4.8 µA current source, and Q_1 is held off by a 4.1 mA pull-down current at the GATE pin regardless of the input voltage. The insertion time delay allows ringing and transients on V_{SYS} to settle before Q_1 is enabled. The insertion time ends when the TIMER pin voltage reaches 3.9V. C_T is then quickly discharged by an internal 1.5 mA pull-down current. The GATE pin then switches on Q_1 when the operating voltage exceeds the UVLO threshold. If the operating voltage is above the UVLO threshold at the end of the insertion time,(t_1 in Figure 2) the GATE pin sources 52 µA to charge the gate capacitance of Q_1. The maximum voltage on GATE is limited by an internal 12.6V zener diode to VEE.

As the voltage at the OUT pin transitions to V_{SYS}, the LM5064 monitors the drain current and power dissipation of MOSFET Q_1. In-rush current limiting and/or power limiting circuits actively control the current delivered to the load. During the in-rush limiting interval (t_2 in Figure 2), an internal 74 µA fault timer current source charges C_T. If Q_1's power dissipation and the input current reduce below their respective limiting thresholds before the TIMER pin reaches 3.9V, the 74 µA current source is switched off, and C_T is discharged by the internal 2.4 µA current sink (t_3 in Figure 2). The in-rush limiting will no longer engage unless a current-limit condition occurs.

If the TIMER pin voltage reaches 3.9V before in-rush current limiting or power limiting ceases during t_2, a fault is declared and Q_1 is turned off. See the Fault Timer & Restart section for a complete description of the fault mode.

The LM5064 will assert the $\overline{\text{SMBA}}$ pin after the operating voltage has exceeded the POR threshold to indicate that the volatile memory and device settings are in their default state. The CONFIG_PRESET bit within the MFR_SPECIFIC_17 register (E1h) indicates default configuration of warning thresholds and device operation and will remain high until a CLEAR_FAULTS command is received.

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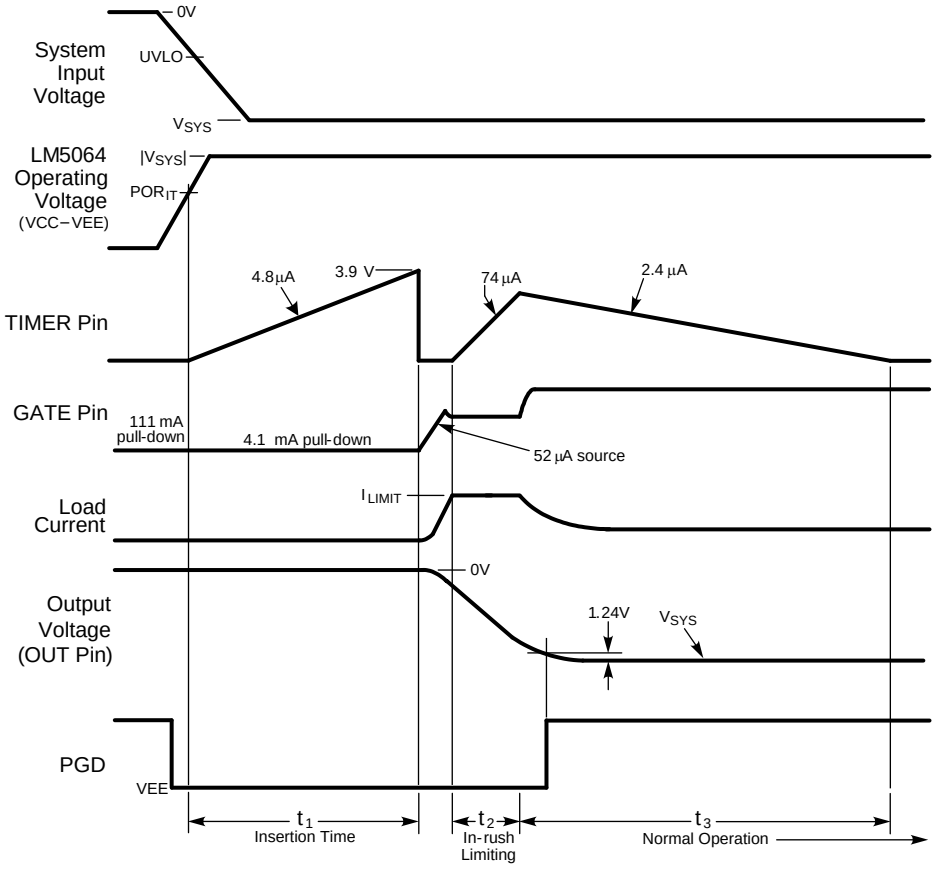


Figure 2. Power Up Sequence

Gate Control

A current source provides the charge at the GATE pin to enhance the N-Channel MOSFET's gate (Q_1). During normal operating conditions (t_3 in Figure 2) the gate of Q_1 is held charged by an internal 52 µA current source. The GATE pin peak voltage is roughly 12.6V, which will force a V_{GS} across Q_1 of 12.6V under normal operation. When the system voltage is initially applied, the GATE pin is held low by a 111 mA pull-down current. This helps prevent an inadvertent turn on of Q_1 through its drain-gate capacitance as the applied system voltage increases.

During the insertion time (t_1 in Figure 2), the GATE pin is held low by a 4.1 mA pull-down current. This maintains Q_1 in the off-state until the end of t_1, regardless of the voltage on V_{SYS} or UVLO/EN. Following the insertion time, during t_2 in Figure 2, the gate voltage of Q_1 is modulated to keep the current or power dissipation level from exceeding the programmed levels. While in the current or power limiting mode, the TIMER pin capacitor is charging. If the current and power limiting cease before the TIMER pin reaches 3.9V, the TIMER pin capacitor then discharges, and the circuit begins normal operation. If the in-rush limiting condition persists such that the TIMER pin reached 3.9V during t_2, the GATE pin is then pulled low by the 4.1 mA pull-down current. The GATE pin is then held low until either a power up sequence is initiated ($\overline{\text{RETRY}}$ pin to VDD), an automatic retry is attempted ($\overline{\text{RETRY}}$ pin to VEE or floating), or a PMBus ON/OFF command is initiated. See the Fault Timer & Restart section. If the operating voltage falls below the UVLO threshold, or rises above the OVLO threshold, the GATE pin is pulled low by the 4.1 mA pull-down current to switch off Q_1.

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Current Limit

The current limit threshold is reached when the voltage across the sense resistor R_S (SENSE to VEE) exceeds the internal voltage limit of 26 mV or 50 mV depending on whether the CL pin is connected to VDD or VEE, respectively. In the current limiting condition, the GATE voltage is controlled to limit the current in MOSFET Q_1. While the current limit circuit is active, the fault timer is active as described in the Fault Timer & Restart section. If the load current falls below the current limit threshold before the end of the Fault Timeout Period, the LM5064 resumes normal operation. If the current limit condition persists for longer than the Fault Timeout Period set by C_T, the IIN OC Fault bit in the STATUS_INPUT (7Ch) register, the INPUT bit in the STATUS_WORD (79h) register, and IIN_OC/PFET_OP_FAULT bit in the DIAGNOSTIC_WORD (E1h) register will be toggled high and $\overline{\text{SMBA}}$ pin will be asserted. $\overline{\text{SMBA}}$ toggling can be disabled using the ALERT_MASK (D8h) register. For proper operation, the R_S resistor value should be no higher than 200 mΩ. Higher values may create instability in the current limit control loop. The current limit threshold pin value may be overridden by setting appropriate bits in the DEVICE_SETUP register (D9h).

Circuit Breaker

If the load current increases rapidly (e.g., the load is short circuited), the current in the sense resistor (R_S) may exceed the current limit threshold before the current limit control loop is able to respond. If the current exceeds 1.9x or 3.7x (CL = VEE) the current limit threshold, Q_1 is quickly switched off by the 111 mA pull-down current at the GATE pin, and a Fault Timeout Period begins. When the voltage across R_S falls below the circuit breaker (CB) threshold, the 111 mA pull-down current at the GATE pin is switched off, and the gate voltage of Q_1 is then determined by the current limit or the power limit functions. If the TIMER pin reaches 3.9V before the current limiting or power limiting condition ceases, Q_1 is switched off by the 4.1 mA pull-down current at the GATE pin as described in the Fault Timer & Restart section. A circuit breaker event will cause the CIRCUIT_BREAKER_FAULT bit in the STATUS_MFR_SPECIFIC (80h) and DIAGNOSTIC_WORD (E1h) registers to be toggled high, and $\overline{\text{SMBA}}$ pin will be asserted unless this feature is disabled using the ALERT_MASK (D8h) register. The circuit breaker pin configuration may be overridden by setting appropriate bits in the DEVICE_SETUP (D9h) register.

Power Limit

An important feature of the LM5064 is the MOSFET power limiting. The power limit function can be used to maintain the maximum power dissipation of MOSFET Q_1 within the device SOA rating. The LM5064 determines the power dissipation in Q_1 by monitoring its drain-source voltage (OUT to SENSE), and the drain current through the R_S (SENSE to VEE). The product of the current and voltage is compared to the power limit threshold programmed by the resistor at the PWR pin. If the power dissipation reaches the limiting threshold, the GATE voltage is modulated to regulate the current in Q_1. While the power limiting circuit is active, the fault timer is active as described in the Fault Timer & Restart section. If the power limit condition persists for longer than the Fault Timeout Period set by the timer capacitor, C_T, the IIN OC Fault bit in the STATUS_INPUT (7Ch) register, the INPUT bit in the STATUS_WORD (79h) register, and the IIN_OC/PFET_OP_FAULT bit in the DIAGNOSTIC_WORD (E1h) register will be toggled high and $\overline{\text{SMBA}}$ pin will be asserted unless this feature is disabled using the ALERT_MASK (D8h) register.

Fault Timer & Restart

When the current limit or power limit threshold is reached during turn-on, or as a result of a fault condition, the gate-to-source voltage of Q_1 is modulated to regulate the load current and power dissipation in Q_1. When either limiting function is active, a 74 µA fault timer current source charges the external capacitor (C_T) at the TIMER pin as shown in Figure 2(Fault Timeout Period). If the fault condition subsides during the Fault Timeout Period before the TIMER pin reaches 3.9V, the LM5064 returns to the normal operating mode and C_T is discharged by the 1.5 mA current sink. If the TIMER pin reaches 3.9V during the Fault Timeout Period, Q_1 is switched off by a 4.1 mA pull-down current at the GATE pin. The subsequent restart procedure then depends on the selected retry configuration.

If the $\overline{\text{RETRY}}$ pin is high (VDD), the LM5064 latches the GATE pin low at the end of the Fault Timeout Period. C_T is then discharged to VEE by the 2.4 µA fault current sink. The GATE pin is held low by the 4.1 mA pull-down current until a power up sequence is externally initiated by cycling the operating voltage (VCC-VEE), or momentarily pulling the UVLO/EN pin below its threshold with an open-collector or open-drain device as shown in Figure 3. The voltage at the TIMER pin must be <0.3V for the restart procedure to be effective. The TIMER_LATCHED_OFF bit in the DIAGNOSTIC_WORD (E1h) register will remain high while the latched off condition persists.

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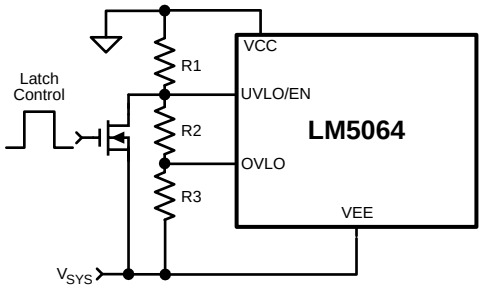


Figure 3. Latched Fault Restart Control

The LM5064 provides an automatic restart sequence which consists of the TIMER pin cycling between 3.9V and 1.2V eight times after the Fault Timeout Period, as shown in Figure 4. The period of each cycle is determined by the 74 µA charging current, and the 2.4 µA discharge current, and the value of the capacitor C_T. When the TIMER pin reaches 0.3V during the eighth high-to-low ramp, the 52 µA current source at the GATE pin turns on Q_1. If the fault condition is still present, the Fault Timeout Period and the restart sequence repeat. The $\overline{\text{RETRY}}$ pin allows selecting no retries or infinite retries. Finer control of the retry behavior can be achieved through the DEVICE_SETUP (D9h) register. Retry counts of 0, 1, 2, 4, 8, 16 or infinite may be selected by setting the appropriate bits in the DEVICE_SETUP (D9h) register.

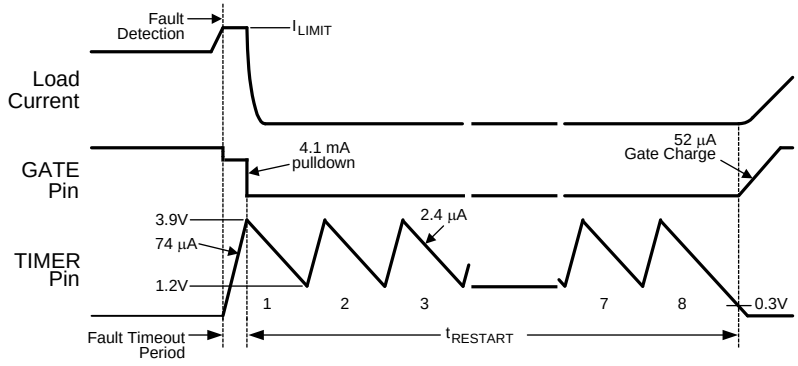


Figure 4. Restart Sequence

Under-Voltage Lockout (UVLO)

The series pass MOSFET (Q_1) is enabled when the input supply voltage (V_{SYS}) is within the operating range defined by the programmable under-voltage lockout (UVLO) and over-voltage lockout (OVLO) levels. Typically, the UVLO level at V_{SYS} is set with a resistor divider (R1-R3) as shown in Figure 5. Referring to the Block Diagram when V_{SYS} is below the UVLO level, the internal 20 µA current source at UVLO/EN is enabled, the current source at OVLO is off, and Q_1 is held off by the 4.1 mA pull-down current at the GATE pin. As V_{SYS} is increased, raising the voltage at UVLO/EN above its threshold with respect to VEE, the 20 µA current source at UVLO/EN is switched off, increasing the voltage at UVLO/EN, providing hysteresis for this threshold. With the UVLO/EN pin above its threshold, Q_1 is switched on by the 52 µA current source at the GATE pin if the insertion time delay has expired.

See the Application Information section for a procedure to calculate the values of the threshold setting resistors (R1-R3). The minimum possible UVLO level at V_{SYS} can be set by connecting the UVLO/EN pin to VCC. In this case Q_1 is enabled after the insertion time when the operating voltage (VCC-VEE) reaches the POR threshold. After power up an UVLO condition will cause the INPUT bit in the STATUS_WORD (79h) register, the VIN_UV_FAULT bit in the STATUS_INPUT (7Ch) register, and the VIN_UNDERVOLTAGE_FAULT bit in the DIAGNOSTIC_WORD (E1h) registers to be toggled high and $\overline{\text{SMBA}}$ pin will be pulled low unless this feature is disabled using the ALERT_MASK (D8h) register.

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Over-Voltage Lockout (OVLO)

The series pass MOSFET (Q_1) is enabled when the input supply voltage (V_{SYS}) is within the operating range defined by the programmable under-voltage lockout (UVLO) and over-voltage lockout (OVLO) levels. If V_{SYS} raises the OVLO pin voltage above its threshold (2.47V above VEE), Q_1 is switched off by the 4.1 mA pull-down current at the GATE pin, denying power to the load. When the OVLO pin is above its threshold, the internal 21 µA current source at OVLO is switched on, raising the voltage at OVLO to provide threshold hysteresis. When V_{SYS} is reduced below the OVLO level Q_1 is re-enabled. An OVLO condition will toggle the VIN_OV_FAULT bit in the STATUS_INPUT (7Ch) register, the INPUT bit in the STATUS_WORD (79h) register and the VIN_OVERVOLTAGE_FAULT bit in the DIAGNOSTIC_WORD (E1h) register. The SMBA pin will be pulled low unless this feature is disabled using the ALERT_MASK (D8h) register.

Shutdown Control

The load current can be remotely switched off by taking the UVLO/EN pin below its threshold with an open collector or open drain device, as shown in Figure 5. Upon releasing the UVLO/EN pin the LM5064 switches on the load current with in-rush current and power limiting.

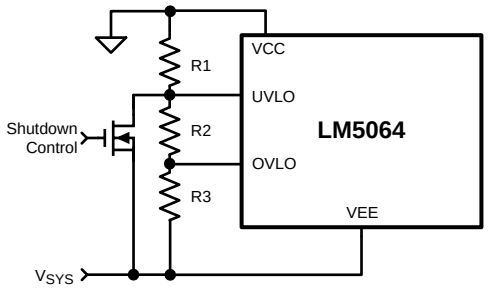


Figure 5. Shutdown Control

Power Good Pin

The Power Good output indicator pin (PGD) is connected to the drain of an internal N-channel MOSFET. An external pull-up resistor is required at PGD to an appropriate voltage to indicate the status to downstream circuitry. The off-state voltage at the PGD pin must be more positive than VEE, and can be up to 80V above VEE with transient capability to 100V. PGD is switched high at the end of the turn-on sequence when the voltage from OUT to SENSE (the external MOSFET's V_{DS}) decreases below 1.24V. PGD switches low if the MOSFET's V_{DS} increases passed 2.5V, if the system input voltage goes below the UVLO threshold or above the OVLO threshold, or if a fault is detected. However, the PGD output cannot stay low when the operating voltage (VCC-VEE) is less than 2V.

VDD Sub-Regulator

The LM5064 contains an internal linear sub-regulator which steps down the VCC voltage to generate a 4.9V rail (above VEE) used for powering low voltage circuitry. The VDD sub-regulator should be used as the pull-up supply for the CL, RETRY, ADR2, ADR1, ADR0 pins if they are to be tied high. It may also be used as the pull-up supply for the PGD and the SMBus signals (SDA, SCL, SMBA). The VDD sub-regulator is not designed to drive high currents. Careful consideration of internal power dissipation should be practiced when VDD is loaded with other integrated circuits. The VDD pin is current limited to 30 mA in order to protect the LM5064 in the event of a short. The sub-regulator requires a ceramic bypass capacitance (terminated to VEE) having a value of 1 µF or greater to be placed as close to the VDD pin as the PCB layout allows.

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Remote Temperature Sensing

The LM5064 is designed to measure temperature remotely using an MMBT3904 NPN transistor. The base and collector of the MMBT3904 should be connected to the DIODE pin and the emitter to VEE. Place the MMBT3904 near the device that requires temperature sensing. If the temperature of the hot swap pass MOSFET, Q_1, is to be measured, the MMBT3904 should be placed as close to Q_1 as the layout allows. The temperature is measured by means of a change in the diode voltage in response to a step in current supplied by the DIODE pin. The DIODE pin sources a constant 9.4 µA but pulses 250 µA once every millisecond in order to measure the diode temperature. Care must be taken in the PCB layout to keep the parasitic resistance between the DIODE pin and the MMBT3904 low so as not to degrade the measurement. Additionally, a small 1000 pF bypass capacitor should be placed in parallel with the MMBT3904 (collector to emitter) to reduce the effects of noise. The temperature can be read using the READ_TEMPERATURE_1 PMBus command (8Dh). The default limits of the LM5064 will cause $\overline{\text{SMBA}}$ pin to be pulled low if the measured temperature exceeds 125°C and will disable Q_1 if the temperature exceeds 150°C. These thresholds can be reprogrammed via the PMBus interface using the OT_WARN_LIMIT (51h) and OT_FAULT_LIMIT (4Fh) commands. If the temperature measurement and protection capability of the LM5064 are not used, the DIODE pin should be connected to VEE.

Erroneous temperature measurements may result when the device input voltage is below the minimum operating voltage (10V) due to VREF dropping out below the nominal voltage (2.97V). At higher ambient temperatures, this measurement could read a value higher than the OT_FAULT_LIMIT, and will trigger a fault, disabling Q_1. In this case, the faults should be removed and the device reset by writing a 0h, followed by an 80h to the OPERATION (01h) register.

Damaged MOSFET Detection

The LM5064 is able to detect whether the external MOSFET, Q_1, is damaged under certain conditions. If the voltage across the sense resistor exceeds 4 mV while the GATE voltage is low or the internal logic indicates that the GATE should be low, the EXT_MOSFET_SHORTED bit in the STATUS_MFR_SPECIFIC (80h) and DIAGNOSTIC_WORD (E1h) registers will be toggled high and the $\overline{\text{SMBA}}$ pin will be asserted unless this feature is disabled using the ALERT_MASK register (D8h). This method effectively determines whether Q_1 is shorted because of damage present between the drain and gate and/or drain and source.

Enabling/Disabling and Resetting

The output can be disabled at any time during normal operation by either pulling the UVLO/EN pin to below its threshold or the OVLO pin above its threshold, causing the GATE voltage to be forced low with a pull-down strength of 4.1 mA. Toggling the UVLO/EN pin will also reset the LM5064 from a latched-off state due to an over-current or over-power limit condition which has caused the maximum allowed number of retries to be exceeded. While the UVLO/EN or OVLO pins can be used to disable the output they have no effect on the volatile memory or address location of the LM5064. User stored values for address, device operation, and warning and fault levels programmed via the SMBus are preserved while the LM5064 is powered regardless of the state of the UVLO/EN and OVLO pins.The output may also be enabled or disabled by writing 80h or 0h to the OPERATION (01h) register. To re-enable after a fault, the fault condition should be cleared and the OPERATION (01h) register should be written with a 0h and then 80h.

The SMBus address of the LM5064 is captured based on the states (VEE, NC, VDD) of the ADR0, ADR1, and ADR2 pins during turn-on and is latched into a volatile register once VDD has exceeded its POR threshold of 4.1V. Reassigning or postponing the address capture is accomplished by holding the VREF pin to VEE. Pulling the VREF pin low will also reset the logic and erase the volatile memory of the LM5064. Once released, the VREF pin will charge up to its final value and the address will be latched into a volatile register once the voltage at the VREF exceeds 2.55V.

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APPLICATION INFORMATION

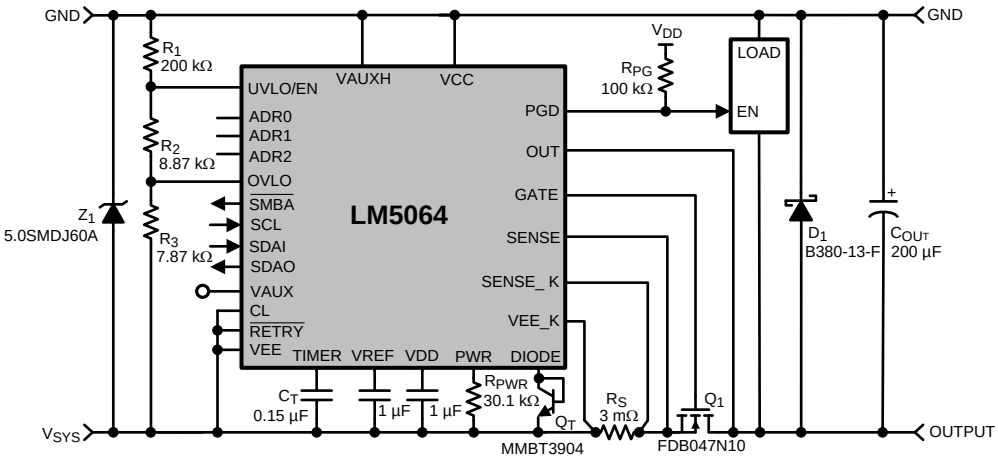


Figure 6. Typical Application Circuit

DESIGN-IN PROCEDURE

Refer to Figure 6 for a Typical Application Circuit. The following is a step-by-step procedure for hardware design of the LM5064. This procedure refers to section numbers that provide detailed information on the following design steps. The recommended design-in procedure is as follows:

MOSFET Selection: Determine the MOSFET based on breakdown voltage, current and power ratings.

Current Limit, R_S: Determine the current limit threshold (I_{LIM}). This threshold must be higher than the normal maximum load current, allowing for tolerances in the current sense resistor value and the LM5064 Current Limit threshold voltage. Use Equation 1 to determine the value for R_S.

Power Limit Threshold: Determine the maximum allowable power dissipation for the series pass MOSFET (Q_1), using the device's SOA information. Use Equation 2 to determine the value for R_{PWR}. Note that many MOSFET manufacturers do not accurately specify the device SOA so it is usually beneficial to choose a conservative value when selecting R_{PWR}.

Turn-on Time and TIMER Capacitor, C_T: Determine the value for the timing capacitor at the TIMER pin (C_T) using Equation 7 and Equation 8. The fault timeout period (t_{FAULT}) **MUST** be longer than the circuit's turn-on time. The turn-on time can be estimated using the equations in the TURN-ON TIME section, but should be verified experimentally. Review the resulting insertion time and the restart timing if retry is enabled.

UVLO, OVLO: Choose option A, B, C, or D from the UVLO, OVLO section to set the UVLO and OVLO thresholds and hysteresis. Use the procedure for the appropriate option to determine the resistor values at the UVLO/EN and OVLO pins.

MOSFET SELECTION

It is recommended that the external MOSFET (Q_1) selection is based on the following criteria:

- The BV_{DSS} rating should be greater than the maximum system voltage (V_{SYS}), plus ringing and transients which can occur when the circuit card, or adjacent cards, are inserted or removed.

- The maximum continuous current rating should be based on the current limit threshold (for example, 26 mV/R_S for CL = VDD), not the maximum load current, since the circuit can operate near the current limit threshold continuously.

- The Pulsed Drain Current spec (I_{DM}) must be greater than the current threshold for the circuit breaker function (49/93/187 mV/R_S, depending on CL and CB configuration).

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- The SOA (Safe Operating Area) chart of the device, and the thermal properties, should be used to determine the maximum power dissipation threshold set by the R_{PWR} resistor. The programmed maximum power dissipation should have a reasonable margin from the maximum power defined by the MOSFET's SOA curve. If the device is set to infinitely retry, the MOSFET will be repeatedly stressed during fault restart cycles. The MOSFET manufacturer should be consulted for guidelines.

- $R_{DS(on)}$ should be sufficiently low such that the power dissipation at maximum load current (I_{LIM}^2 x $R_{DS(on)}$) does not raise its junction temperature above the manufacturer's recommendation.

- The gate-to-source voltage provided by the LM5064 can be as high as 12.6V. Q_1 must be able to tolerate this voltage for its V_{GS} rating. An additional zener diode can be added from GATE to VEE to lower this voltage and limit the peak V_{GS}.

CURRENT LIMIT (R_S)

The LM5064 monitors the current in the external MOSFET Q_1 by measuring the voltage across the sense resistor (R_S), connected from SENSE to VEE. The required resistor value is calculated from:

$$R_S = \frac{V_{CL}}{I_{LIM}} \quad (1)$$

where I_{LIM} is the desired current limit threshold. If the voltage across R_S reaches V_{CL}, the current limit circuit modulates the gate of Q_1 to regulate the current at I_{LIM}. While the current limiting circuit is active, the fault timer is active as described in the Fault Timer & Restart section. For proper operation, R_S must be less than 200 mΩ.

V_{CL} can be set to either 26 mV or 50 mV via hardware and/or software. This setting defaults to use of CL pin which, when connected to VDD is 26 mV, or VEE is 50 mV. The value, when powered, can be set via the PMBus with the DEVICE_SETUP (D9h) command, which defaults to the 26 mV setting.

Once the desired setting is known, calculate the shunt based on that input voltage and maximum current. While the maximum load current in normal operation can be used to determine the required power rating for resistor R_S, basing it on the current limit value provides a more reliable design since the circuit can operate near the current limit threshold continuously. The resistor's surge capability must also be considered since the circuit breaker threshold is 1.9 or 3.7 times the current limit threshold.

Connections from R_S to the LM5064 should be made using Kelvin techniques. In the suggested layout of Figure 7 the small pads at the lower corners of the sense resistor connect only to the sense resistor terminals, and not to the traces carrying the high current. With this technique, only the voltage across the sense resistor is applied to SENSE_K, SENSE, and VEE_K, eliminating the voltage drop across the high current solder connections.

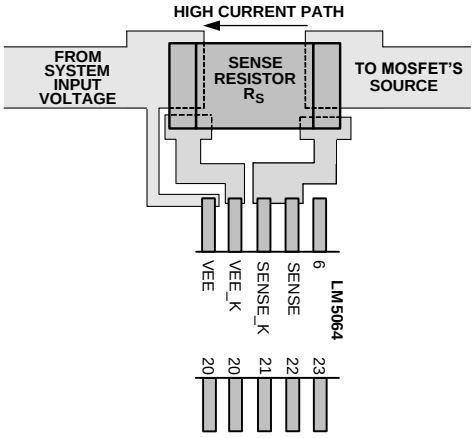


Figure 7. Sense Resistor Connections

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POWER LIMIT THRESHOLD

The LM5064 determines the power dissipation in the external MOSFET (Q_1) by monitoring the drain current (the current in R_S) and the V_{DS} of Q_1 (OUT to SENSE pins). The resistor at the PWR pin (R_{PWR}) sets the maximum power dissipation for Q_1, and is calculated from the following equation:

$$R_{PWR} = 1.25 \times 10^5 \times R_S \times P_{MOSFET(LIM)} \quad (2)$$

where $P_{MOSFET(LIM)}$ is the desired power limit threshold for Q_1, and R_S is the current sense resistor described in the CURRENT LIMIT (R_S) section. For example, if R_S is 3 mΩ, V_{IN} = 48V, and the desired power limit threshold is 80W, R_{PWR} calculates to 30.1 kΩ (standard 1% value). If Q_1's power dissipation reaches the threshold Q_1's gate is modulated to regulate the load current, keeping Q_1's power from exceeding the threshold. For proper operation of the power limiting feature, R_{PWR} must be ≤150 kΩ. While the power limiting circuit is active, the fault timer is active as described in the Fault Timer & Restart section. Typically, power limit is reached during startup, or if the output voltage falls due to a severe over-load or short circuit. The programmed maximum power dissipation should have a reasonable margin from the maximum power defined by the SOA chart, especially if retry is enabled, because the MOSFET will be repeatedly stressed during fault restart cycles. The MOSFET manufacturer should be consulted for guidelines. If the application does not require use of the power limit function the PWR pin can be left open. The accuracy of the power limit function at turn-on may degrade if a very low power dissipation limit is set. The reason for this caution is that the voltage across the sense resistor, which is monitored and regulated by the power limit circuit, is lowest at turn-on when the regulated current is at a minimum. The voltage across the sense resistor during power limit can be expressed as follows:

$$V_{SENSE} = I_{LIM} \times R_S = \frac{R_S \times P_{MOSFET(LIM)}}{V_{DS}} \quad (3)$$

where I_{LIM} is the current in R_S, and V_{DS} is the voltage across Q_1. For example, if the power limit is set at 80W with R_S = 3 mΩ, and V_{DS} = 48V the sense resistor voltage calculates to 5.0 mV, which is comfortably regulated by the LM5064. However, if the power limit is set lower (e.g., 25W), the sense resistor voltage calculates to 1.6 mV. At this low level noise and offsets within the LM5064 may degrade the power limit accuracy. To maintain accuracy, the sense resistor voltage should not be less than 3 mV.

TURN-ON TIME

The output turn-on time depends on whether the LM5064 operates in current limit, or in both power limit and current limit, during turn-on.

A) Turn-on with current limit only: The current limit threshold (I_{LIM}) is determined by the current sense resistor (R_S). If the current limit threshold is less than the current defined by the power limit threshold at maximum V_{DS} the circuit operates only at the current limit threshold during turn-on. Referring to Figure 8(A), as the load current reaches I_{LIM}, the gate-to-source voltage is controlled at GATE to maintain the current at I_{LIM}. As the output voltage reaches its final value (V_{DS} ≅ 0V) the drain current reduces to its normal operating value. The time for the OUT pin voltage to transition from zero volts to V_{SYS} is equal to:

$$t_{on} = \frac{|V_{SYS}| \quad C_L}{I_{LIM}} \quad (4)$$

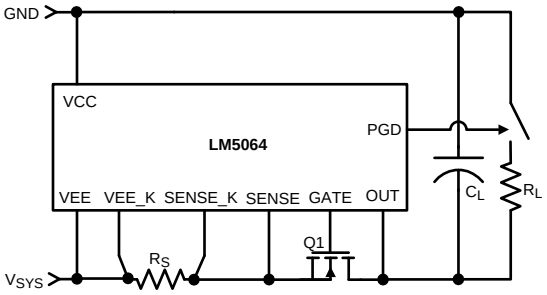
where C_L is the load capacitance. For example, if V_{SYS} = -48V, C_L = 200 µF, and I_{LIM} = 8.7A, t_{ON} calculates to 1.1 ms. The maximum instantaneous power dissipated in the MOSFET is 418W. This calculation assumes the time from t_1 to t_2 in Figure 9 (A) is small compared to t_{ON}, the load does not draw any current until after the output voltage has reached its final value, and PGD switches high (Figure 8 (A)). The Fault Timeout Period must be set longer than t_{ON} to prevent a fault shut-down before the turn-on sequence is complete.

If the load draws current during the turn-on sequence (Figure 8 (B)), the turn-on time is longer than the above calculation, and is approximately equal to:

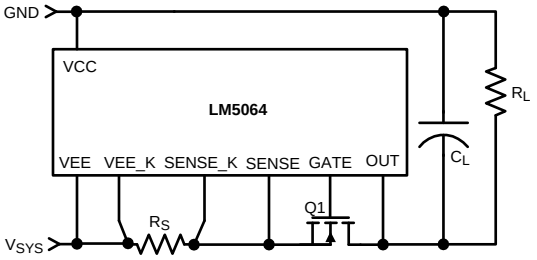
$$t_{ON} = -(R_L \times C_L) \times \ln\left[\frac{(I_{LIM} \times R_L) - |V_{SYS}|}{(I_{LIM} \times R_L)}\right] \quad (5)$$

where R_L is the load resistance. The Fault Timeout Period must be set longer than t_{ON} to prevent a fault shutdown before the turn-on sequence is complete.

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A. No Load Current During Turn-On



B. Load Draws Current During Turn-On

Figure 8. Current During Turn-On

B) Turn-On with Power Limit and Current Limit: The maximum allowed power dissipation in Q_1 ($P_{MOSFET(LIM)}$) is defined by the resistor at the PWR pin, and the current sense resistor R_S. See the POWER LIMIT THRESHOLD section. If the current limit threshold (I_{LIM}) is higher than the current defined by the power limit threshold at maximum V_{DS} ($P_{MOSFET(LIM)}/|V_{SYS}|$) the circuit operates initially in the power limit mode when the V_{DS} of Q_1 is high, and then transitions to current limit mode as the current increases to I_{LIM} and V_{DS} decreases. Assuming the load (R_L) is not connected during turn-on, the time for the output voltage to reach its final value is approximately equal to:

$$t_{ON} = \frac{C_L \times V_{SYS}^2}{2 \times P_{MOSFET(LIM)}} + \frac{C_L \times P_{MOSFET(LIM)}}{2 \times I_{LIM}^2} \quad (6)$$

For example, if V_{SYS} = -48V, C_L = 200 µF, I_{LIM} = 8.7A, and $P_{MOSFET(LIM)}$ = 80W, t_{ON} calculates to ≅3.0 ms, and the initial current level (I_P) is approximately 1.67A. The Fault Timeout Period must be set longer than t_{ON}.

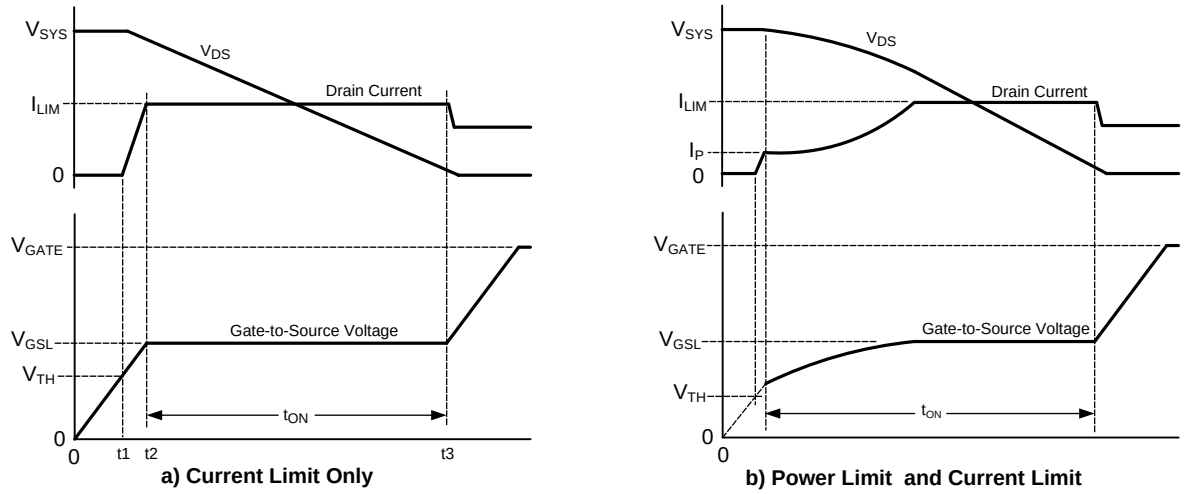


Figure 9. MOSFET Power Up Waveforms

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TIMER CAPACITOR, C_T

The TIMER pin capacitor (C_T) sets the timing for the insertion time delay, fault timeout period, and the restart timing of the LM5064.

A) Insertion Delay -Upon applying the system voltage (V_{SYS}) to the circuit, the external MOSFET (Q_1) is held off during the insertion time (t_1 in Figure 2) to allow ringing and transients at V_{SYS} to settle. Since each backplane's response to a circuit card plug-in is unique, the worst case settling time must be determined for each application. The insertion time starts when V_{SYS} reaches the POR threshold, at which time the internal 4.8 µA current source charges C_T from 0V to 3.9V. The required capacitor value is calculated from:

$$C_T = \frac{t_1 \times 4.8\,\mu A}{3.9V} = t_1 \times 1.2 \times 10^{-6} \quad (7)$$

For example, if the desired insertion delay is 125 ms, C_T calculates to 0.15 µF. At the end of the insertion delay, C_T is quickly discharged by a 1.5 mA current sink.

B) Fault Timeout Period -During in-rush current limiting or upon detection of a fault condition where the current limit and/or power limit circuits regulate the current through Q_1, the fault timer current source (74 µA) is switched on to charge C_T. The Fault Timeout Period is the time required for the TIMER pin voltage to reach 3.9V, at which time Q_1 is switched off. The required capacitor value for the desired Fault Timeout Period t_{FAULT} is calculated from:

$$C_T = \frac{t_{FAULT} \times 74\,\mu A}{3.9V} = t_{FAULT} \times 1.9 \times 10^{-5} \quad (8)$$

For example, if the desired Fault Timeout Period is 8 ms, C_T calculates to 0.15 µF. C_T is discharged by the 2.4 µA current sink at the end of the Fault Timeout Period. After the Fault Timeout Period, if $\overline{\text{RETRY}}$ = VDD, the LM5064 latches the GATE pin low until a power up sequence is initiated by external circuitry. When the Fault Timeout Period of the LM5064 expires, a restart sequence starts as described below (Restart Timing). During consecutive cycles of the restart sequence, the fault timeout period is shorter than the initial fault time out period described above by approximately 8% since the voltage at the TIMER pin starts ramping up from 0.3V rather than VEE.

Since the LM5064 normally operates in power limit and/or current limit during a power up sequence, the Fault Timeout Period **MUST** be longer than the time required for the output voltage to reach its final value. See the TURN-ON TIME section.

C) Restart Timing For the LM5064, after the Fault Timeout Period described above, C_T is discharged by the 2.4 µA current sink to 1.2V. The TIMER pin then cycles through seven additional charge/discharge cycles between 1.2V and 3.9V as shown in Figure 4. The restart time ends when the TIMER pin voltage reaches 0.3V during the final high-to-low ramp. The restart time, after the Fault Timeout Period, is equal to:

$$t_{RESTART} = C_T \times \left[\frac{7 \times 2.7V}{2.4\,\mu A} + \frac{7 \times 2.7V}{74\,\mu A} + \frac{3.6V}{2.4\,\mu A} \right] \quad (9)$$

$$= C_T \times 9.6 \times 10^6 \quad (10)$$

For example, if C_T = 0.15 µF, $t_{RESTART}$ = 1.4 seconds. At the end of the restart time, Q_1 is switched on. If the fault is still present, the fault timeout and restart sequence repeats. The on-time duty cycle of Q_1 is approximately 0.5% in this mode.

UVLO, OVLO

By programming the UVLO and OVLO thresholds the LM5064 enables the series pass device (Q_1) when the input supply voltage (V_{SYS}) is within the desired operational range. If V_{CC} is below the UVLO threshold, or above the OVLO threshold, Q_1 is switched off, denying power to the load. Hysteresis is provided for each threshold.

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Option A: The configuration shown in Figure 10 requires three resistors (R1-R3) to set the thresholds.

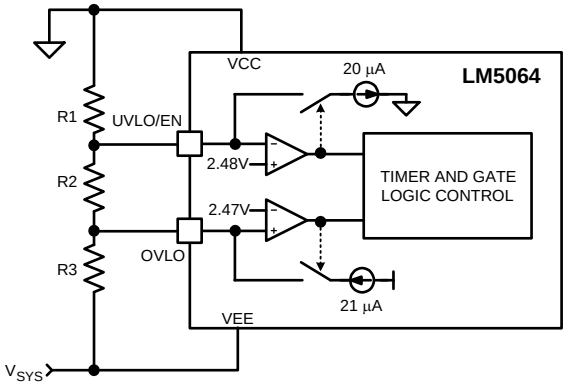


Figure 10. UVLO and OVLO Thresholds Set By R1-R3

The procedure to calculate the resistor values is as follows:

- Choose the upper UVLO threshold (V_{UVH}), and the lower UVLO threshold (V_{UVL}).

- Choose the upper OVLO threshold (V_{OVH}).

- The lower OVLO threshold (V_{OVL}) cannot be chosen in advance in this case, but is determined after the values for R1-R3 are determined. If V_{OVL} must be accurately defined in addition to the other three thresholds, see **Option B** below. The resistors are calculated as follows:

$$R1 = \frac{V_{UVH} - V_{UVL}}{20\,\mu A} = \frac{V_{UV(HYS)}}{20\,\mu A} \quad (11)$$

$$R3 = \frac{R1 \times V_{UVL} \times 2.47V}{V_{OVH} \times (V_{UVL} - 2.48V)} \quad (12)$$

$$R2 = \frac{2.48V \times R1}{V_{UVL} - 2.48V} - R3 \quad (13)$$

The lower OVLO threshold is calculated from:

$$V_{OVL} = \left[(R1 + R2) \times \left(\left(\frac{2.47V}{R3}\right) - 21\,\mu A\right)\right] + 2.47V \quad (14)$$

As an example, assume the application requires the following thresholds: V_{UVH} = 36V, V_{UVL} = 32V, V_{OVH} = 60V.

$$R1 = \frac{36V - 32V}{20\,\mu A} = \frac{4V}{20\,\mu A} = 200k \quad (15)$$

$$R3 = \frac{R1 \times 32V \times 2.47V}{60V \times (32V - 2.48)} = 8.93k\Omega \quad (16)$$

$$R2 = \frac{2.48V \times R1}{32V - 2.48V} - R3 = 7.87\,k\Omega \quad (17)$$

Using standard values of R1 = 200 kΩ, R2 = 8.87 kΩ, and R3 = 7.87 kΩ, the lower OVLO threshold calculates to 56V, and the OVLO hysteresis is 4.4V. Note that the OVLO hysteresis is always slightly greater than the UVLO hysteresis in this configuration. When the R1-R3 resistor values are known, the threshold voltages and hysteresis are calculated from the following:

$$V_{UVH} = 2.48V + R1 \times \left(\frac{2.48V}{R2 + R3} + 20\,\mu A\right) \quad (18)$$

$$V_{UVL} = \frac{2.48V \times (R1 + R2 + R3)}{R2 + R3} \quad (19)$$

$$V_{UV(HYS)} = R1 \times 20\ \mu A \quad (20)$$

$$V_{OVH} = \frac{2.47V \times (R1 + R2 + R3)}{R3} \quad (21)$$

$$V_{OVL} = \left(\frac{2.47V}{R3} - 21\,\mu A\right) \times (R1 + R2) + 2.47V \quad (22)$$

$$V_{OV(HYS)} = (R1 + R2) \times 21\ \mu A \quad (23)$$

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Option B: If all four thresholds must be accurately defined, the configuration in Figure 11 can be used.

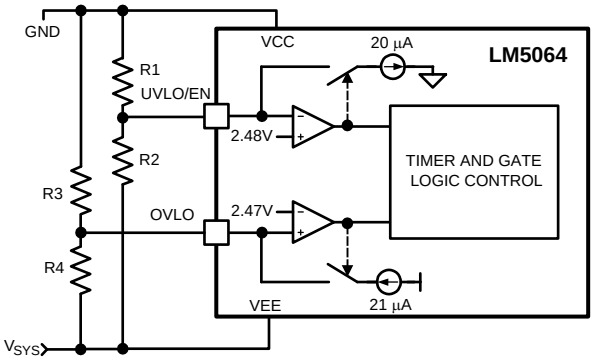


Figure 11. Programming the Four Thresholds

The four resistor values are calculated as follows: - Choose the upper and lower UVLO thresholds (V_{UVH}) and (V_{UVL}).

$$R1 = \frac{V_{UVH} - V_{UVL}}{20\,\mu A} = \frac{V_{UV(HYS)}}{20\,\mu A} \quad (24)$$

$$R2 = \frac{2.48V \times R1}{(V_{UVL} - 2.48V)} \quad (25)$$

- Choose the upper and lower OVLO threshold (V_{OVH}) and (V_{OVL}).

$$R3 = \frac{V_{OVH} - V_{OVL}}{21\,\mu A} = \frac{V_{OV(HYS)}}{21\,\mu A} \quad (26)$$

$$R4 = \frac{2.47V \times R3}{(V_{OVH} - 2.47V)} \quad (27)$$

As an example, assume the application requires the following thresholds: V_{UVH} = 36V, V_{UVL} = 32V, V_{OVH} = 60V, and V_{OVL} = 56V. Therefore $V_{UV(HYS)}$ = 4V, and $V_{OV(HYS)}$ = 4V. The resistor values are:

R1 = 200 kΩ, R2 = 16.8 kΩ

R3 = 190 kΩ, R4 = 8.2 kΩ

When the R1-R4 resistor values are known, the threshold voltages and hysteresis are calculated from the following:

$$V_{UVH} = 2.48V + \left[R1 \times \left(\frac{2.48V}{R2} + 20\,\mu A\right)\right] \quad (28)$$

$$V_{UVL} = \frac{2.48V \times (R1 + R2)}{R2} \quad (29)$$

$$V_{UV(HYS)} = R1 \times 20\ \mu A \quad (30)$$

$$V_{OVH} = \frac{2.47V \times (R3 + R4)}{R4} \quad (31)$$

$$V_{OVL} = 2.47V + \left[R3 \times \left(\frac{2.47V}{R4} - 21\,\mu A\right)\right] \quad (32)$$

Option C: The minimum UVLO level is obtained by connecting the UVLO/EN pin to VCC as shown in Figure 12. Q_1 is switched on when the VCC-VEE voltage reaches the POR_{EN} threshold (≅8.7V). The OVLO thresholds are set using R3, R4. Their values are calculated using the procedure in **Option B**.

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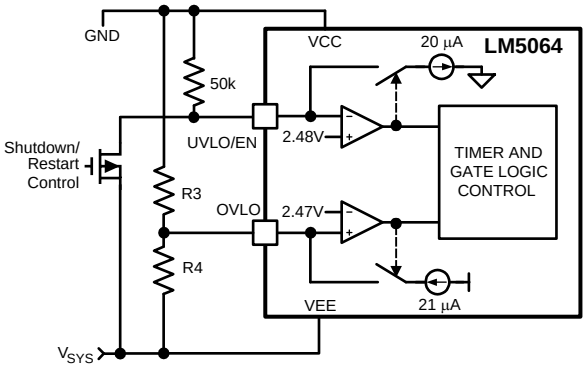


Figure 12. UVLO/EN = POR_{EN}

Option D: The OVLO function can be disabled by connecting the OVLO pin to VEE. The UVLO thresholds are set as described in **Option B** or **Option C**.

POWER GOOD PIN (PGD)

When the Q_1 V_{DS} voltage is below its threshold, the internal pull-down acting on the PGD pin is disabled, allowing PGD to rise to V_{PGD} through the pull-up resistor, R_{PG}, as shown in Figure 13. The pull-up voltage (V_{PGD}) can be as high as 80V, and can be higher or lower than the voltages at VCC and OUT. VDD is a convenient choice for V_{PGD} as it allows interface to low voltage logic and avoids glitching on PGD during power up. If a delay is required at PGD, suggested circuits are shown in Figure 14. In Figure 14(A), capacitor C_{PG} adds delay to the rising edge, but not to the falling edge. In Figure 14(B), the rising edge is delayed by R_{PG1} + R_{PG2} and C_{PG}, while the falling edge is delayed a lesser amount by R_{PG2} and C_{PG}. Adding a diode across R_{PG2} (Figure 14 (C)) allows for equal delays at the two edges, or a short delay at the rising edge and a long delay at the falling edge.

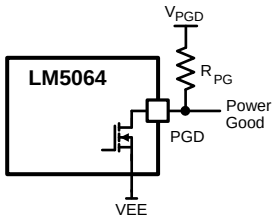
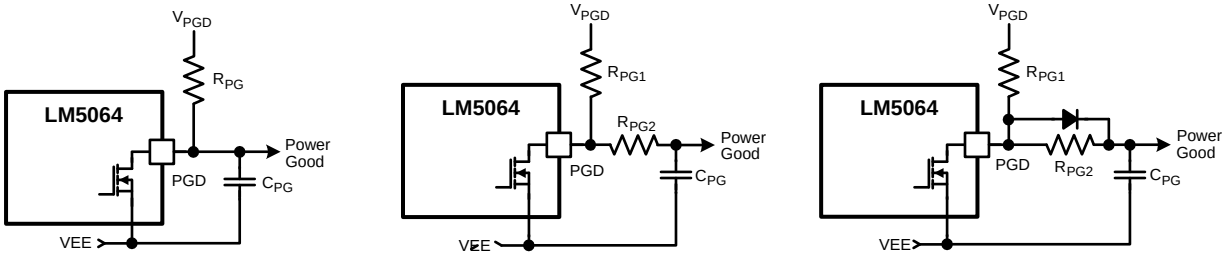


Figure 13. Power Good Output



a) Delay Rising Edge Only

b) Long delay at rising edge, short delay at falling edge

c) Short Delay at Rising Edge and Long Delay at Falling Edge, or Equal Delays

Figure 14. Adding Delay to the Power Good Output Pin

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SYSTEM CONSIDERATIONS

Continued proper operation of the LM5064 hot swap circuit requires a voltage clamping element present on the supply side of the connector into which the hot swap circuit is plugged in. A TVS (Transient Voltage Suppressor) is ideal, as depicted in Figure 15 as Z_1. The TVS is necessary to absorb the voltage transient generated whenever the hot swap circuit shuts off the load current. If the TVS is not present, inductance in the supply lines will generate a voltage transient at shutdown which can exceed the absolute maximum rating of the LM5064, resulting in its destruction. For low current solutions (<2A), a capacitor may be sufficient to limit the voltage surge, however this comes at the expense of input surge current on card insertion.

If the load powered by the LM5064 hot swap circuit has inductive characteristics, a Schottky diode (D_1) is required across the LM5064's output, along with some load capacitance (C_L). The capacitance and the diode are necessary to limit the negative excursion at the OUT pin when the load current is shut off. If the OUT pin transitions more than 0.3V negative the LM5064 can be permanently damaged. See Figure 15.

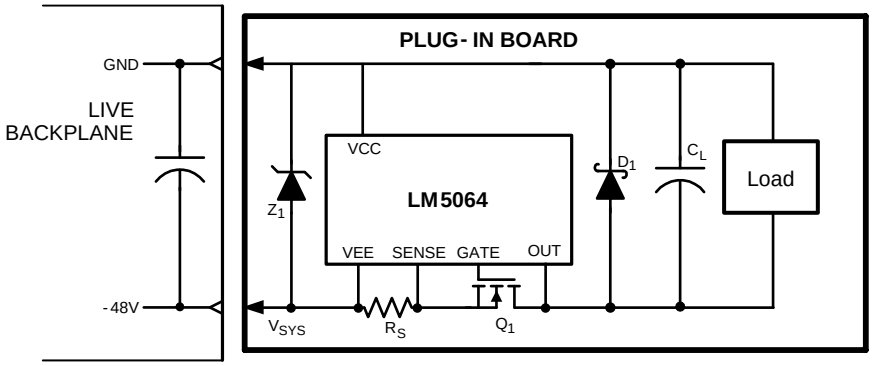
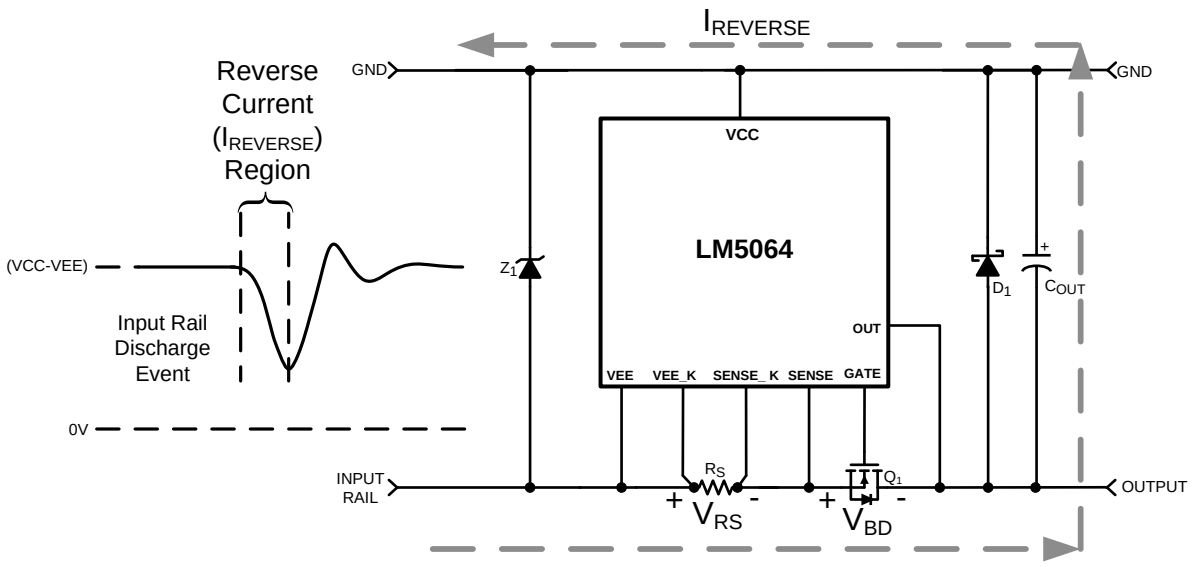


Figure 15. Output Diode Required for Inductive Loads

System Considerations During Surge Events

The control MOSFET, Q_1, has a body-diode, illustrated in Figure 16, where current can freely flow in the reverse direction. The most common cause of a reverse current is a discharge event at the input of the hot-swap circuit when the output capacitance discharges to the input. Normally, reverse current flow presents no issue for hot-swap devices during events such as shutdown and minor input power perturbations. However, extreme situations such as high energy lighting surge line disturbances can expose the hot-swap circuit to pulses of ultra fast - high amplitude reverse currents. It is common to observe current amplitudes on the order of 1000A in these situations. Figure 16 illustrates what an extreme input discharge event may look like and how it affects the circuit.

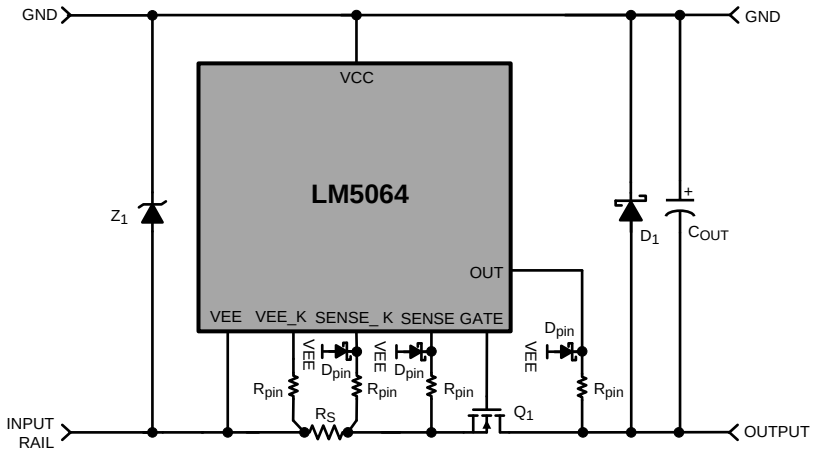
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As the input dips, the output capacitor discharges causing a transient reverse current flow.

Figure 16. Differential Voltage Across Sense Resistor

Figure 16 shows how the induced reverse current spike causes a differential voltage across the sense resistor, V_{RS}, and the Q_1 body-diode, V_{BD}. The transient reverse current, $I_{REVERSE}$, is approximately equal to $I_{REVERSE} = C_{OUT} \times dV_{IN}/dt$ because the output capacitor is discharged through the input. Faster discharge rates (dV_{IN}/dt) will induce larger $I_{REVERSE}$ currents. If $I_{REVERSE}$ is extremely high, it can cause a large negative voltage at the SENSE_K, SENSE, and OUT pins with respect to the VEE pin of the LM5064. If the negative absolute maximum voltage rating is greatly exceeded, harmful currents can flow into the affected pins. Series pin resistors can be implemented to limit the pin current caused by the negative voltage excursion. Schottky diodes may also be implemented to completely clamp the voltage at these pins. Figure 17 illustrates this.



Series resistors are used to limit harmful negative pin currents and schottky diodes are used to clamp the voltage at each pin.

Figure 17. Schottky Diodes Used to Clamp Pin Voltage

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A typical value of R_{pin} can be 22Ω to effectively limit the pin current during extreme negative voltage spikes. If schottky diodes are used, they only need to be applied to SENSE_K, SENSE, and OUT. Each schottky diode return pin should be coupled closely with the VEE plane to provide the most effective clamping. The schottky diode at OUT should be able to withstand at least 100V. VEE_K needs a series resistor even though it's not subjected to negative voltage spikes in order to balance the differential current sense voltage signal. Protecting the SENSE_K, SENSE, and OUT pins from negative voltage spikes will facilitate a robust hot-swap circuit and smooth operation during extreme reverse current surge events.

PC BOARD GUIDELINES

The following guidelines should be followed when designing the PC board for the LM5064:

- Place the LM5064 close to the board's input connector to minimize trace inductance from the connector to the MOSFET (Q_1).

- Place a TVS (Z_1), directly adjacent to the VCC and VEE pins of the LM5064 to help minimize voltage transients which may occur on the input supply line. The TVS should be chosen such that the peak V_{SYS} is just lower the TVS reverse-bias voltage. Transients of 20 volts or greater over the nominal input voltage can easily occur when the load current is shut off. A small capacitor may be sufficient for low current sense applications (I < 2A). It is recommended to test the V_{SYS} input voltage transient performance of the circuit by current limiting or shorting the load and measuring the peak input voltage transient.

- Place a 1 µF ceramic capacitor as close as possible to VREF pin.

- Place a 1 µF ceramic capacitor as close as possible to VDD pin.

- Minimize the inductance between the SENSE, SENSE_K, VEE_K, and VEE pins. There are anti-parallel diodes between these pins so any voltage greater than 0.3V in either polarity will cause significant current flow through the diodes, which can result in device failure. Do not place any resistors between these nodes.

- Minimize the impedance between the VEE_K and SENSE_K pins. There are anti-parallel diodes between these pins so any voltage greater than 0.3V in either polarity will cause significant current flow through the diodes, which can result in device failure.

- The sense resistor (R_S) should be placed close to the LM5064. A trace should connect the VEE source pin and OUT drain pad of Q_1 to the sense resistor to VEE_K and SENSE_K pins, respectively. Connect R_S using the Kelvin techniques shown in Figure 7.

- The high current path from the board's input to the load (via Q_1), and the return path, should be parallel and close to each other to minimize loop inductance.

- The termination connections for the various components around the LM5064 should be connected directly to each other, and to the LM5064's VEE pin connection, and then connected to V_{SYS} at one point. Do not connect the various component terminations to each other through the high current V_{SYS} line.

- Provide adequate thermal sinking for the series pass device (Q_1) to help reduce stresses during turn-on and turn-off.

- The board's edge connector can be designed such that the LM5064 detects via the UVLO/EN pin that the board is being removed, and responds by turning off the load before the supply voltage is disconnected. For example, in Figure 18, the voltage at the UVLO/EN pin goes to VEE before V_{SYS} is removed from the LM5064 as a result of the shorter edge connector pin. When the board is inserted into the edge connector, the system voltage is applied to the LM5064's V_{SYS} pin before the UVLO voltage is taken high, thereby allowing the LM5064 to turn on the output in a controlled fashion.

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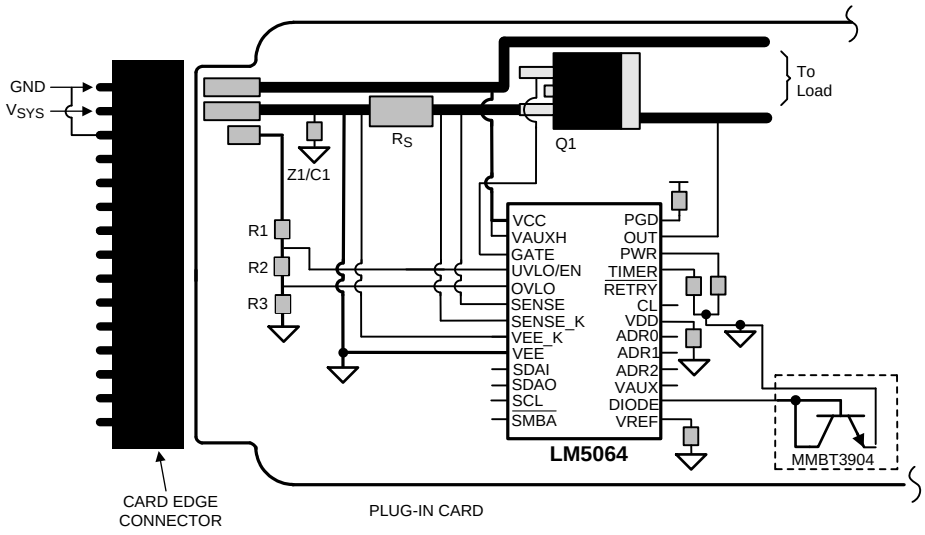


Figure 18. Recommended Board Connector Design

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PMBUS™ COMMAND SUPPORT

The device features an SMBus interface that allows the use of PMBus commands to set warn levels, error masks, and get telemetry on V_{IN} (V_{IN} = VAUXH = V_{VCC}-V_{VEE}), V_{OUT} (V_{OUT} = V_{VCC} - V_{VOUT}), I_{IN}, V_{AUX}, and P_{IN}. The supported PMBus commands are shown in Table 1.

Table 1. Supported PMBus Commands

Code	Name	Function	R/W	Number Of Data Bytes	Default Value
01h	OPERATION	Retrieves or stores the operation status.	R/W	1	80h
03h	CLEAR_FAULTS	Clears the status registers and re-arms the Black Box registers for updating.	Send Byte	0	
19h	CAPABILITY	Retrieves the device capability.	R	1	B0h
43h	VOUT_UV_WARN_LIMIT	Retrieves or stores output under-voltage warn limit threshold.	R/W	2	0000h
4Fh	OT_FAULT_LIMIT	Retrieves or stores over-temperature fault limit threshold.	R/W	2	0960h (150°C)
51h	OT_WARN_LIMIT	Retrieves or stores over-temperature warn limit threshold.	R/W	2	07D0h (125°C)
57h	VIN_OV_WARN_LIMIT	Retrieves or stores input over-voltage warn limit threshold.	R/W	2	0FFFh
58h	VIN_UV_WARN_LIMIT	Retrieves or stores input under-voltage warn limit threshold.	R/W	2	0000h
78h	STATUS_BYTE	Retrieves information about the parts operating status.	R	1	49h
79h	STATUS_WORD	Retrieves information about the parts operating status.	R	2	3849h
7Ah	STATUS_VOUT	Retrieves information about output voltage status.	R	1	00h
7Ch	STATUS_INPUT	Retrieves information about input status.	R	1	10h
7Dh	STATUS_TEMPERATURE	Retrieves information about temperature status.	R	1	00h
7Eh	STATUS_CML	Retrieves information about communications status.	R	1	00h
80h	STATUS_MFR_SPECIFIC	Retrieves information about circuit breaker and MOSFET shorted status.	R	1	10h
88h	READ_VIN	Retrieves input voltage measurement.	R	2	0000h
8Bh	READ_VOUT	Retrieves output voltage measurement.	R	2	0000h
8Dh	READ_TEMPERATURE_1	Retrieves temperature measurement.	R	2	0190h
99h	MFR_ID	Retrieves manufacturer ID in ASCII characters (NSC).	R	3	4Eh 53h 43h
9Ah	MFR_MODEL	Retrieves Part number in ASCII characters. (LM5064\0\0).	R	8	4Ch 4Dh 35h 30h 36h 36h 0h 0h
9Bh	MFR_REVISION	Retrieves part revision letter/number in ASCII (e.g., AA).	R	2	41h 41h
D0h	MFR_SPECIFIC_00 READ_VAUX	Retrieves auxiliary voltage measurement.	R	2	0000h
D1h	MFR_SPECIFIC_01 MFR_READ_IIN	Retrieves input current measurement.	R	2	0000h
D2h	MFR_SPECIFIC_02 MFR_READ_PIN	Retrieves input power measurement.	R	2	0000h
D3h	MFR_SPECIFIC_03 MFR_IIN_OC_WARN_LIMIT	Retrieves or stores input current limit warn threshold.	R/W	2	0FFFh
D4h	MFR_SPECIFIC_04 MFR_PIN_OP_WARN_LIMIT	Retrieves or stores input power limit warn threshold.	R/W	2	0FFFh
D5h	MFR_SPECIFIC_05 READ_PIN_PEAK	Retrieves measured peak input power measurement.	R	2	0000h

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Table 1. Supported PMBus Commands (continued)

Code	Name	Function	R/W	Number Of Data Bytes	Default Value
D6h	MFR_SPECIFIC_06 CLEAR_PIN_PEAK	Resets the contents of the peak input power register to zero.	Send Byte	0	
D7h	MFR_SPECIFIC_07 GATE_MASK	Allows the user to disable MOSFET gate shutdown for various fault conditions.	R/W	1	0000h
D8h	MFR_SPECIFIC_08 ALERT_MASK	Retrieves or stores user $\overline{\text{SMBA}}$ fault mask.	R/W	2	0820h
D9h	MFR_SPECIFIC_09 DEVICE_SETUP	Retrieves or stores information about number of retry attempts.	R/W	1	0000h
DAh	MFR_SPECIFIC_10 BLOCK_READ	Retrieves most recent diagnostic and telemetry information in a single transaction.	R	12	0190h 0000h 0000h 0000h 0000h 0000h
DBh	MFR_SPECIFIC_11 SAMPLES_FOR_AVG	Exponent value AVGN for number of samples to be averaged ($N = 2^{AVGN}$), range = 00h to 0Ch .	R/W	1	00h
DCh	MFR_SPECIFIC_12 READ_AVG_VIN	Retrieves averaged input voltage measurement.	R	2	0000h
DDh	MFR_SPECIFIC_13 READ_AVG_VOUT	Retrieves averaged output voltage measurement.	R	2	0000h
DEh	MFR_SPECIFIC_14 READ_AVG_IIN	Retrieves averaged input current measurement.	R	2	0000h
DFh	MFR_SPECIFIC_15 READ_AVG_PIN	Retrieves averaged input power measurement.	R	2	0000h
E0h	MFR_SPECIFIC_16 BLACK_BOX_READ	Captures diagnostic and telemetry information which are latched when the first $\overline{\text{SMBA}}$ event after faults are cleared.	R	12	0000h 0000h 0000h 0000h 0000h 0000h
E1h	MFR_SPECIFIC_17 DIAGNOSTIC_WORD_READ	Manufacturer-specific parallel of the STATUS_WORD to convey all FAULT/WARN data in a single transaction.	R	2	08E0h
E2h	MFR_SPECIFIC_18 AVG_BLOCK_READ	Retrieves most recent average telemetry and diagnostic information in a single transaction.	R	12	0000h 0000h 0000h 0000h 0000h 0000h

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STANDARD PMBUS COMMANDS

OPERATION (01h)

The OPERATION command is a standard PMBus command that controls the MOSFET switch. This command may be used to switch the MOSFET ON and OFF under host control. It is also used to re-enable the MOSFET after a fault triggered shutdown. Writing an OFF command, followed by an ON command, will clear all faults and re-enable the device. Writing only an ON after a fault-triggered shutdown will not clear the fault registers or re-enable the device. The OPERATION command is issued with the write byte protocol.

Table 2. Recognized OPERATION Command Values

Value	Meaning	Default
80h	Switch ON	80h
00h	Switch OFF	n/a

CLEAR FAULTS (03h)

The CLEAR_FAULTS command is a standard PMBus command that resets all stored warning and fault flags and the SMBA signal. If a fault or warning condition still exists when the CLEAR_FAULTS command is issued, the SMBA signal may not clear or will re-assert almost immediately. Issuing a CLEAR_FAULTS command will not cause the MOSFET to switch back on in the event of a fault turnoff - that must be done by issuing an OPERATION command after the fault condition is cleared. This command uses the PMBus send byte protocol.

CAPABILITY (19h)

The CAPABILITY command is a standard PMBus command that returns information about the PMBus functions supported by the LM5064. This command is read with the PMBus read byte protocol.

Table 3. CAPABILITY Register

Value	Meaning	Default
B0h	Supports Packet Error Check, 400Kbits/sec, Supports SMBus Alert	B0h

VOUT_UV_WARN_LIMIT (43h)

The VOUT_UV_WARN_LIMIT command is a standard PMBus command that allows configuring or reading the threshold for the VOUT under-voltage Warning detection. Reading and writing to this register should use the coefficients shown in Table 41. Accesses to this command should use the PMBus read or write word protocol. If the measured value of VOUT falls below the value in this register, VOUT UV Warn flags are set and the SMBA signal is asserted.

Table 4. VOUT_UV_WARN_LIMIT Register

Value	Meaning	Default
1h – 0FFFh	VOUT Under-Voltage Warning detection threshold	0000h (disabled)
0000h	VOUT Under-Voltage Warning disabled	n/a

OT_FAULT_LIMIT (4Fh)

The OT_FAULT_LIMIT command is a standard PMBus command that allows configuring or reading the threshold for the over-temperature fault detection. Reading and writing to this register should use the coefficients shown in Table 41. Accesses to this command should use the PMBus read or write word protocol. If the measured temperature exceeds this value, an over-temperature fault is triggered and the MOSFET is switched off, OT FAULT flags set, and the SMBA signal asserted. After the measured temperature falls below the value in this register, the MOSFET may be switched back on with the OPERATION command. A single temperature measurement is an average of 16 round-robin cycles; therefore, the minimum temperature fault detection time is 16 ms.

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Table 5. OT_FAULT_LIMIT Register

Value	Meaning	Default
0h – 0FFEh	Over-temperature Fault threshold value	0960h (150°C)
0FFFh	Over-temperature Fault detection disabled	n/a

OT_WARN_LIMIT (51h)

The OT_WARN_LIMIT command is a standard PMBus command that allows configuring or reading the threshold for the over-temperature warning detection. Reading and writing to this register should use the coefficients shown in Table 41. Accesses to this command should use the PMBus read or write word protocol. If the measured temperature exceeds this value, an over-temperature warning is triggered and the OT WARN flags set in the respective registers and the SMBA signal asserted. A single temperature measurement is an average of 16 round-robin cycles; therefore, the minimum temperature warn detection time is 16 ms.

Table 6. OT_WARN_LIMIT Register

Value	Meaning	Default
0h – 0FFEh	Over-Temperature Warn threshold value	07D0h (125°C)
0FFFh	Over-Temperature Warn detection disabled	n/a

VIN_OV_WARN_LIMIT (57h)

The VIN_OV_WARN_LIMIT command is a standard PMBus command that allows configuring or reading the threshold for the VIN over-voltage warning detection. Reading and writing to this register should use the coefficients shown in Table 41. Accesses to this command should use the PMBus read or write word protocol. If the measured value of VIN falls below the value in this register, VIN OV Warn flags are set in the respective registers and the SMBA signal is asserted.

Table 7. VIN_OV_WARN_LIMIT Register

Value	Meaning	Default
0h – 0FFEh	VIN Over-Voltage Warning detection threshold	0FFFh (disabled)
0FFFh	VIN Over-Voltage Warning disabled	n/a

VIN_UV_WARN_LIMIT (58h)

The VIN_UV_WARN_LIMIT command is a standard PMBus command that allows configuring or reading the threshold for the VIN under-voltage warning detection. Reading and writing to this register should use the coefficients shown in Table 41. Accesses to this command should use the PMBus read or write word protocol. If the measured value of VIN falls below the value in this register, VIN UV Warn flags are set in the respective register, and the SMBA signal is asserted.

Table 8. VIN_UV_WARN_LIMIT Register

Value	Meaning	Default
1h – 0FFFh	VIN Under-Voltage Warning detection threshold	0000h (disabled)
0000h	VIN Under-Voltage Warning disabled	n/a

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STATUS_BYTE (78h)

The STATUS BYTE is a standard PMBus command that returns the value of a number of flags indicating the state of the LM5064. Accesses to this command should use the PMBus read byte protocol. To clear bits in this register, the underlying fault should be removed on the system and a CLEAR_FAULTS command issued.

Table 9. STATUS_BYTE Definitions

Bit	NAME	Meaning	Default
7	BUSY	Not Supported, always 0	0
6	OFF	This bit is asserted if the MOSFET is not switched on for any reason.	1
5	VOUT OV	Not Supported, always 0	0
4	IOUT OC	Not Supported, always 0	0
3	VIN UV FAULT	A VIN Under-Voltage Fault has occurred	1
2	TEMPERATURE	A Temperature Fault or Warning has occurred	0
1	CML	A Communication Fault has occurred	0
0	None of the Above	A fault or warning not listed in bits [7:1] has occurred	1

STATUS_WORD (79h)

The STATUS_WORD command is a standard PMBus command that returns the value of a number of flags indicating the state of the LM5064. Accesses to this command should use the PMBus read word protocol. To clear bits in this register, the underlying fault should be removed and a CLEAR _FAULTS command issued. The INPUT and VIN UV flags will default to 1 on startup, however, they will be cleared to 0 after the first time the input voltage exceeds the resistor-programmed UVLO threshold.

Table 10. STATUS_WORD Definitions

Bit	NAME	Meaning	Default
15	VOUT	An output voltage fault or warning has occurred	0
14	IOUT/POUT	Not Supported, always 0	0
13	INPUT	An input voltage or current fault has occurred	1
12	MFR	A Manufacturer Specific Fault or Warning has occurred	1
11	$\overline{\text{POWER GOOD}}$	The Power Good signal has been negated	1
10	FANS	Not Supported, always 0	0
9	OTHER	Not Supported, always 0	0
8	UNKNOWN	Not Supported, always 0	0
7	BUSY	Not Supported, always 0	0
6	OFF	This bit is asserted if the MOSFET is not switched on for any reason.	1
5	VOUT OV	Not Supported, always 0	0
4	IOUT OC	Not Supported, always 0	0
3	VIN UV FAULT	A VIN Under-Voltage Fault has occurred	1
2	TEMPERATURE	A Temperature Fault or Warning has occurred	0
1	CML	A Communication Fault has occurred	0
0	None of the Above	A fault or warning not listed in bits [7:1] has occurred	1

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STATUS_VOUT (7Ah)

The STATUS_VOUT command is a standard PMBus command that returns the value of the VOUT UV Warn flag. Accesses to this command should use the PMBus read byte protocol. To clear bits in this register, the underlying fault should be cleared and a CLEAR_FAULTS command issued.

Table 11. STATUS_VOUT Definitions

Bit	NAME	Meaning	Default
7	VOUT OV Fault	Not Supported, always 0	0
6	VOUT OV Warn	Not Supported, always 0	0
5	VOUT UV Warn	A VOUT Under-Voltage Warning has occurred	0
4	VOUT UV Fault	Not Supported, always 0	0
3	VOUT Max	Not Supported, always 0	0
2	TON Max Fault	Not Supported, always 0	0
1	TOFF Max Fault	Not Supported, always 0	0
0	VOUT Tracking Error	Not Supported, always 0	0

STATUS_INPUT (7Ch)

The STATUS_INPUT command is a standard PMBus command that returns the value of a number of flags related to input voltage, current, and power. Accesses to this command should use the PMBus read byte protocol. To clear bits in this register, the underlying fault should be cleared and a CLEAR_FAULTS command issued. The VIN UV Warn flag will default to 1 on startup, however, it will be cleared to 0 after the first time the input voltage increases above the resistor-programmed UVLO threshold.

Table 12. STATUS_INPUT Definitions

Bit	NAME	Meaning	Default
7	VIN OV Fault	A VIN Over-Voltage Fault has occurred	0
6	VIN OV Warn	A VIN Over-Voltage Warning has occurred	0
5	VIN UV Warn	A VIN Under-Voltage Warning has occurred	1
4	VIN UV Fault	A VIN Under-Voltage Fault has occurred	0
3	Insufficient Voltage	Not Supported, always 0	0
2	IIN OC Fault	An IIN Over-Current Fault has occurred	0
1	IIN OC Warn	An IIN Over-Current Warning has occurred	0
0	PIN OP Warn	A PIN Over-Power Warning has occurred	0

STATUS_TEMPERATURE (7dh)

The STATUS_TEMPERATURE is a standard PMBus command that returns the value of the of a number of flags related to the temperature telemetry value. Accesses to this command should use the PMBus read byte protocol. To clear bits in this register, the underlying fault should be cleared and a CLEAR_FAULTS command issued.

Table 13. STATUS_TEMPERATURE Definitions

Bit	NAME	Meaning	Default
7	Overtemp Fault	An Over-Temperature Fault has occurred	0
6	Overtemp Warn	An Over-Temperature Warning has occurred	0
5	Undertemp Warn	Not Supported, always 0	0
4	Undertemp Fault	Not Supported, always 0	0
3	reserved	Not Supported, always 0	0
2	reserved	Not Supported, always 0	0
1	reserved	Not Supported, always 0	0
0	reserved	Not Supported, always 0	0

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STATUS_CML (7Eh)

The STATUS_CML is a standard PMBus command that returns the value of a number of flags related to communication faults. Accesses to this command should use the PMBus read byte protocol. To clear bits in this register, a CLEAR_FAULTS command should be issued.

Table 14. STATUS_CML Definitions

Bit	NAME	Default
7	Invalid or unsupported command received	0
6	Invalid or unsupported data received	0
5	Packet Error Check failed	0
4	Not supported, always 0	0
3	Not supported, always 0	0
2	Not supported, always 0	0
1	Miscellaneous communications fault has occurred	0
0	Not supported, always 0	0

STATUS_MFR_SPECIFIC (80h)

The STATUS_MFR_SPECIFIC command is a standard PMBus command that contains manufacturer specific status information. Accesses to this command should use the PMBus read byte protocol. To clear bits in this register, the underlying fault should be removed and a CLEAR_FAULTS command should be issued.

Table 15. STATUS_MFR_SPECIFIC Definitions

Bit	Meaning	Default
7	Circuit breaker fault	0
6	Ext. MOSFET shorted fault	0
5	Not Supported, Always 0	0
4	Defaults loaded	1
3	Not supported: Always 0	0
2	Not supported: Always 0	0
1	Not supported: Always 0	0
0	Not supported: Always 0	0

READ_VIN (88h)

The READ_VIN command is a standard PMBus command that returns the 12-bit measured value of the input voltage. Reading this register should use the coefficients shown in Table 41. Accesses to this command should use the PMBus read word protocol. This value is also used internally for the VIN Over and Under-Voltage Warning detection.

Table 16. READ_VIN Register

Value	Meaning	Default
0h – 0FFFh	Measured value for VIN	0000h

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READ_VOUT (8Bh)

The READ_VOUT command is a standard PMBus command that returns the 12-bit measured value of the output voltage. Reading this register should use the coefficients shown in Table 41. Accesses to this command should use the PMBus read word protocol. This value is also used internally for the VOUT Under-Voltage Warning detection.

Table 17. READ_VOUT Register

Value	Meaning	Default
0h – 0FFFh	Measured value for VOUT	0000h

READ_TEMPERATURE_1 (8Dh)

The READ_TEMPERATURE_1 command is a standard PMBus command that returns the signed value of the temperature measured by the external temperature sense diode. Reading this register should use the coefficients shown in Table 41. Accesses to this command should use the PMBus read word protocol. This value is also used internally for the Over-Temperature Fault and Warning detection. This data has a range of -256°C to + 255°C after the coefficients are applied.

Table 18. READ_TEMPERATURE_1 Register

Value	Meaning	Default
0h – 0FFFh	Measured value for TEMPERATURE	0000h

MFR_ID (99h)

The MFR_ID command is a standard PMBus command that returns the identification of the manufacturer. To read the MFR_ID, use the PMBus block read protocol.

Table 19. MFR_ID Register

Byte	Name	Value
0	Number of bytes	03h
1	MFR ID-1	4Eh ‘N’
2	MFR ID-2	53h ‘S’
3	MFR ID-3	43h ‘C’

MFR_MODEL (9Ah)

The MFR_MODEL command is a standard PMBus command that returns the part number of the chip. To read the MFR_MODEL, use the PMBus block read protocol.

Table 20. MFR_MODEL Register

Byte	Name	Value
0	Number of bytes	08h
1	MFR ID-1	4Ch ‘L’
2	MFR ID-2	4Dh ‘M’
3	MFR ID-3	35h ‘5’
4	MFR ID-4	30h ‘0’
5	MFR ID-5	36h ‘6’
6	MFR ID-6	36h ‘4’
7	MFR ID-7	00h
8	MFR ID-8	00h

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MFR_REVISION (9Bh)

The MFR_REVISION command is a standard PMBus command that returns the revision level of the part. To read the MFR_REVISION, use the PMBus block read protocol.

Table 21. MFR_REVISION Register

Byte	Name	Value
0	Number of bytes	02h
1	MFR ID-1	41h 'A'
2	MFR ID-2	41h 'A'

MANUFACTURER SPECIFIC PMBUS™ COMMANDS

MFR_SPECIFIC_00: READ_VAUX (D0h)

The READ_VAUX command will report the 12-bit ADC measured auxiliary voltage. Voltages greater than or equal to 2.97V to VEE will be reported at plus full scale (0FFFh). Voltages less than or equal to 0V referenced to VEE will be reported as 0 (0000h). To read data from the READ_VAUX command, use the PMBus Read Word protocol.

Table 22. READ_VAUX Register

Value	Meaning	Default
0h – 0FFFh	Measured value for VAUX input	0000h

MFR_SPECIFIC_01: MFR_READ_IIN (D1h)

The MFR_READ_IIN command will report the 12-bit ADC measured current sense voltage. To read data from the MFR_READ_IIN command, use the PMBus Read Word protocol. Reading this register should use the coefficients shown in Table 41. Please see the section on coefficient calculations to calculate the values to use.

Table 23. MFR_READ_IIN Register

Value	Meaning	Default
0h – 0FFFh	Measured value for input current sense voltage	0000h

MFR_SPECIFIC_02: MFR_READ_PIN (D2h)

The MFR_READ_PIN command will report the upper 12 bits of the VIN x IIN product as measured by the 12-bit ADC. To read data from the MFR_READ_PIN command, use the PMBus Read Word protocol. Reading this register should use the coefficients shown in Table 41. Please see the section on coefficient calculations to calculate the values to use.

Table 24. MFR_READ_PIN Register

Value	Meaning	Default
0h – 0FFFh	Value for input current x input voltage	0000h

MFR_SPECIFIC_03: MFR_IN_OC_WARN_LIMIT (D3h)

The MFR_IIN_OC_WARN_LIMIT PMBus command sets the input over-current warning threshold. In the event that the input current rises above the value set in this register, the IIN over-current flags are set in the respective registers and the $\overline{\text{SMBA}}$ is asserted. To access the MFR_IIN_OC_WARN_LIMIT register, use the PMBus Read/Write Word protocol. Reading/writing to this register should use the coefficients shown in Table 41.

Table 25. MFR_IIN_OC_WARN_LIMIT Register

Value	Meaning	Default
0h – 0FFEh	Value for input over-current warn limit	0FFFh
0FFFh	Input over-current warning disabled	n/a

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MFR_SPECIFIC_04: MFR_PIN_OP_WARN_LIMIT (D4h)

The MFR_PIN_OP_WARN_LIMIT PMBus command sets the input over-power warning threshold. In the event that the input power rises above the value set in this register, the PIN over-power flags are set in the respective registers and the SMBA is asserted. To access the MFR_PIN_OP_WARN_LIMIT register, use the PMBus Read/Write Word protocol. Reading/writing to this register should use the coefficients shown in Table 41.

Table 26. MFR_PIN_OPWARN_LIMIT Register

Value	Meaning	Default
0h – 0FFEh	Value for input over-power warn limit	0FFFh
0FFFh	Input over-power warning disabled	n/a

MFR_SPECIFIC_05: READ_PIN_PEAK (D5h)

The READ_PIN_PEAK command will report the maximum input power measured since a Power On reset or the last CLEAR_PIN_PEAK command. To access the READ_PIN_PEAK command, use the PMBus Read Word protocol. Use the coefficients shown in Table 41.

Table 27. READ_PIN_PEAK Register

Value	Meaning	Default
0h – 0FFEh	Maximum Value for input current x input voltage since reset or last clear	0h

MFR_SPECIFIC_06: CLEAR_PIN_PEAK (D6h)

The CLEAR_PIN_PEAK command will clear the PIN PEAK register. This command uses the PMBus Send Byte protocol.

MFR_SPECIFIC_07: GATE_MASK (D7h)

The GATE_MASK register allows the hardware to prevent fault conditions from switching off the MOSFET. When the bit is high, the corresponding FAULT has no control over the MOSFET gate. All status registers will still be updated (STATUS, DIAGNOSTIC) and an SMBA will still be asserted. This register is accessed with the PMBus Read / Write Byte protocol.

The IIN/PFET Fault refers to the input current fault and the MOSFET power dissipation fault. There is no input power fault detection; only input power warning detection.

WARNING

Inhibiting the MOSFET switch off in response to over-current or circuit breaker fault conditions will likely result in the destruction of the MOSFET! This functionality should be used with great care and supervision!

Table 28. MFR_SPECIFIC_07 GATE MASK Definitions

Bit	NAME	Default
7	Not used, always 0	0
6	Not used, always 0	0
5	VIN UV FAULT	0
4	VIN OV FAULT	0
3	IIN/PFET FAULT	0
2	OVERTEMP FAULT	0
1	Not used, always 0	0
0	CIRCUIT BREAKER FAULT	0

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MFR_SPECIFIC_08: ALERT_MASK (D8h)

The ALERT_MASK command is used to mask the $\overline{\text{SMBA}}$ when a specific fault or warning has occurred. Each bit corresponds to one of the 14 different analog and digital faults or warnings that would normally result in an $\overline{\text{SMBA}}$ being asserted. When the corresponding bit is high, that condition will not cause the $\overline{\text{SMBA}}$ to be asserted. If that condition occurs, the registers where that condition is captured will still be updated (STATUS registers, DIAGNOSTIC_WORD) and the external MOSFET gate control will still be active (VIN_OV_FAULT, VIN_UV_FAULT, IIN/PFET_FAULT, CB_FAULT, OT_FAULT). This register is accessed with the PMBus Read / Write Word protocol. The VIN UNDERVOLTAGE FAULT flag will default to 1 on startup, however, it will be cleared to 0 after the first time the input voltage increases above the resistor-programmed UVLO threshold.

Table 29. ALERT_MASK Definitions

BIT	NAME	DEFAULT
15	VOUT UNDERVOLTAGE WARN	0
14	IIN LIMIT WARN	0
13	VIN UNDERVOLTAGE WARN	0
12	VIN OVERVOLTAGE WARN	0
11	$\overline{\text{POWER GOOD}}$	1
10	OVERTEMP WARN	0
9	Not Used	0
8	OVERPOWER LIMIT WARN	0
7	Not Used	0
6	EXT_MOSFET_SHORTED	0
5	VIN UNDERVOLTAGE FAULT	1
4	VIN OVERVOLTAGE FAULT	0
3	IIN/PFET FAULT	0
2	OVERTEMPERATURE FAULT	0
1	CML FAULT (Communications Fault)	0
0	CIRCUIT BREAKER FAULT	0

MFR_SPECIFIC_09: DEVICE_SETUP (D9h)

The DEVICE_SETUP command may be used to override pin settings to define operation of the LM5064 under host control. This command is accessed with the PMBus read / write byte protocol.

Table 30. DEVICE_SETUP Byte Format

Bit	Name	Meaning
7:5	Retry setting	111 = Unlimited retries
		110 = Retry 16 times
		101 = Retry 8 times
		100 = Retry 4 times
		011 = Retry 2 times
		010 = Retry 1 time
		001 = No retries
		000 = Pin configured retries
4	Current limit setting	0 = High setting (50 mV)
		1 = Low setting (26 mV)
3	CB/CL Ratio	0 = Low setting (1.8/1.9x for 26/50 mV)
		1 = High setting (3.6/3.7x for 26/50 mV)
2	Current Limit Configuration	0 = Use pin settings
		1 = Use SMBus settings
1	Unused	

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Table 30. DEVICE_SETUP Byte Format (continued)

Bit	Name	Meaning
0	Unused	

In order to configure the Current Limit Setting via this register, it is necessary to set the Current Limit Configuration bit (2) to 1 to enable the register to control the current limit function and the Current Limit Setting bit (4) to select the desired setting. If the Current Limit Configuration bit is not set, the pin setting will be used. The Circuit Breaker to Current Limit ratio value is set by the CB / CL Ratio bit (3). Note that if the Current Limit Configuration is changed, the samples for the telemetry averaging function will not be reset. It is recommeded to allow a full averaging update period with the new Current Limit Configuration before processing the averaged data.

Note that the Current Limit Configuration affects the coefficients used for the Current and Power measurements and warning registers.

MFR_SPECIFIC_10: BLOCK_READ (DAh)

The BLOCK_READ command concatenates the DIAGNOSTIC_WORD with input and output telemetry information (IIN, VOUT, VIN, PIN) as well as READ_TEMPERATURE_1 to capture all of the operating information of the LM5064 in a single SMBus transaction. The block is 12 bytes long with telemetry information being sent out in the same manner as if an individual READ_XXX command had been issued (shown below). The contents of the block read register are updated every clock cycle (85ns) as long as the SMBus interface is idle. BLOCK_READ also ensures that the VIN, VOUT, IIN and PIN measurements are all time-aligned. If separate commands are used, individual samples may not be time-aligned, because of the delay necessary for the communication protocol.

The Block Read command is read via the PMBus block read protocol.

Table 31. BLOCK_READ Register Format

Byte Count (always 12)	(1 byte)
DIAGNOSTIC_WORD	(1 Word)
IIN_BLOCK	(1 Word)
VOUT_BLOCK	(1 Word)
VIN_BLOCK	(1 Word)
PIN_BLOCK	(1 Word)
TEMP_BLOCK	(1 Word)

MFR_SPECIFIC_11: SAMPLES_FOR_AVG (DBh)

The SAMPLES_FOR_AVG command is a manufacturer specific command for setting the number of samples used in computing the average values for IIN, VIN, VOUT, PIN. The decimal equivalent of the AVGN nibble is the power of 2 samples, (e.g. AVGN=12 equates to N=4096 samples used in computing the average). The LM5064 supports average numbers of 1, 2, 4, 8, 16, 32, 64, 128, 256, 512, 1024, 2048, 4096. The SAMPLES_FOR_AVG number applies to average values of IIN, VIN, VOUT, PIN simultaneously. The LM5064 uses simple averaging. This is accomplished by summing consecutive results up to the number programmed, then dividing by the number of samples. Averaging is calculated according to the following sequence:

$$Y = (X_{(N)} + X_{(N-1)} + ... + X_{(0)}) / N \quad (33)$$

When the averaging has reached the end of a sequence (for example, 4096 samples are averaged), then a whole new sequence begins that will require the same number of samples (in this example, 4096) to be taken before the new average is ready.

Table 32. SAMPLES_FOR_AVG Register

AVGN	$N = 2^{AVGN}$	Averaging/Register Update Period (ms)
0000	1	1
0001	2	2
0010	4	4

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Table 32. SAMPLES_FOR_AVG Register (continued)

AVGN	$N = 2^{AVGN}$	Averaging/Register Update Period (ms)
0011	8	8
0100	16	16
0101	32	32
0110	64	64
0111	128	128
1000	256	256
1001	512	512
1010	1024	1024
1011	2048	2048
1100	4096	4096

Note that a change in the SAMPLES_FOR_AVG register will not be reflected in the average telemetry measurements until the present averaging interval has completed. The default setting for AVGN is 0000, therefore, the average telemetry will mirror the instantaneous telemetry until a value higher than zero is programmed.

The SAMPLES_FOR_AVG register is accessed via the PMBus read / write byte protocol.

Table 33. SAMPLES_FOR_AVG Register

Value	Meaning	Default
0h – 0Ch	Exponent (AVGN) for number of samples to average over	00h

MFR_SPECIFIC_12: READ_AVG_VIN (DCh)

The READ_AVG_VIN command will report the 12-bit ADC measured input average voltage. If the data is not ready, the returned value will be the previous averaged data. However, if there is no previously averaged data, the default value (0000h) will be returned. This data is read with the PMBus Read Word protocol. This register should use the coefficients shown in Table 41.

Table 34. READ_AVG_VIN Register

Value	Meaning	Default
0h – 0FFFh	Average of measured values for input voltage	0000h

MFR_SPECIFIC_13: READ_AVG_VOUT (DDh)

The READ_AVG_VOUT command will report the 12-bit ADC measured OUT pin average voltage. The returned value will be the default value (0000h) or previous data when the average data is not ready. This data is read with the PMBus Read Word protocol. This register should use the coefficients shown in Table 41.

Table 35. READ_AVG_VOUT Register

Value	Meaning	Default
0h – 0FFFh	Average of measured values for output voltage	0000h

MFR_SPECIFIC_14: READ_AVG_IIN (DEh)

The READ_AVG_IIN command will report the 12-bit ADC measured VAUXH average voltage. The returned value will be the default value (0000h) or previous data when the average data is not ready. This data is read with the PMBus Read Word protocol. This register should use the coefficients shown in Table 41.

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Table 36. READ_AVG_IIN Register

Value	Meaning	Default
0h – 0FFFh	Average of measured values for current sense voltage	0000h

MFR_SPECIFIC_15: READ_AVG_PIN

The READ_AVG_PIN command will report the upper 12-bits of the average VIN x IIN product as measured by the 12-bit ADC. You will read the default value (0000h) or previous data when the average data is not ready. This data is read with the PMBus Read Word protocol. This register should use the coefficients shown in Table 41.

Table 37. READ_AVG_PIN Register

Value	Meaning	Default
0h – 0FFFh	Average of measured value for input voltage x input current sense voltage	0000h

MFR_SPECIFIC_16: BLACK_BOX_READ (E0h)

The BLACK BOX READ command retrieves the BLOCK READ data which was latched in at the first assertion of SMBA by the LM5064. It is re-armed with the CLEAR_FAULTS command. It is the same format as the BLOCK_READ registers, the only difference being that its contents are updated with the SMBA edge rather than the internal clock edge. This command is read with the PMBus Block Read protocol.

MFR_SPECIFIC_17: READ_DIAGNOSTIC_WORD (E1h)

The READ_DIAGNOSTIC_WORD PMBus command will report all of the LM5064 faults and warnings in a single read operation. The standard response to the assertion of the SMBA signal of issuing multiple read requests to various status registers can be replaced by a single word read to the DIAGNOSTIC_WORD register. The READ_DIAGNOSTIC_WORD command should be read with the PMBus Read Word protocol. The READ_DIAGNOSTIC_WORD is also returned in the BLOCK_READ, BLACK_BOX_READ, and AVG_BLOCK_READ operations.

Table 38. DIAGNOSTIC_WORD Format

Bit	Meaning	Default
15	VOUT UNDERVOLTAGE WARN	0
14	OC/OP WARN	0
13	VIN UNDERVOLTAGE WARN	0
12	VIN OVERVOLTAGE WARN	0
11	$\overline{\text{POWER GOOD}}$	1
10	OVER TEMPERATURE WARN	0
9	TIMER LATCHED OFF	0
8	EXT MOSFET SHORTED	0
7	CONFIG PRESET	1
6	DEVICE OFF	1
5	VIN UNDERVOLTAGE FAULT	1
4	VIN OVERVOLTAGE FAULT	0
3	IIN OC/PFET OP FAULT	0
2	OVER TEMPERATURE FAULT	0
1	CML FAULT	0
0	CIRCUIT BREAKER FAULT	0

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MFR_SPECIFIC_18: AVG_BLOCK_READ (E2h)

The AVG_BLOCK_READ command concatenates the DIAGNOSTIC_WORD with input and output average telemetry information (IIN, VOUT, VIN, PIN) as well as temperature to capture all of the operating information of the part in a single PMBus transaction. The block is 12 bytes long with telemetry information being sent out in the same manner as if an individual READ_AVG_XXX command had been issued (shown below). AVG_BLOCK_READ also ensures that the VIN, VOUT, and IIN measurements are all time-aligned whereas there is a chance they may not be if read with individual PMBus commands. To read data from the AVG_BLOCK_READ command, use the SMBus Block Read protocol.

Table 39. AVG_BLOCK_READ Register Format

Byte Count (always 12)	(1 byte)
DIAGNOSTIC_WORD	(1 word)
AVG_IIN	(1 word)
AVG_VOUT	(1 word)
AVG_VIN	(1 word)
AVG_PIN	(1 word)
TEMPERATURE	(1 word)

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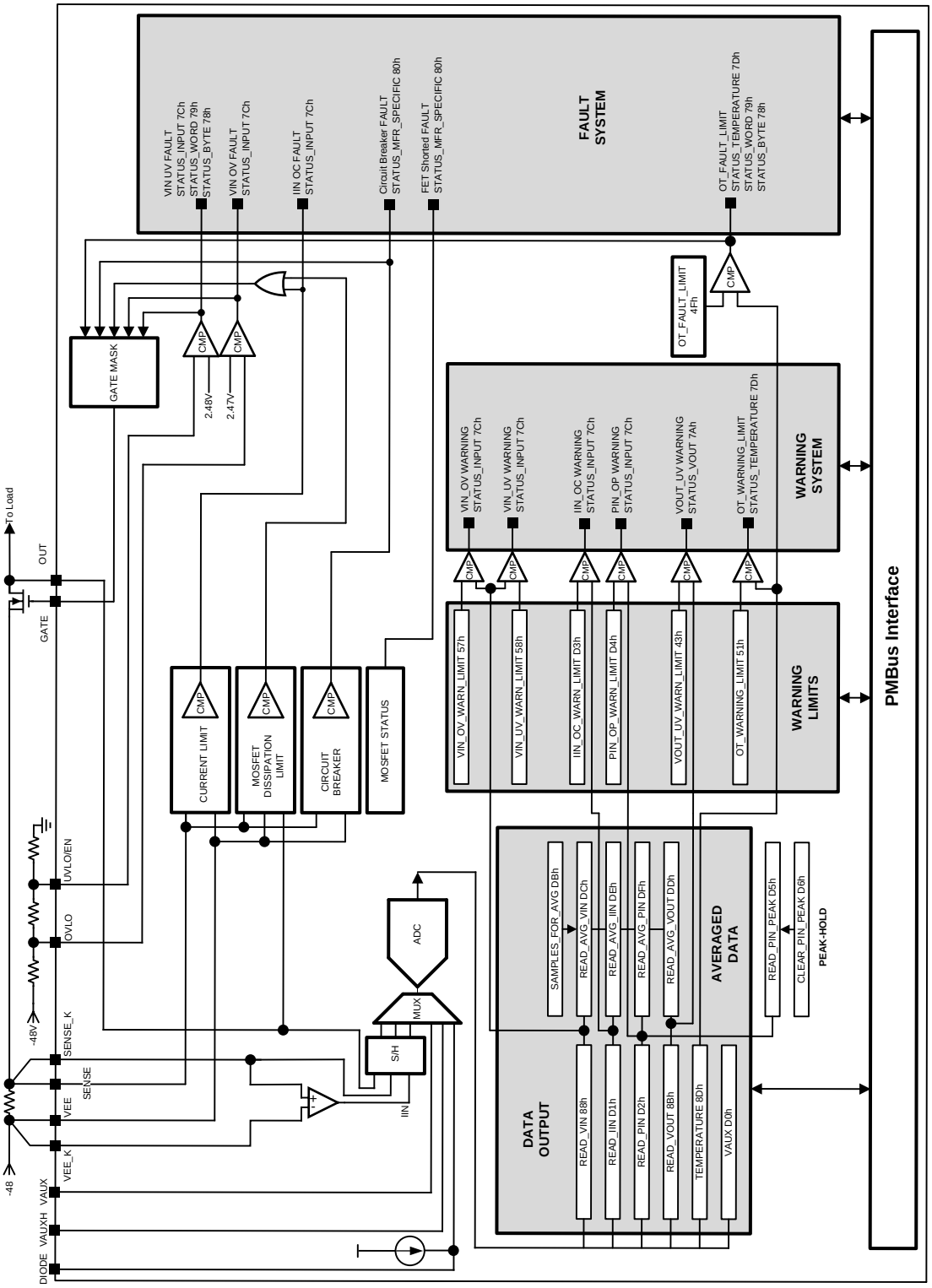


Figure 19. Command/Register and Alert Flow Diagram

READING AND WRITING TELEMETRY DATA AND WARNING THRESHOLDS

All measured telemetry data and user programmed warning thresholds are communicated in 12-bit two's compliment binary numbers read/written in 2 byte increments conforming to the Direct format as described in section 8.3.3 of the PMBus Power System Management Protocol Specification 1.1 (Part II). The organization of the bits in the telemetry or warning word is shown in Table 40, where Bit_11 is the most significant bit (MSB) and Bit_0 is the least significant bit (LSB). The decimal equivalent of all warning and telemetry words are constrained to be within the range of 0 to 4095, with the exception of temperature. The decimal equivalent value of the temperature word ranges from 0 to 65535.

Table 40. Telemetry and Warning Word Format

Byte	B7	B6	B5	B4	B3	B2	B1	B0
1	Bit_7	Bit_6	Bit_5	Bit_4	Bit_3	Bit_2	Bit_1	Bit_0
2	0	0	0	0	Bit_11	Bit_10	Bit_9	Bit_8

Conversion from direct format to real-world dimensions of current, voltage, power, and temperature is accomplished by determining appropriate coefficients as described in section 7.2.1 of the PMBus Power System Management Protocol Specification 1.1 (Part II). According to this specification, the host system converts the values received into a reading of volts, amperes, watts, or other units using the following relationship:

$$X = \frac{1}{m}(Y \times 10^{-R} - b) \quad (34)$$

Where:

X: the calculated "real-world" value (volts, amps, watt, etc.)

m: the slope coefficient

Y: a two byte two's complement integer received from device

b: the offset, a two byte, two's complement integer

R: the exponent, a one byte two's complement integer

R is only necessary in systems where m is required to be an integer (for example, where m may be stored in a register in an integrated circuit). In those cases, R only needs to be large enough to yield the desired accuracy.

Table 41. Telemetry and Warning Conversion Coefficients

Commands	Condition	Format	Number of Data Bytes	m	b	R	Units
READ_VIN, READ_AVG_VIN VIN_OV_WARN_LIMIT VIN_UV_WARN_LIMIT		DIRECT	2	4611	-642	-2	V
READ_VOUT, READ_AVG_VOUT VOUT_UV_WARN_LIMIT		DIRECT	2	4621	423	-2	V
READ_VAUX		DIRECT	2	13808	0	-1	V
(1)READ_IIN, READ_AVG_IIN MFR_IIN_OC_WARN_LIMIT	CL = VDD	DIRECT	2	10742	1552	-2	A
(1)READ_IN, READ_AVG_IN MFR_IIN_OC_WARN_LIMIT	CL = VEE	DIRECT	2	5456	2118	-2	A
(1)READ_PIN, READ_AVG_PIN, READ_PIN_PEAK MFR_PIN_OP_WARN_LIMIT	CL = VDD	DIRECT	2	1204	8524	-3	W
(1)READ_PIN, READ_AVG_PIN, READ_PIN_PEAK MFR_PIN_OP_WARN_LIMIT	CL = VEE	DIRECT	2	612	11202	-3	W
READ_TEMPERATURE_1 OT_WARN_LIMIT OT_FAULT_LIMIT		DIRECT	2	16000	0	-3	°C

(1) The coefficients relating to current/power measurements and warning thresholds shown are normalized to a sense resistor (R_S) value of 1 mΩ. In general, the current/power coefficients can be calculated using the relationships shown in Table 42.

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Table 42. Current and Power Telemetry and Warning Conversion Coefficients (R_S in mΩ)

Commands	Condition	Format	Number of Data Bytes	m	b	R	Units
(1)READ_IIN, READ_AVG_IIN MFR_IIN_OC_WARN_LIMIT	CL = VDD	DIRECT	2	10742 x R_S	1552	-2	A
(1)READ_IIN, READ_AVG_IIN MFR_IIN_OC_WARN_LIMIT	CL = VEE	DIRECT	2	5456 x R_S	2118	-2	A
(1)READ_PIN, READ_AVG_PIN, READ_PIN_PEAK MFR_PIN_OP_WARN_LIMIT	CL = VDD	DIRECT	2	1204 x R_S	8524	-3	W
(1)READ_PIN, READ_AVG_PIN, READ_PIN_PEAK MFR_PIN_OP_WARN_LIMIT	CL = VEE	DIRECT	2	612 x R_S	11202	-3	W

(1) The coefficients relating to current/power measurements and warning thresholds shown in Table 41 are normalized to a sense resistor (R_S) value of 1 mΩ. In general, the current/power coefficients can be calculated using the relationships shown.

Care must be taken to adjust the exponent coefficient, R, such that the value of m remains within the range of -32768 to +32767. For example, if a 5 mΩ sense resistor is used, the correct coefficients for the READ_IIN command with CL = VDD would be m = 5371, b = 155, R = -1.

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DETERMINING TELEMETRY COEFFICIENTS EMPIRICALLY WITH LINEAR FIT

The coefficients for telemetry measurements and warning thresholds presented in Table 41 are adequate for the majority of applications. Current and power coefficients must be calculated per application as they are dependent on the value of the sense resistor, R_S, used. Table 42 provides the equations necessary for calculating the current and power coefficients for the general case. The small signal nature of the current measurement make it and the power measurement more susceptible to PCB parasitics than other telemetry channels. This may cause slight variations in the optimum coefficients (m, b, R) for converting from Direct format digital values to real-world values (for example, Amps and Watts). The optimum coefficients can be determined empirically for a specific application and PCB layout using two or more measurements of the telemetry channel of interest. The current coefficients can be determined using the following method:

1. While the LM5064 is in normal operation measure the voltage across the sense resistor using kelvin test points and a high accuracy DVM while controlling the load current. Record the integer value returned by the READ_AVG_IIN command (with the SAMPLES_FOR_AVG set to a value greater than 0) for two or more voltages across the sense resistor. For best results, the individual READ_AVG_IIN measurements should span nearly the full scale range of the current (For example, voltage across R_S of 5 mV and 20 mV).
2. Convert the measured voltages to currents by dividing them by the value of R_S. For best accuracy the value of R_S should be measured. Table 43 assumes a sense resistor value of 5mΩ.

Table 43. Measurements for linear fit determination of current coefficients:

Measured voltage across R_S (V)	Measured Current (A)	READ_AVG_IIN (integer value)
0.005	1	568
0.01	2	1108
0.02	4	2185

1. Using the spreadsheet or math program of your choice determine the slope and the y-intercept of the data returned by the READ_AVG_IIN command versus the measured current. For the data shown in Table 42:
   - READ_AVG_IN value = slope x (Measured Current) + (y-intercept)
   - slope = 538.9
   - y-intercept = 29.5
2. To determine the '**m**' coefficient, simply shift the decimal point of the calculated slope to arrive at an integer with a suitable number of significant digits for accuracy (typically 4) while staying with the range of -32768 to +32767. This shift in the decimal point equates to the '**R**' coefficient. For the slope value shown above, the decimal point would be shifted to the right once hence **R** = -1.
3. Once the '**R**' coefficient has been determined, the '**b**' coefficient is found by multiplying the y-intercept by 10^{-R}. In this case the value of **b** = 295.
   - Calculated Current Coefficients:
   - **m** = 5389
   - **b** = 295
   - **R** = -1

$$X = \frac{1}{m}(Y \times 10^{-R} - b) \quad (35)$$

Where:

X: the calculated "real-world" value (volts, amps, watts, temperature)

m: the slope coefficient, is the two byte, two's complement integer

Y: a two byte two's complement integer received from device

b: the offset, a two byte, two's complement integer

R: the exponent, a one byte two's complement integer

The above procedure can be repeated to determine the coefficients of any telemetry channel simply by substituting measured current for some other parameter (for example, power, voltage, etc.).

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WRITING TELEMETRY DATA

There are several locations that will require writing data if their optional usage is desired. Use the same coefficients previously calculated for your application, and apply them using this method as prescribed by the PMBus revision section 7.2.2 "Sending a Value"

$$Y = (mX + b) \times 10^{R} \quad (36)$$

Where:

X: the calculated "real-world" value (volts, amps, watts, temperature)

m: the slope coefficient, is the two byte, two's complement integer

Y: a two byte two's complement integer received from device

b: the offset, a two byte, two's complement integer

R: the exponent, a one byte two's complement integer

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PMBUS™ ADDRESS LINES (ADR0, ADR1, ADR2)

The three address lines are to be set high (connect to VDD), low (connect to VEE), or open to select one of 27 addresses for communicating with the LM5064. Table 44 depicts 7-bit addresses (eighth bit is read/write bit):

Table 44. Device Addressing

ADR2	ADR1	ADR0	Decoded Address
Z	Z	Z	40h
Z	Z	0	41h
Z	Z	1	42h
Z	0	Z	43h
Z	0	0	44h
Z	0	1	45h
Z	1	Z	46h
Z	1	0	47h
Z	1	1	10h
0	Z	Z	11h
0	Z	0	12h
0	Z	1	13h
0	0	Z	14h
0	0	0	15h
0	0	1	16h
0	1	Z	17h
0	1	0	50h
0	1	1	51h
1	Z	Z	52h
1	Z	0	53h
1	Z	1	54h
1	0	Z	55h
1	0	0	56h
1	0	1	57h
1	1	Z	58h
1	1	0	59h
1	1	1	5Ah

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SMBUS COMMUNICATIONS TIMING REQUIREMENTS

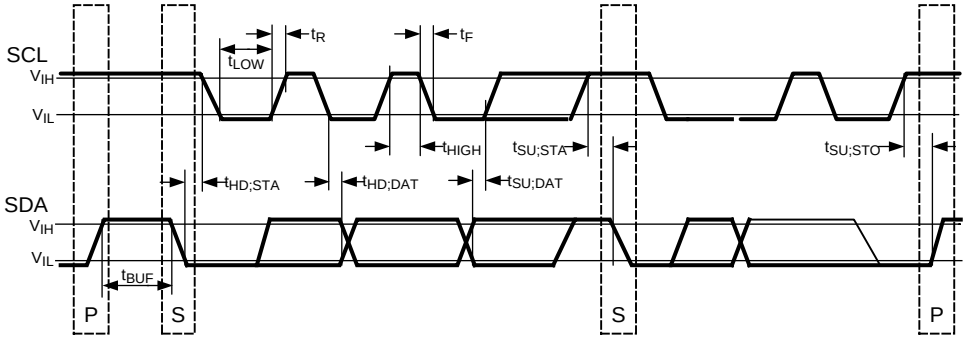


Figure 20. SMBus Timing Diagram

Table 45. SMBus Timing Definition

Symbol	Parameter	Limits		Units	Comments
		Min	Max		
F_{SMB}	SMBus Operating Frequency	10	400	kHz	
T_{BUF}	Bus free time between Stop and Start Condition	1.3		µs	
$T_{HD:STA}$	Hold time after (Repeated) Start Condition. After this period, the first clock is generated.	0.6		µs	
$T_{SU:STA}$	Repeated Start Condition setup time	0.6		µs	
$T_{SU:STO}$	Stop Condition setup time	0.6		µs	
$T_{HD:DAT}$	Data hold time	85		ns	
$T_{SU:DAT}$	Data setup time	100		ns	
$T_{TIMEOUT}$	Clock low time-out	25	35	ms	(1)
T_{LOW}	Clock low period	1.5		µs	
T_{HIGH}	Clock high period	0.6		µs	(2)
$T_{LOW:SEXT}$	Cumulative clock low extend time (slave device)		25	ms	(3)
$T_{LOW:MEXT}$	Cumulative low extend time (master device)		10	ms	(4)
T_F	Clock or Data Fall Time	20	300	ns	(5)
T_R	Clock or Data Rise Time	20	300	ns	(5)

(1) Devices participating in a transfer will timeout when any clock low exceeds the value of $T_{TIMEOUT,MIN}$ of 25 ms. Devices that have detected a timeout condition must reset the communication no later than $T_{TIMEOUT,MAX}$ of 35 ms. The maximum value must be adhered to by both a master and a slave as it incorporates the cumulative stretch limit for both a master (10ms) and a slave (25ms).
(2) $T_{HIGH\ MAX}$ provides a simple method for devices to detect bus idle conditions.
(3) $T_{LOW:SEXT}$ is the cumulative time a slave device is allowed to extend the clock cycles in one message from the initial start to the stop. If a slave exceeds this time, it is expected to release both its clock and data lines and reset itself.
(4) $T_{LOW:MEXT}$ is the cumulative time a master device is allowed to extend its clock cycles within each byte of a message as defined from start-to-ack, ack-to-ack, or ack-to-stop.
(5) Rise and fall time is defined as follows:• T_R = (V_{ILMAX} – 0.15) to (V_{IHMIN} + 0.15)• T_F = 0.9 VDD to (V_{ILMAX} – 0.15)

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SMBA RESPONSE

The SMBA effectively has two masks:

1. The Alert Mask Register at D8h, and

2. The ARA Automatic Mask.

The ARA Automatic Mask is a mask that is set in response to a successful ARA read. An ARA read operation returns the PMBus address of the lowest addressed part on the bus that has its SMBA asserted. A successful ARA read means that THIS part was the one that returned its address. When a part responds to the ARA read, it releases the SMBA signal. When the last part on the bus that has an SMBA set has successfully reported its address, the SMBA signal will de-assert.

The way that the LM5064 releases the SMBA signal is by setting the ARA Automatic mask bit for all fault conditions present at the time of the ARA read. All status registers will still show the fault condition, but it will not generate and SMBA on that fault again until the ARA Automatic mask is cleared by the host issuing a CLEAR_FAULTS command to this part. This should be done as a routine part of servicing an SMBA condition on a part, even if the ARA read is not done. Figure 21 depicts a schematic version of this flow.

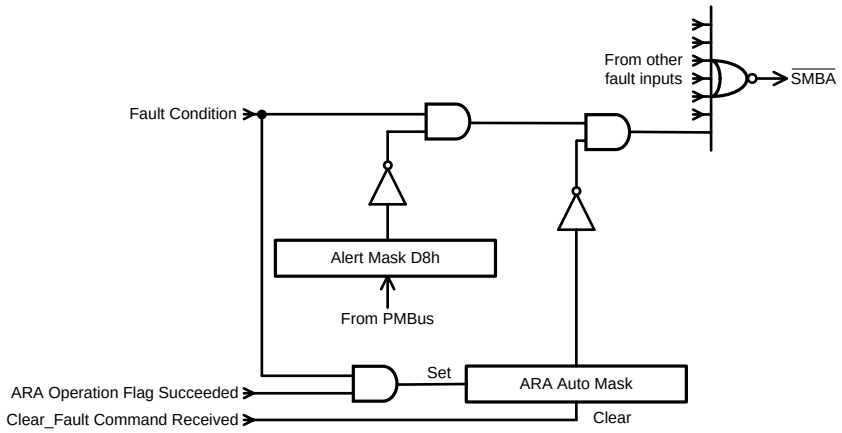


Figure 21. Typical Flow Schematic for SMBA Fault

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REVISION HISTORY

Changes from Revision D (February 2013) to Revision E	Page
• Changed layout of National Data Sheet to TI format	54

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PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
LM5064PMH/NOPB	ACTIVE	HTSSOP	PWP	28	48	Green (RoHS & no Sb/Br)	SN	Level-3-260C-168 HR	-40 to 125	LM5064 PMH	Samples
LM5064PMHE/NOPB	ACTIVE	HTSSOP	PWP	28	250	Green (RoHS & no Sb/Br)	SN	Level-3-260C-168 HR	-40 to 125	LM5064 PMH	Samples
LM5064PMHX/NOPB	ACTIVE	HTSSOP	PWP	28	2500	Green (RoHS & no Sb/Br)	SN	Level-3-260C-168 HR	-40 to 125	LM5064 PMH	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

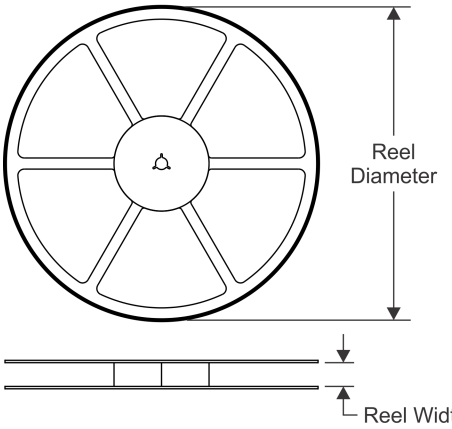
(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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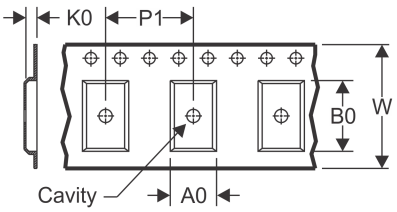
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

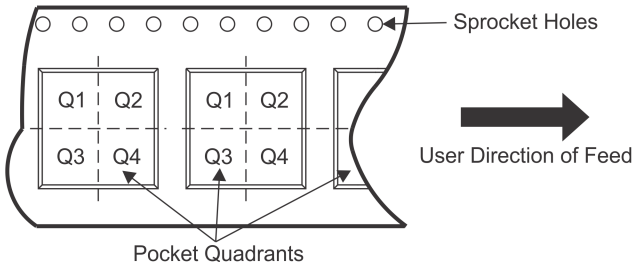


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

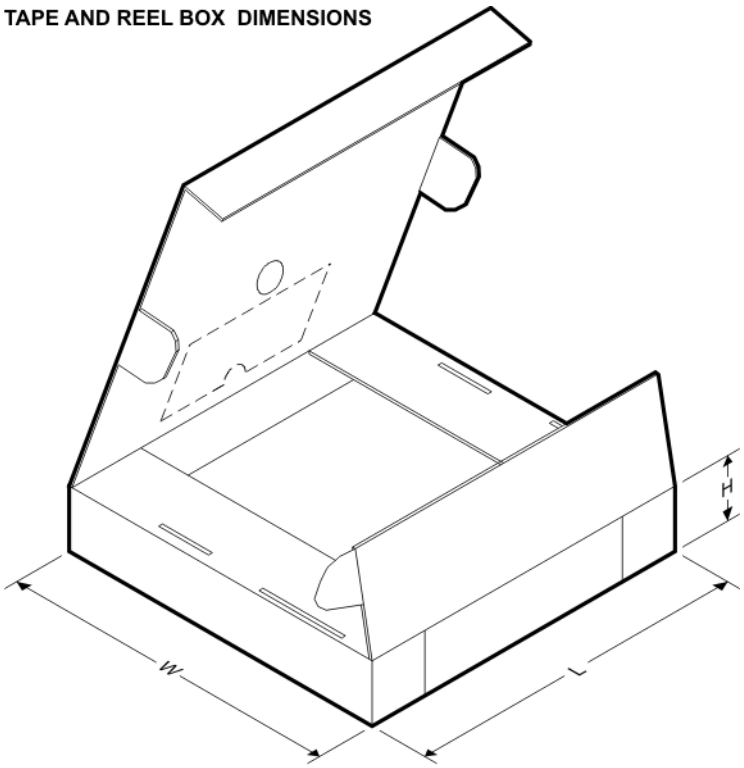
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
LM5064PMHE/NOPB	HTSSOP	PWP	28	250	178.0	16.4	6.8	10.2	1.6	8.0	16.0	Q1
LM5064PMHX/NOPB	HTSSOP	PWP	28	2500	330.0	16.4	6.8	10.2	1.6	8.0	16.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
LM5064PMHE/NOPB	HTSSOP	PWP	28	250	210.0	185.0	35.0
LM5064PMHX/NOPB	HTSSOP	PWP	28	2500	367.0	367.0	38.0

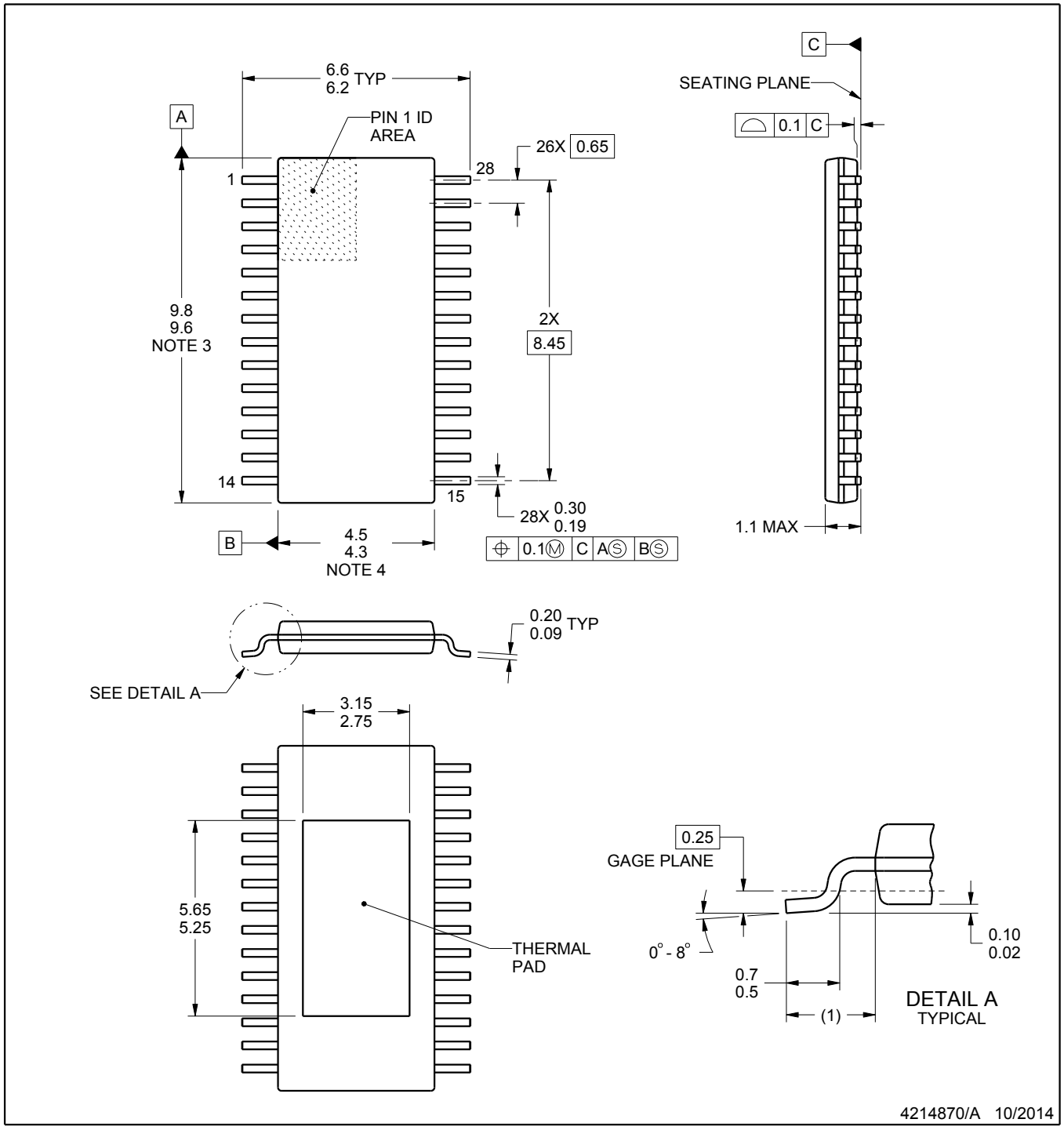


PACKAGE OUTLINE

PWP0028A

PowerPAD™ - 1.1 mm max height

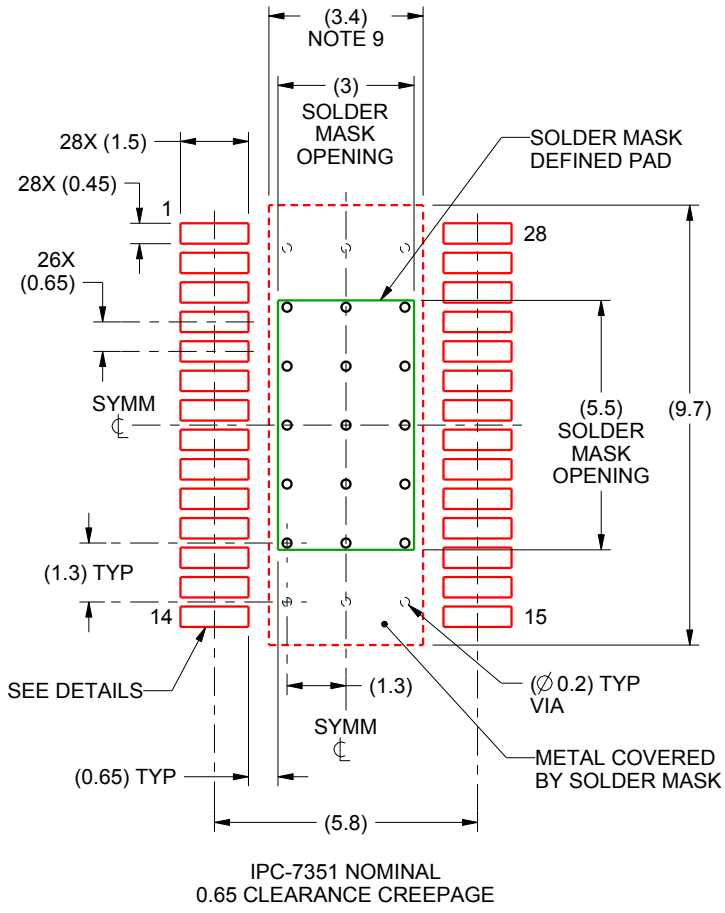
PLASTIC SMALL OUTLINE



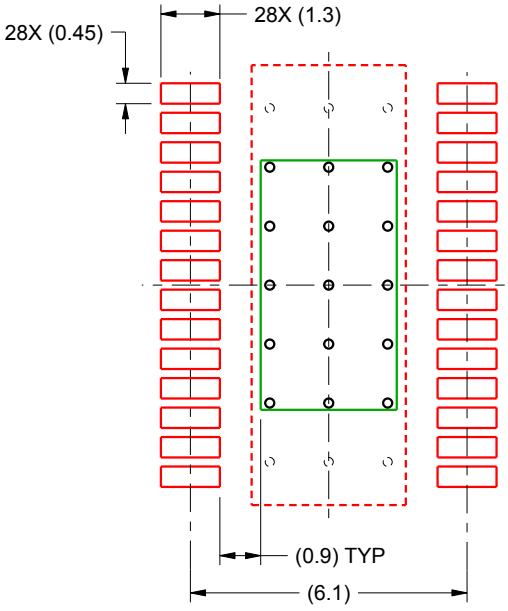
NOTES:

PowerPAD is a trademark of Texas Instruments.

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm, per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm, per side.
5. Reference JEDEC registration MO-153, variation AET.

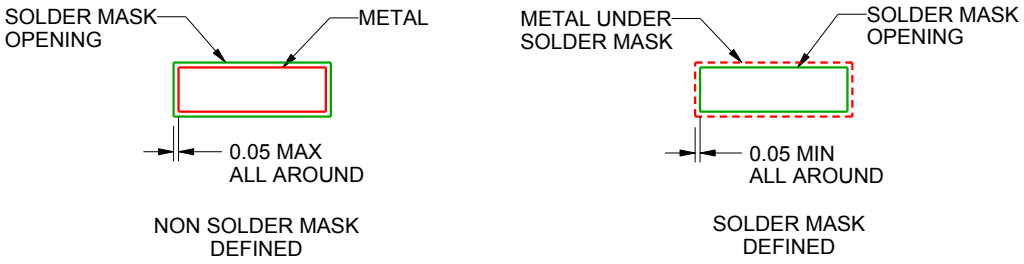


IPC-7351 NOMINAL
0.65 CLEARANCE CREEPAGE



HV / ISOLATION OPTION
0.9 CLEARANCE CREEPAGE
OTHER DIMENSIONS IDENTICAL TO IPC-7351

LAND PATTERN EXAMPLE
SCALE:6X

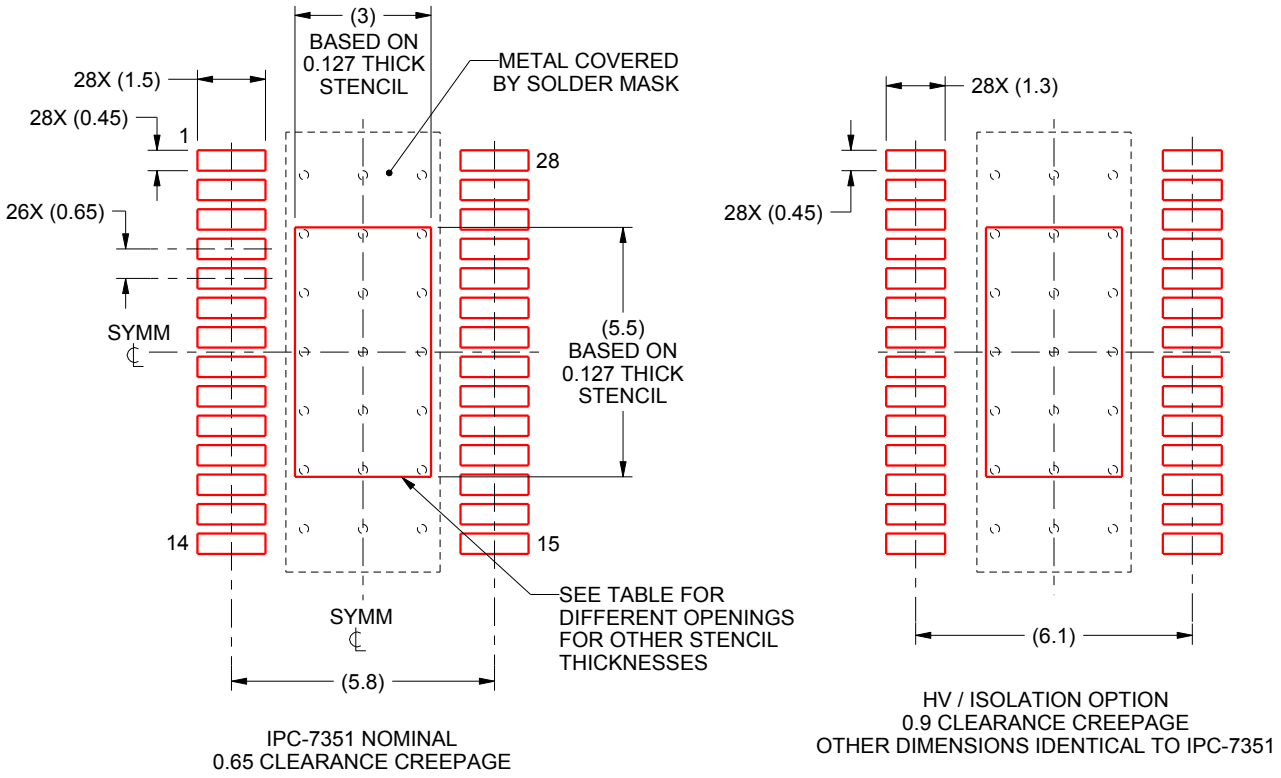


SOLDER MASK DETAILS

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NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
8. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature numbers SLMA002 (www.ti.com/lit/slma002) and SLMA004 (www.ti.com/lit/slma004).
9. Size of metal pad may vary due to creepage requirement.



SOLDER PASTE EXAMPLE
EXPOSED PAD
100% PRINTED SOLDER COVERAGE AREA
SCALE:6X

STENCIL THICKNESS	SOLDER STENCIL OPENING
0.1	3.55 X 6.37
0.127	3.0 X 5.5 (SHOWN)
0.152	2.88 X 5.16
0.178	2.66 X 4.77

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NOTES: (continued)

10. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
11. Board assembly site may have different recommendations for stencil design.

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