LM5021 AC-DC Current Mode PWM Controller

Check for Samples: LM5021

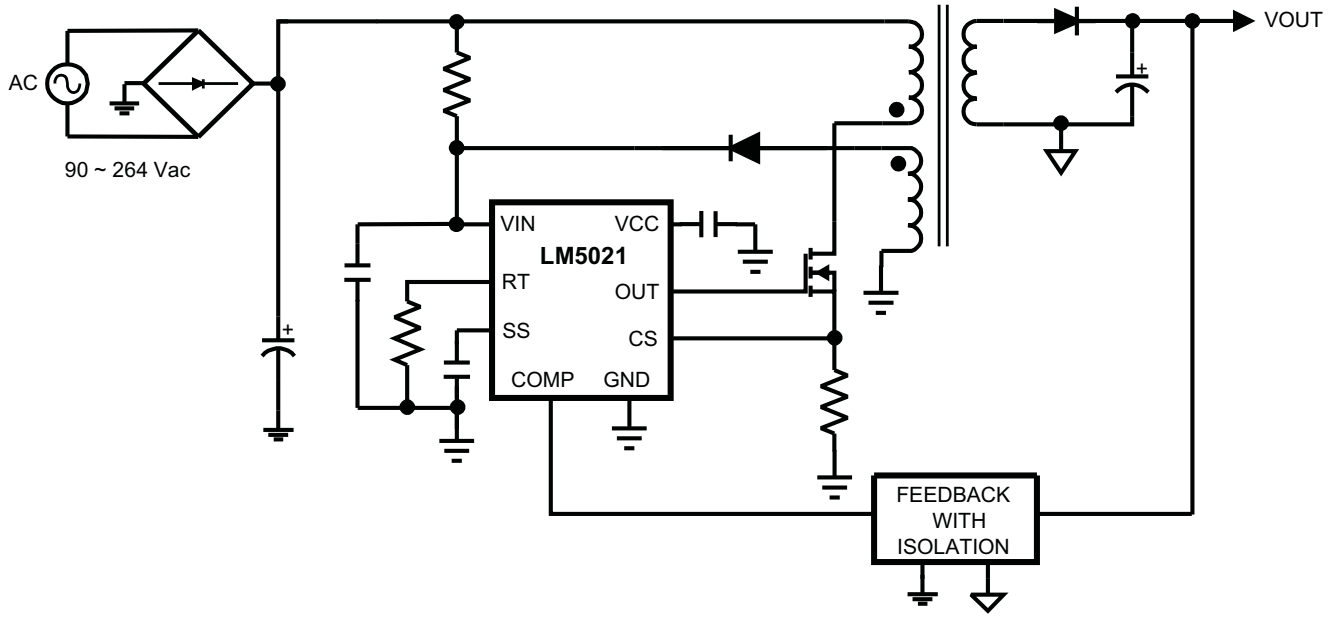
FEATURES

- **Ultra Low Start-up Current (25 µA maximum)**
- **Current Mode Control**
- **Skip Cycle Mode for Low Standby Power**
- **Single Resistor Programmable Oscillator**
- **Synchronizable Oscillator**
- **Adjustable Soft-Start**
- **Integrated 0.7A Peak Gate Driver**
- **Direct Opto-Coupler Interface**
- **Maximum Duty Cycle Limiting (80% for LM5021-1 or 50% for LM5021-2)**
- **Slope Compensation for (LM5021-1 Only)**
- **Under Voltage Lockout (UVLO) with Hysteresis**
- **Cycle-by-Cycle Over-Current Protection**
- **Hiccup Mode for Continuous Overload Protection**
- **Leading Edge Blanking of Current Sense Signal**
- **Packages: VSSOP-8 or PDIP-8**

DESCRIPTION

The LM5021 off-line pulse width modulation (PWM) controller contains all of the features needed to implement highly efficient off-line single-ended flyback and forward power converters using current-mode control. The LM5021 features include an ultra-low (25 µA) start-up current, which minimizes power losses in the high voltage start-up network. A skip cycle mode reduces power consumption with light loads for energy conserving applications (ENERGY STAR®, CECP, etc.). Additional features include under-voltage lockout, cycle-by-cycle current limit, hiccup mode overload protection, slope compensation, soft-start and oscillator synchronization capability. This high performance 8-pin IC has total propagation delays less than 100nS and a 1MHz capable oscillator that is programmed with a single resistor.

Simplified Application Diagram



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Connection Diagram

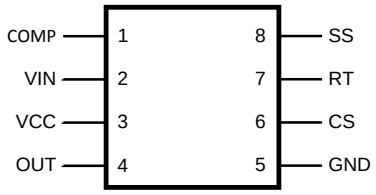


Figure 1. Top View
VSSOP-8
(See Package Number DGK0008A)
PDIP-8
(See Package Number P0008E)

PIN DESCRIPTIONS

Pin	Name	Description	Application Information
1	COMP	Control input for the Pulse Width Modulator and Hiccup comparators.	COMP pull-up is provided by an internal 5K resistor which may be used to bias an opto-coupler transistor.
2	VIN	Input voltage.	Input to start-up regulator. The VIN pin is clamped at 36V by an internal zener diode.
3	VCC	Output only of a linear bias supply regulator. Nominally 8.5V.	VCC provides bias to controller and gate drive sections of the LM5021. An external capacitor must be connected from this pin to ground.
4	OUT	MOSFET gate driver output.	High current output to the external MOSFET gate input with source/sink current capability of 0.3A and 0.7A respectively.
5	GND	Ground return.	
6	CS	Current Sense input.	Current sense input for current mode control and over-current protection. Current limiting is accomplished using a dedicated current sense comparator. If the CS comparator input exceeds 0.5 Volts the OUT pin switches low for cycle-by-cycle current limit. CS is held low for 90ns after OUT switches high to blank the leading edge current spike.
7	RT / SYNC	Oscillator timing resistor pin and synchronization input.	An external resistor connected from RT to GND sets the oscillator frequency. This pin will also accept synchronization pulses from an external clock.
8	SS	Soft-start / Hiccup time	An external capacitor and an internal 22 µA current source set the soft-start ramp. The soft -start capacitor controls both the soft-start rate and the hiccup mode period.



These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

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Absolute Maximum Ratings (1)(2)

VIN to GND	-0.3V to 30V
VIN Clamp Continuous Current	5mA
CS to GND	-0.3V to 1.25V
RT to GND	-0.3V to 5.5V
All other pins to GND	-0.3V to 7.0V
ESD Rating (3) Human Body Model	2kV
Storage Temperature	-65°C to +150°C
Operating Junction Temperature	+150°C

(1) Absolute Maximum Ratings are limits beyond which damage to the device may occur. Operating Ratings are conditions under which operation of the device is intended to be functional. For specifications and test conditions, see the Electrical Characteristics.
(2) If Military/Aerospace specified devices are required, please contact the Texas Instruments Sales Office/ Distributors for availability and specifications.
(3) The human body model is a 100 pF capacitor discharged through a 1.5kΩ resistor into each pin.

Operating Ratings (1)

VIN Voltage (2)	8V to 30V
Junction Temperature	-40°C to +125°C

(1) Absolute Maximum Ratings are limits beyond which damage to the device may occur. Operating Ratings are conditions under which operation of the device is intended to be functional. For specifications and test conditions, see the Electrical Characteristics.
(2) After initial turn-on at VIN = 20V.

Electrical Characteristics (1)

Specifications in standard type face are for T_J= +25°C and those in **boldface type** apply over the full **Operating Junction Temperature Range**. Unless otherwise specified: V_{IN} = 15V, R_T = 44.2KΩ.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
STARTUP CIRCUIT						
	Start Up Current	Before VCC Enable		18	**25**	µA
	VCC Regulator enable threshold		**17**	20	**23**	V
	VCC Regulator disable threshold			7.25		V
	VIN ESD Clamp voltage	I = 5mA	**30**	36	**40**	V
I_{VIN}	Operating supply current	COMP = 0VDC		2.5	**3.75**	mA
VCC SUPPLY						
	Controller enable threshold		**6.5**	7	**7.5**	V
	Controller disable threshold		**5.3**	5.8	**6.3**	V
	VCC regulated output	No External Load	**8**	8.5	**9**	V
	VCC dropout voltage (VIN - VCC)	I = 5 mA		1.7		V
	VCC regulator current limit	VCC = 7.5V (2)	**15**	22		mA
SKIP CYCLE MODE COMPARATOR						
	Skip Cycle mode enable threshold	⅓ [COMP - 1.25V]	**75**	125	**175**	mV
	Skip Cycle mode hysteresis			5		mV
CURRENT LIMIT						
	CS limit to OUT delay	CS stepped from 0 to 0.6V, time to OUT transition low, C_{load} = 0.		35		ns
	CS limit threshold		**0.45**	0.5	**0.55**	V
	Leading Edge Blanking time			90		ns
	CS blanking sinking impedance			35	**55**	Ω

(1) Min and Max limits are 100% production tested at 25°C. Limits over the operating temperature range are specified through correlation using Statistical Quality Control (SQC) methods. Limits are used to calculate Average Outgoing Quality Level (AOQL).
(2) Device thermal limitations may limit usable range.

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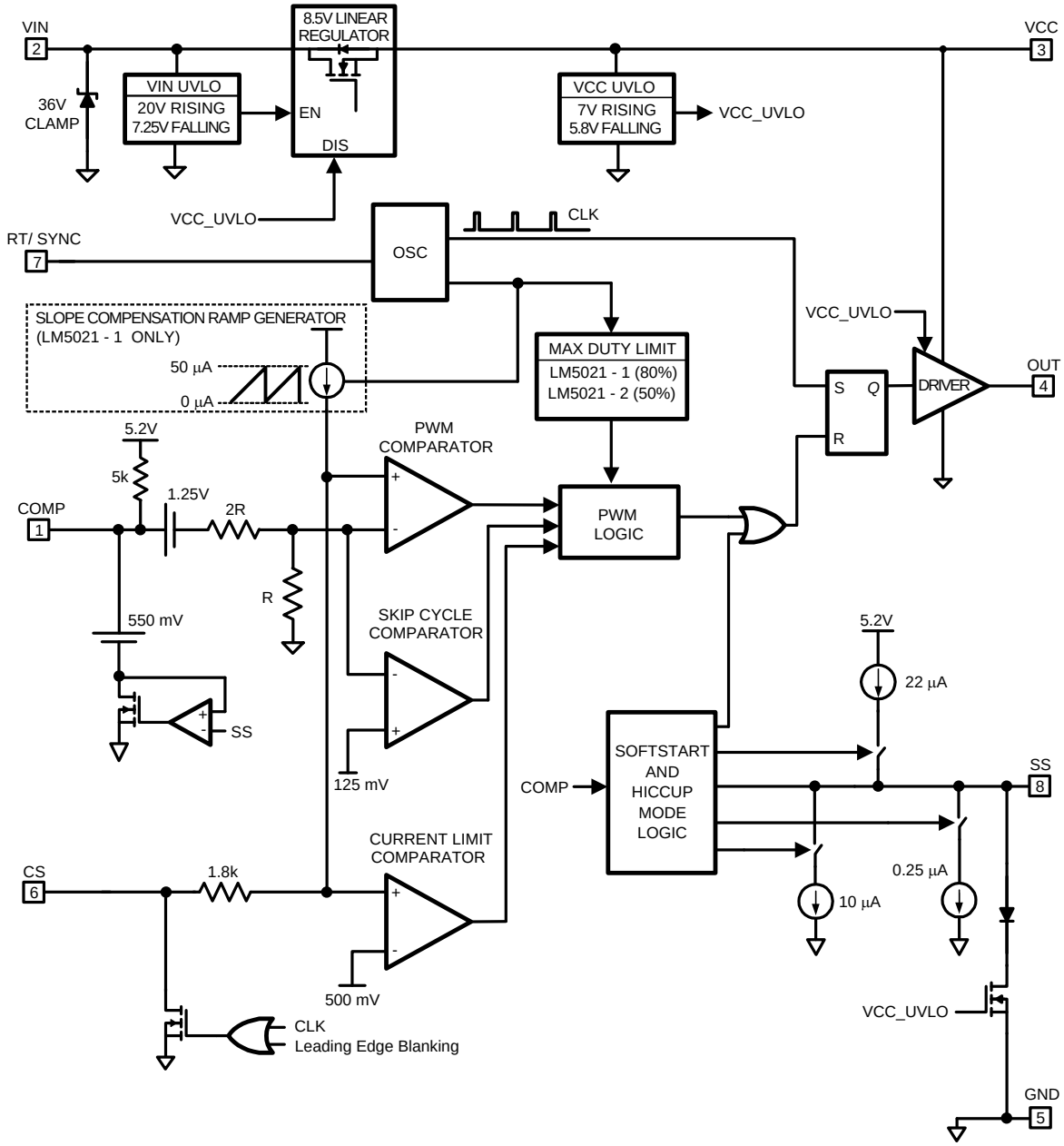
Electrical Characteristics[1] (continued)

Specifications in standard type face are for T_J= +25°C and those in **boldface type** apply over the full **Operating Junction Temperature Range**. Unless otherwise specified: V_{IN} = 15V, R_T = 44.2KΩ.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
SOFT-START						
V_{SS-OCV}	SS pin open-circuit voltage		**4.3**	5.2	**6.1**	V
	Soft-start Current Source		**15**	22	**30**	µA
	Soft-start to COMP Offset		**0.35**	0.55	**0.75**	V
	COMP sinking impedance	During SS ramp		60		Ω
OSCILLATOR						
	Frequency1 (RT = 44.2K)		**135**	150	**165**	kHz
	Frequency2 (RT = 13.3K)		**440**	500	**560**	kHz
	Sync threshold		**2.4**	3.2	**3.8**	V
PWM COMPARATOR						
	COMP to OUT delay	COMP set to 2V CS stepped 0 to 0.4V, time to OUT transition low, C_{load} = 0.		20		ns
	Min Duty Cycle	COMP = 0V			**0**	%
	Max Duty Cycle (-1 Device)		**75**	80	**85**	%
	Max Duty Cycle (-2 Device)			50		%
	COMP to PWM comparator gain			0.33		
	COMP Open Circuit Voltage		**4.2**	5.1	**6**	V
	COMP at Max Duty Cycle			2.75		V
	COMP Short Circuit Current	COMP = 0V	**0.6**	1.1	**1.5**	mA
SLOPE COMPENSATION						
	Slope Comp Amplitude (LM5021-1 only)	CS pin to PWM Comparator offset at maximum duty cycle	**70**	90	**110**	mV
OUTPUT SECTION						
	OUT High Saturation	IOUT = 50mA, VCC - OUT		0.6	**1.1**	V
	OUT Low Saturation	IOUT = 100mA		0.3	**1**	V
	Peak Source Current	OUT = VCC/2.		0.3		A
	Peak Sink Current	OUT = VCC/2.		0.7		A
	Rise time	C_{load} = 1nF		25		ns
	Fall time	C_{load} = 1nF		10		ns
HICCUP MODE						
V_{OVLD}	Over load detection threshold	COMP pin	**V_{SS-OCV} – 0.8**	V_{SS-OCV} – 0.6	**V_{SS-OCV}– 0.4**	V
V_{HIC}	Hiccup mode threshold	SS pin	**V_{SS-OCV} – 0.8**	V_{SS-OCV} – 0.6	**V_{SS-OCV}– 0.4**	V
V_{RST}	Hiccup mode Restart threshold	SS pin	**0.1**	0.3	**0.5**	V
I_{DTCS}	Dead-time current source		**0.1**	0.25	**0.4**	µA
I_{OVCS}	Overload detection timer current source		**6**	10	**14**	µA
THERMAL RESISTANCE						
θ_{JA}	VSSOP-8 Junction to Ambient	0 LFM		200		°C/W
θ_{JA}	PDIP-8 Junction to Ambient	0 LFM		107		°C/W

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Simplified Block Diagram



Typical Performance Characteristics

Unless otherwise specified: T_J = 25°C.

VIN Start-Up Current

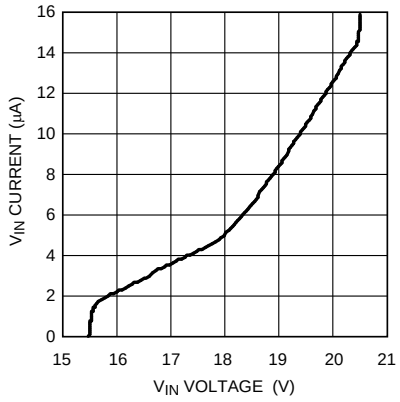


Figure 2.

VIN UVLO

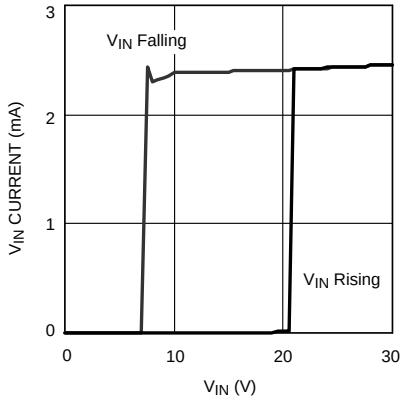


Figure 3.

VIN Current vs OUT Load

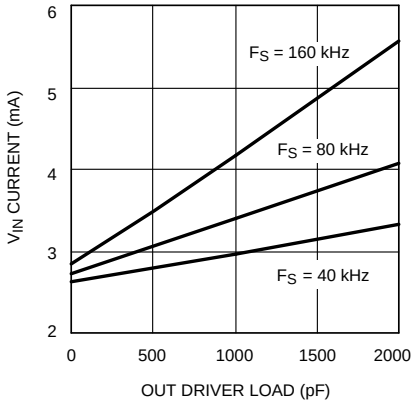


Figure 4.

VIN Voltage Falling vs VCC Voltage

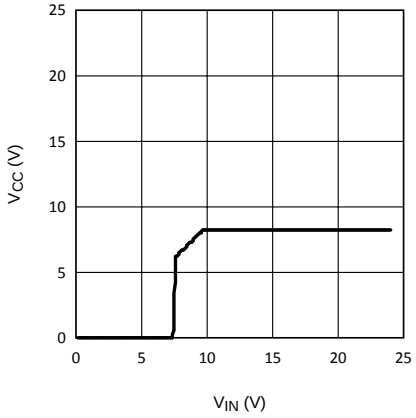


Figure 5.

OUT Driver Current vs Temperature

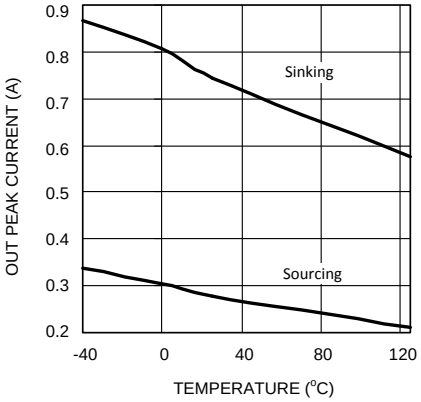


Figure 6.

Hiccup Mode Deadtime vs Softstart Capacitance

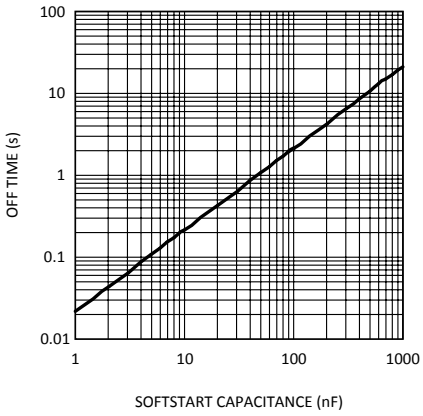


Figure 7.

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Typical Performance Characteristics (continued)

Unless otherwise specified: T_J = 25°C.

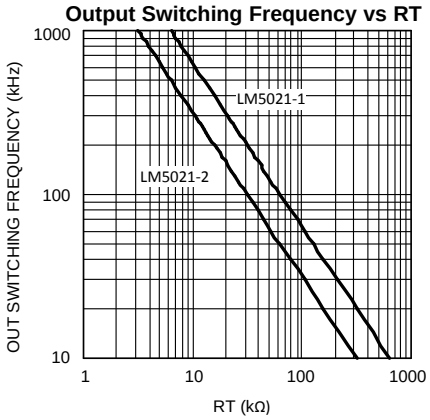


Figure 8.

DETAILED OPERATING DESCRIPTION

START UP CIRCUIT

Referring to Figure 9, the input capacitor C_{VIN} is trickle charged through the start-up resistor Rstart, when the rectified ac input voltage HV is applied. The VIN current consumed by the LM5021 is only 18 µA (nominal) while the capacitor C_{VIN} is initially charged to the start-up threshold. When the input voltage, VIN reaches the upper VIN UVLO threshold of 20V, the internal VCC linear regulator is enabled. The VCC regulator will remain on until VIN falls to the lower UVLO threshold of 7.25V (12.5V hysteresis). When the VCC regulator is turned on, the external capacitor at the VCC pin begins to charge. The PWM controller, soft-start circuit and gate driver are enabled when the VCC voltage reaches the VCC UVLO upper threshold of 7V. The VCC UVLO has 1.2V hysteresis between the upper and lower thresholds to avoid chattering during transients on the VCC pin. When the VCC UVLO enables the switching power supply, energy is transferred from the primary to the secondary transformer winding(s). A bias winding, shown in Figure 9, delivers power to the VIN pin to sustain the VCC regulator. The voltage supplied should be from 11V (VCC regulated voltage maximum plus VCC regulator dropout voltage) to 30V (maximum operating VIN voltage). The bias winding should always be connected to the VIN pin as shown in Figure 9. Do not connect the bias winding to the VCC pin. The start-up sequence is completed and normal operation begins when the voltage from the bias winding is sufficient to maintain VCC level greater than the VCC UVLO threshold (5.8V typical).

The LM5021 is designed for ultra-low start-up current into the VIN pin. To accomplish this very low start-up current, the VCC regulator of the LM5021 is unique as compared to the VCC regulator used in other controllers of the LM5xxx family. The LM5021 is designed specifically for applications with the bias winding connected to the VIN pin as shown in Figure 9. **It is not recommended that the bias winding be connected to the VCC pin of the LM5021.**

The size of the start-up resistor Rstart not only affects power supply start-up time, but also power supply efficiency since the resistor dissipates power in normal operation. The ultra low start-up current of the LM5021 allows a large value Rstart resistor (up to 3 MΩ) for improved efficiency with reasonable start-up time.

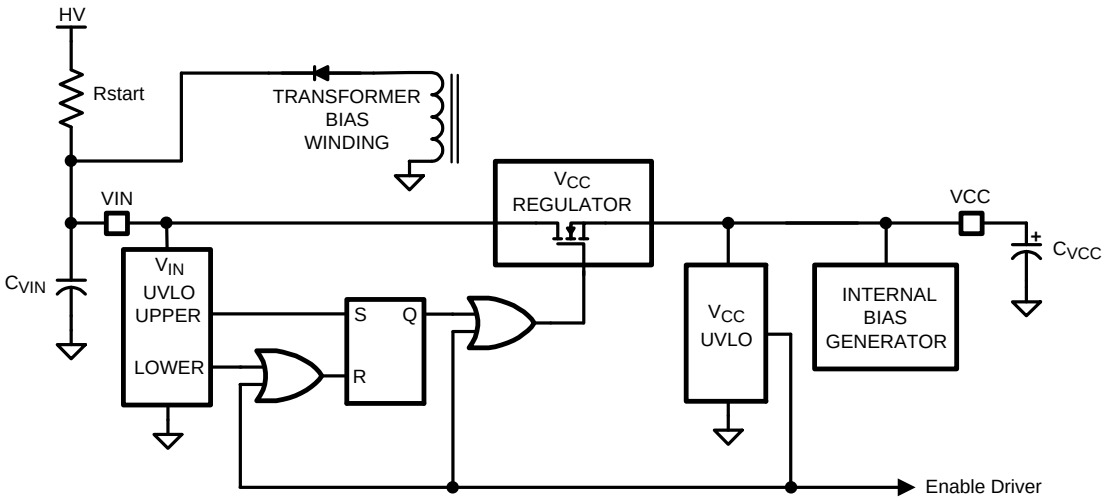


Figure 9. Start-Up Circuit Block Diagram

RELATIONSHIP BETWEEN INPUT CAPACITOR C_{IN} & V_{CC} CAPACITOR C_{VCC}

The internal VCC linear regulator is enabled when VIN reaches 20V. The drop in VIN due to charge transfer from C_{VIN} to C_{VCC} after the regulator is enabled can be calculated from the following equations where VIN' is the voltage on C_{VIN} immediately after the VCC regulator charges C_{VCC}.

$$\Delta VIN \times C_{VIN} = \Delta VCC \times C_{VCC} \quad (1)$$

$$(20V - V_{IN'}) \, C_{VIN} = 8.5V \, C_{VCC} \quad (2)$$

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$$VIN = 20V - \left(8.5V \times \frac{C_{VCC}}{C_{VIN}}\right) \quad (3)$$

Assuming C_{VIN} value as 10 µF, and C_{VCC} of 1µF, then the drop in VIN will be 0.85V, or the VIN value drops to 19.15V. The value of the VCC capacitor can be small (less than 1uF) as it supplies only transient gate drive current of a short duration. The C_{VIN} capacitor must be sized to supply the gate drive current and the quiescent current of LM5021until the transformer bias winding delivers sufficient voltage to VIN to sustain the VCC voltage.

The C_{VIN} capacitor value can be calculated from the operating VCC load current after it's output voltage reaches the VCC UVLO threshold. For example, if the LM5021 is driving an external MOSFET with total gate charge (Qg) of 25nC, the average gate drive current is Qg x Fsw, where Fsw is the switching frequency. Assuming a switching frequency of 150KHz, the average gate drive current is 3.75mA. Since the IC consumes approximately 2.5mA operating current in addition to the gate current, the total current drawn from C_{VIN} capacitor is the operating current plus the gate charge current, or 6.25mA. The C_{VIN} capacitor must supply this current for a brief time until the transformer bias winding takes over. The C_{VIN} voltage must not fall below 8.5V during the start-up sequence or the cycle will be restarted. The maximum allowable start-up time can be calculated using the value of C_{VIN}, the change in voltage allow at VIN (19.15V – 8.5V) and the VCC regulator current (6.25mA). Tmax, the maximum time allowed to energize the bias winding is:

$$Tmax = \frac{C_{VIN} \times (19.15V - 8.5V)}{6.25\ mA} = 17\ ms \quad (4)$$

If the calculated value of Tmax is too small, the value of Cin should be increased further to allow more time before the transformer bias winding takes over and delivers the operating current to the VCC regulator. Increasing C_{VIN} will increase the time from the application of the rectified ac (HV in the Figure 9) to the time when VIN reaches the 20V start threshold. The initial charging time of C_{VIN} is:

$$T_{VIN_THRESHOLD} = R_{START} \times C_{VIN} \times \ln\left[\left(1 - \frac{20V}{HV}\right)^{-1}\right] \quad (5)$$

PWM COMPARATOR/SLOPE COMPENSATION

The PWM comparator compares the current sense signal with the loop error voltage from the COMP pin. The COMP pin voltage is reduced by 1.25V then attenuated by a 3:1 resistor divider. The PWM comparator input offset voltage is designed such that less than 1.25V at the COMP pin will result in a zero duty cycle at the controller output.

For duty cycles greater than 50 percent, current mode control circuits are subject to sub-harmonic oscillation. By adding an additional fixed slope voltage ramp signal (slope compensation) to the current sense signal, this oscillation can be avoided. The LM5021-1 integrates this slope compensation by summing a ramp signal generated by the oscillator with the current sense signal. The slope compensation is generated by a current ramp driven through an internal 1.8 kΩ resistor connected to the CS pin. Additional slope compensation may be added by increasing the resistance between the current sense filter capacitor and the CS pin, thereby increasing the voltage ramp created by the oscillator current ramp. Since the LM5021-2 is not capable of duty cycles greater than 50%, there is no slope compensation feature in this device.

CURRENT LIMIT/CURRENT SENSE

The LM5021 provides a cycle-by-cycle over current protection feature. Current limit is triggered by an internal current sense comparator threshold which is set at 500mV. If the CS pin voltage plus the slope compensation voltage exceeds 500mV, the OUT pin output pulse will be immediately terminated.

An RC filter, located near the LM5021, is recommended for the CS pin to attenuate the noise coupled from the power FET's gate to source. The CS pin capacitance is discharged at the end of each PWM clock cycle by an internal switch. The discharge switch remains on for an additional 90ns leading edge blanking interval to attenuate the current sense transient that occurs when the external power FET is turned on. In addition to providing leading edge blanking, this circuit also improves dynamic performance by discharging the current sense filter capacitor at the conclusion of every cycle.

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The LM5021 CS comparator is very fast, and may respond to short duration noise pulses. Layout considerations are critical for the current sense filter and sense resistor. The capacitor associated with the CS filter must be placed very close to the device and connected directly to the pins of the IC (CS and GND). If a current sense transformer is used, both leads of the transformer secondary should be routed to the sense resistor, which should also be located close to the IC. If a current sense resistor located in the power FET's source is used for current sense, a low inductance resistor is required. In this case, all of the noise sensitive low current grounds should be connected in common near the IC and then a single connection should be made to the power ground (sense resistor ground point).

OSCILLATOR, SHUTDOWN and SYNC CAPABILITY

A single external resistor connected between RT and GND pins sets the LM5021 oscillator frequency. The LM5021-2 device, with 50% maximum duty cycle, includes an internal flip-flop that divides the oscillator frequency by two. This method produces a precise 50% maximum duty cycle limit. Because of this frequency divider, the oscillator frequency of the LM5021-2 is actually twice the frequency of the gate drive output (OUT). For the LM5021-1 device, the oscillator frequency and the operational output frequency are the same. To set a desired output switching frequency (Fsw), the RT resistor can be calculated from:

LM5021-1:

$$RT = \frac{6.63 \times 10^9}{F_{SW}} \quad (6)$$

LM5021-2:

$$RT = \frac{6.63 \times 10^9}{2 \times F_{SW}} \quad (7)$$

The LM5021 can also be synchronized to an external clock. The external clock must have a higher frequency than the free running oscillator frequency set by the RT resistor. The clock signal should be capacitively coupled into the RT pin with a 100pF capacitor. A peak voltage level greater than 3.8 Volts at the RT pin is required for detection of the sync pulse. The dc voltage across the RT resistor is internally regulated at 2 volts. Therefore, the ac pulse superimposed on the RT resistor must have 1.8V or greater amplitude to successfully synchronize the oscillator. The sync pulse width should be set between 15ns to 150ns by the external components. The RT resistor is always required, whether the oscillator is free running or externally synchronized. The RT resistor should be located very close to the device and connected directly to the pins of the LM5021 (RT and GND).

GATE DRIVER and MAX DUTY CYCLE LIMIT

The LM5021 provides a gate driver (OUT), which can source peak current of 0.3A and sink 0.7A. The LM5021 is available in two duty-cycle limit options. The maximum output duty-cycle is typically 80% for the LM5021-1 option, and precisely equal to 50% for the LM5021-2 option. The maximum duty cycle function for the LM5021-2 is accomplished with an internal toggle flip-flop to ensure an accurate duty cycle limit. The internal oscillator frequency of the LM5021-2 is therefore twice the switching frequency of the PWM controller (OUT pin).

The 80% maximum duty-cycle function for the LM5021-1 is determined by the internal oscillator. For the LM5021-1 the internal oscillator frequency and the switching frequency of the PWM controller are the same.

SOFT-START

The soft-start feature allows the power converter to gradually reach the initial steady state operating point, thus reducing start-up stresses and current surges. An internal 22 µA current source charges an external capacitor connected to the SS pin. The capacitor voltage will ramp up slowly, limiting the COMP pin voltage and the duty cycle of the output pulses. The soft-start capacitor is also used to generate the hiccup mode delay time when the output of the switching power supply is continuously overloaded.

HICCUP MODE OVERLOAD CURRENT LIMITING

Hiccup mode is a method of protecting the power supply from over-heating and damage during an extended overload condition. When the output fault is removed the power supply will automatically restart.

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Figure 10, Figure 11, and Figure 12 illustrate the equivalent circuit of the hiccup mode for LM5021 and the relevant waveforms. During start-up and in normal operation, the external soft-start capacitor Css is pulled up by a current source that delivers 22 µA to the SS pin capacitor. In normal operation, the soft-start capacitor continues to charge and eventually reaches the saturation voltage of the current source (V_{SS_OCV}, nominally 5.2V). During start-up the COMP pin voltage follows the SS capacitor voltage and gradually increases the peak current delivered by the power supply. When the output of the switching power supply reaches the desired voltage, the voltage feedback amplifier takes control of the COMP signal (via the opto-coupler). In normal operation the COMP level is held at an intermediate voltage between 1.25V and 2.75V controlled by the voltage regulation loop. When the COMP pin voltage is below 1.25V, the duty-cycle is zero. When the COMP level is above 2.75V, the duty cycle will be limited by the 0.5V threshold of cycle-by-cycle current limit comparator.

If the output of the power supply is overloaded, the voltage regulation loop demands more current by increasing the COMP pin control voltage. When the COMP pin exceeds the over voltage detection threshold (V_{OVLD}, nominally 4.6V), the SS capacitor Css will be discharged by a 10 µA overload detection timer current source, I_{OVCS}. If COMP remains above V_{OVLD} long enough for the SS capacitor to discharge to the Hiccup mode threshold (V_{HIC}, nominally 4.6V), the controller enters the hiccup mode. The OUT pin is then latched low and the SS capacitor discharge current source is reduced from 10 µA to 0.25 µA, the dead-time current source, I_{DTCS}. The SS pin voltage is slowly reduced until it reaches the Restart threshold (V_{RST}, nominally 0.3V). Then a new start-up sequence commences with 22 µA current source charging the capacitor C_{SS}. The slow discharge of the SS capacitor from the Hiccup threshold to the Restart threshold provides an extended off time that reduces the overheating of components including diodes and MOSFETs due to the continuous overload. The off time during the hiccup mode can be calculated from the following equation:

$$Toff = \frac{C_{SS} \times (V_{HC} - V_{RST})}{I_{DTCS}} = \frac{C_{SS} \times (4.6V - 0.3V)}{0.25\ \mu A} \quad (8)$$

Example:

Toff = 808 ms, assuming the C_{SS} capacitor value is 0.047 µF

Short duration intermittent overloads will not trigger the hiccup mode. The overload duration required to trigger the hiccup response is set by the capacitor C_{SS}, the 10 µA discharge current source and voltage difference between the saturation level of the SS pin and the Hiccup mode threshold. Figure 12 shows the waveform of SS pin with a short duration overload condition. The overload time required to enter the hiccup mode can be calculated from the following equation:

$$Toverload = \frac{C_{SS} \times (V_{SS_OCV} - V_{HC})}{I_{OVCS}} = \frac{C_{SS} \times 0.6V}{10\ \mu A} \quad (9)$$

Example:

Toverload = 2.82 ms, assuming the C_{SS} capacitor value is 0.047 µF

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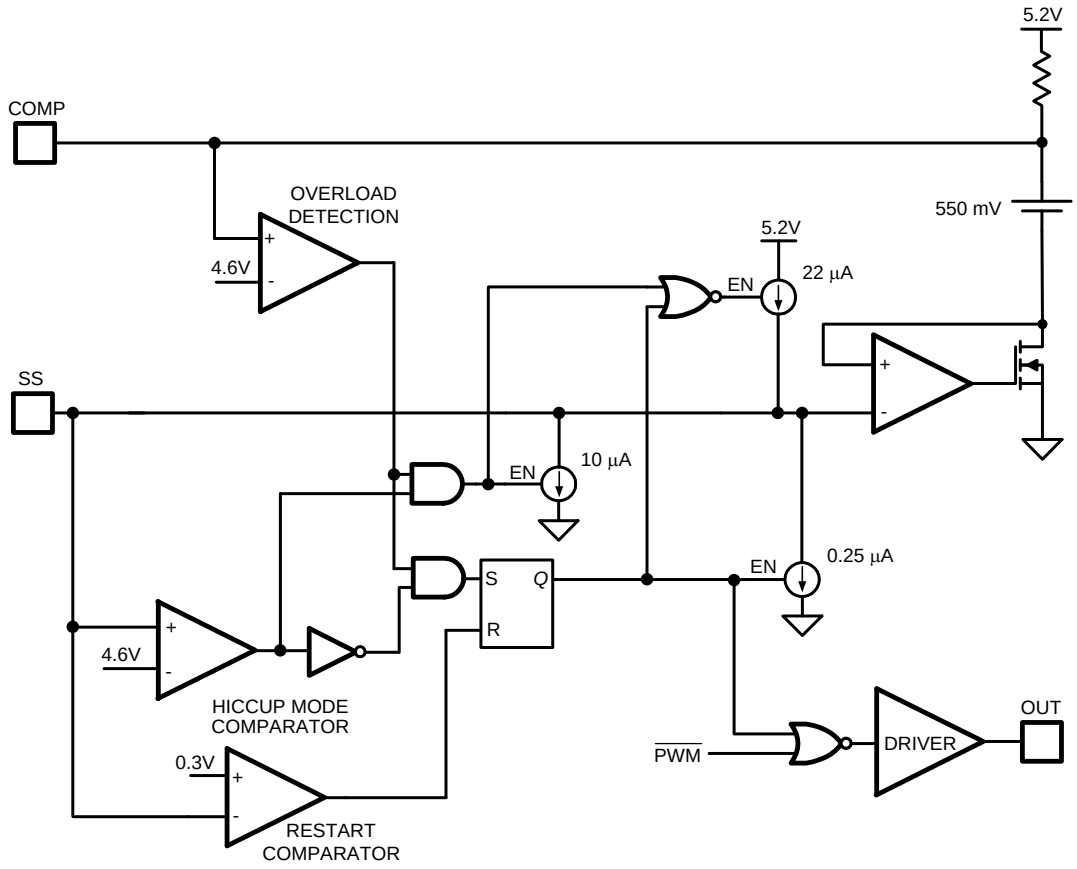


Figure 10. Hiccup Mode Control

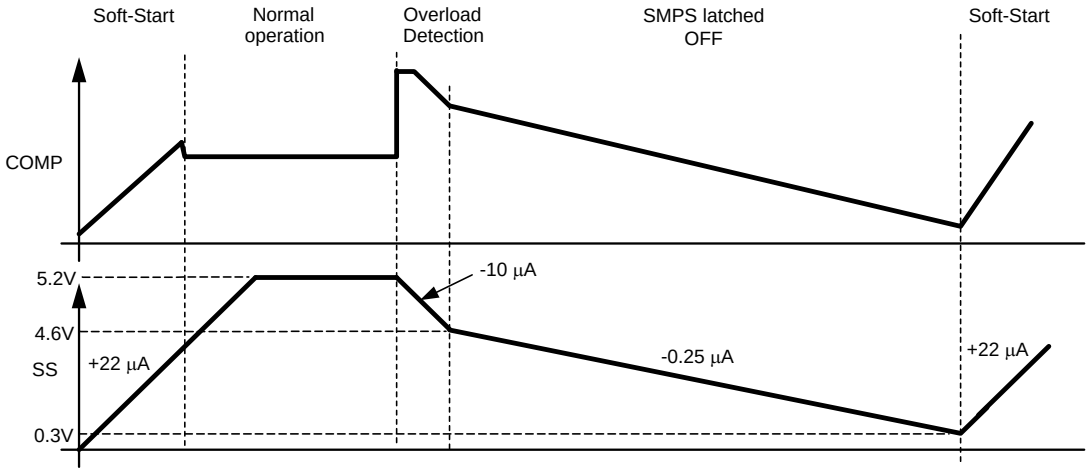


Figure 11. Waveform at SS and COMP Pin due to Continuous Overload

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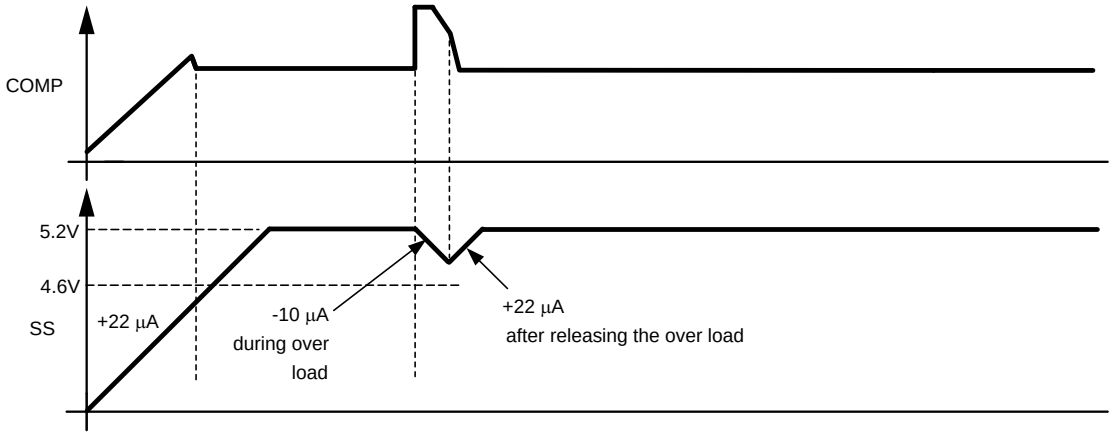


Figure 12. Waveform at SS and COMP Pin due to Brief Overload

SKIP CYCLE OPERATION

During light load conditions, the efficiency of the switching power supply typically drops as the losses associated with switching and operating bias currents of the converter become a significant percentage of the power delivered to the load. The largest component of the power loss is the switching loss associated with the gate driver and external MOSFET gate charge. Each PWM cycle consumes a finite amout of energy as the MOSFET is turned on and then turned off. These switching losses are proportional to the frequency of operation. The Skip Cycle function integrated within the LM5021 controller reduces the average switching frequency to reduce switching losses and improve efficiency during light load conditions.

When a light load condition occurs, the COMP pin voltage is reduced by the voltage feedback loop to reduce the peak current delivered by the controller. Referring to Figure 13, the PWM comparator input tracks the COMP pin voltage through a 1.25V level shift circuit and a 3:1 resistor divider. As the COMP pin voltage falls, the input to the PWM comparator falls proportionately. When the PWM comparator input falls to 125mV, the Skip Cycle comparator detects the light load condition and disables output pulses from the controller. The controller continues to skip switching cycles until the power supply output falls and the COMP pin voltage increases to demand more output current. The number of cycles skipped will depend on the load and the response time of the frequency compensation network. Eventually the COMP voltage will increase when the voltage loop requires more current to sustain the regulated output voltage. When the PWM comparator input exceeds 130mV (5mV hysteresis), normal fixed frequency switching resumes. Typical power supply designs will produce a short burst of output pulses followed by a long skip cycle interval. The average switching frequency in the Skip Cycle mode can be a small fraction of the normal operating frequency of the power supply.

The skip cycle mode of operation can be disabled by adding an offset voltage to the CS pin (refer to Figure 14). A resistive divider connected to a regulated source, injecting a 125mV offset (minimum) on the CS pin, will force the voltage at the PWM Comparator to be greater than 125 mV, disabling the Skip Cycle Comparator.

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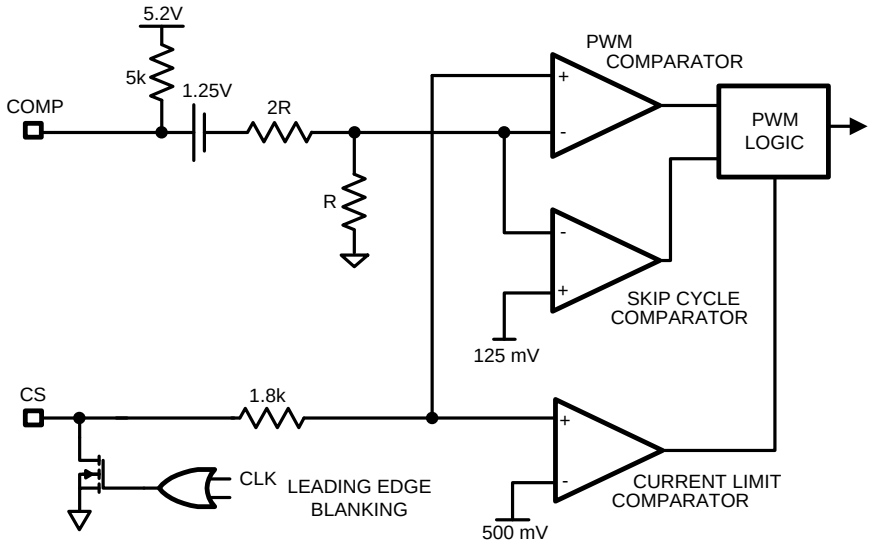


Figure 13. Skip Cycle Control

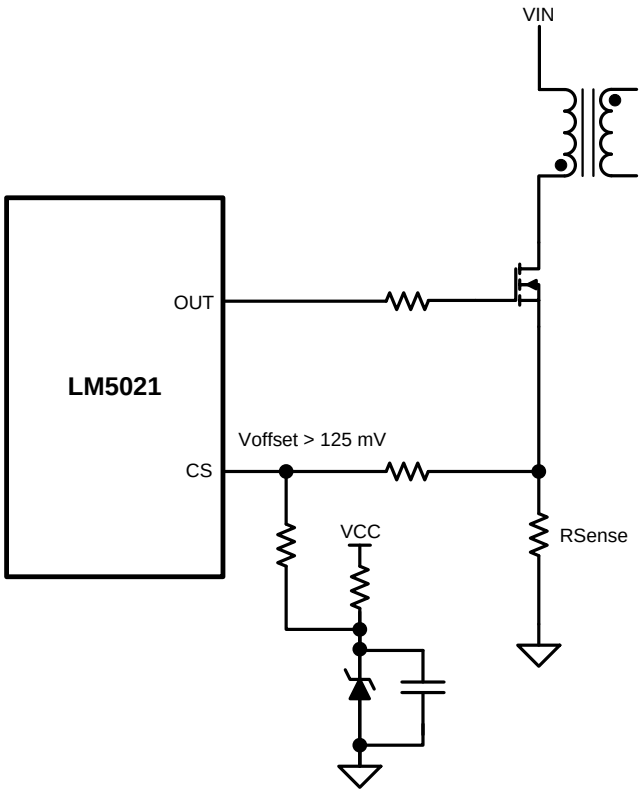
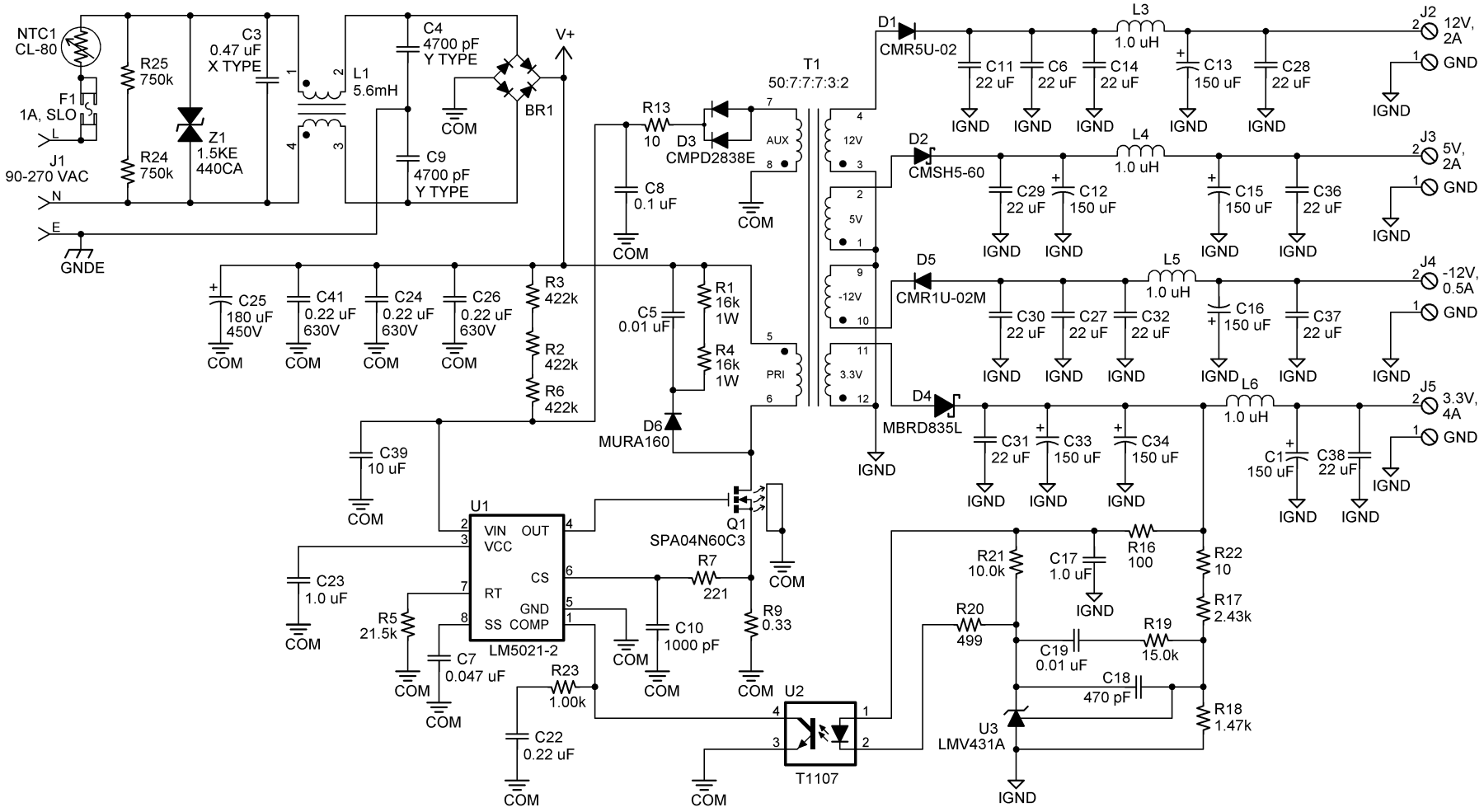


Figure 14. Disabling the Skip Cycle Mode

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Typical Application Circuit



REVISION HISTORY

Changes from Revision C (March 2013) to Revision D	Page
• Changed layout of National Data Sheet to TI format	15

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PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
LM5021MM-1/NOPB	ACTIVE	VSSOP	DGK	8	1000	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 125	21-1	Samples
LM5021MM-2	NRND	VSSOP	DGK	8	1000	TBD	Call TI	Call TI	-40 to 125	21-2	
LM5021MM-2/NOPB	ACTIVE	VSSOP	DGK	8	1000	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 125	21-2	Samples
LM5021MMX-1/NOPB	ACTIVE	VSSOP	DGK	8	3500	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 125	21-1	Samples
LM5021MMX-2	NRND	VSSOP	DGK	8	3500	TBD	Call TI	Call TI	-40 to 125	21-2	
LM5021MMX-2/NOPB	ACTIVE	VSSOP	DGK	8	3500	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 125	21-2	Samples
LM5021NA-1/NOPB	ACTIVE	PDIP	P	8	40	Green (RoHS & no Sb/Br)	CU SN	Level-1-NA-UNLIM	-40 to 125	LM5021NA -1	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

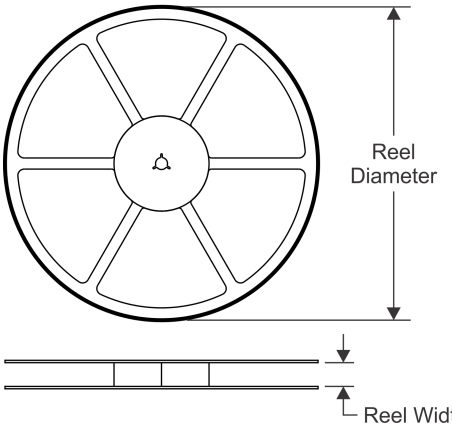
(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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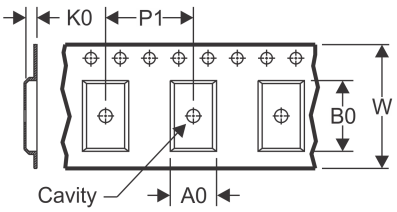
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TAPE AND REEL INFORMATION

REEL DIMENSIONS

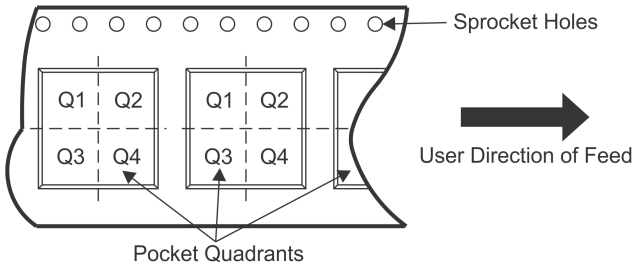


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

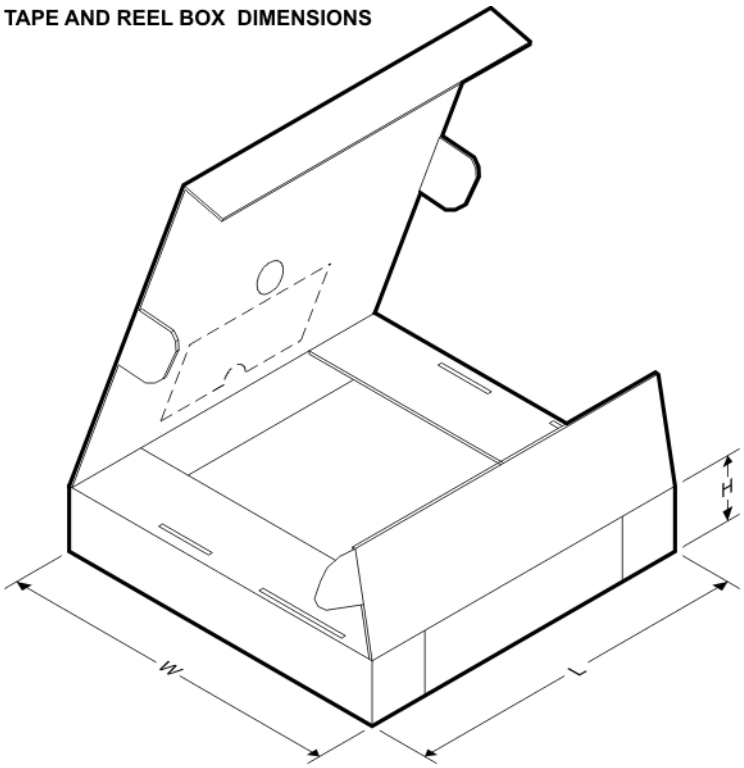
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
LM5021MM-1/NOPB	VSSOP	DGK	8	1000	178.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
LM5021MM-2	VSSOP	DGK	8	1000	178.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
LM5021MM-2/NOPB	VSSOP	DGK	8	1000	178.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
LM5021MMX-1/NOPB	VSSOP	DGK	8	3500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
LM5021MMX-2	VSSOP	DGK	8	3500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
LM5021MMX-2/NOPB	VSSOP	DGK	8	3500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1

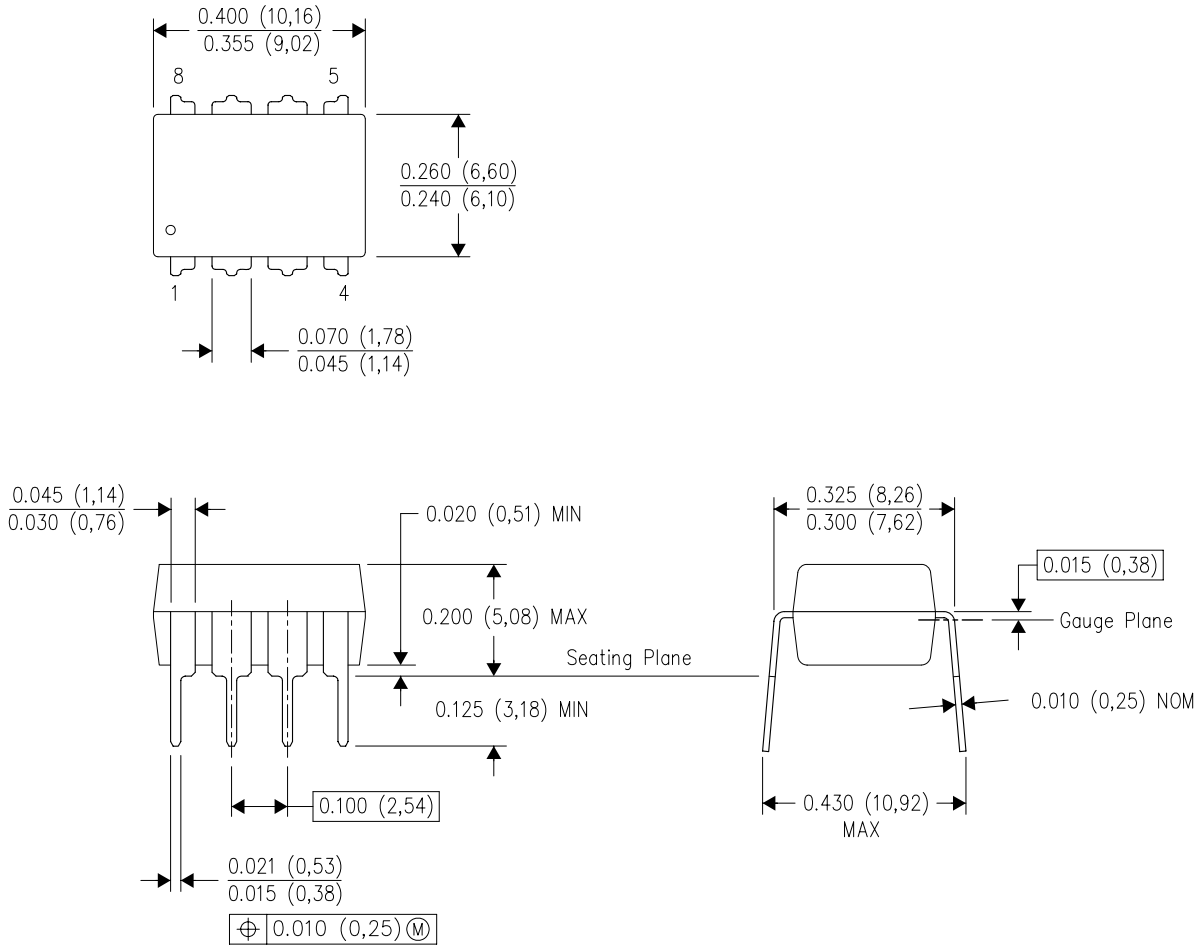
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

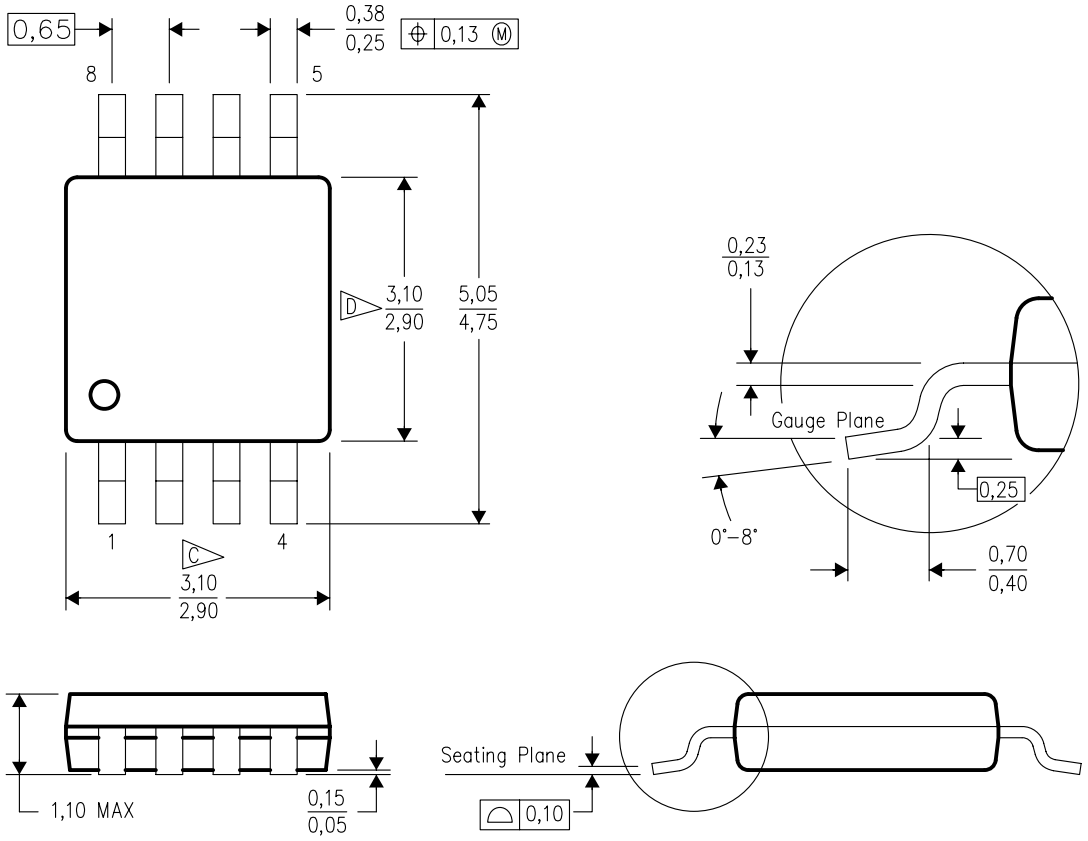
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
LM5021MM-1/NOPB	VSSOP	DGK	8	1000	210.0	185.0	35.0
LM5021MM-2	VSSOP	DGK	8	1000	210.0	185.0	35.0
LM5021MM-2/NOPB	VSSOP	DGK	8	1000	210.0	185.0	35.0
LM5021MMX-1/NOPB	VSSOP	DGK	8	3500	367.0	367.0	35.0
LM5021MMX-2	VSSOP	DGK	8	3500	367.0	367.0	35.0
LM5021MMX-2/NOPB	VSSOP	DGK	8	3500	367.0	367.0	35.0

P (R–PDIP–T8) PLASTIC DUAL–IN–LINE PACKAGE



NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Falls within JEDEC MS–001 variation BA.

DGK (S–PDSO–G8) PLASTIC SMALL–OUTLINE PACKAGE



4073329/E 05/06

NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 per end.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0.50 per side.
E. Falls within JEDEC MO–187 variation AA, except interlead flash.

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