LM5000 High Voltage Switch Mode Regulator

Check for Samples: LM5000

FEATURES

- **80V Internal Switch**
- **Operating Input Voltage Range of 3.1V to 40V**
- **Pin Selectable Operating Frequency**
  - **300kHz/700kHz (-3)**
  - **600kHz/1.3MHz (-6)**
- **Adjustable Output Voltage**
- **External Compensation**
- **Input Undervoltage Lockout**
- **Softstart**
- **Current Limit**
- **Over Temperature Protection**
- **External Shutdown**
- **Small 16-Lead TSSOP or 16-Lead WSON Package**

APPLICATIONS

- **Flyback Regulator**
- **Forward Regulator**
- **Boost Regulator**
- **DSL Modems**
- **Distributed Power Converters**

DESCRIPTION

The LM5000 is a monolithic integrated circuit specifically designed and optimized for flyback, boost or forward power converter applications. The internal power switch is rated for a maximum of 80V, with a current limit set to 2A. Protecting the power switch are current limit and thermal shutdown circuits. The current mode control scheme provides excellent rejection of line transients and cycle-by-cycle current limiting. An external compensation pin and the built-in slope compensation allow the user to optimize the frequency compensation. Other distinctive features include softstart to reduce stresses during start-up and an external shutdown pin for remote ON/OFF control. There are two operating frequency ranges available. The LM5000-3 is pin selectable for either 300kHz (FS Grounded) or 700kHz (FS Open). The LM5000-6 is pin selectable for either 600kHz (FS Grounded) or 1.3MHz (FS Open). The device is available in a low profile 16-lead TSSOP package or a thermally enhanced 16-lead WSON package.

Typical Application Circuit

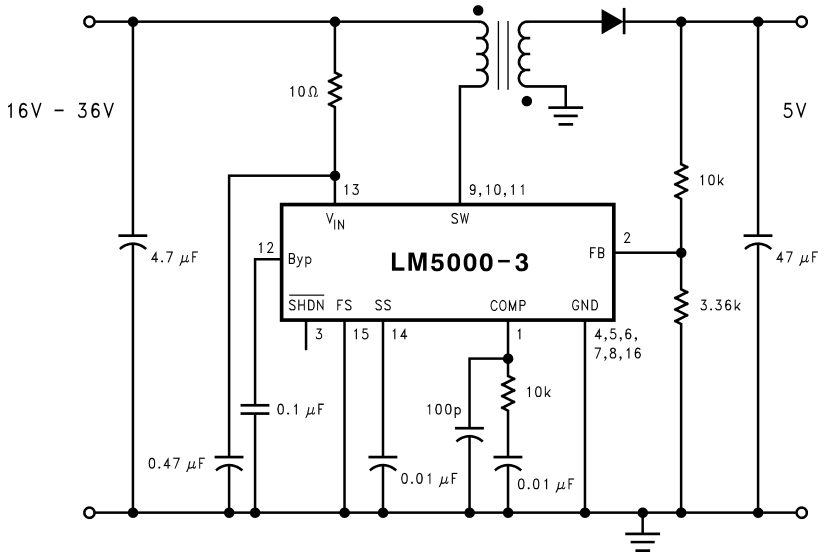


Figure 1. LM5000 Flyback Converter

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Connection Diagram

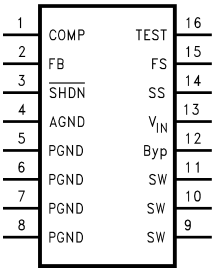


Figure 2. Top View

PIN DESCRIPTIONS

Pin	Name	Function
1	COMP	Compensation network connection. Connected to the output of the voltage error amplifier. The RC compenstion network should be connected from this pin to AGND. An additional 100pF high frequency capacitor to AGND is recommended.
2	FB	Output voltage feedback input.
3	$\overline{\text{SHDN}}$	Shutdown control input, Open = enable, Ground = disable.
4	AGND	Analog ground, connect directly to PGND.
5	PGND	Power ground.
6	PGND	Power ground.
7	PGND	Power ground.
8	PGND	Power ground.
9	SW	Power switch input. Switch connected between SW pins and PGND pins
10	SW	Power switch input. Switch connected between SW pins and PGND pins
11	SW	Power switch input. Switch connected between SW pins and PGND pins
12	BYP	Bypass-Decouple Capacitor Connection, 0.1µF ceramic capacitor recommended.
13	V_{IN}	Analog power input. A small RC filter is recommended, to suppress line glitches. Typical values of 10Ω and ≥ 0.1µF are recommended.
14	SS	Softstart Input. External capacitor and internal current source sets the softstart time.
15	FS	Switching frequency select input. Open = F_{high}. Ground = F_{low}
16	TEST	Factory test pin, connect to ground.
-	Exposed Pad underside of WSON package	Connect to system ground plane for reduced thermal resistance.

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These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

Absolute Maximum Ratings[1][2]

V_{IN}		-0.3V to 40V
SW Voltage		-0.3V to 80V
FB Voltage		-0.3V to 5V
COMP Voltage		-0.3V to 3V
All Other Pins		-0.3V to 7V
Maximum Junction Temperature		150°C
Power Dissipation[3]		Internally Limited
Lead Temperature		216°C
Infrared (15 sec.)		235°C
ESD Susceptibility[4]	Human Body Model	2kV
	Machine Model	200V
Storage Temperature		−65°C to +150°C

(1) Absolute maximum ratings are limits beyond which damage to the device may occur. Operating Ratings are conditions for which the device is intended to be functional, but device parameter specifications may not be ensured. For ensured specifications and test conditions, see the Electrical Characteristics.
(2) If Military/Aerospace specified devices are required, please contact the Texas Instruments Sales Office/Distributors for availability and specifications.
(3) The maximum allowable power dissipation is a function of the maximum junction temperature, $T_J(MAX)$, the junction-to-ambient thermal resistance, θ_{JA}, and the ambient temperature, T_A. See the Electrical Characteristics table for the thermal resistance of various layouts. The maximum allowable power dissipation at any ambient temperature is calculated using: $P_D (MAX) = (T_{J(MAX)} - T_A)/\theta_{JA}$. Exceeding the maximum allowable power dissipation will cause excessive die temperature, and the regulator will go into thermal shutdown.
(4) The human body model is a 100 pF capacitor discharged through a 1.5kΩ resistor into each pin. The machine model is a 200pF capacitor discharged directly into each pin.

Operating Conditions

Operating Junction Temperature Range[1]	−40°C to +125°C
Supply Voltage[1]	3.1V to 40V

(1) Supply voltage, bias current product will result in aditional device power dissipation. This power may be significant. The thermal dissipation design should take this into account.

Electrical Characteristics

Specifications in standard type face are for T_J = 25°C and those with **boldface type** apply over the full **Operating Temperature Range** (T_J = −40°C to +125°C) Unless otherwise specified. V_{IN} = 12V and I_L = 0A, unless otherwise specified.

Symbol	Parameter	Conditions	Min[1]	Typ[2]	Max[1]	Units
I_Q	Quiescent Current	FB = 2V (Not Switching) FS = 0V		2.0	**2.5**	mA
		FB = 2V (Not Switching) FS = Open		2.1	**2.5**	mA
		$V_{\overline{SHDN}}$ = 0V		18	**30**	µA
V_{FB}	Feedback Voltage		**1.2330**	1.259	**1.2840**	V
I_{CL}	Switch Current Limit		**1.35**	2.0	**2.7**	A
$\%V_{FB}/\Delta V_{IN}$	Feedback Voltage Line Regulation	3.1V ≤ V_{IN} ≤ 40V		0.001	**0.04**	%/V
I_B	FB Pin Bias Current[3]			55	**200**	nA

(1) All limits specified at room temperature (standard typeface) and at temperature extremes (bold typeface). All room temperature limits are 100% production tested. All limits at temperature extremes are specified via correlation using standard Statistical Quality Control (SQC) methods. All limits are used to calculate Average Outgoing Quality Level (AOQL).
(2) Typical numbers are at 25°C and represent the most likely norm.
(3) Bias current flows into FB pin.

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Electrical Characteristics (continued)

Specifications in standard type face are for T_J = 25°C and those with **boldface type** apply over the full **Operating Temperature Range** (T_J = −40°C to +125°C) Unless otherwise specified. V_{IN} = 12V and I_L = 0A, unless otherwise specified.

Symbol	Parameter	Conditions	Min(1)	Typ(2)	Max(1)	Units
BV	Output Switch Breakdown Voltage	T_J = 25°C, I_{SW} = 0.1µA	80			V
		T_J = -40°C to + 125°C, I_{SW} = 0.5µA	**76**			
V_{IN}	Input Voltage Range		**3.1**		**40**	V
g_m	Error Amp Transconductance	ΔI = 5µA	**150**	410	**750**	µmho
A_V	Error Amp Voltage Gain			280		V/V
D_{MAX}	Maximum Duty Cycle LM5000-3	FS = 0V	**85**	90		%
	Maximum Duty Cycle LM5000-6	FS = 0V	**85**	90		%
T_{MIN}	Minimum On Time			165		ns
f_S	Switching Frequency LM5000-3	FS = 0V	**240**	300	**360**	kHz
		FS = Open	**550**	700	**840**	
	Switching Frequency LM5000-6	FS = 0V	**485**	600	**715**	
		FS = Open	**1.055**	1.3	**1.545**	MHz
$I_{\overline{SHDN}}$	Shutdown Pin Current	$V_{\overline{SHDN}}$ = 0V		−1	**-2**	µA
I_L	Switch Leakage Current	V_{SW} = 80V		0.008	**5**	µA
R_{DSON}	Switch R_{DSON}	I_{SW} = 1A		160	**445**	mΩ
Th_{SHDN}	$\overline{SHDN}$ Threshold	Output High	**0.9**	0.6		V
		Output Low		0.6	**0.3**	V
UVLO	On Threshold		**2.74**	2.92	**3.10**	V
	Off Threshold		**2.60**	2. 77	**2.96**	V
OVP	V_{COMP} Trip			0.67		V
I_{SS}	Softstart Current		**8**	11	**14**	µA
θ_{JA}	Thermal Resistance	TSSOP, Package only		150		°C/W
		WSON, Package only		45		

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Typical Performance Characteristics

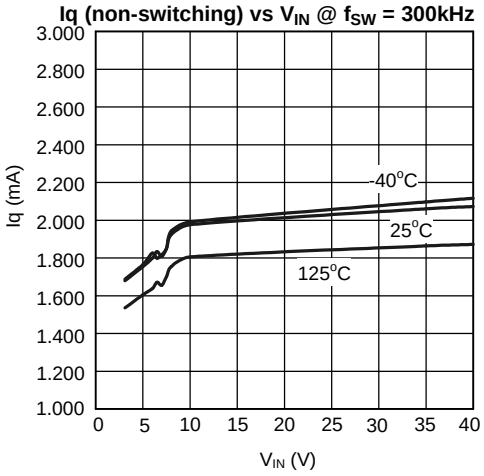


Figure 3.

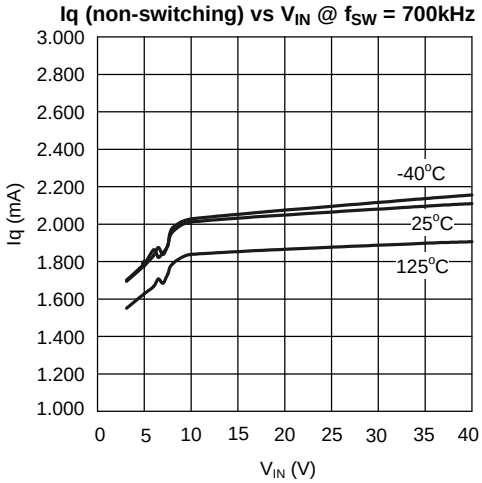


Figure 4.

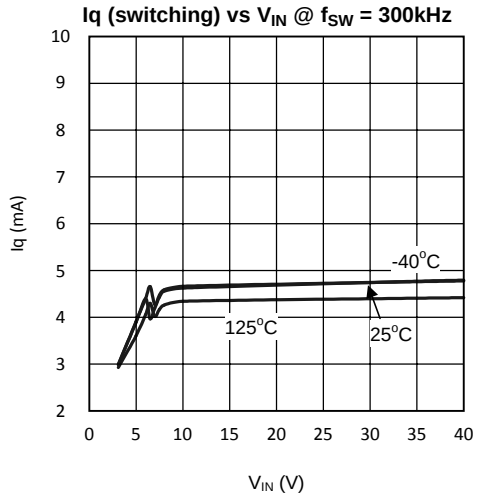


Figure 5.

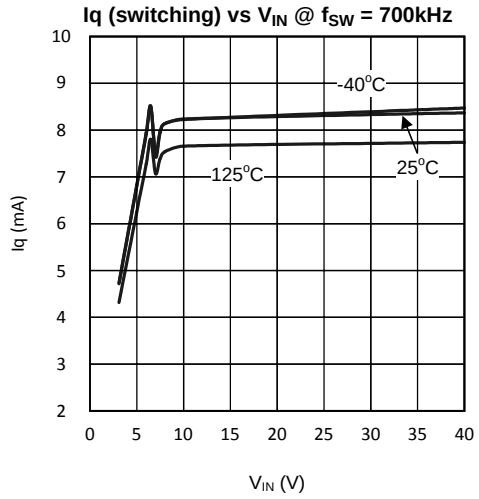


Figure 6.

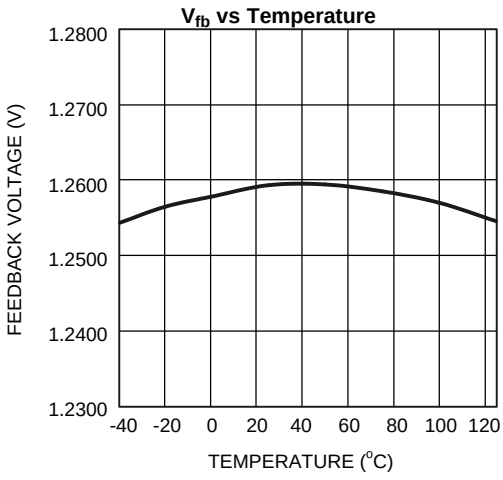


Figure 7.

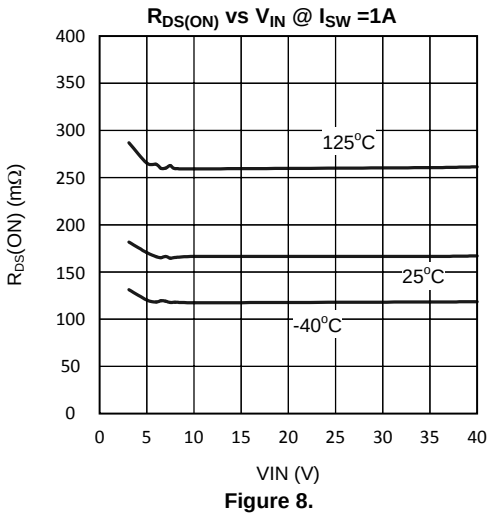


Figure 8.

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Typical Performance Characteristics (continued)

Current Limit vs Temperature

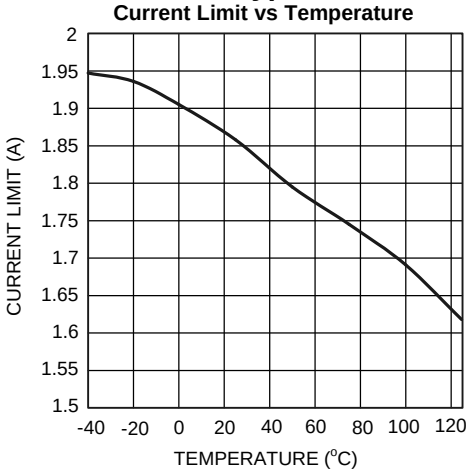


Figure 9.

Current Limit vs V_{IN}

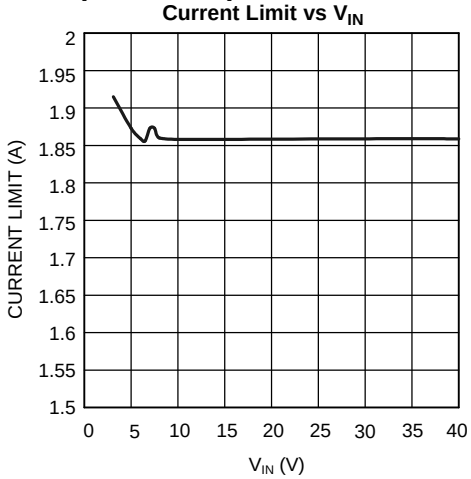


Figure 10.

f_{SW} vs. V_{IN} @ FS = Low (-3)

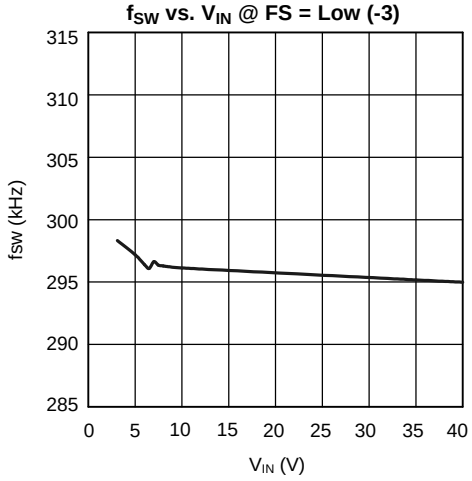


Figure 11.

f_{SW} vs. V_{IN} @ FS = OPEN (-3)

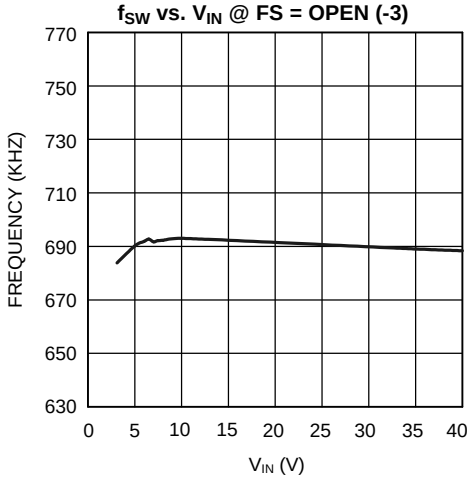


Figure 12.

f_{SW} vs. Temperature @ FS = Low (-3)

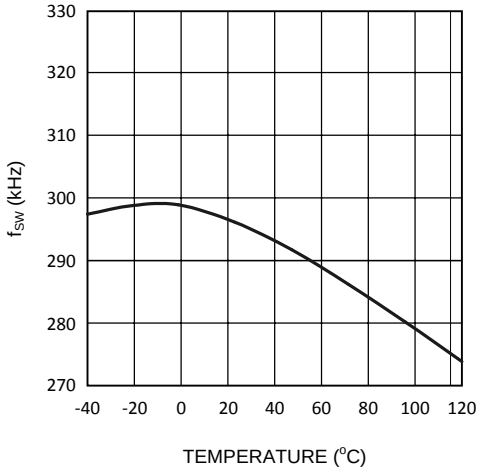


Figure 13.

f_{SW} vs. Temperature @ FS = OPEN (-3)

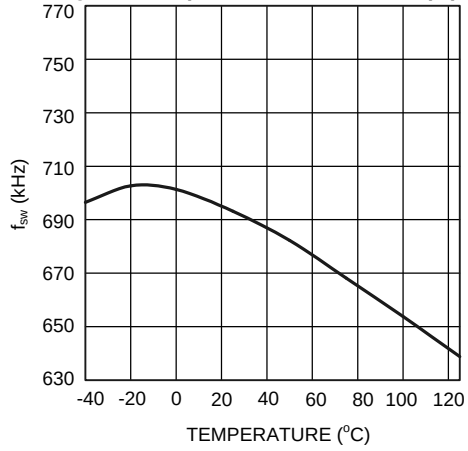


Figure 14.

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Typical Performance Characteristics (continued)

f_{SW} vs. Temperature @ FS = Low (-6)

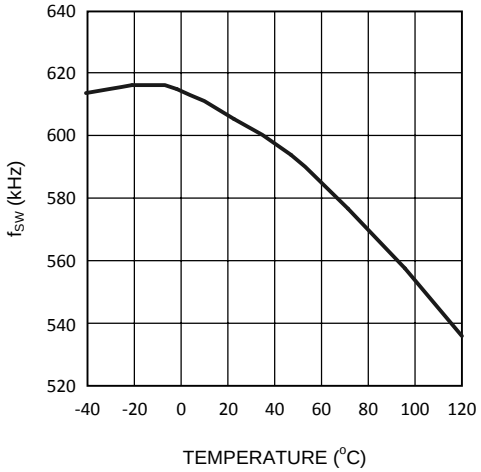


Figure 15.

f_{SW} vs. Temperature @ FS = OPEN (-6)

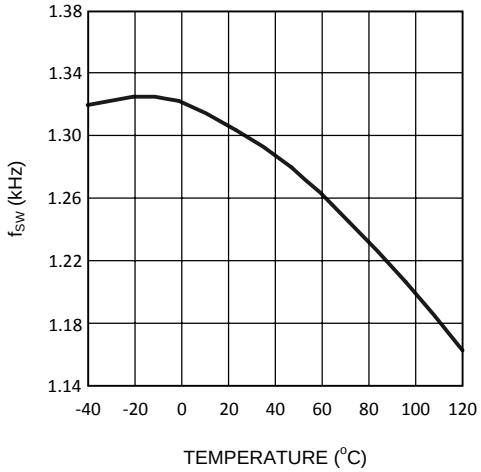


Figure 16.

Error Amp. Transconductance vs Temp.

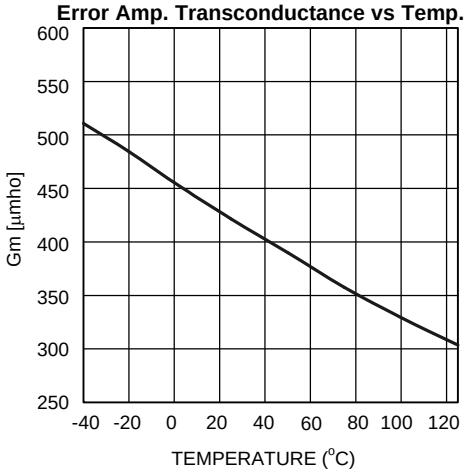


Figure 17.

BYP Pin Voltage vs V_{IN}

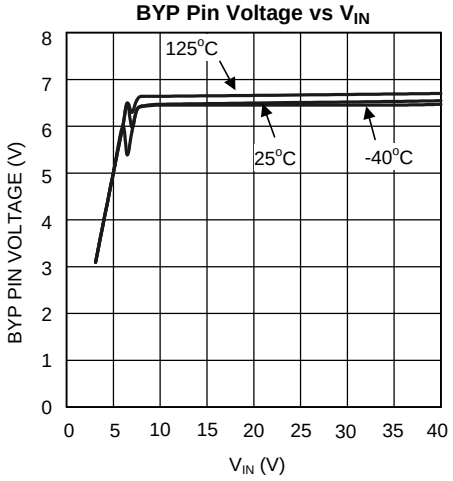


Figure 18.

Typical Application Diagrams

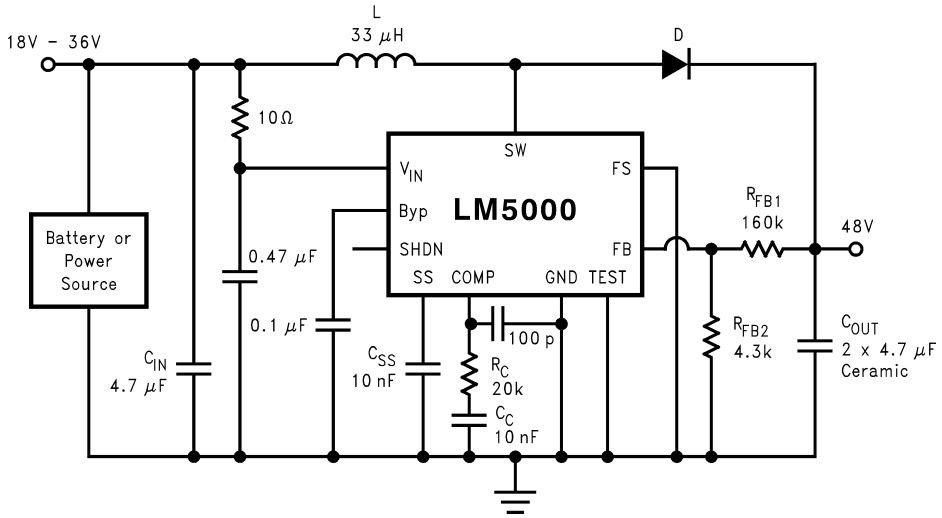


Figure 19. 300 kHz operation, 48V output

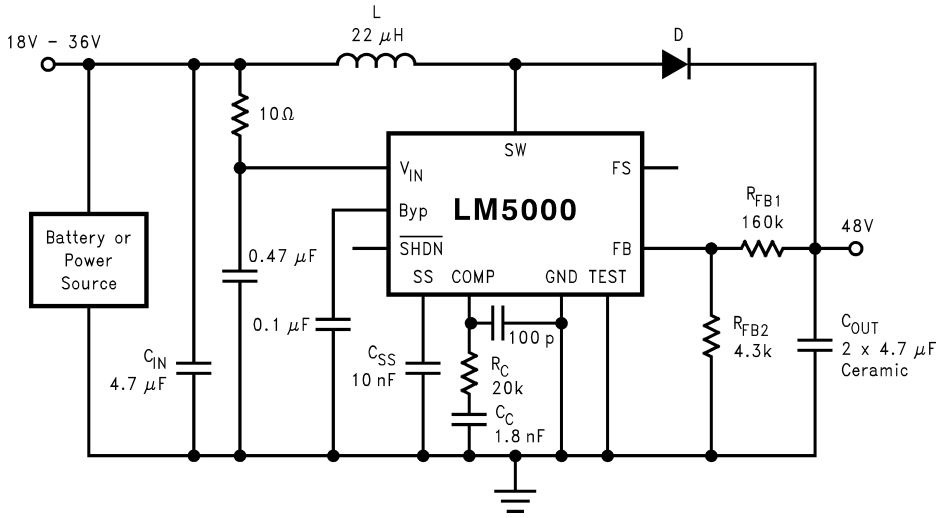
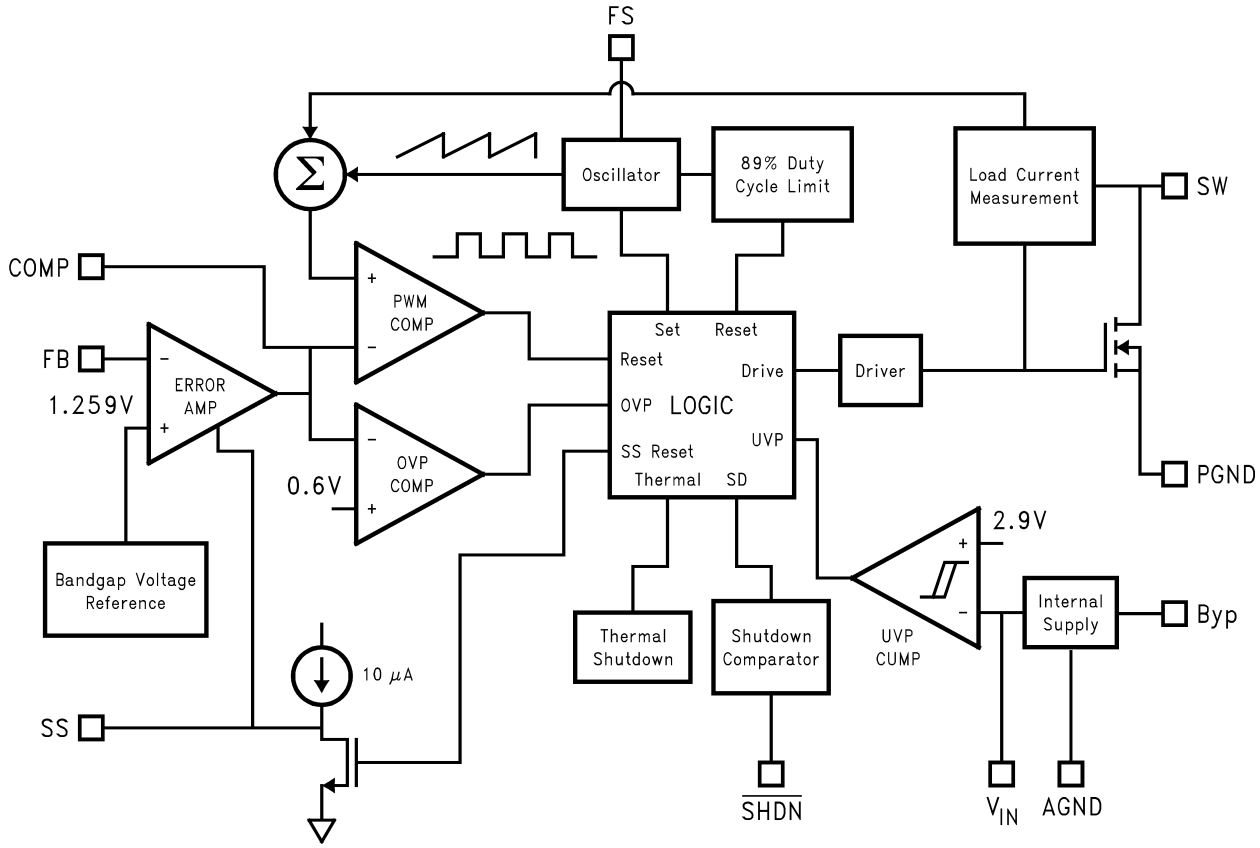


Figure 20. 700 kHz operation, 48V output

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Block Diagram



BOOST REGULATOR OPERATION

The LM5000 utilizes a PWM control scheme to regulate the output voltage over all load conditions. The operation can best be understood referring to the block diagram and Figure 21. At the start of each cycle, the oscillator sets the driver logic and turns on the NMOS power device conducting current through the inductor, cycle 1 of Figure 21 (a). During this cycle, the voltage at the COMP pin controls the peak inductor current. The COMP voltage will increase with larger loads and decrease with smaller. This voltage is compared with the summation of the SW volatge and the ramp compensation.The ramp compensation is used in PWM architectures to eliminate the sub-harmonic oscillations that occur during duty cycles greater than 50%. Once the summation of the ramp compensation and switch voltage equals the COMP voltage, the PWM comparator resets the driver logic turning off the NMOS power device. The inductor current then flows through the output diode to the load and output capacitor, cycle 2 of Figure 21 (b). The NMOS power device is then set by the oscillator at the end of the period and current flows through the inductor once again.

The LM5000 has dedicated protection circuitry running during the normal operation to protect the IC. The Thermal Shutdown circuitry turns off the NMOS power device when the die temperature reaches excessive levels. The UVP comparator protects the NMOS power device during supply power startup and shutdown to prevent operation at voltages less than the minimum input voltage. The OVP comparator is used to prevent the output voltage from rising at no loads allowing full PWM operation over all load conditions. The LM5000 also features a shutdown mode. An external capacitor sets the softstart time by limiting the error amp output range, as the capacitor charges up via an internal 10µA current source.

The LM5000 is available in two operating frequency ranges. The LM5000-3 is pin selectable for either 300kHz (FS Grounded) or 700kHz (FS Open). The LM5000-6 is pin selectable for either 600kHz (FS Grounded) or 1.3MHz (FS Open)

Operation

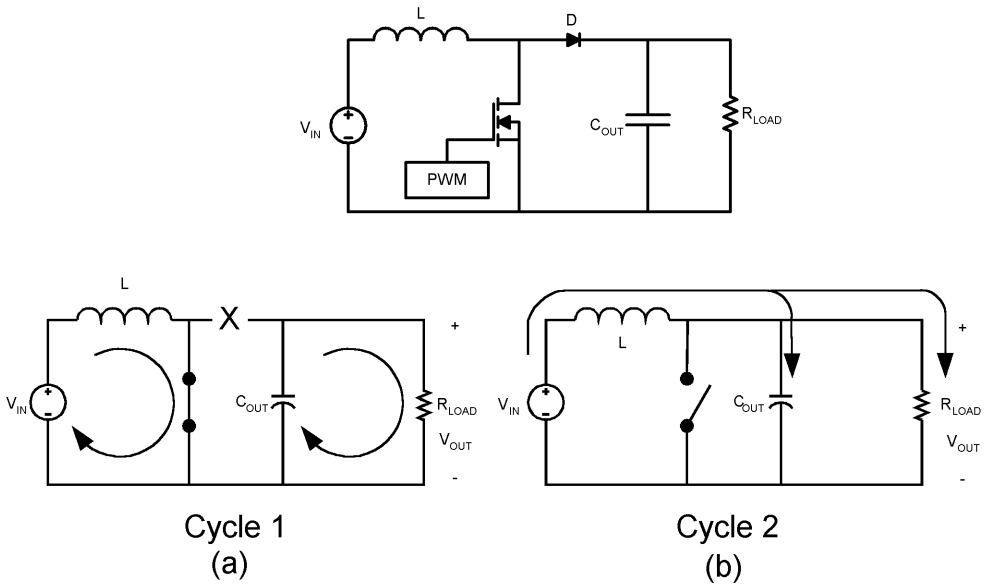


Figure 21. Simplified Boost Converter Diagram
(a) First Cycle of Operation (b) Second Cycle Of Operation

CONTINUOUS CONDUCTION MODE

The LM5000 is a current-mode, PWM regulator. When used as a boost regulator the input voltage is stepped up to a higher output voltage. In continuous conduction mode (when the inductor current never reaches zero at steady state), the boost regulator operates in two cycles.

In the first cycle of operation, shown in Figure 21 (a), the transistor is closed and the diode is reverse biased. Energy is collected in the inductor and the load current is supplied by C_{OUT}.

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The second cycle is shown in Figure 21 (b). During this cycle, the transistor is open and the diode is forward biased. The energy stored in the inductor is transferred to the load and output capacitor.

The ratio of these two cycles determines the output voltage. The output voltage is defined approximately as:

$$V_{OUT} = \frac{V_{IN}}{1-D}, \quad D' = (1-D) = \frac{V_{IN}}{V_{OUT}} \tag{1}$$

where

- D is the duty cycle of the switch
- D and D′ will be required for design calculations

SETTING THE OUTPUT VOLTAGE

The output voltage is set using the feedback pin and a resistor divider connected to the output as shown in Figure 19. The feedback pin is always at 1.259V, so the ratio of the feedback resistors sets the output voltage.

$$R_{FB1} = R_{FB2} \times \frac{V_{OUT} - 1.259}{1.259} \ \Omega \tag{2}$$

INTRODUCTION TO COMPENSATION

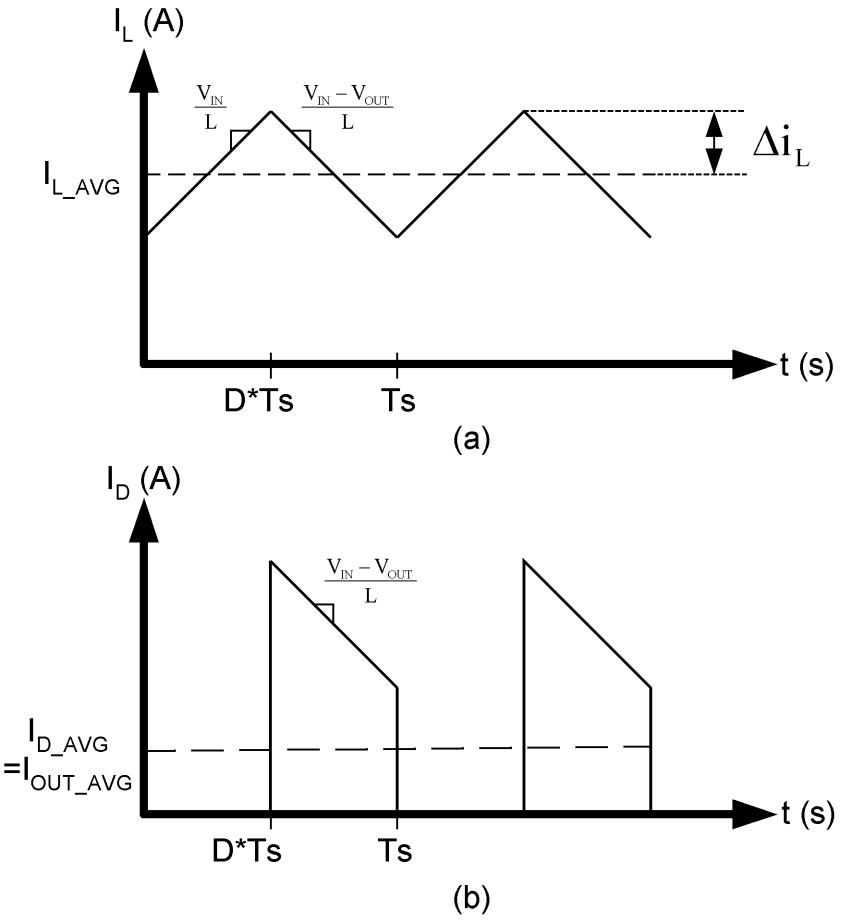


Figure 22. (a) Inductor current. (b) Diode current.

The LM5000 is a current mode PWM regulator. The signal flow of this control scheme has two feedback loops, one that senses switch current and one that senses output voltage.

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To keep a current programmed control converter stable above duty cycles of 50%, the inductor must meet certain criteria. The inductor, along with input and output voltage, will determine the slope of the current through the inductor (see Figure 22 (a)). If the slope of the inductor current is too great, the circuit will be unstable above duty cycles of 50%.

The LM5000 provides a compensation pin (COMP) to customize the voltage loop feedback. It is recommended that a series combination of R_C and C_C be used for the compensation network, as shown in Figure 19. The series combination of R_C and C_C introduces pole-zero pair according to the following equations:

$$f_{ZC} = \frac{1}{2\pi R_C C_C} \text{ Hz}$$

$$f_{PC} = \frac{1}{2\pi (R_C + R_O) C_C} \text{ Hz} \quad (3)$$

where

- R_O is the output impedance of the error amplifier, 850kΩ (4)

For most applications, performance can be optimized by choosing values within the range 5kΩ ≤ R_C ≤ 20kΩ and 680pF ≤ C_C ≤ 4.7nF.

COMPENSATION

This section will present a general design procedure to help insure a stable and operational circuit. The designs in this datasheet are optimized for particular requirements. If different conversions are required, some of the components may need to be changed to ensure stability. Below is a set of general guidelines in designing a stable circuit for continuous conduction operation (loads greater than 100mA), in most all cases this will provide for stability during discontinuous operation as well. The power components and their effects will be determined first, then the compensation components will be chosen to produce stability.

INDUCTOR SELECTION

To ensure stability at duty cycles above 50%, the inductor must have some minimum value determined by the minimum input voltage and the maximum output voltage. This equation is:

$$L > \frac{V_{IN} R_{DSON}}{0.144\ fs} \left[\frac{\left(\frac{D}{D'}\right)^2 - 1}{\left(\frac{D}{D'}\right) + 1} \right] \text{ (in H)}$$

where

- fs is the switching frequency
- D is the duty cycle
- R_{DSON} is the ON resistance of the internal switch (5)

This equation is only good for duty cycles greater than 50% (D>0.5).

$$\Delta i_L = \frac{V_{IN} D}{2Lfs} \text{ (in Amps)} \quad (6)$$

The inductor ripple current is important for a few reasons. One reason is because the peak switch current will be the average inductor current (input current) plus Δi_L. Care must be taken to make sure that the switch will not reach its current limit during normal operation. The inductor must also be sized accordingly. It should have a saturation current rating higher than the peak inductor current expected. The output voltage ripple is also affected by the total ripple current.

DC GAIN AND OPEN-LOOP GAIN

Since the control stage of the converter forms a complete feedback loop with the power components, it forms a closed-loop system that must be stabilized to avoid positive feedback and instability. A value for open-loop DC gain will be required, from which you can calculate, or place, poles and zeros to determine the crossover frequency and the phase margin. A high phase margin (greater than 45°) is desired for the best stability and transient response. For the purpose of stabilizing the LM5000, choosing a crossover point well below where the right half plane zero is located will ensure sufficient phase margin. A discussion of the right half plane zero and checking the crossover using the DC gain will follow.

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OUTPUT CAPACITOR SELECTION

The choice of output capacitors is somewhat more arbitrary. It is recommended that low ESR (Equivalent Series Resistance, denoted R_{ESR}) capacitors be used such as ceramic, polymer electrolytic, or low ESR tantalum. Higher ESR capacitors may be used but will require more compensation which will be explained later on in the section. The ESR is also important because it determines the output voltage ripple according to the approximate equation:

$$\Delta V_{OUT} \cong 2\Delta i_L R_{ESR} \text{ (in Volts)} \tag{7}$$

After choosing the output capacitor you can determine a pole-zero pair introduced into the control loop by the following equations:

$$f_{P1} = \frac{1}{2\pi(R_{ESR} + R_L)C_{OUT}} \text{ (in Hz)}$$
$$f_{Z1} = \frac{1}{2\pi R_{ESR} C_{OUT}} \text{ (in Hz)} \tag{8}$$

where

- R_L is the minimum load resistance corresponding to the maximum load current (9)

The zero created by the ESR of the output capacitor is generally very high frequency if the ESR is small. If low ESR capacitors are used it can be neglected. If higher ESR capacitors are used see the HIGH OUTPUT CAPACITOR ESR COMPENSATION section.

RIGHT HALF PLANE ZERO

A current mode control boost regulator has an inherent right half plane zero (RHP zero). This zero has the effect of a zero in the gain plot, causing an imposed +20dB/decade on the rolloff, but has the effect of a pole in the phase, subtracting another 90° in the phase plot. This can cause undesirable effects if the control loop is influenced by this zero. To ensure the RHP zero does not cause instability issues, the control loop should be designed to have a bandwidth of ½ the frequency of the RHP zero or less. This zero occurs at a frequency of:

$$\text{RHPzero} = \frac{V_{OUT}(D')^2}{2\pi I_{LOAD} L} \text{ (in Hz)}$$

where

- I_{LOAD} is the maximum load current (10)

SELECTING THE COMPENSATION COMPONENTS

The first step in selecting the compensation components R_C and C_C is to set a dominant low frequency pole in the control loop. Simply choose values for R_C and C_C within the ranges given in the INTRODUCTION TO COMPENSATION section to set this pole in the area of 10Hz to 100Hz. The frequency of the pole created is determined by the equation:

$$f_{PC} = \frac{1}{2\pi(R_C + R_O)C_C} \text{ (in Hz)}$$

where

- R_O is the output impedance of the error amplifier, 850kΩ (11)

Since R_C is generally much less than R_O, it does not have much effect on the above equation and can be neglected until a value is chosen to set the zero f_{ZC}. f_{ZC} is created to cancel out the pole created by the output capacitor, f_{P1}. The output capacitor pole will shift with different load currents as shown by the equation, so setting the zero is not exact. Determine the range of f_{P1} over the expected loads and then set the zero f_{ZC} to a point approximately in the middle. The frequency of this zero is determined by:

$$f_{ZC} = \frac{1}{2\pi C_C R_C} \text{ (in Hz)} \tag{12}$$

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Now R_C can be chosen with the selected value for C_C. Check to make sure that the pole f_{PC} is still in the 10Hz to 100Hz range, change each value slightly if needed to ensure both component values are in the recommended range. After checking the design at the end of this section, these values can be changed a little more to optimize performance if desired. This is best done in the lab on a bench, checking the load step response with different values until the ringing and overshoot on the output voltage at the edge of the load steps is minimal. This should produce a stable, high performance circuit. For improved transient response, higher values of R_C (within the range of values) should be chosen. This will improve the overall bandwidth which makes the regulator respond more quickly to transients. If more detail is required, or the most optimal performance is desired, refer to a more in depth discussion of compensating current mode DC/DC switching regulators.

HIGH OUTPUT CAPACITOR ESR COMPENSATION

When using an output capacitor with a high ESR value, or just to improve the overall phase margin of the control loop, another pole may be introduced to cancel the zero created by the ESR. This is accomplished by adding another capacitor, C_{C2}, directly from the compensation pin V_C to ground, in parallel with the series combination of R_C and C_C. The pole should be placed at the same frequency as f_{Z1}, the ESR zero. The equation for this pole follows:

$$f_{PC2} = \frac{1}{2\pi C_{C2}(R_C // R_O)} \text{ (in Hz)} \tag{13}$$

To ensure this equation is valid, and that C_{C2} can be used without negatively impacting the effects of R_C and C_C, f_{PC2} must be greater than $10f_{PC}$.

CHECKING THE DESIGN

The final step is to check the design. This is to ensure a bandwidth of ½ or less of the frequency of the RHP zero. This is done by calculating the open-loop DC gain, A_{DC}. After this value is known, you can calculate the crossover visually by placing a −20dB/decade slope at each pole, and a +20dB/decade slope for each zero. The point at which the gain plot crosses unity gain, or 0dB, is the crossover frequency. If the crossover frequency is at less than ½ the RHP zero, the phase margin should be high enough for stability. The phase margin can also be improved some by adding C_{C2} as discussed earlier in the section. The equation for A_{DC} is given below with additional equations required for the calculation:

$$A_{DC(DB)} = 20\log_{10}\left\langle \left(\frac{R_{FB2}}{R_{FB1} + R_{FB2}} \right) \frac{g_m R_O D'}{R_{DSON}} \{[(\omega c \text{Leff}) // R_L] // R_L\} \right\rangle \text{ (in dB)} \tag{14}$$

$$\omega c \cong \frac{2fs}{nD'} \text{ (in rad/s)} \tag{15}$$

$$\text{Leff} = \frac{L}{(D')^2} \tag{16}$$

$$n = 1 + \frac{2mc}{m1} \text{ (no unit)} \tag{17}$$

$$mc \cong 0.072fs \text{ (in A/s)} \tag{18}$$

$$m1 \cong \frac{V_{IN} R_{DSON}}{L} \text{ (in V/s)}$$

where

- R_L is the minimum load resistance
- V_{IN} is the maximum input voltage
- R_{DSON} is the value chosen from the graph "R_{DSON} vs. V_{IN} " in the Typical Performance Characteristics section (19)

SWITCH VOLTAGE LIMITS

In a flyback regulator, the maximum steady-state voltage appearing at the switch, when it is off, is set by the transformer turns ratio, N, the output voltage, V_{OUT}, and the maximum input voltage, V_{IN} (Max):

$$V_{SW(OFF)} = V_{IN} \text{ (Max)} + (V_{OUT} + V_F)/N$$

where

- V_F is the forward biased voltage of the output diode, and is typically 0.5V for Schottky diodes and 0.8V for ultra-fast recovery diodes (20)

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In certain circuits, there exists a voltage spike, V_{LL}, superimposed on top of the steady-state voltage . Usually, this voltage spike is caused by the transformer leakage inductance and/or the output rectifier recovery time. To "clamp" the voltage at the switch from exceeding its maximum value, a transient suppressor in series with a diode is inserted across the transformer primary.

If poor circuit layout techniques are used, negative voltage transients may appear on the Switch pin. Applying a negative voltage (with respect to the IC's ground) to any monolithic IC pin causes erratic and unpredictable operation of that IC. This holds true for the LM5000 IC as well. When used in a flyback regulator, the voltage at the Switch pin can go negative when the switch turns on. The "ringing" voltage at the switch pin is caused by the output diode capacitance and the transformer leakage inductance forming a resonant circuit at the secondary(ies). The resonant circuit generates the "ringing" voltage, which gets reflected back through the transformer to the switch pin. There are two common methods to avoid this problem. One is to add an RC snubber around the output rectifier(s). The values of the resistor and the capacitor must be chosen so that the voltage at the Switch pin does not drop below −0.4V. The resistor may range in value between 10Ω and 1 kΩ, and the capacitor will vary from 0.001 µF to 0.1 µF. Adding a snubber will (slightly) reduce the efficiency of the overall circuit.

The other method to reduce or eliminate the "ringing" is to insert a Schottky diode clamp between the SW pin and the PGND pin. The reverse voltage rating of the diode must be greater than the switch off voltage.

OUTPUT VOLTAGE LIMITATIONS

The maximum output voltage of a boost regulator is the maximum switch voltage minus a diode drop. In a flyback regulator, the maximum output voltage is determined by the turns ratio, N, and the duty cycle, D, by the equation:

$$V_{OUT} \approx N \times V_{IN} \times D/(1 - D) \tag{21}$$

The duty cycle of a flyback regulator is determined by the following equation:

$$D = \frac{V_{OUT} + V_F}{N(V_{IN} - V_{SAT}) + V_{OUT} + V_F} \approx \frac{V_{OUT}}{N(V_{IN}) + V_{OUT}} \tag{22}$$

Theoretically, the maximum output voltage can be as large as desired—just keep increasing the turns ratio of the transformer. However, there exists some physical limitations that prevent the turns ratio, and thus the output voltage, from increasing to infinity. The physical limitations are capacitances and inductances in the LM5000 switch, the output diode(s), and the transformer—such as reverse recovery time of the output diode (mentioned above).

INPUT LINE CONDITIONING

A small, low-pass RC filter should be used at the input pin of the LM5000 if the input voltage has an unusually large amount of transient noise. Additionally, the RC filter can reduce the dissipation within the device when the input voltage is high.

Flyback Regulator Operation

The LM5000 is ideally suited for use in the flyback regulator topology. The flyback regulator can produce a single output voltage, or multiple output voltages.

The operation of a flyback regulator is as follows: When the switch is on, current flows through the primary winding of the transformer, T1, storing energy in the magnetic field of the transformer. Note that the primary and secondary windings are out of phase, so no current flows through the secondary when current flows through the primary. When the switch turns off, the magnetic field collapses, reversing the voltage polarity of the primary and secondary windings. Now rectifier D5 is forward biased and current flows through it, releasing the energy stored in the transformer. This produces voltage at the output.

The output voltage is controlled by modulating the peak switch current. This is done by feeding back a portion of the output voltage to the error amp, which amplifies the difference between the feedback voltage and a 1.259V reference. The error amp output voltage is compared to a ramp voltage proportional to the switch current (i.e., inductor current during the switch on time). The comparator terminates the switch on time when the two voltages are equal, thereby controlling the peak switch current to maintain a constant output voltage.

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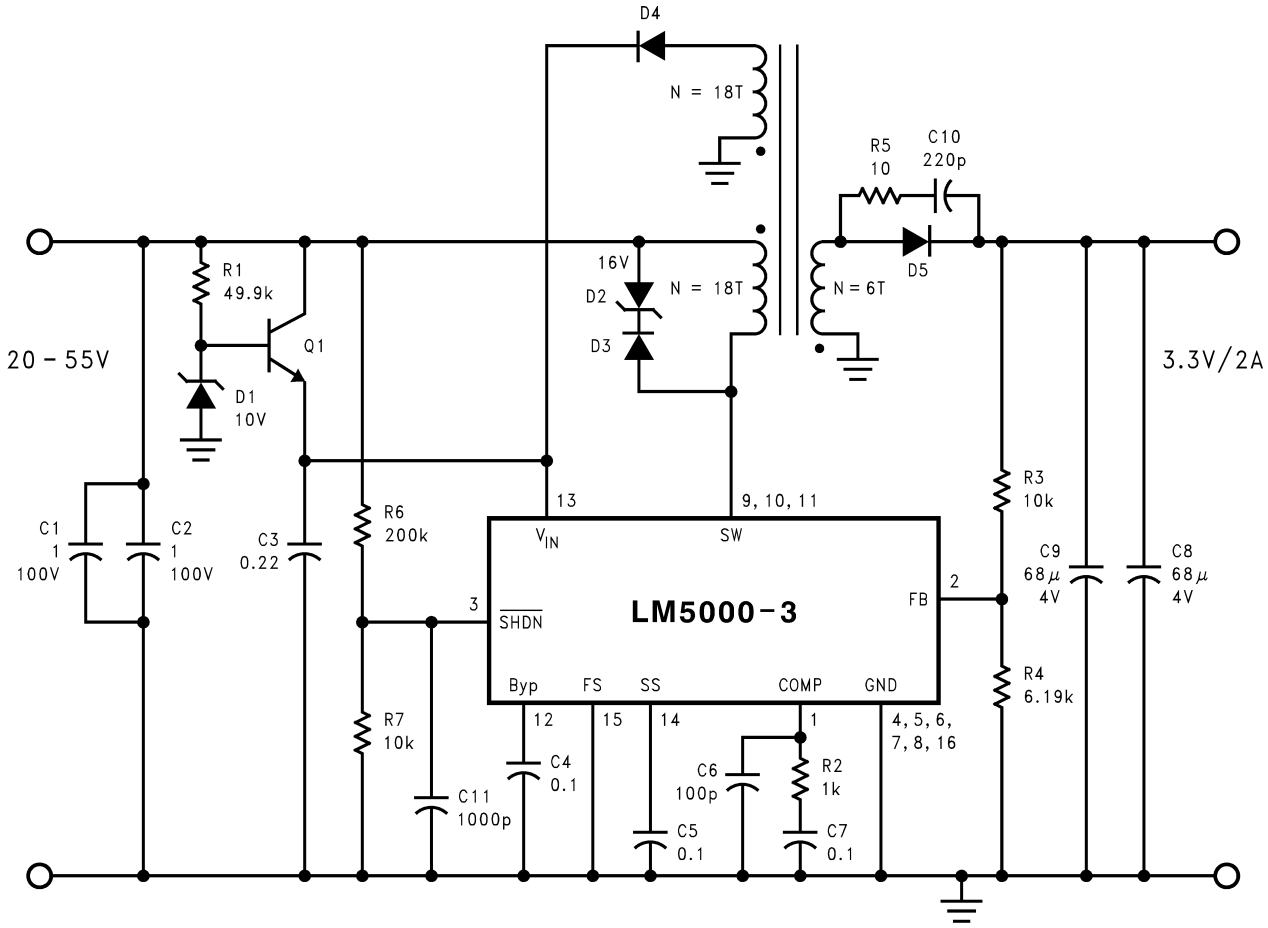


Figure 23. LM5000 Flyback Converter

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ITEM		PART NUMBER	DESCRIPTION	VALUE
C	1	C4532X7R2A105MT	Capacitor, CER, TDK	1µ, 100V
C	2	C4532X7R2A105MT	Capacitor, CER, TDK	1µ, 100V
C	3	C1206C224K5RAC	Capacitor, CER, KEMET	0.22µ, 50V
C	4	C1206C104K5RAC	Capacitor, CER, KEMET	0.1µ, 50V
C	5	C1206C104K5RAC	Capacitor, CER, KEMET	0.1µ, 50V
C	6	C1206C101K1GAC	Capacitor, CER, KEMET	100p, 100V
C	7	C1206C104K5RAC	Capacitor, CER, KEMET	0.1µ, 50V
C	8	C4532X7S0G686M	Capacitor, CER, TDK	68µ, 4V
C	9	C4532X7S0G686M	Capacitor, CER, TDK	68µ, 4V
C	10	C1206C221K1GAC	Capacitor, CER, KEMET	220p, 100V
C	11	C1206C102K5RAC	Capacitor, CER, KEMET	1000p, 500V
D	1	BZX84C10-NSA	Central, 10V Zener, SOT-23	
D	2	CMZ5930B-NSA	Central, 16V Zener, SMA	
D	3	CMPD914-NSA	Central, Switching, SOT-23	
D	4	CMPD914-NSA	Central, Switching, SOT-23	
D	5	CMSH3-40L-NSA	Central, Schottky, SMC	
T	1	A0009-A	Coilcraft, Transformer	
R	1	CRCW12064992F	Resistor	49.9K
R	2	CRCW12061001F	Resistor	1K
R	3	CRCW12061002F	Resistor	10K
R	4	CRCW12066191F	Resistor	6.19K
R	5	CRCW120610R0F	Resistor	10
R	6	CRCW12062003F	Resistor	200K
R	7	CRCW12061002F	Resistor	10K
Q	1	CXT5551-NSA	Central, NPN, 180V	
U	1	LM5000-3	Regulator, TI	

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PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
LM5000-3MTC	NRND	TSSOP	PW	16	92	TBD	Call TI	Call TI	-40 to 125	LM5000 3MTC	
LM5000-3MTC/NOPB	ACTIVE	TSSOP	PW	16	92	Green (RoHS & no Sb/Br)	SN	Level-1-260C-UNLIM	-40 to 125	LM5000 3MTC	Samples
LM5000-3MTCX	NRND	TSSOP	PW	16	2500	TBD	Call TI	Call TI	-40 to 125	LM5000 3MTC	
LM5000-3MTCX/NOPB	ACTIVE	TSSOP	PW	16	2500	Green (RoHS & no Sb/Br)	SN	Level-1-260C-UNLIM	-40 to 125	LM5000 3MTC	Samples
LM5000SD-3/NOPB	ACTIVE	WSON	NHQ	16	1000	Green (RoHS & no Sb/Br)	SN	Level-1-260C-UNLIM	-40 to 125	5000-3	Samples
LM5000SD-6/NOPB	ACTIVE	WSON	NHQ	16	1000	Green (RoHS & no Sb/Br)	SN	Level-1-260C-UNLIM	-40 to 125	5000-6	Samples
LM5000SDX-3/NOPB	ACTIVE	WSON	NHQ	16	4500	Green (RoHS & no Sb/Br)	SN	Level-1-260C-UNLIM	-40 to 125	5000-3	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

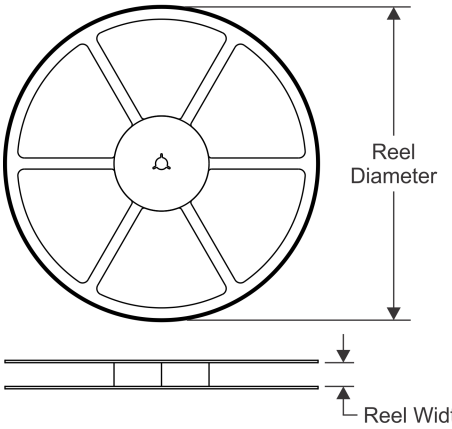
(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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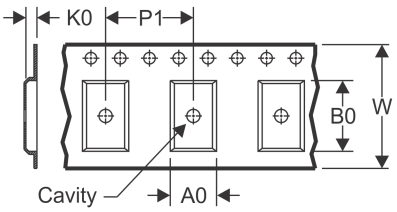
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TAPE AND REEL INFORMATION

REEL DIMENSIONS

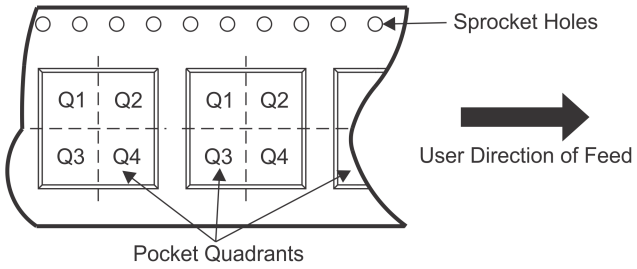


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

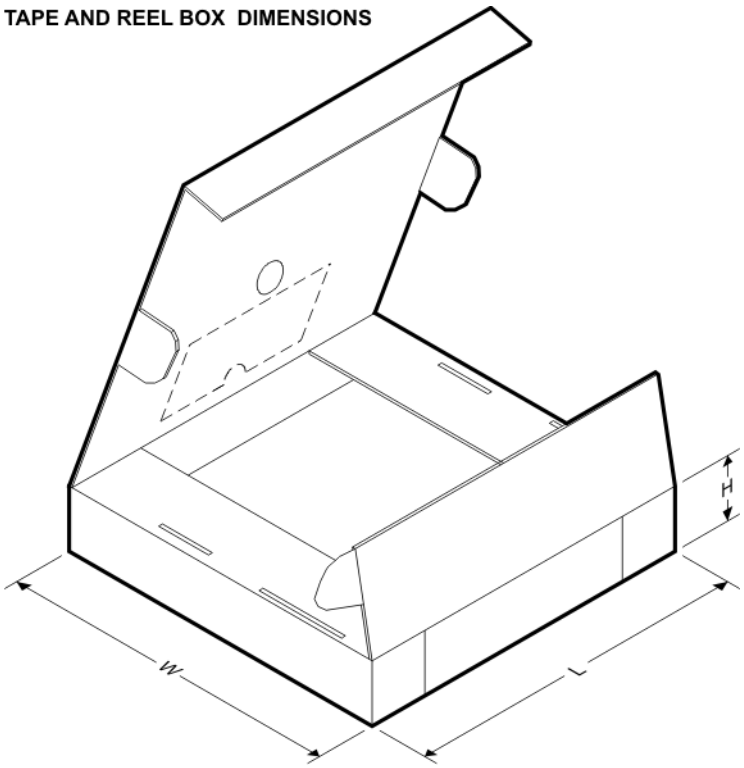
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
LM5000-3MTCX	TSSOP	PW	16	2500	330.0	12.4	6.95	5.6	1.6	8.0	12.0	Q1
LM5000-3MTCX/NOPB	TSSOP	PW	16	2500	330.0	12.4	6.95	5.6	1.6	8.0	12.0	Q1
LM5000SD-3/NOPB	WSON	NHQ	16	1000	178.0	12.4	5.3	5.3	1.3	8.0	12.0	Q1
LM5000SD-6/NOPB	WSON	NHQ	16	1000	178.0	12.4	5.3	5.3	1.3	8.0	12.0	Q1
LM5000SDX-3/NOPB	WSON	NHQ	16	4500	330.0	12.4	5.3	5.3	1.3	8.0	12.0	Q1

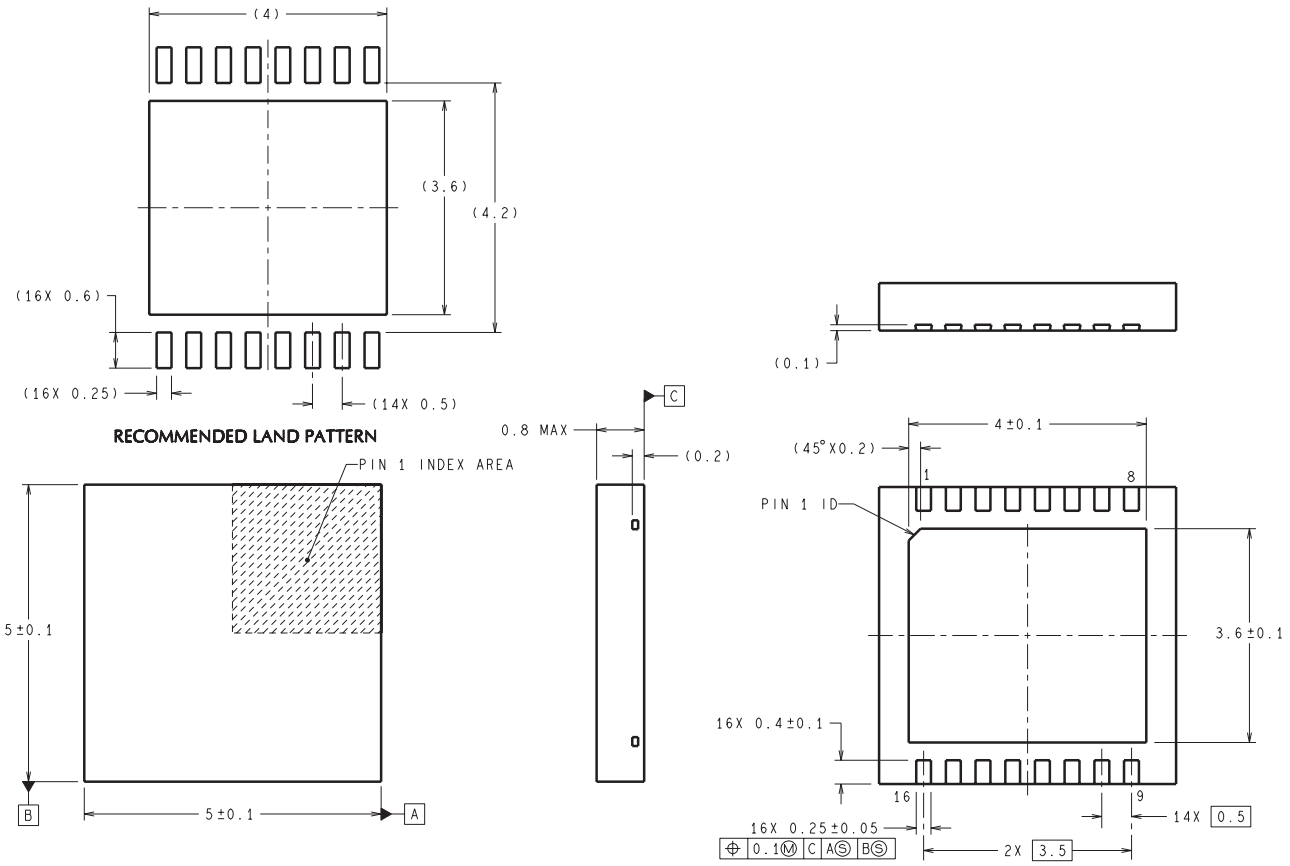
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
LM5000-3MTCX	TSSOP	PW	16	2500	367.0	367.0	35.0
LM5000-3MTCX/NOPB	TSSOP	PW	16	2500	367.0	367.0	35.0
LM5000SD-3/NOPB	WSON	NHQ	16	1000	210.0	185.0	35.0
LM5000SD-6/NOPB	WSON	NHQ	16	1000	210.0	185.0	35.0
LM5000SDX-3/NOPB	WSON	NHQ	16	4500	367.0	367.0	35.0

NHQ0016A



DIMENSIONS ARE IN MILLIMETERS

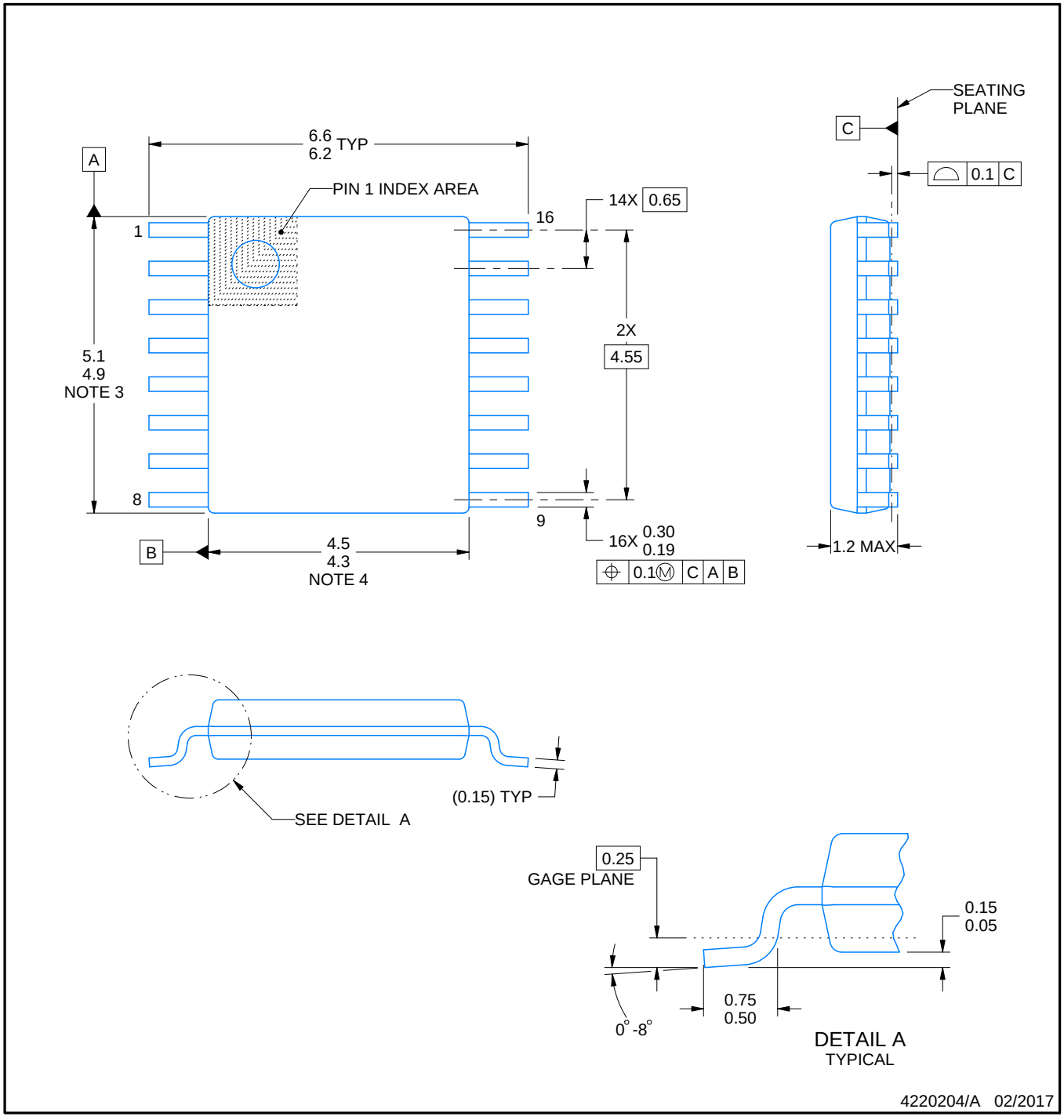
SDA16A (Rev A)

PACKAGE OUTLINE

PW0016A

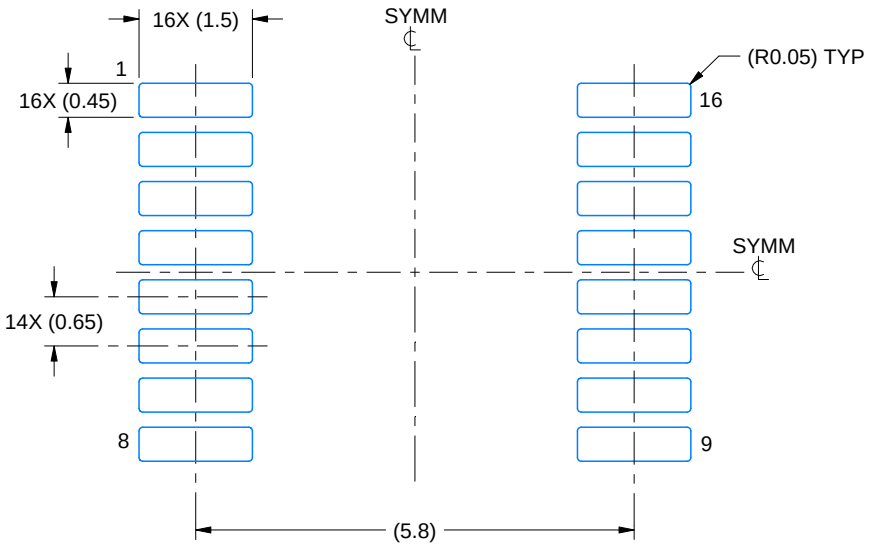
TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE

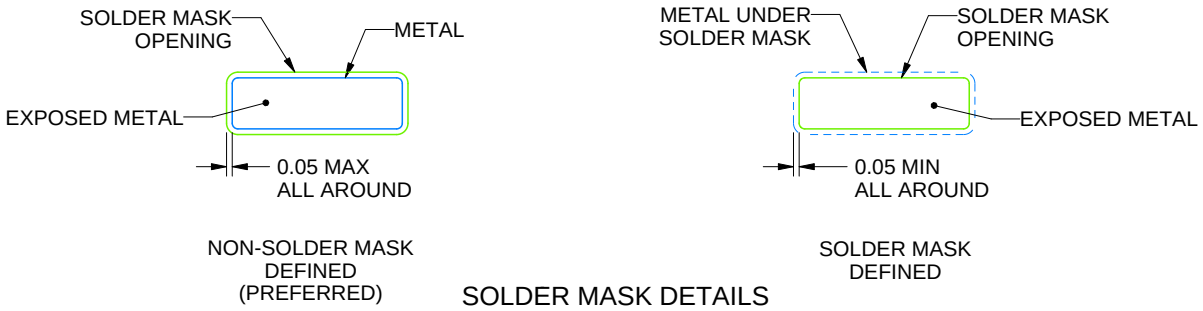


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X

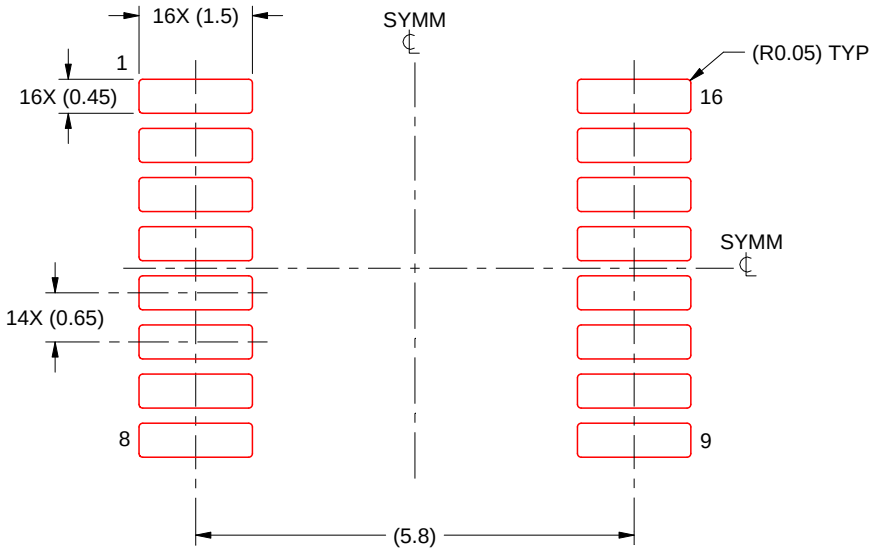


SOLDER MASK DETAILS

4220204/A 02/2017

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 10X

4220204/A 02/2017

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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