# LM48413 Boomer™ Audio Power Amplifier Series Ultra Low EMI, Filterless, 1.2W Stereo Class D Audio Power Amplifier with E²S and Texas Instruments 3D Enhancement

**Check for Samples: LM48413**

## FEATURES

- **E²S System Reduces EMI Preserving Audio Quality and Efficiency**
- **Output Short Circuit Protection**
- **Stereo Class D Operation**
- **No Output Filter Required**
- **Texas Instruments 3D Enhancement**
- **Minimum External Components**
- **Click and Pop Suppression**
- **Micro-Power Shutdown**
- **Available in Space-Saving Approximately 2mm x 2.2mm DSBGA Package**

## APPLICATIONS

- **Mobile Phones**
- **PDAs**
- **Laptops**

## KEY SPECIFICATIONS

- **Quiescent Power Supply Current at 3.6V Supply 4mA (Typ)**
- **Power Output at $V_{DD}$ = 5V, $R_L$ = 8Ω, THD ≤ 1% 1.2 W (Typ)**
- **Shutdown Current 0.03µA (Typ)**
- **Efficiency at 3.6V, 100mW into 8Ω 80% (Typ)**
- **Efficiency at 3.6V, 500mW into 8Ω 80% (Typ)**
- **Efficiency at 5V, 1W into 8Ω 86% (Typ)**

## DESCRIPTION

The LM48413 is a single supply, high efficiency, 1.2W/channel, filterless switching audio amplifier. The LM48413 features Texas Instruments' Enhanced Emissions Suppression (E²S) system - a unique patented ultra low EMI, spread spectrum, PWM architecture. It significantly reduces RF emission while preserving audio quality and efficiency. The E²S system improves battery life, reduces external component count, board area consumption, system cost and product design cycle time. The LM48413TL is available in a micro-SMD package, further saving space.

The LM48413 is designed to meet the demands of mobile phones and other portable communication devices. Operating from a single 5V supply, the device is capable of delivering 1.2W/channel of continuous output power to a 8Ω load with less than 1% THD+N. Flexible power supply requirements allow operation from 2.4V to 5.5V. The wide band spread spectrum architecture of the LM48413 reduces EMI-radiated emissions due to the modulator frequency.

The LM48413 features high efficiency compared with conventional Class AB amplifiers. The E²S system includes an advanced, patent-pending edge rate control (ERC) architecture that further reduce emissions by minimizing the high frequency components of the device output, while maintaining its high quality audio reproduction and high efficiency ($\eta$ = 85% at $V_{DD}$ = 3.6V, $P_O$ = 500mW). The LM48413 also includes Texas Instruments' 3D audio enhancement that improves stereo sound quality. In devices where the left and right speakers are in close proximity, 3D enhancement affects channel specialization, widening the perceived soundstage.

Output short circuit protection prevents the device from being damaged during fault conditions. Superior click and pop suppression eliminates audible transients on power up/down and during shutdown. Shutdown control also provided to maximizes power savings.

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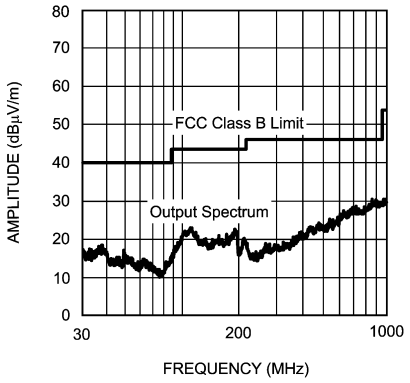
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## EMI Plot Using 6 inch Speaker Cables

**Figure 1. EMI Radiation vs Frequency**
**$V_{DD}$ = 3V, $R_L$ = 15µH + 8Ω + 15µH**




## Typical Application

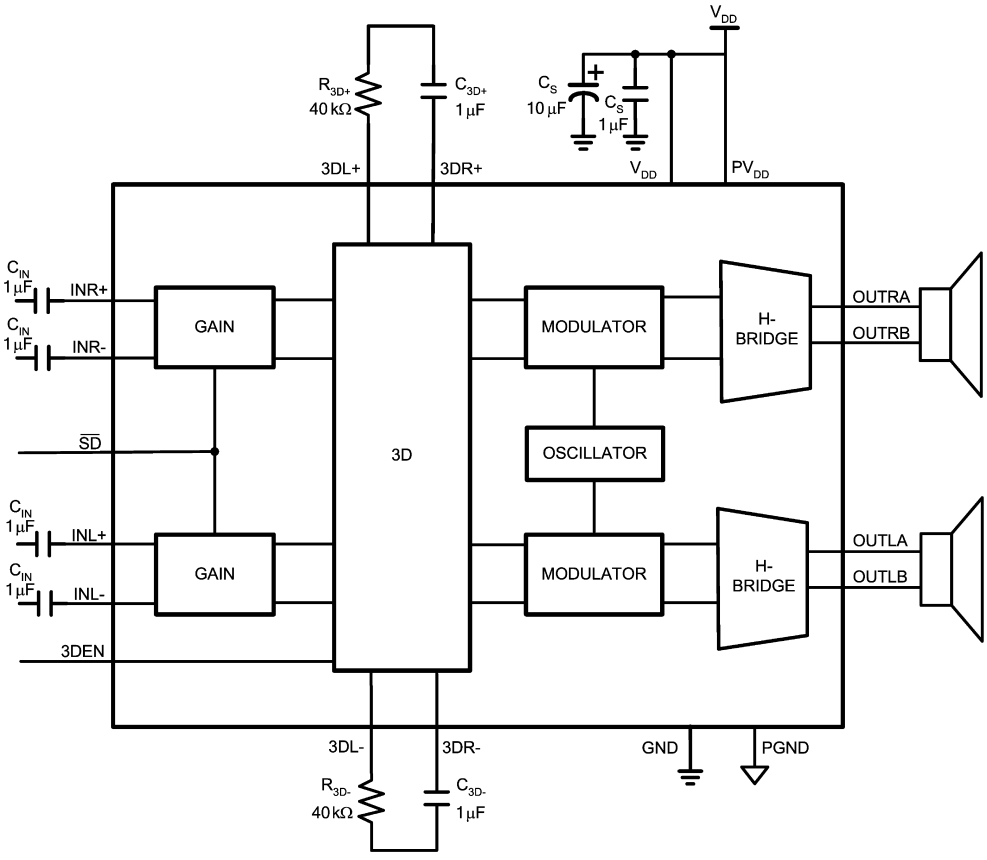



**Figure 2. Typical Audio Amplifier Application Circuit**


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## Connection Diagram

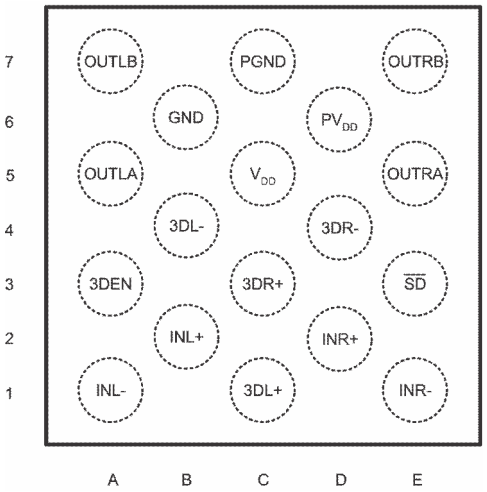



**Figure 3. 18 bump DSBGA package**
**Top View**
**See Package Number YZR0018**

### BUMP DESCRIPTIONS

| Bump | Name | Description |
|---|---|---|
| A1 | INL- | Left Channel Inverting Input |
| A3 | 3DEN | 3D Enable Input |
| A5 | OUTLA | Left Channel Non-Inverting Output |
| A7 | OUTLB | Left Channel Inverting Output |
| B2 | INL+ | Left Channel Non-Inverting Input |
| B4 | 3DL- | Left Channel inverting 3D connection. Connect to 3DR- through $C_{3D-}$ and $R_{3D-}$ |
| B6 | GND | Ground |
| C1 | 3DL+ | Left Channel non-inverting 3D connection. Connect to 3DR+ through $C_{3D+}$ and $R_{3D+}$ |
| C3 | 3DR+ | Right Channel non-inverting 3D connection. Connect to 3DL+ through $C_{3D+}$ and $R_{3D+}$ |
| C5 | $V_{DD}$ | Power Supply. Connect to $PV_{DD}$ supplying same voltage. |
| C7 | PGND | Power Ground |
| D2 | INR+ | Right Channel Non-inverting Input |
| D4 | 3DR- | Right Channel inverting 3D connection. Connect to 3DL- through $C_{3D-}$ and $R_{3D-}$ |
| D6 | $PV_{DD}$ | Amplifier Power Supply |
| E1 | INR- | Right Channel Inverting Input |
| E3 | $\overline{SD}$ | Connect to GND for disabling the device. Connect to $V_{DD}$ for normal operation. |
| E5 | OUTRA | Right Channel Non-inverting Output |
| E7 | OUTRB | Right Channel Inverting Output |

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

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## Absolute Maximum Ratings(1)(2)(3)

| | | |
|---|---|---|
| Supply Voltage(1) | | 6.0V |
| Storage Temperature | | −65°C to +150°C |
| Input Voltage | | –0.3V to $V_{DD}$ + 0.3V |
| Power Dissipation(4) | | Internally Limited |
| ESD Rating(5) | | 2000V |
| ESD Rating(6) | | 200V |
| Junction Temperature | | 150°C |
| Thermal Resistance | $\theta_{JA}$ | 47°C/W |

(1) *"Absolute Maximum Ratings"* indicate limits beyond which damage to the device may occur, including inoperability and degradation of device reliability and/or performance. Functional operation of the device and/or non-degradation at the *Absolute Maximum Ratings* or other conditions beyond those indicated in the *Recommended Operating Conditions* is not implied. The *Recommended Operating Conditions*indicate conditions at which the device is functional and the device should not be operated beyond such conditions. All voltages are measured with respect to the ground pin, unless otherwise specified.
(2) The *Electrical Characteristics* tables list ensured specifications under the listed *Recommended Operating Conditions* except as otherwise modified or specified by the *Electrical Characteristics Conditions* and/or Notes. Typical specifications are estimations only and are not ensured.
(3) If Military/Aerospace specified devices are required, please contact the Texas Instruments Sales Office/Distributors for availability and specifications.
(4) The maximum power dissipation must be derated at elevated temperatures and is dictated by $T_{JMAX}$, $\theta_{JA}$, and the ambient temperature, $T_A$. The maximum allowable power dissipation is $P_{DMAX} = (T_{JMAX} - T_A) / \theta_{JA}$ or the number given in *Absolute Maximum Ratings*, whichever is lower.
(5) Human body model, applicable std. JESD22-A114C.
(6) Machine model, applicable std. JESD22-A115-A. The ESD Machine Model rating of device bump E3 = 150V.

## Operating Ratings(1)(2)

| | | |
|---|---|---|
| Temperature Range | $T_{MIN} \le T_A \le T_{MAX}$ | −40°C ≤ $T_A$ ≤ 85°C |
| | Supply Voltage ($V_{DD}$, $PV_{DD}$) | 2.4V ≤ $V_{DD}$ ≤ 5.5V |

(1) *"Absolute Maximum Ratings"* indicate limits beyond which damage to the device may occur, including inoperability and degradation of device reliability and/or performance. Functional operation of the device and/or non-degradation at the *Absolute Maximum Ratings* or other conditions beyond those indicated in the *Recommended Operating Conditions* is not implied. The *Recommended Operating Conditions*indicate conditions at which the device is functional and the device should not be operated beyond such conditions. All voltages are measured with respect to the ground pin, unless otherwise specified.
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## Electrical Characteristics $V_{DD}$ = $PV_{DD}$ = 3.6V[1][2]

The following specifications apply for $R_L$ = 8Ω[3], f = 1kHz, unless otherwise specified. Limits apply for $T_A$ = 25°C.

| Symbol | Parameter | Conditions | LM48413 | | Units (Limits) |
|---|---|---|---|---|---|
| | | | Typical [4] | Limit [5] | |
| $V_{OS}$ | Differential Output Offset Voltage | $V_{IN}$ = 0, $V_{DD}$ = 2.4V to 5.0V | 3 | | mV |
| $I_{DD}$ | Quiescent Power Supply Current | $V_{IN}$ = 0, No Load, $V_{SD}$ = $V_{DD}$,<br>$V_{DD}$ = 3.6V<br>$V_{DD}$ = 5V | <br>4.3<br>5.2 | <br>5.5<br>7 | <br>mA (max)<br>mA (max) |
| $I_{SD}$ | Shutdown Current | $V_{SD}$ = GND | 0.03 | 1 | µA (max) |
| $V_{IH}$ | Logic Input High Voltage | | | 1.4 | V (min) |
| $V_{IL}$ | Logic Input Low Voltage | | | 0.4 | V (max) |
| $T_{WU}$ | Wake-Up Time | | 4 | | ms |
| $A_V$ | Gain | | 24 | 23.5<br>24.5 | dB (min)<br>dB (max) |
| $R_{IN}$ | Input Resistance | | 20 | | kΩ |
| $P_O$ | Output Power (Per Channel) | THD ≤ 10%, f = 1kHz, 22kHz BW | | | |
| | | $V_{DD}$ = 5V | 1.5 | | W |
| | | $V_{DD}$ = 3.6V | 720 | 600 | mW (min) |
| | | $V_{DD}$ = 2.5V | 320 | | mW |
| | | THD ≤ 1%, f = 1kHz, 22kHz BW | | | |
| | | $V_{DD}$ = 5V | 1.2 | | W |
| | | $V_{DD}$ = 3.6V | 600 | | mW |
| | | $V_{DD}$ = 2.5V | 260 | | mW |
| THD+N | Total Harmonic Distortion + Noise | $P_O$ = 500mW/Ch, f = 1kHz, 22kHz BW | 0.03 | | % |
| | | $P_O$ = 300mW/Ch, f = 1kHz, 22kHz BW | 0.03 | | % |
| PSRR | Power Supply Rejection Ratio | $V_{RIPPLE}$ = 200m$V_{P-P}$ Sine, Inputs AC GND, $C_{IN}$ = 1µF, input referred<br>$f_{RIPPLE}$ = 217Hz<br>$f_{RIPPLE}$ = 1kHz | <br>91<br>90 | | <br>dB<br>dB |
| CMRR | Common Mode Rejection Ratio | $V_{RIPPLE}$ = 1$V_{P-P}$<br>$f_{RIPPLE}$ = 217Hz | 72 | | dB |
| η | Efficiency | $P_O$ = 1W/Ch, f = 1kHz, $R_L$ = 8Ω, $V_{DD}$ = 5V | 86 | | % |
| $X_{TALK}$ | Crosstalk | $P_O$ = 500mW/Ch, f = 1kHz | 93 | | dB |
| SNR | Signal-to-Noise Ratio | $V_{DD}$ = 5V, $P_O$ = 1W | 88 | | dB |
| $\varepsilon_{OS}$ | Output Noise | Input referred, A-Weighted | 5 | | µV |

(1) *"Absolute Maximum Ratings"* indicate limits beyond which damage to the device may occur, including inoperability and degradation of device reliability and/or performance. Functional operation of the device and/or non-degradation at the *Absolute Maximum Ratings* or other conditions beyond those indicated in the *Recommended Operating Conditions* is not implied. The *Recommended Operating Conditions*indicate conditions at which the device is functional and the device should not be operated beyond such conditions. All voltages are measured with respect to the ground pin, unless otherwise specified.

(2) The *Electrical Characteristics* tables list ensured specifications under the listed *Recommended Operating Conditions* except as otherwise modified or specified by the *Electrical Characteristics Conditions* and/or Notes. Typical specifications are estimations only and are not ensured.

(3) $R_L$ is a resistive load in series with two inductors to simulate an actual speaker load. For $R_L$ = 8Ω, the load is 15µH + 8Ω +15µH.

(4) Typical values represent most likely parametric norms at $T_A$ = +25°C, and at the *Recommended Operation Conditions* at the time of product characterization and are not ensured.

(5) Datasheet min/max specification limits are ensured by test or statistical analysis.

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## Typical Performance Characteristics

THD+N vs Output Power/Channel
f = 1kHz, $R_L$ = 8Ω, 22kHz BW

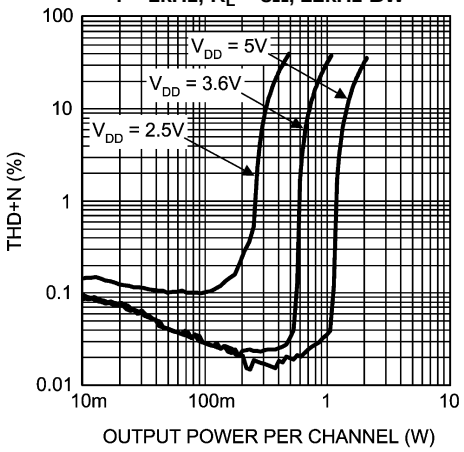



**Figure 4.**

THD+N vs Frequency
$V_{DD}$ = 2.5V, $P_{OUT}$ = 100mW/Ch
$R_L$ = 8Ω, 22kHz BW

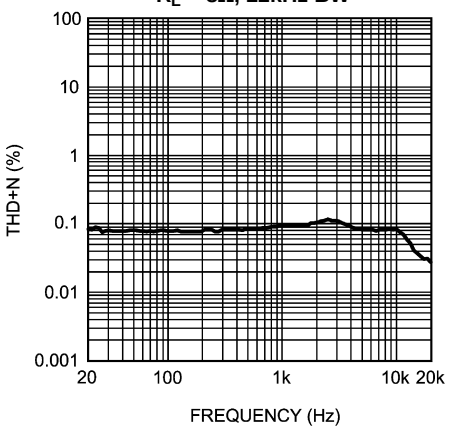



**Figure 5.**

THD+N vs Frequency
$V_{DD}$ = 3.6V, $P_{OUT}$ = 250mW/Ch
$R_L$ = 8Ω, 22kHz BW

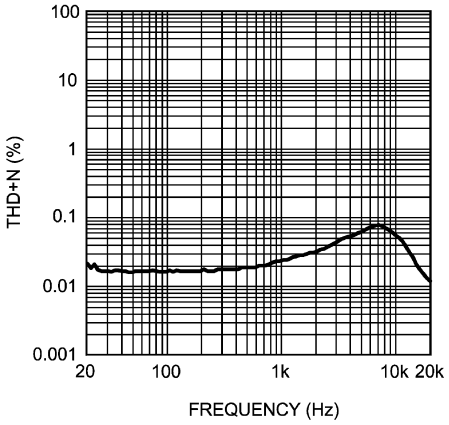



**Figure 6.**

THD+N vs Frequency
$V_{DD}$ = 5V, $P_{OUT}$ = 375mW/Ch
$R_L$ = 8Ω, 22kHz BW

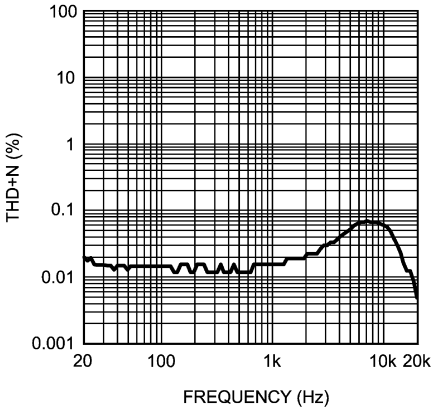



**Figure 7.**

Efficiency vs Output Power
$R_L$ = 8Ω, f = 1kHz

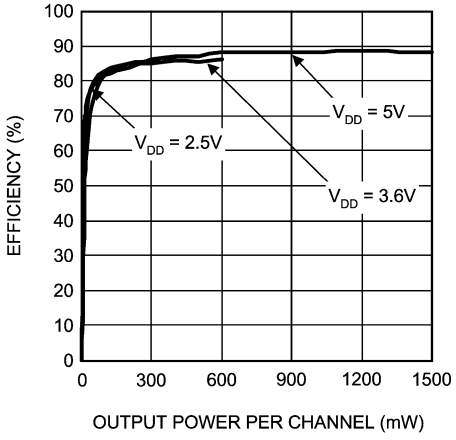



**Figure 8.**

Power Dissipation vs Total Output Power
$R_L$ = 8Ω, f = 1kHz

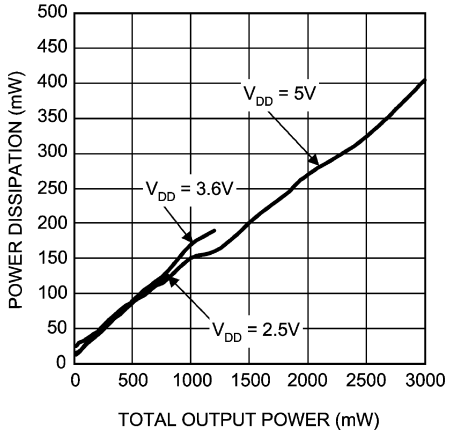



**Figure 9.**


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## Typical Performance Characteristics (continued)

**Output Power/Channel vs Supply Voltage**
**$R_L$ = 8Ω, f = 1kHz, 22kHz BW**

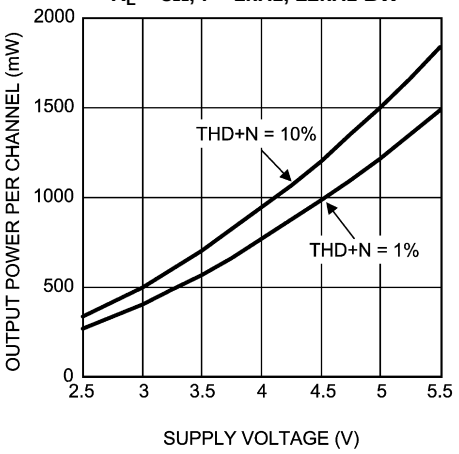



**Figure 10.**

**PSRR and CMRR vs Frequency**
**$V_{DD}$ = 3.6V, $R_L$ = 8Ω**

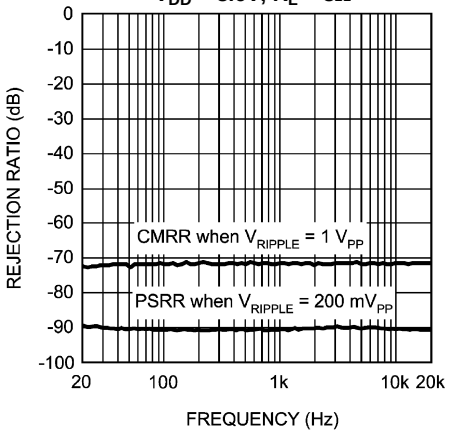



**Figure 11.**

**Crosstalk vs Frequency**
**$V_{DD}$ = 3.6V, $P_O$ = 500mW, $R_L$ = 8Ω**

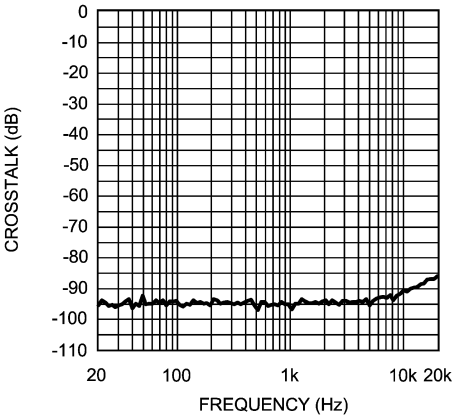



**Figure 12.**

**Supply Current vs Supply Voltage**
**No Load**

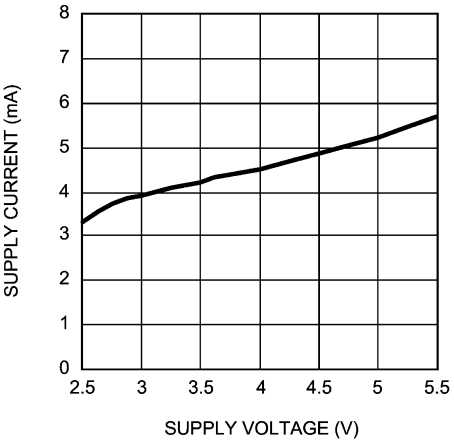



**Figure 13.**

**EMI Radiation vs Frequency**
**$V_{DD}$ = 3V, $R_L$ = 8Ω, 3 inch cables**

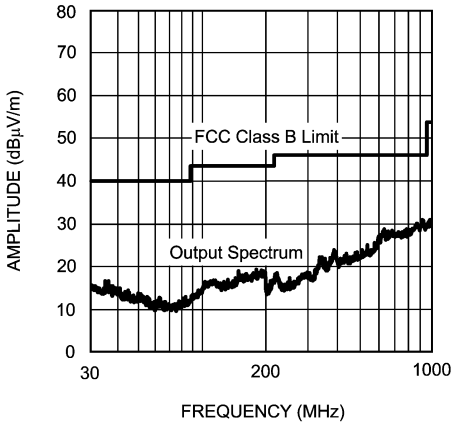



**Figure 14.**

**EMI Radiation vs Frequency**
**$V_{DD}$ = 3V, $R_L$ = 8Ω, 6 inch cables**

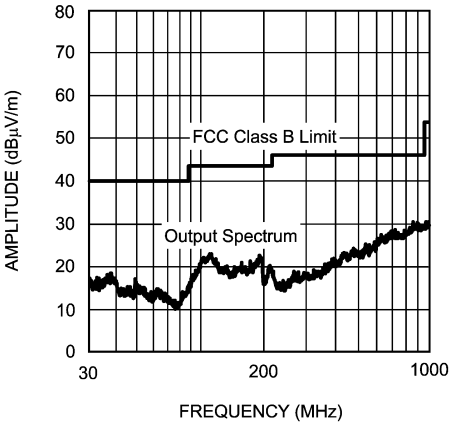



**Figure 15.**

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## Typical Performance Characteristics (continued)

**EMI Radiation vs Frequency**
**$V_{DD}$ = 3V, $R_L$ = 8Ω, 12 inch cables**

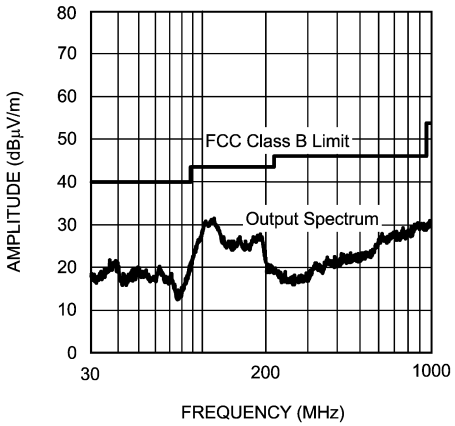



**Figure 16.**


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# APPLICATION INFORMATION

## GENERAL AMPLIFIER FUNCTION

The LM48413 stereo Class D audio power amplifier features a filterless modulation scheme that reduces external component count, conserving board space and reducing system cost. The outputs of the device transition from $PV_{DD}$ to GND with a 390kHz switching frequency. With no signal applied, the outputs switch with a 50% duty cycle, in phase, causing the two outputs to cancel. This cancellation results in no net voltage across the speaker, thus there is no current to the load in the idle state.

When an input signal is applied, the duty cycle (pulse width) of the LM48413 output's change. For increasing output voltage, the duty cycle of one side of each output increases, while the duty cycle of the other side of each output decreases. For decreasing output voltages, the converse occurs. The difference between the two pulse widths yields the differential output voltage.

## SHUTDOWN FUNCTION

The LM48413 features a low current shutdown mode. Set $\overline{SD}$ = GND to disable the amplifier and reduce supply current to 0.03µA.

Switch $\overline{SD}$ between GND and $V_{DD}$ for minimum current consumption in shutdown. The LM48413 may be disabled with shutdown voltages in between GND and $V_{DD}$, but the idle current will be greater than the typical value. The LM48413 shutdown input has an internal 300kΩ pull-down resistor. The purpose of this resistor is to eliminate any unwanted state changes when this pin is floating. To minimize shutdown current, it should be driven to GND or left floating. If it is not driven to GND, or floating, a small increase in shutdown supply current will be noticed.

## SPREAD SPECTRUM

The LM48413 outputs are modulated in spread spectrum scheme eliminating the need for output filters, ferrite beads or chokes. During its operation, the switching frequency varies randomly by 30% about a 390kHz center frequency, reducing the wideband spectral content and improving EMI emissions radiated by the speaker and associated cables and traces. A fixed frequency class D exhibits large amounts of spectral energy at multiples of the switching frequency. The spread spectrum architecture of the LM48413 spreads the same energy over a larger bandwidth. The cycle-to-cycle variation of the switching period does not affect the audio reproduction, efficiency, or PSRR.

## ENHANCED EMISSIONS SUPPRESSION SYSTEM ($E^2S$)

The LM48413 features Texas Instruments' patented $E^2S$ system that further reduces EMI, while maintaining high quality audio reproduction and efficiency. The advanced edge rate control (ERC) embedded within the E2S system works simultaneously with the spread spectrum already activated. The LM48413 ERC greatly reduces the high frequency components of the output square waves by controlling the output rise and fall times, slowing the transitions to reduce RF emissions, while maximizing THD+N and efficiency performance.

## DIFFERENTIAL AMPLIFIER EXPLANATION

As logic supplies continue to shrink, system designers are increasingly turning to differential analog signal handling to preserve signal to noise ratios with restricted voltage swings. The LM48413 features two fully differential speaker amplifiers. A differential amplifier amplifies the difference between the two input signals. Traditional audio power amplifiers have typically offered only single-ended inputs resulting in a 6dB reduction of SNR relative to differential inputs. The LM48413 also offers the possibility of DC input coupling which eliminates the input coupling capacitors. A major benefit of the fully differential amplifier is the improved common mode rejection ratio (CMRR) over single-ended input amplifiers. The increased CMRR of the differential amplifier reduces sensitivity to ground offset related noise injection, especially important in noisy systems.

## POWER DISSIPATION AND EFFICIENCY

The major benefit of a Class D amplifier is increased efficiency versus a Class AB. The efficiency of the LM48413 is attributed to the region of operation of the transistors in the output stage. The Class D output stage acts as current steering switches, consuming negligible amounts of power compared to a Class AB amplifier. Most of the power loss associated with the output stage is due to the IR loss of the MOSFET on-resistance, along with switching losses due to gate charge.

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## PROPER SELECTION OF EXTERNAL COMPONENTS

### Power Supply Bypassing/Filtering

Proper power supply bypassing is important for low noise performance and high PSRR. Place the 1µF supply bypass capacitor as close to the device as possible. Traditionally, a pair of bypass capacitors with typical value 0.1µF and 10µF are applied to the supply rail for increasing stability. Nevertheless, these capacitors do not eliminate the need for bypassing of the LM48413 supply pins.

### Input Capacitor Selection

Input capacitors may be required for some applications, or when the audio source is single-ended. Input capacitors block the DC component of the audio signal, eliminating any conflict between the DC component of the audio source and the bias voltage of the LM48413. The input capacitors create a high-pass filter with the input resistance $R_{IN}$. The -3dB point of the high-pass filter is found using Equation 1 below.

$$f = 1 / 2\pi R_{IN} C_{IN} \quad (Hz) \tag{1}$$

The input capacitors can also be used to remove low frequency content from the audio signal. When the LM48413 is using a single-ended source, power supply noise on the ground is seen as an input signal. Setting the high-pass filter point above the power supply noise frequencies, 217Hz in a GSM phone, for example, filters out the noise such that it is not amplified and heard on the output. Capacitors with a tolerance of 10% or better are recommended for impedance matching and improved CMRR and PSRR.

### Texas Instruments 3D Enhancement

The LM48413 features Texas Instruments' 3D enhancement effect that widens the perceived soundstage of a stereo audio signal. The 3D enhancement increases the apparent stereo channel separation, improving audio reproduction whenever the left and right speakers are too close to one another.

An external RC network shown in Figure 2 is required to enable the 3D effect. Because the LM48413 is a fully differential amplifier, there are two separate RC networks, one for each stereo input pair (INL+ and INR+, and INL- and INR-). Set 3DEN high to enable the 3D effect. Set 3DEN low to disable the 3D effect.

The 3D RC network acts as a high-pass filter. The amount of the 3D effect is set by the $R_{3D}$ resistor. Decreasing the value of R3D increases the 3D effect. The $C_{3D}$ capacitor sets the frequency at which the 3D effect occurs. Increasing the value of $C_{3D}$ decreases the low frequency cutoff point, extending the 3D effect over a wider bandwidth. The low frequency cutoff point is given by Equation 2:

$$f_{3D(-3dB)} = 1 / 2\pi(R_{3D})(C_{3D}) \quad (Hz) \tag{2}$$

Enabling the 3D effect increase the gain by a factor of $(1+40k\Omega/R_{3D})$. Setting $R_{3D}$ to 40kΩ results in a gain increase of 6dB whenever the 3D effect is enabled. The Equation 2 holds for both differential and single-end configuration. The recommended tolerance of the resistor value and capacitor value of the two RC networks are 5% and 10% respectively. Tolerance out of this range may affect the 3D gain and low frequency cut-off point too much. The desired sound quality of the 3D effect may not be obtained consequently.

## SINGLE-ENDED AUDIO AMPLIFIER CONFIGURATION

The LM48413 is compatible with single-ended sources. When configured for single-ended inputs, input capacitors must be used to block and DC component at the input of the device. Figure 17 shows the typical single-ended applications circuit.


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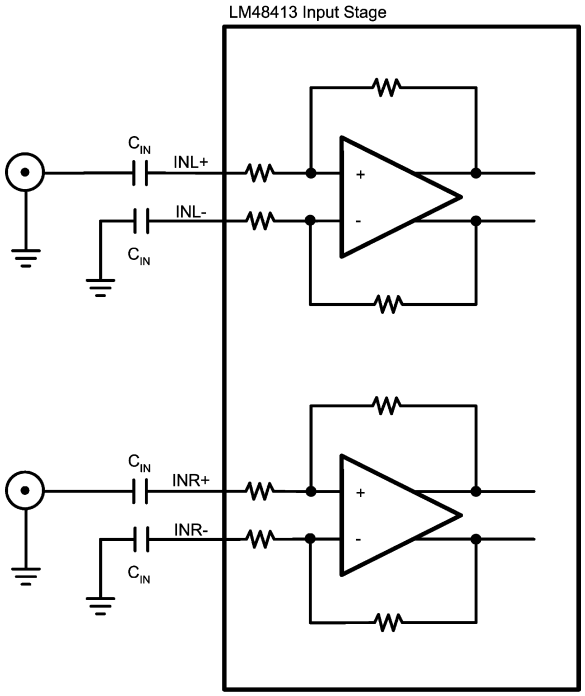



**Figure 17. Single-Ended Circuit Diagram**

## AUDIO AMPLIFIER GAIN

The LM48413 has a fix gain value 24dB which is suitable for ordinary audio applications. To reduce the amplifier gain, insert two pairs of external input resistors with same value before the IC's input signal pins. Figure 18 show the configuration of these input resistors and the amplifier's internal gain setting. Accordingly, the overall amplifier gain is given by Equation 3:

$$A_V = 2 * (160k) / (20k + R_{IN}) \quad (3)$$

For example, if the gain to be set is 12dB, then $A_V$ is equal to 4. Thus, Equation 3 the input resistors' value $R_{IN}$ = [(2 * 160k)/4] –20k = 60kΩ.

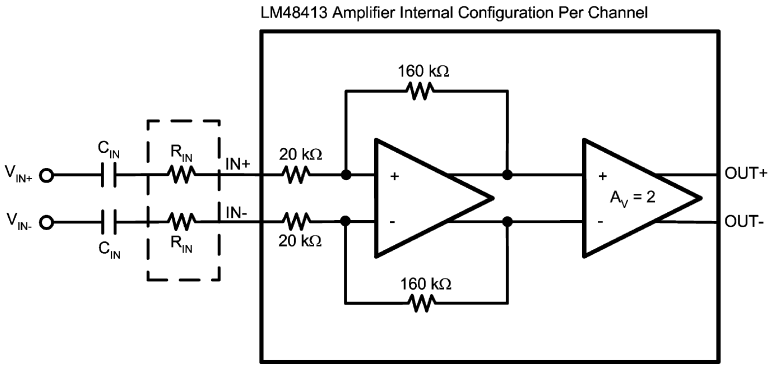



**Figure 18. Audio Amplifier Gain Setting**

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## PCB LAYOUT GUIDELINES

As output power increases, interconnect resistance (PCB traces and wires) between the amplifier, load and power supply create a voltage drop. The voltage loss due to the traces between the LM48413 and the load results in lower output power and decreased efficiency. Higher trace resistance between the supply and the LM48413 has the same effect as a poorly regulated supply, increasing ripple on the supply line, and reducing peak output power. The effects of residual trace resistance increases as output current increases due to higher output power, decreased load impedance or both. To maintain the highest output voltage swing and corresponding peak output power, the PCB traces that connect the output pins to the load and the supply pins to the power supply should be as wide as possible to minimize trace resistance.

The use of power and ground planes will give the best THD+N performance. In addition to reducing trace resistance, the use of power planes creates parasitic capacitors that help to filter the power supply line.

The inductive nature of the transducer load can also result in overshoot on one or both edges, clamped by the parasitic diodes to GND and $V_{DD}$ in each case. From an EMI standpoint, this is an aggressive waveform that can radiate or conduct to other components in the system and cause interference. It is essential to keep the power and output traces short and well shielded if possible. Use of ground planes beads and micros-strip layout techniques are all useful in preventing unwanted interference.

As the distance from the LM48413 and the speaker increases, the amount of EMI radiation increases due to the output wires or traces acting as antennas. The EMI output spectrums of LM48413 evaluation board connected with different speaker cable lengths to an 8Ω load were measured (See Typical Performance Characteristics). Lengths from 3 inches to 12 inches are shown all fall within the limit of the FCC Class B requirement.

## THD+N MEASUREMENT

Class D amplifiers, by design, switch their output power devices at a much higher frequency than the accepted audio range (20Hz – 22kHz). Alternately switching the output voltage between $V_{DD}$ and GND allows the LM48413 to operate at much higher efficiency. However, it also increases the out-of-band noise. Since THD+N measurement is a bandwidth limited measurement, it can be significantly affected by out-of-band noise, resulting in a higher than expected THD+N measurement. To achieve a more accurate measurement of THD+N, the test equipment's input bandwidth must be limited. The input filter limits the out-of-band noise resulting in a more relevant THD+N value. A low-pass filter with a cut-off at 28kHz was used in addition to the internal filter of the THD+N measurement equipment (See Figure 19).

In real applications, the output filters are not necessary since the speakers will act as low-pass filters blocking the remaining switching noise and smoothing the output signals. Instead of connecting the LM48413's BTL outputs to speakers during measurements, the 28kHz low-pass filter is used as shown in Figure 19. This measurement technique also applies to measurements such as PSRR, CMRR, and output power.

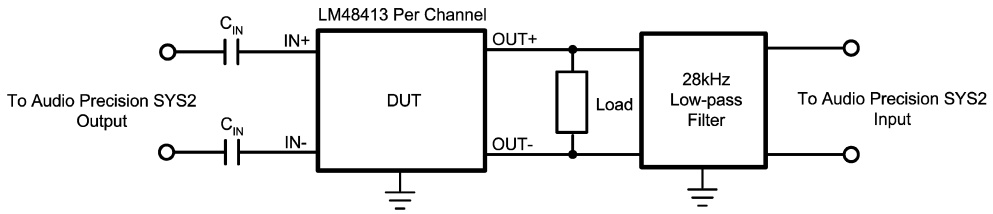



**Figure 19. THD+N Measurement Test Setup**


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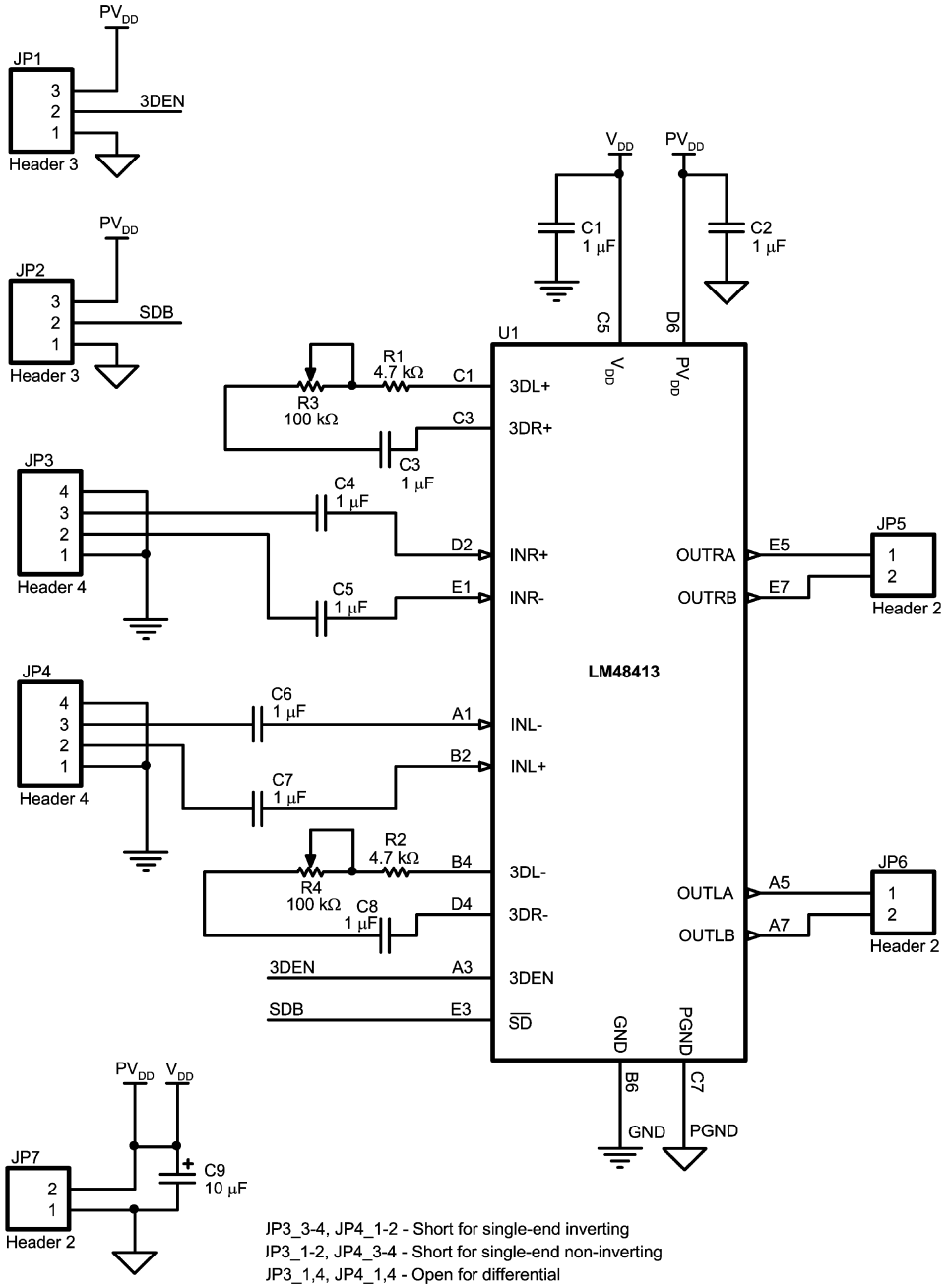
## Bill Of Materials

**Table 1. LM48413 Demonstration Board Bill of Materials**

| Item | Designator | Description | Part Number | Qty | Value | Recommended Supplier |
|---|---|---|---|---|---|---|
| 1 | U1 | Stereo Class-D | LM48413TL | 1 | | Texas Instruments |
| 2 | R1, R2 | Resistor (0603) | | 2 | 4.7kΩ ± 5% | Towa |
| 3 | C1, C2, C3, C8 | Ceramic Capacitor (0603) X7R | GRM188R71C105KA01D | 4 | 1µF ± 10%, 25V | Murata |
| 4 | C4, C5, C6, C7 | Ceramic Capacitor (1206) X7R | C3216X741H105K | 4 | 1µF ± 10%, 25V | TDK |
| 5 | C9 | Tantium Capacitor (1210) | 594D106X0025B2T | 1 | 10µF ± 10%, 25V | Vishay |
| 6 | JP5, JP6, JP7 | Header 2-pin | | 3 | | |
| 7 | JP1, JP2 | Header 3-pin | | 2 | | |
| 8 | JP3, JP4 | Header 4-pin | | 2 | | |
| 9 | R3, R4 | Potentiometer | ST-4EB100k | 2 | 100kΩ | Copal Electronics |

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## Demonstration Board Schematic





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## Demonstration Board Layout

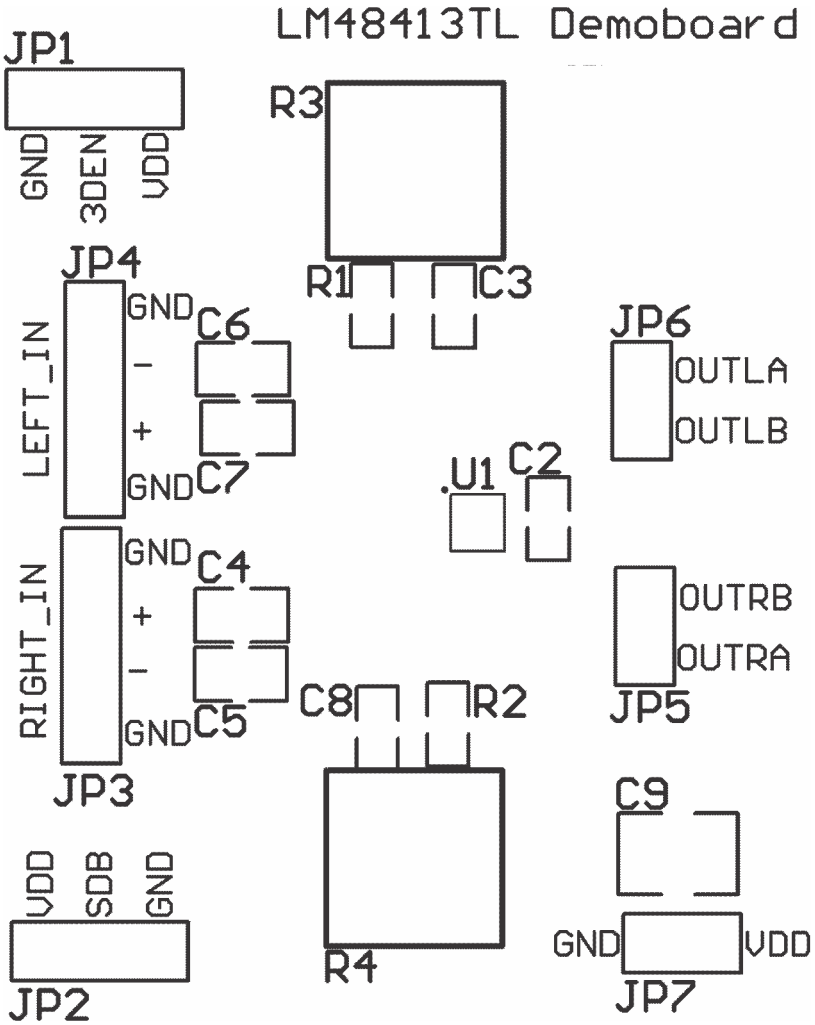



**Figure 20. Top Silkscreen**

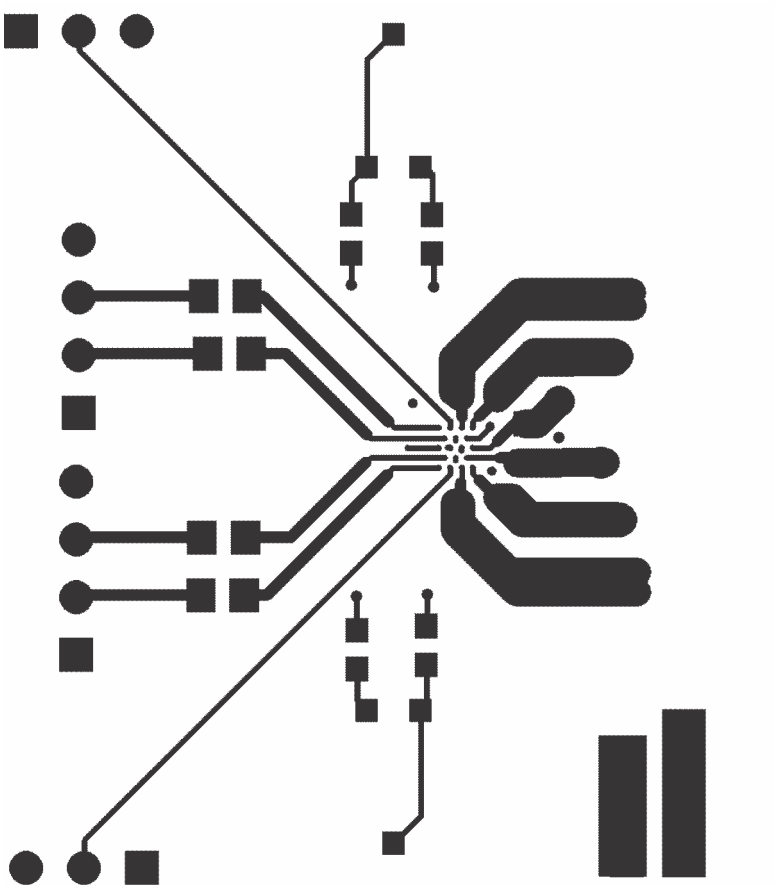


**Figure 21. Top Layer**


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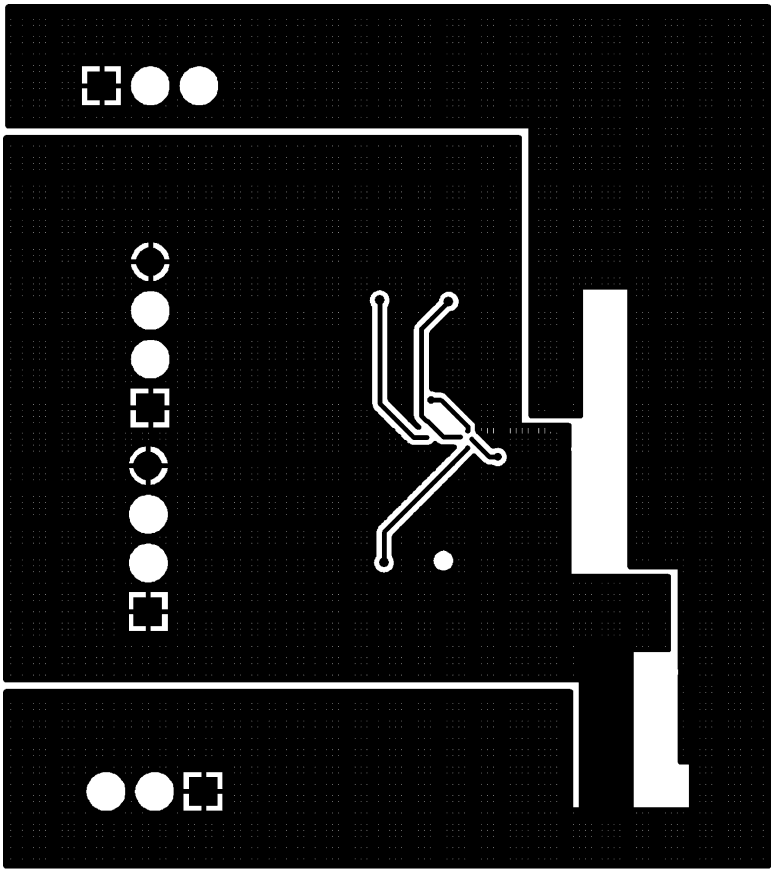


**Figure 22. Middle Layer 1**

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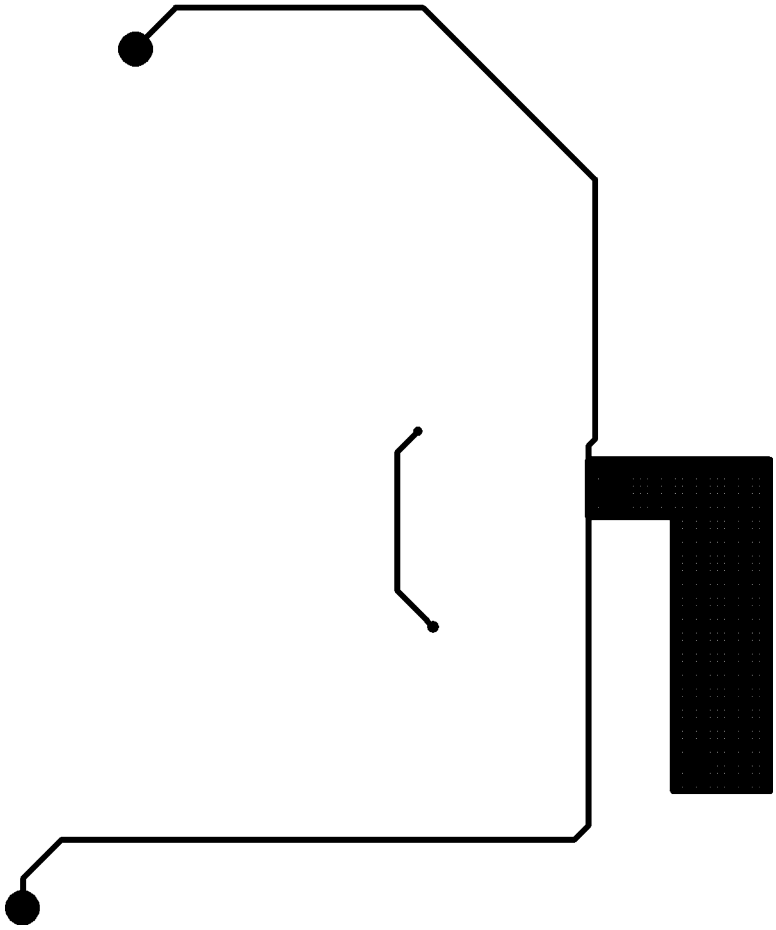


**Figure 23. Middle Layer 2**


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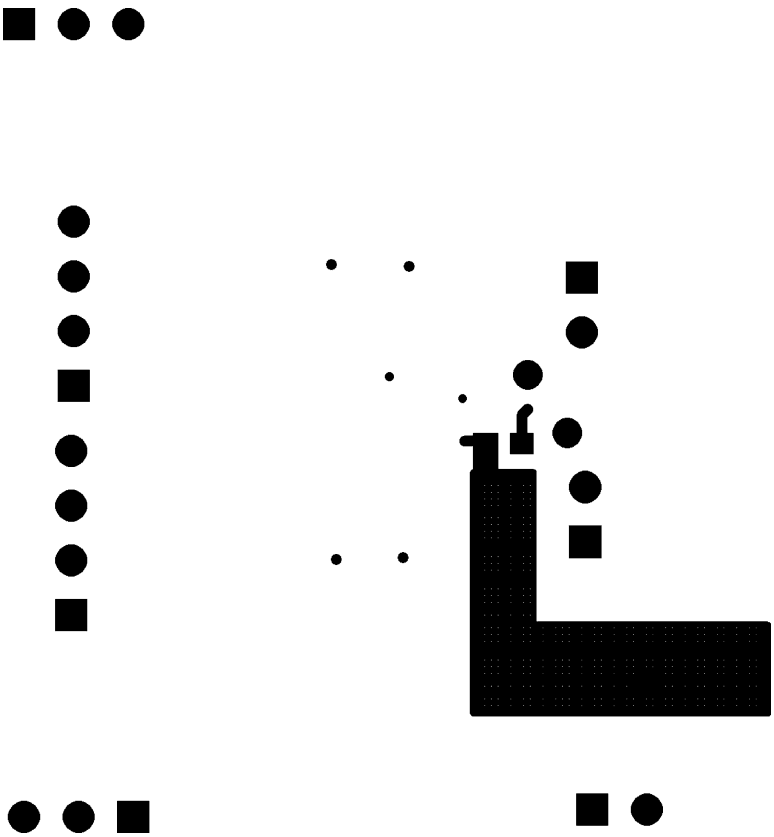


**Figure 24. Bottom Layer**

## Revision Table

| Rev | Date | Description |
|---|---|---|
| 1.0 | 11/19/08 | Initial release. |
| 1.01 | 01/08/09 | Text edits. |
| B | 03/21/2013 | Changed layout of National Data Sheet to TI format |

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## PACKAGING INFORMATION

| Orderable Device | Status (1) | Package Type | Package Drawing | Pins | Package Qty | Eco Plan (2) | Lead/Ball Finish (6) | MSL Peak Temp (3) | Op Temp (°C) | Device Marking (4/5) | Samples |
|---|---|---|---|---|---|---|---|---|---|---|---|
| LM48413TL/NOPB | ACTIVE | DSBGA | YZR | 18 | 250 | Green (RoHS & no Sb/Br) | SNAGCU | Level-1-260C-UNLIM | -40 to 85 | GL2 | Samples |

(1) The marketing status values are defined as follows:
**ACTIVE:** Product device recommended for new designs.
**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.
**OBSOLETE:** TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
**TBD:** The Pb-Free/Green conversion plan has not been defined.
**Pb-Free (RoHS):** TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
**Pb-Free (RoHS Exempt):** This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
**Green (RoHS & no Sb/Br):** TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

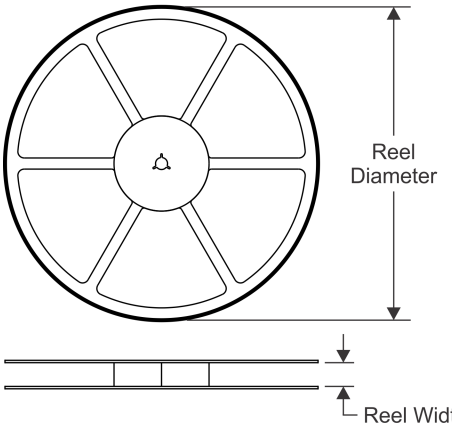
(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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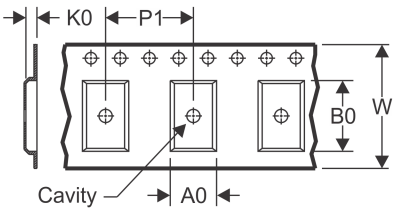
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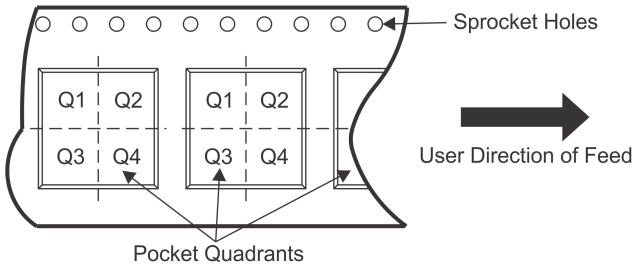



**TAPE DIMENSIONS**




| | |
|---|---|
| A0 | Dimension designed to accommodate the component width |
| B0 | Dimension designed to accommodate the component length |
| K0 | Dimension designed to accommodate the component thickness |
| W | Overall width of the carrier tape |
| P1 | Pitch between successive cavity centers |

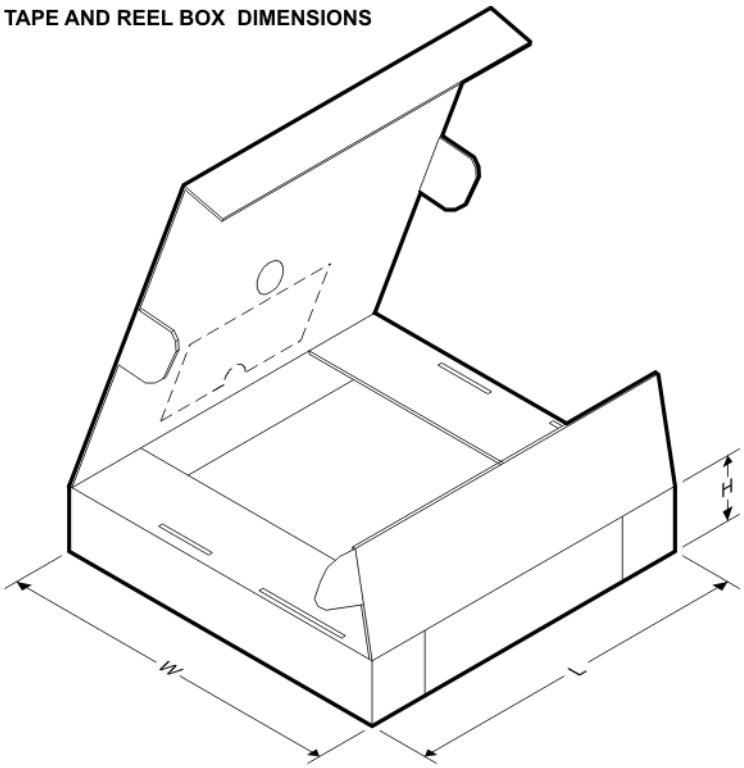
**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**




*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| LM48413TL/NOPB | DSBGA | YZR | 18 | 250 | 178.0 | 8.4 | 2.29 | 2.59 | 0.76 | 4.0 | 8.0 | Q1 |

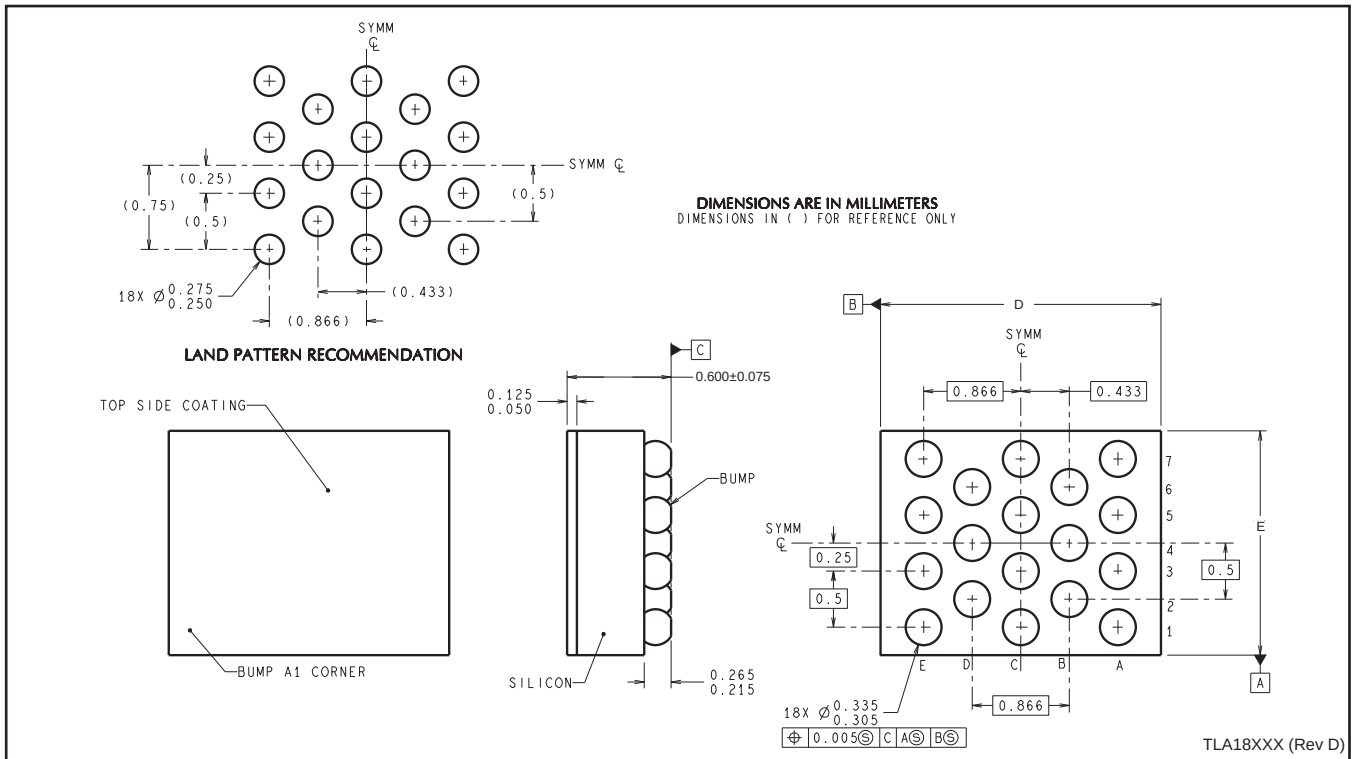
**TAPE AND REEL BOX DIMENSIONS**




*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Length (mm) | Width (mm) | Height (mm) |
|---|---|---|---|---|---|---|---|
| LM48413TL/NOPB | DSBGA | YZR | 18 | 250 | 210.0 | 185.0 | 35.0 |

# YZR0018




D: Max = 2.271 mm, Min =2.211 mm

E: Max = 2.071 mm, Min =2.011 mm

4215052/A 12/12

NOTES: A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.
B. This drawing is subject to change without notice.

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