LM4125 Precision Micropower Low Dropout Voltage Reference

Check for Samples: LM4125

FEATURES

- **Small SOT23-5 Package**
- **Low Dropout Voltage: 120 mV Typ @ 1 mA**
- **High Output Voltage Accuracy: 0.2%**
- **Source and Sink Current Output: ±5 mA**
- **Supply Current: 160 µA Typ.**
- **Low Temperature Coefficient: 50 ppm/°C**
- **Fixed Output Voltages: 2.048, 2.5,and 4.096**
- **Industrial Temperature Range: −40°C to +85°C**
- **(For Extended Temperature Range, −40°C to 125°C, Contact TI)**

APPLICATIONS

- **Portable, Battery Powered Equipment**
- **Instrumentation and Process Control**
- **Automotive & Industrial**
- **Test Equipment**
- **Data Acquisition Systems**
- **Precision Regulators**
- **Battery Chargers**
- **Base Stations**
- **Communications**
- **Medical Equipment**

DESCRIPTION

The LM4125 is a precision low power low dropout bandgap voltage reference with up to 5 mA output current source and sink capability.

This series reference operates with input voltages as low as 2V and up to 6V consuming 160 µA (Typ.) supply current. In power down mode, device current drops to less than 2 µA.

The LM4125 comes in two grades (A and Standard) and three voltage options for greater flexibility. The best grade devices (A) have an initial accuracy of 0.2%, while the standard have an initial accuracy of 0.5%, both with a tempco of 50ppm/°C ensured from −40°C to +125°C.

The very low dropout voltage, low supply current and power-down capability of the LM4125 makes this product an ideal choice for battery powered and portable applications.

The device performance is ensured over the industrial temperature range (−40°C to +85°C), while certain specs are ensured over the extended temperature range (−40°C to +125°C). Please contact TI for full specifications over the extended temperature range. The LM4125 is available in a standard 5-pin SOT-23 package.

Connection Diagram

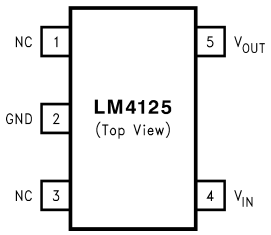


Figure 1. 5-Pin SOT-23 Surface Mount Package
See Package Number DBV

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

All trademarks are the property of their respective owners.

PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of the Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

Copyright © 2004–2013, Texas Instruments Incorporated

Absolute Maximum Ratings[1][2]

Maximum Voltage on input or enable pins		−0.3V to 8V
Output Short-Circuit Duration		Indefinite
Power Dissipation (T_A = 25°C)[3]	DBV package − θ_{JA}	280°C/W
	Power Dissipation	350 mW
ESD Susceptibility[4]	Human Body Model	2 kV
	Machine Model	200V
Lead Temperature:	Soldering, (10 sec.)	+260°C
	Vapor Phase (60 sec.)	+215°C
	Infrared (15 sec.)	+220°C

(1) "Absolute Maximum Ratings" indicate limits beyond which damage to the device may occur. Operating Ratings indicate conditions for which the device is intended to be functional, but do not ensure specific performance limits. For ensured specifications and test conditions, see Electrical Characteristics. The ensured specifications apply only for the test conditions listed. Some performance characteristics may degrade when the device is not operated under the listed test conditions.

(2) If Military/Aerospace specified devices are required, please contact the Texas Instruments Sales Office/Distributors for availability and specifications.

(3) Without PCB copper enhancements. The maximum power dissipation must be de-rated at elevated temperatures and is limited by T_{JMAX} (maximum junction temperature), θ_{J-A} (junction to ambient thermal resistance) and T_A (ambient temperature). The maximum power dissipation at any temperature is: $PDiss_{MAX} = (T_{JMAX} - T_A)/\theta_{J-A}$ up to the value listed in the Absolute Maximum Ratings.

(4) The human body model is a 100 pF capacitor discharged through a 1.5 kΩ resistor into each pin. The machine model is a 200 pF capacitor discharged directly into each pin.

Operating Range[1]

Storage Temperature Range	−65°C to +150°C
Ambient Temperature Range	−40°C to +85°C
Junction Temperature Range	−40°C to +125°C

(1) "Absolute Maximum Ratings" indicate limits beyond which damage to the device may occur. Operating Ratings indicate conditions for which the device is intended to be functional, but do not ensure specific performance limits. For ensured specifications and test conditions, see Electrical Characteristics. The ensured specifications apply only for the test conditions listed. Some performance characteristics may degrade when the device is not operated under the listed test conditions.

Copyright © 2004–2013, Texas Instruments Incorporated

Electrical Characteristics — LM4125-2.048V and 2.5V

Unless otherwise specified V_{IN} = 3.3V, I_{LOAD} = 0, C_{OUT} = 0.01µF, T_A = T_j = 25°C. Limits with standard typeface are for T_j = 25°C, and limits in **boldface type** apply over the −40°C ≤ T_A ≤ +85°C temperature range.

Symbol	Parameter	Conditions	Min (1)	Typ (2)	Max (1)	Units
V_{OUT}	Output Voltage Initial Accuracy LM4125A-2.048 LM4125A-2.500				±0.2	%
	LM4125-2.048 LM4125-2.500				±0.5	%
TCV_{OUT}/°C	Temperature Coefficient	−40°C ≤ T_A ≤ +125°C		14	50	ppm/°c
$\Delta V_{OUT}/\Delta V_{IN}$	Line Regulation	3.3V ≤ V_{IN} ≤ 6V		0.0007	0.008 **0.01**	%/V
$\Delta V_{OUT}/\Delta I_{LOAD}$	Load Regulation	0 mA ≤ I_{LOAD} ≤ 1 mA		0.03	0.08 **0.17**	%/mA
		1 mA ≤ I_{LOAD} ≤ 5 mA		0.01	0.04 **0.1**	
		−1 mA ≤ I_{LOAD} ≤ 0 mA		0.04	0.12	
		−5 mA ≤ I_{LOAD} ≤ −1 mA		0.01		
$V_{IN}-V_{OUT}$	Dropout Voltage (3)	I_{LOAD} = 0 mA		45	65 **100**	mV
		I_{LOAD} = +1 mA		120	150 **200**	
		I_{LOAD} = +5 mA		180	210 **300**	
V_N	Output Noise Voltage (4)	0.1 Hz to 10 Hz		20		μV_{PP}
		10 Hz to 10 kHz		36		μV_{PP}
I_S	Supply Current			160	257 **290**	µA
I_{SC}	Short Circuit Current	V_{IN} = 3.3V, V_{OUT} = 0		15		mA
			6		**30**	
		V_{IN} = 6V, V_{OUT} = 0		17		
			6		**30**	
Hyst	Thermal Hysteresis (5)	−40°C ≤ T_A ≤ 125°C		0.5		mV/V
ΔV_{OUT}	Long Term Stability (6)	1000 hrs. @ 25°C		100		ppm

(1) Limits are 100% production tested at 25°C. Limits over the operating temperature range are ensured through correlation using Statistical Quality Control (SQC) methods. The limits are used to calculate Outgoing Quality Level (AOQL).
(2) Typical numbers are at 25°C and represent the most likely parametric norm.
(3) Dropout voltage is the differential voltage between V_{OUT} and V_{IN} at which V_{OUT} changes ≤ 1% from V_{OUT} at V_{IN} = 3.3V for 2.0V, 2.5V and 5V for 4.1V. A parasitic diode exists between input and output pins; it will conduct if V_{OUT} is pulled to a higher voltage than V_{IN}.
(4) Output noise voltage is proportional to V_{OUT}. V_N for other voltage option is calculated using ($V_{N(1.8V)}$/1.8) * V_{OUT}. V_N (2.5V) = (36µV_{PP}/1.8) * 2.5 = 46µV_{PP}.
(5) Thermal hysteresis is defined as the change in +25°C output voltage before and after exposing the device to temperature extremes.
(6) Long term stability is change in V_{REF} at 25°C measured continuously during 1000 hrs.

Copyright © 2004–2013, Texas Instruments Incorporated

Electrical Characteristics — LM4125-4.096V

Unless otherwise specified V_{IN} = 5V, I_{LOAD} = 0, C_{OUT} = 0.01µF, T_A = T_j = 25°C. Limits with standard typeface are for T_j = 25°C, and limits in **boldface type** apply over the −40°C ≤ T_A ≤ +85°C temperature range.

Symbol	Parameter	Conditions	Min (1)	Typ (2)	Max (1)	Units
V_{OUT}	Output Voltage Initial Accuracy LM4125A-4.096				±0.2	%
	LM4125-4.096				±0.5	%
TCV_{OUT}/°C	Temperature Coefficient	−40°C ≤ T_A ≤ +125°C		14	50	ppm/°c
$\Delta V_{OUT}/\Delta V_{IN}$	Line Regulation	5V ≤ V_{IN} ≤ 6V		0.0007	0.008 **0.01**	%/V
$\Delta V_{OUT}/\Delta I_{LOAD}$	Load Regulation	0 mA ≤ I_{LOAD} ≤ 1 mA		0.03	0.08 **0.17**	%/mA
		1 mA ≤ I_{LOAD} ≤ 5 mA		0.01	0.04 **0.1**	
		−1 mA ≤ I_{LOAD} ≤ 0 mA		0.04	0.12	
		−5 mA ≤ I_{LOAD} ≤ −1 mA		0.01		
$V_{IN}-V_{OUT}$	Dropout Voltage(3)	I_{LOAD} = 0 mA		45	65 **100**	mV
		I_{LOAD} = +1 mA		120	150 **200**	
		I_{LOAD} = +5 mA		180	210 **300**	
V_N	Output Noise Voltage(4)	0.1 Hz to 10 Hz		20		μV_{PP}
		10 Hz to 10 kHz		36		μV_{PP}
I_S	Supply Current			160	257 **290**	µA
I_{SC}	Short Circuit Current	V_{OUT} = 0		15		mA
			6		**30**	
		V_{IN} = 6V, V_{OUT} = 0		17		
			6		**30**	
Hyst	Thermal Hysteresis(5)	−40°C ≤ T_A ≤ 125°C		0.5		mV/V
ΔV_{OUT}	Long Term Stability(6)	1000 hrs. @ 25°C		100		ppm

(1) Limits are 100% production tested at 25°C. Limits over the operating temperature range are ensured through correlation using Statistical Quality Control (SQC) methods. The limits are used to calculate Outgoing Quality Level (AOQL).
(2) Typical numbers are at 25°C and represent the most likely parametric norm.
(3) Dropout voltage is the differential voltage between V_{OUT} and V_{IN} at which V_{OUT} changes ≤ 1% from V_{OUT} at V_{IN} = 3.3V for 2.0V, 2.5V and 5V for 4.1V. A parasitic diode exists between input and output pins; it will conduct if V_{OUT} is pulled to a higher voltage than V_{IN}.
(4) Output noise voltage is proportional to V_{OUT}. V_N for other voltage option is calculated using ($V_{N(1.8V)}$/1.8) * V_{OUT}. V_N (2.5V) = (36µV_{PP}/1.8) * 2.5 = 46µV_{PP}.
(5) Thermal hysteresis is defined as the change in +25°C output voltage before and after exposing the device to temperature extremes.
(6) Long term stability is change in V_{REF} at 25°C measured continuously during 1000 hrs.

Copyright © 2004–2013, Texas Instruments Incorporated

LM4125 Typical Operating Characteristics

Unless otherwise specified, V_{IN} = 3.3V, V_{OUT} = 2.5V, I_{LOAD} = 0, C_{OUT} = 0.022µF and T_A = 25°C.

Long Term Drift

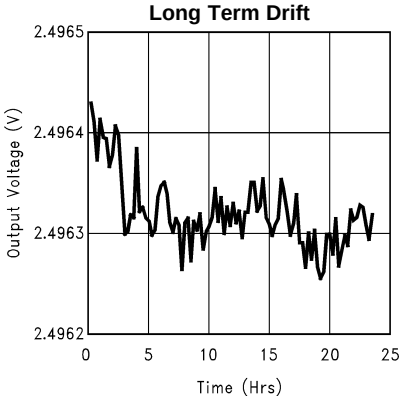


Figure 2.

Typical Temperature Drift

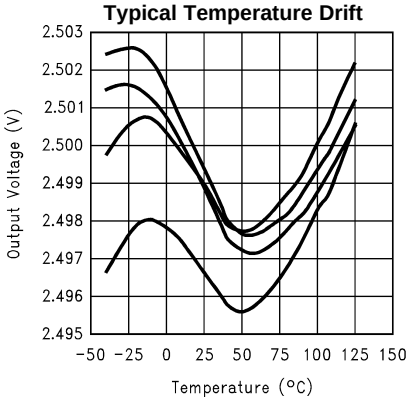


Figure 3.

Short Circuit Current vs Temperature

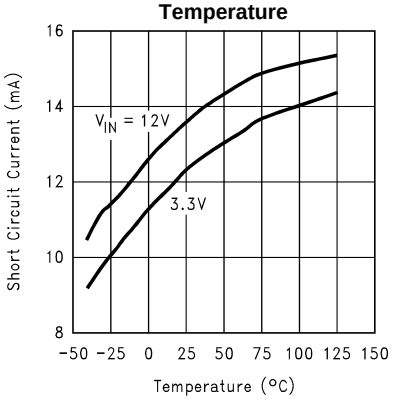


Figure 4.

Dropout Voltage vs Output Error

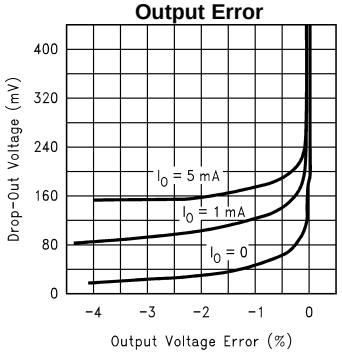


Figure 5.

Dropout Voltage vs Load Current

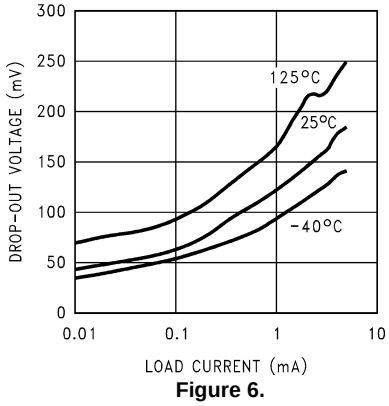


Figure 6.

Load Regulation

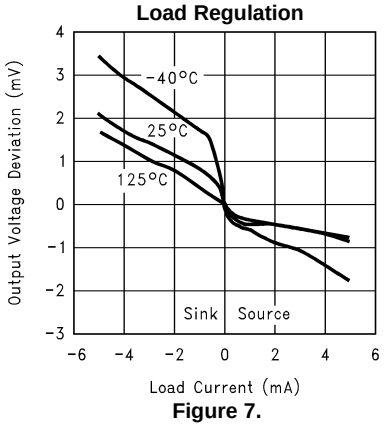


Figure 7.

Copyright © 2004–2013, Texas Instruments Incorporated

LM4125 Typical Operating Characteristics (continued)

Unless otherwise specified, V_{IN} = 3.3V, V_{OUT} = 2.5V, I_{LOAD} = 0, C_{OUT} = 0.022µF and T_A = 25°C.

GND Pin Current

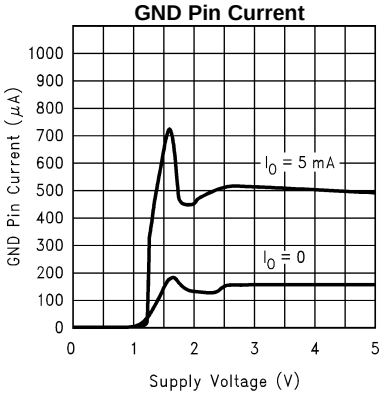


Figure 8.

GND Pin Current at No Load vs Temperature

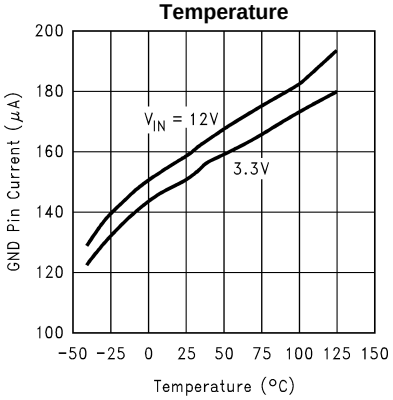


Figure 9.

GND Pin Current vs Load

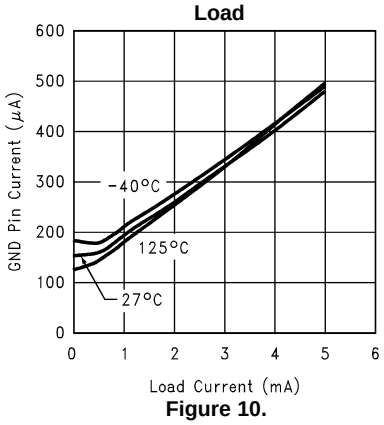


Figure 10.

0.1Hz to 10Hz output Noise

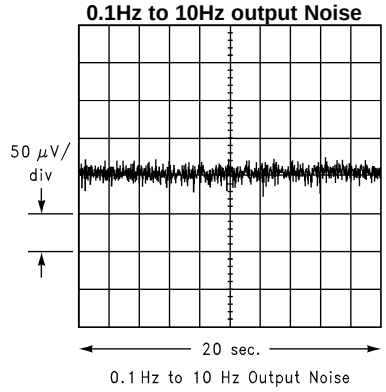


Figure 11.

Output Impedance vs Frequency

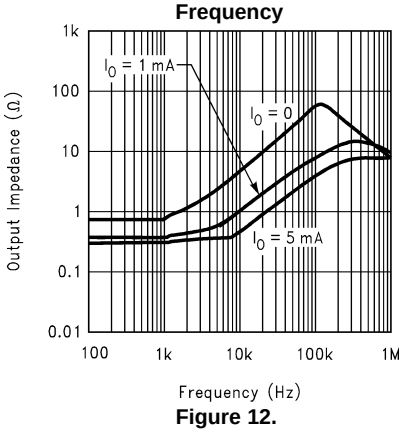


Figure 12.

PSRR vs Frequency

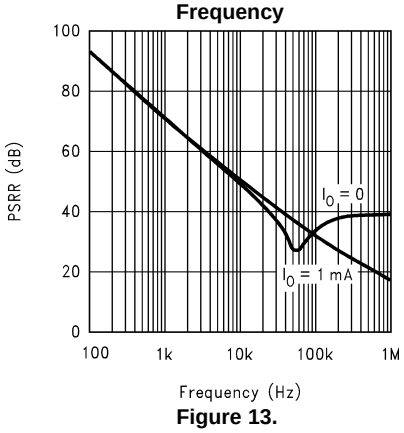


Figure 13.

Copyright © 2004–2013, Texas Instruments Incorporated

LM4125 Typical Operating Characteristics (continued)

Unless otherwise specified, V_{IN} = 3.3V, V_{OUT} = 2.5V, I_{LOAD} = 0, C_{OUT} = 0.022µF and T_A = 25°C.

Start-Up Response

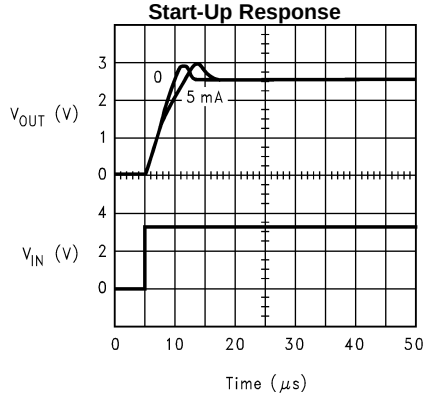


Figure 14.

Load Step Response

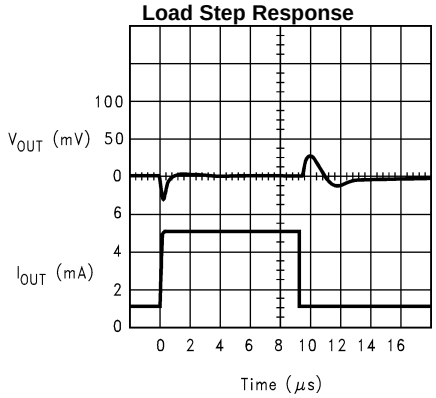


Figure 15.

Load Step Response

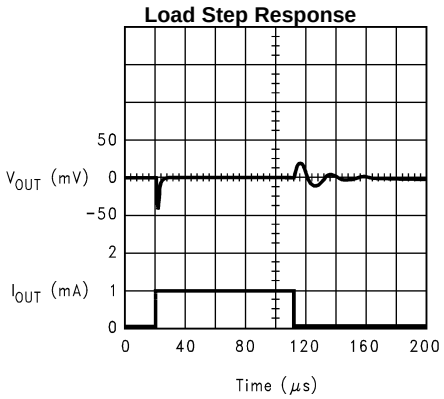


Figure 16.

Line Step Response

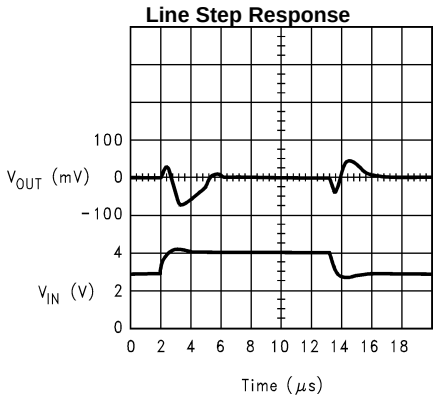


Figure 17.

Thermal Hysteresis

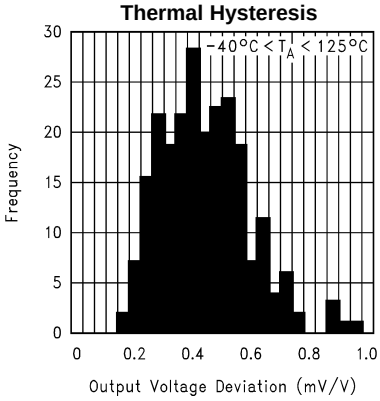


Figure 18.

PIN FUNCTIONS

Output (Pin 5): Reference Output.

Input (Pin 4): Positive Supply.

Ground (Pin 2): Negative Supply or Ground Connection.

APPLICATION HINTS

The standard application circuit for the LM4125 is shown in Figure 19. It is designed to be stable with ceramic output capacitors in the range of 0.022µF to 0.1µF. Note that 0.022µF is the minimum required output capacitor. These capacitors typically have an ESR of about 0.1 to 0.5Ω. Smaller ESR can be tolerated, however larger ESR can not. The output capacitor can be increased to improve load transient response, up to about 1µF. However, values above 0.047µF must be tantalum. With tantalum capacitors, in the 1µF range, a small capacitor between the output and the reference pin is required. This capacitor will typically be in the 50pF range. Care must be taken when using output capacitors of 1µF or larger. These application must be thoroughly tested over temperature, line and load.

An input capacitor is typically not required. However, a 0.1µF ceramic can be used to help prevent line transients from entering the LM4125. Larger input capacitors should be tantalum or aluminum.

The typical thermal hysteresis specification is defined as the change in +25°C voltage measured after thermal cycling. The device is thermal cycled to temperature -40°C and then measured at 25°C. Next the device is thermal cycled to temperature +125°C and again measured at 25°C. The resulting V_{OUT} delta shift between the 25°C measurements is thermal hysteresis. Thermal hysteresis is common in precision references and is induced by thermal-mechanical package stress. Changes in environmental storage temperature, operating temperature and board mounting temperature are all factors that can contribute to thermal hysteresis.

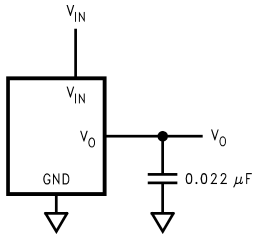


Figure 19. Standard Application Circuit

INPUT CAPACITOR

Noise on the power-supply input can effect the output noise, but can be reduced by using an optional bypass capacitor between the input pin and the ground.

PRINTED CIRCUIT BOARD LAYOUT CONSIDERATION

The mechanical stress due to PC board mounting can cause the output voltage to shift from its initial value. References in SOT packages are generally less prone to assembly stress than devices in Small Outline (SOIC) package.

To reduce the stress-related output voltage shifts, mount the reference on the low flex areas of the PC board such as near to the edge or the corner of the PC board.

Copyright © 2004–2013, Texas Instruments Incorporated

Typical Application Circuits

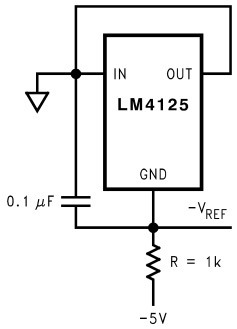


Figure 20. Voltage Reference with Negative Output

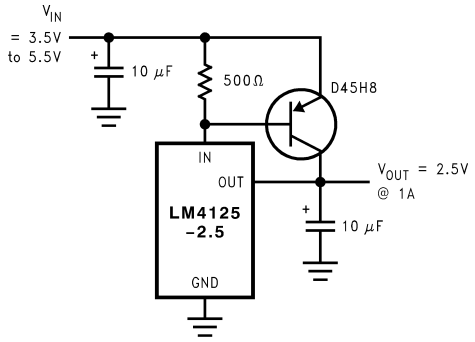


Figure 21. Precision High Current Low Dropout Regulator

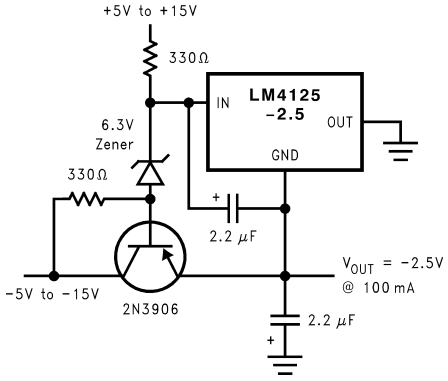


Figure 22. Precision High Current Negative Voltage Regulator

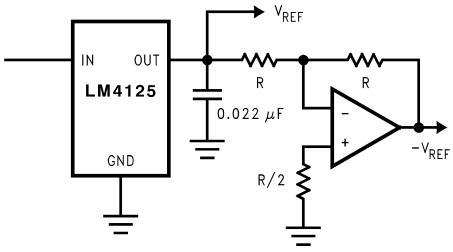


Figure 23. Voltage Reference with Complimentary Output

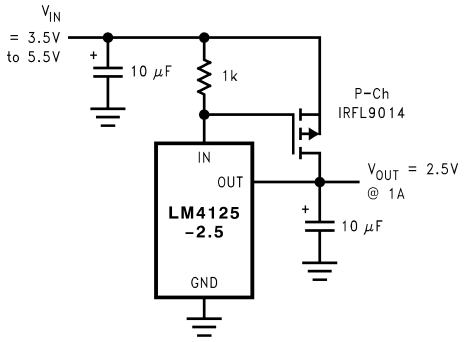


Figure 24. Precision High Current Low Droput Regulator

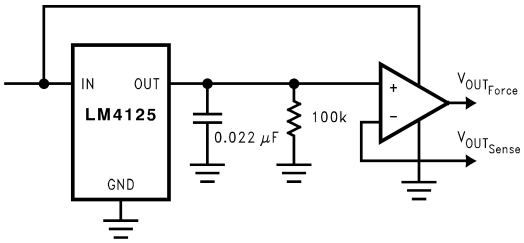


Figure 25. Precision Voltage Reference with Force and Sense Output

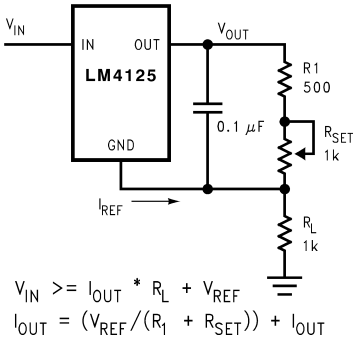


Figure 26. Programmable Current Source

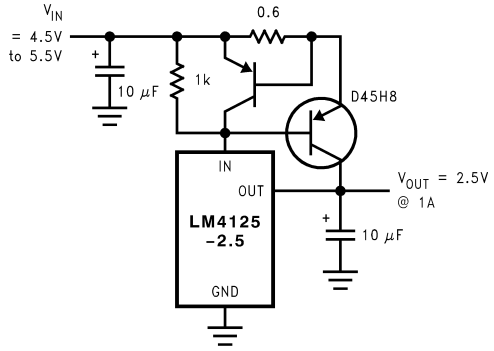


Figure 27. Precision Regulator with Current Limiting Circuit

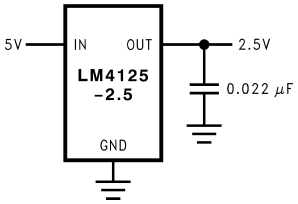


Figure 28. Power Supply Splitter

Copyright © 2004–2013, Texas Instruments Incorporated

REVISION HISTORY

Changes from Original (April 2013) to Revision A	Page
• Changed layout of National Data Sheet to TI format	10

Copyright © 2004–2013, Texas Instruments Incorporated

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
LM4125AIM5-2.5/NOPB	ACTIVE	SOT-23	DBV	5	1000	Green (RoHS & no Sb/Br)	SN	Level-1-260C-UNLIM	-40 to 125	R81A	Samples
LM4125IM5-2.0/NOPB	ACTIVE	SOT-23	DBV	5	1000	Green (RoHS & no Sb/Br)	SN	Level-1-260C-UNLIM	-40 to 125	R80B	Samples
LM4125IM5-2.5/NOPB	ACTIVE	SOT-23	DBV	5	1000	Green (RoHS & no Sb/Br)	SN	Level-1-260C-UNLIM	-40 to 125	R81B	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

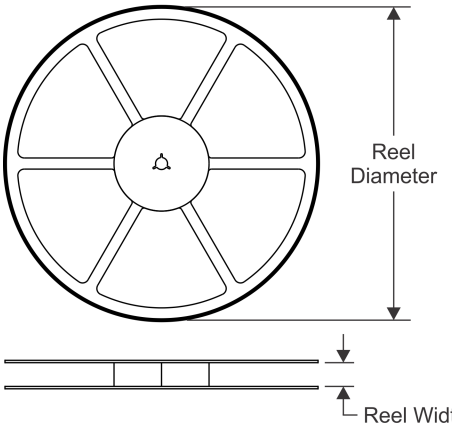
(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

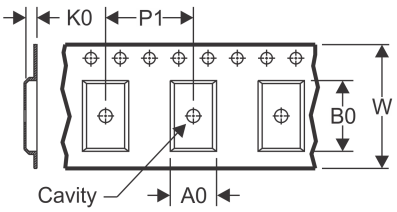
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

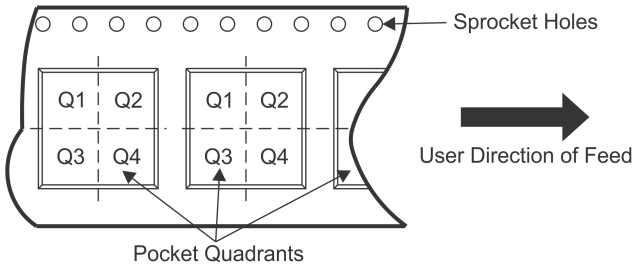


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

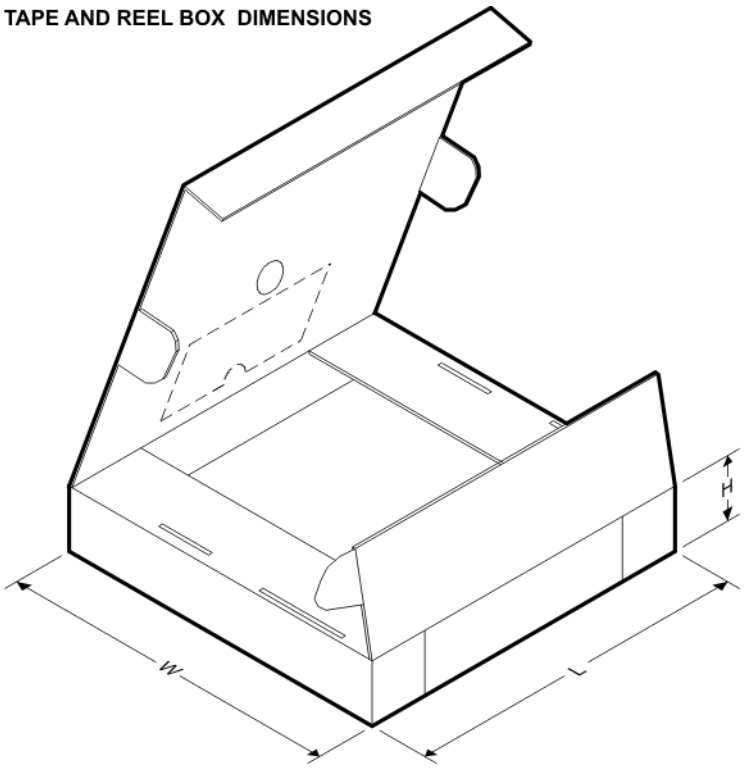
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
LM4125AIM5-2.5/NOPB	SOT-23	DBV	5	1000	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
LM4125IM5-2.0/NOPB	SOT-23	DBV	5	1000	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
LM4125IM5-2.5/NOPB	SOT-23	DBV	5	1000	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

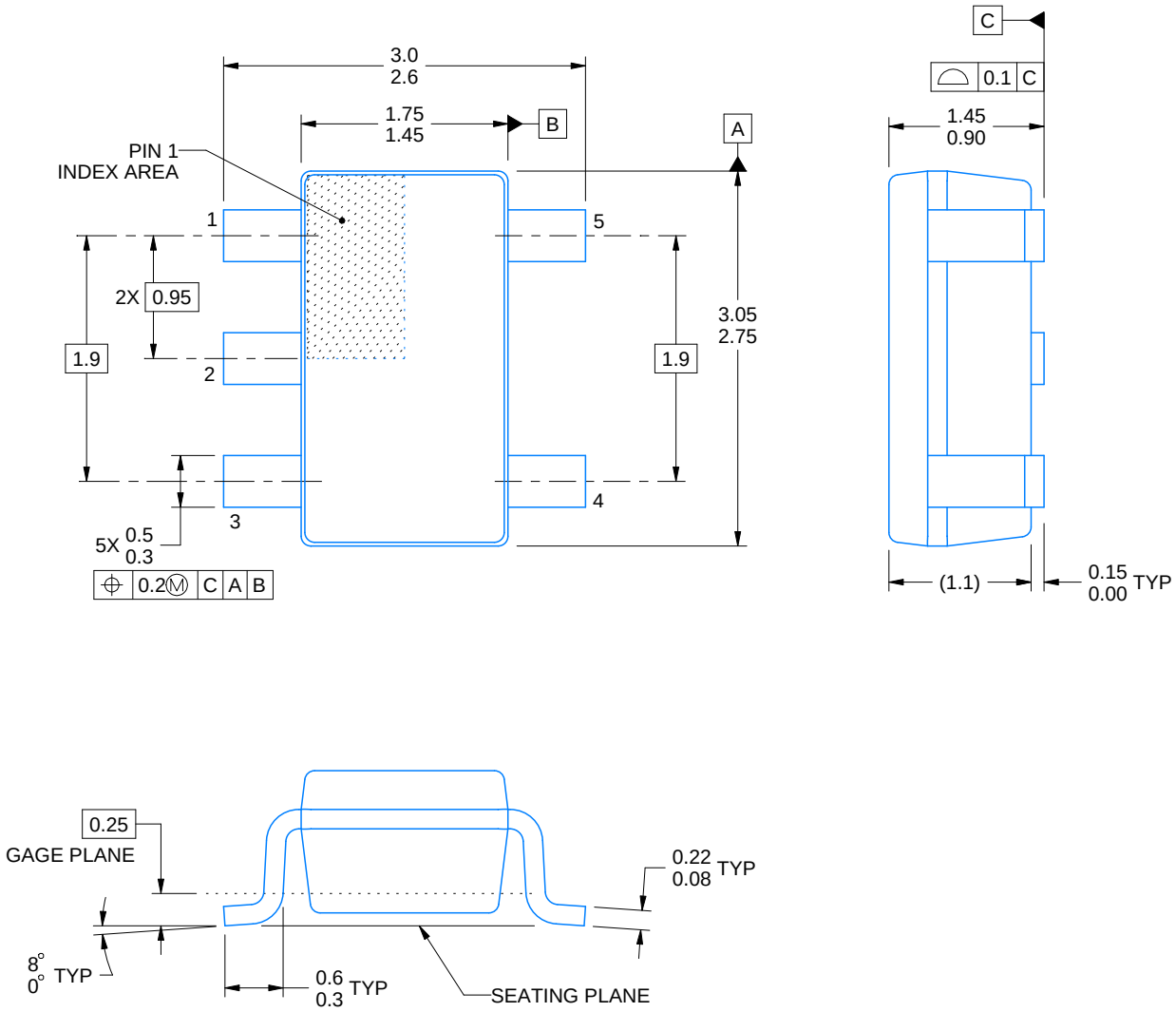
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
LM4125AIM5-2.5/NOPB	SOT-23	DBV	5	1000	210.0	185.0	35.0
LM4125IM5-2.0/NOPB	SOT-23	DBV	5	1000	210.0	185.0	35.0
LM4125IM5-2.5/NOPB	SOT-23	DBV	5	1000	210.0	185.0	35.0

PACKAGE OUTLINE

DBV0005A

SOT-23 - 1.45 mm max height

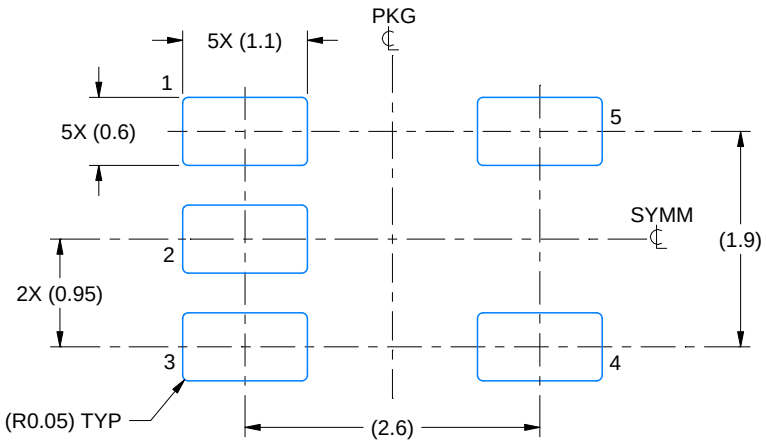
SMALL OUTLINE TRANSISTOR



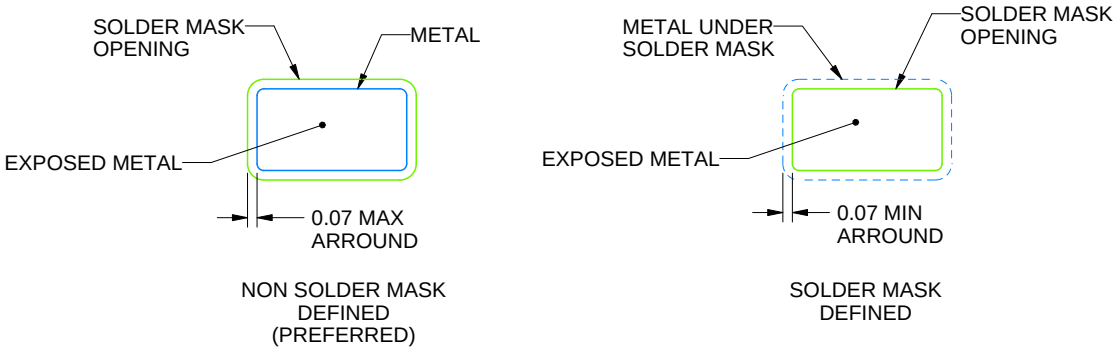
4214839/E 09/2019

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Refernce JEDEC MO-178.
4. Body dimensions do not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:15X

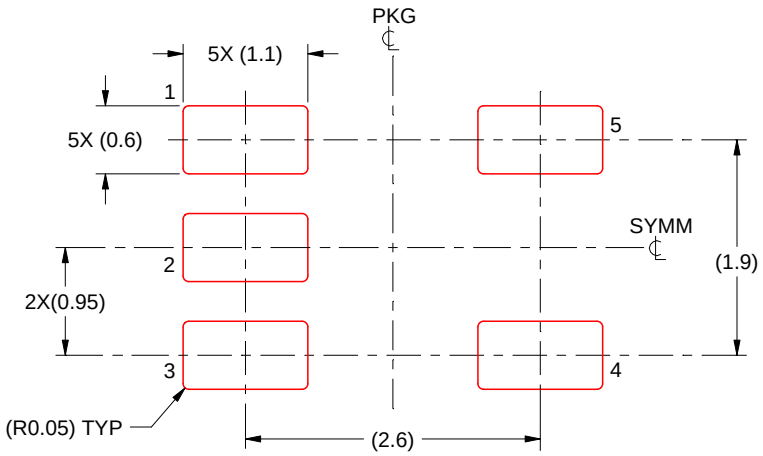


SOLDER MASK DETAILS

4214839/E 09/2019

NOTES: (continued)

5. Publication IPC-7351 may have alternate designs.
6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:15X

4214839/E 09/2019

NOTES: (continued)

7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
8. Board assembly site may have different recommendations for stencil design.

IMPORTANT NOTICE AND DISCLAIMER

TI PROVIDES TECHNICAL AND RELIABILITY DATA (INCLUDING DATASHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES “AS IS” AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS AND IMPLIED, INCLUDING WITHOUT LIMITATION ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE OR NON-INFRINGEMENT OF THIRD PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for skilled developers designing with TI products. You are solely responsible for (1) selecting the appropriate TI products for your application, (2) designing, validating and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, or other requirements. These resources are subject to change without notice. TI grants you permission to use these resources only for development of an application that uses the TI products described in the resource. Other reproduction and display of these resources is prohibited. No license is granted to any other TI intellectual property right or to any third party intellectual property right. TI disclaims responsibility for, and you will fully indemnify TI and its representatives against, any claims, damages, costs, losses, and liabilities arising out of your use of these resources.

TI’s products are provided subject to TI’s Terms of Sale (www.ti.com/legal/termsofsale.html) or other applicable terms available either on ti.com or provided in conjunction with such TI products. TI’s provision of these resources does not expand or otherwise alter TI’s applicable warranties or warranty disclaimers for TI products.

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265
Copyright © 2020, Texas Instruments Incorporated